NCS330, NCV330, NCS2330, NCV2330, NCS4330, NCV4330

Product Preview

50 μV Offset, 0.25 μV/°C, Zero-Drift Operational Amplifier

The NCS330, NCS2330 and NCS4330 family of zero−drift op amps feature offset voltage as low as 50 μV over the 1.8 V to 5.5 V supply voltage range. The zero−drift architecture reduces the offset drift to as low as 0.25 μV/°C and enables high precision measurements over both time and temperature. This family has low power consumption over a wide dynamic range and is available in space saving packages. These features make it well suited for signal conditioning circuits in portable, industrial, automotive, medical and consumer markets.

Features

- Gain−Bandwidth Product: 350 kHz (NCS330)
- Low Supply Current: 17 μA (typ at 3.3 V)
- Low Offset Voltage: 50 μV max
- Low Offset Drift: 0.25 μV/°C max for NCS333/A
- Wide Supply Range: 1.8 V to 5.5 V
- Wide Temperature Range: −40°C to +125°C
- Rail−to−Rail Input and Output
- Available in Single, Dual and Quad Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

Applications

- Automotive
- Battery Powered/ Portable Application
- Sensor Signal Conditioning
- Low Voltage Current Sensing
- Filter Circuits
- Bridge Circuits
- Medical Instrumentation

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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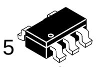
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SOT23−5
SN SUFFIX
CASE 483

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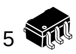
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SC70−5
SQ SUFFIX
CASE 419A


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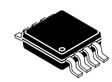
UDFN8
MU SUFFIX
CASE 517AW



MSOP−8
DM SUFFIX
CASE 846A−02

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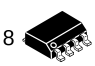
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SOIC−8
D SUFFIX
CASE 751

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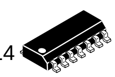
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SOIC−14
D SUFFIX
CASE 751A

DEVICE MARKING INFORMATION

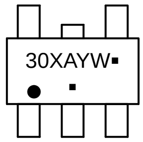
See general marking information in the device marking section on page 2 of this data sheet.

ORDERING INFORMATION

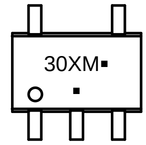
See detailed ordering and shipping information on page 3 of this data sheet.

DEVICE MARKING INFORMATION

Single Channel Configuration
NCS330, NCV330

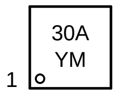


TSOP−5/SOT23−5
CASE 483

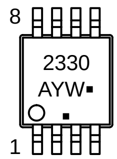


SC70−5
CASE 419A

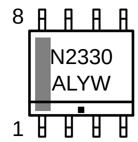
Dual Channel Configuration
NCS2330, NCV2330



UDFN8, 2x2, 0.5P
CASE 517AW

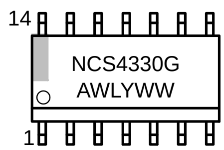


Micro8/MSOP8
CASE 846A−02



SOIC−8
CASE 751

Quad Channel Configuration
NCS4330, NCV4330



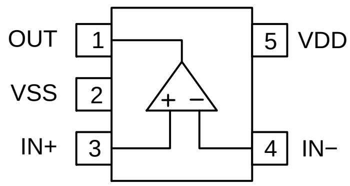
SOIC−14
CASE 751A

X	= Specific Device Code E = NCS330 (SOT23−5) H = NCS330 (SC70−5)
A	= Assembly Location
Y	= Year
W	= Work Week
M	= Date Code
G or ▪	= Pb−Free Package

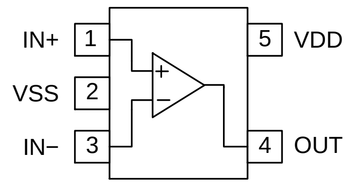
(Note: Microdot may be in either location)

PIN CONNECTIONS

Single Channel Configuration
NCS330, NCV330

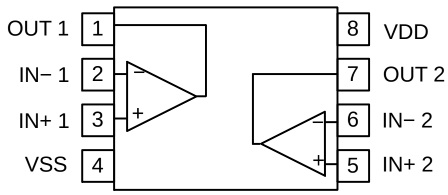


SOT23−5 / TSOP−5



SC70−5 / SC−88−5 / SOT−353−5

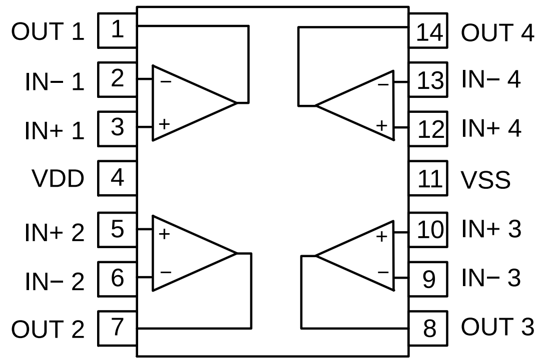
Dual Channel Configuration
NCS2330, NCV2330



UDFN8* / Micro8 / SOIC−8

*The exposed pad of the UDFN8 package can be floated or connected to VSS.

Quad Channel Configuration
NCS4330, NCV4330



SOIC−14

ORDERING INFORMATION

Temperature	Channels	Package	Device Part Number	Shipping †
Commercial and Industrial				
−40 °C to 125 °C	Single	SOT23 – 5 / TSOP – 5	NCS330SN2T1G	3000 / Tape & Reel
		SC70 – 5 / SC – 88 – 5 / SOT – 353 – 5	NCS330SQ3T2G	
	Dual	MICRO – 8	NCS2330DMR2G	4000 / Tape & Reel
		SOIC−8	NCS2330DR2G	3000 / Tape & Reel
		UDFN−8	NCS2330MUTBG	
	Quad	SOIC−14	NCS4333DR2G	2500 / Tape & Reel
Automotive				
−40 °C to 125 °C	Single	SOT23 – 5 / TSOP – 5	NCV330SN2T1G	3000 / Tape & Reel
		SC70 – 5 / SC – 88 – 5 / SOT – 353 – 5	NCV330SQ3T2G	
	Dual	MICRO – 8	NCV2330DMR2G	4000 / Tape & Reel
		SOIC−8	NCV2330DR2G	3000 / Tape & Reel
	Quad	SOIC−14	NCV4330DR2G	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS

Over operating free−air temperature, unless otherwise stated.

Parameter	Rating	Unit
Supply Voltage	6	V
INPUT AND OUTPUT PINS		
Input Voltage (Note 1)	(VSS) − 0.3 to (VDD) + 0.3	V
Input Current (Note 1)	±10	mA
Output Short Circuit Current (Note 2)	Continuous	
TEMPERATURE		
Operating Temperature Range	−40 to +125	°C
Storage Temperature Range	−65 to +150	°C
Junction Temperature	+150	°C
ESD RATINGS (Note 3)		
Human Body Model (HBM)	±4000	V
Charged Device Model (CDM)	±2000	V
OTHER RATINGS		
Latch−up Current (Note 4)	100	mA
MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Input terminals are diode−clamped to the power−supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less
2. Short−circuit to ground.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JEDEC standard JS−001 (AEC−Q100−002)
   ESD Charged Device Model tested per JEDEC standard JESD22−C101 (AEC−Q100−011)
4. Latch−up Current tested per JEDEC standard: JESD78.

THERMAL INFORMATION (Note 5)

Parameter	Symbol	Package	Value	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	SOT23−5 / TSOP5	290	°C/W
		SC70−5 / SC−88−5 / SOT−353−5	425	
		Micro8 / MSOP8	298	
		SOIC−8	250	
		UDFN8	228	
		SOIC−14	216	

5. As mounted on an 80x80x1.5 mm FR4 PCB with 650 mm^2 and 2 oz (0.07 mm) thick copper heat spreader. Following JEDEC JESD/EIA 51.1, 51.2, 51.3 test guidelines

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Range	Unit
Supply Voltage ($V_{DD} - V_{SS}$)	V_S	1.8 to 5.5	V
Specified Operating Temperature Range	T_A	−40 to 125	°C
Input Common Mode Voltage Range	V_{CM}	V_{SS}−0.1 to V_{DD}+0.1	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = 1.8 V to 5.5 V
At T_A = +25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
Boldface limits apply over the specified operating temperature range, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_S = +5 V		6	50	μV
Offset Voltage Drift vs Temp	$\Delta V_{OS}/\Delta T$	V_S = 5 V		**0.1**	**0.25**	μV/°C
Offset Voltage Drift vs Temp	$\Delta V_{OS}/\Delta V_S$	T_A = +25°C		0.4	8	μV/V
		Full temperature range			**12.6**	
Input Bias Current (Note 6)	I_{IB}	T_A = +25°C		±60	±300	pA
		Full temperature range		**±400**		
Input Offset Current (Note 6)	I_{OS}	T_A = +25°C		±50	±600	pA
Common Mode Rejection Ratio (Note 7)	CMRR	V_S = 1.8 V		111		dB
		V_S = 3.3 V		118		
		V_S = 5.0 V	100	123		
		V_S = 5.5 V		127		
Input Capacitance	C_{IN}	Differential		4.1		pF
		Common Mode		7.9		
OUTPUT CHARACTERISTICS						
Open Loop Voltage Gain (Note 6)	A_{VOL}	V_{SS} + 100 mV < V_O < V_{DD} − 100 mV	**100**	145		dB
Open Loop Output Impedance	Z_{out-OL}		See Figure 18			Ω
Output Voltage High, Referenced to V_{DD}	V_{OH}	T_A = +25°C		10	50	mV
		Full temperature range			**70**	
Output Voltage Low, Referenced to V_{SS}	V_{OL}	T_A = +25°C		10	50	mV
		Full temperature range			**70**	
	I_O	Sinking Current		11		mA
		Sourcing Current		5.0		
Capacitive Load Drive	C_L		See Figure 14			
NOISE PERFORMANCE						
Voltage Noise Density	e_N	f_{IN} = 1 kHz		62		nV / $\sqrt{Hz}$
Voltage Noise	e_{P-P}	f_{IN} = 0.1 Hz to 10 Hz		1.1		μV_{PP}
		f_{IN} = 0.01 Hz to 1 Hz		0.5		
Current Noise Density	i_N	f_{IN} = 10 Hz		350		fA / $\sqrt{Hz}$
Channel Separation		NCS330, NCS4330		135		dB
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBWP	C_L = 100 pF, NCS330, NCS4330		350		kHz
		C_L = 100 pF, NCS2330		270		
Gain Margin	A_M	C_L = 100 pF		18		dB
Phase Margin	ϕ_M	C_L = 100 pF		55		°
Slew Rate	SR	G = +1		0.15		V/μs

6. Guaranteed by characterization and/or design
7. Specified over the full common mode range: V_{SS} − 0.1 < V_{CM} < V_{DD} + 0.1
8. No load, per channel

ELECTRICAL CHARACTERISTICS: V_S = 1.8 V to 5.5 V
At T_A = +25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.
Boldface limits apply over the specified operating temperature range, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	T_A = +25°C	106	130		dB
		Full temperature range	**98**			
Turn−on Time	t_{ON}	V_S = 5 V		100		μs
Quiescent Current (Note 8)	I_Q	1.8 V ≤ V_S ≤ 3.3 V		20	30	μA
					35	
		3.3 V < V_S ≤ 5.5 V		28	40	
					45	

6. Guaranteed by characterization and/or design
7. Specified over the full common mode range: V_{SS} − 0.1 < V_{CM} < V_{DD} + 0.1
8. No load, per channel

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

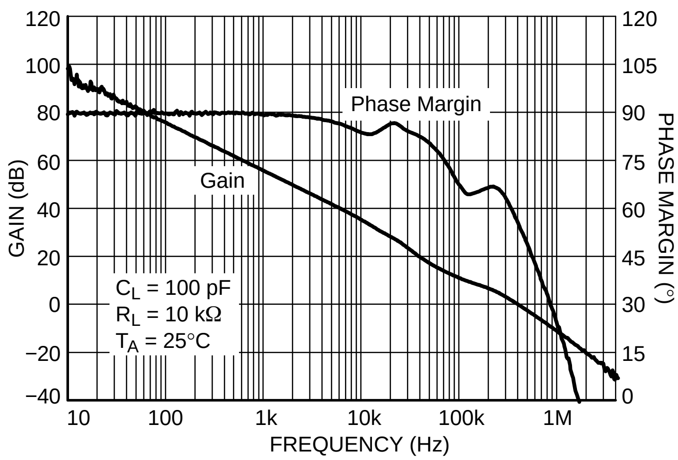


Figure 1. Open Loop Gain and Phase Margin vs. Frequency

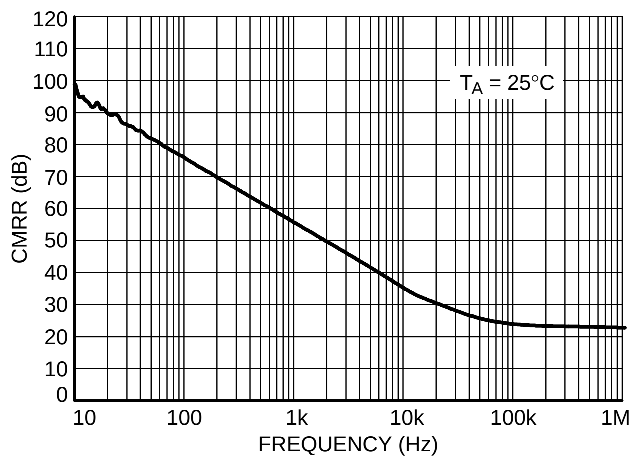


Figure 2. CMRR vs. Frequency

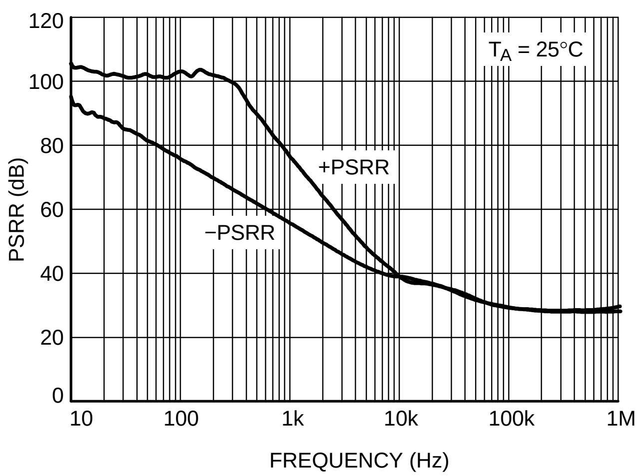


Figure 3. PSRR vs. Frequency

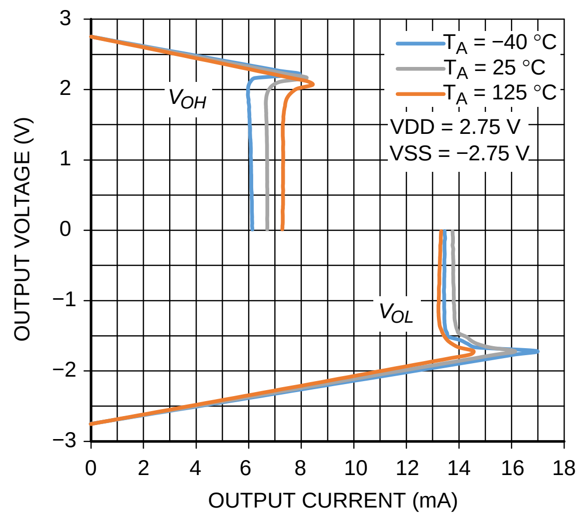


Figure 4. Output Voltage Swing vs. Output Current at V_S = 5.5 V

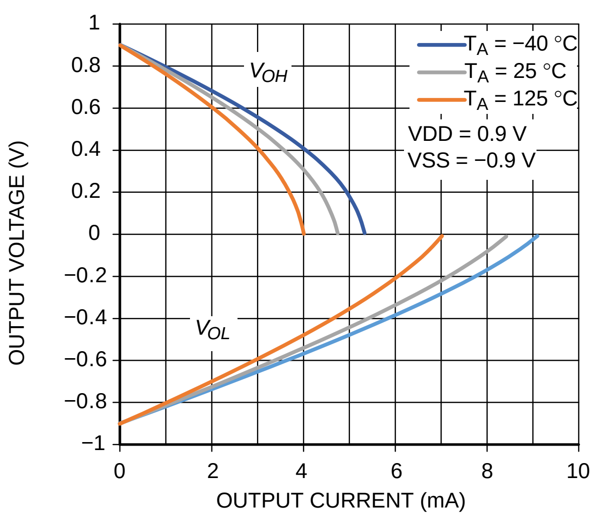


Figure 5. Output Voltage Swing vs. Output Current at V_S = 1.8 V

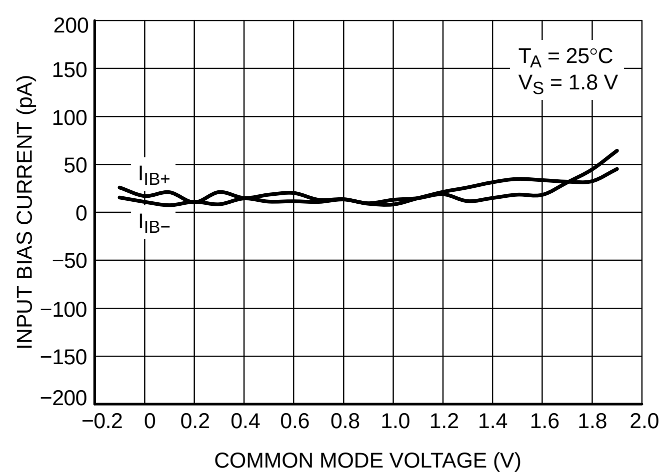


Figure 6. Input Bias Current vs. Common Mode Voltage

TYPICAL CHARACTERISTICS

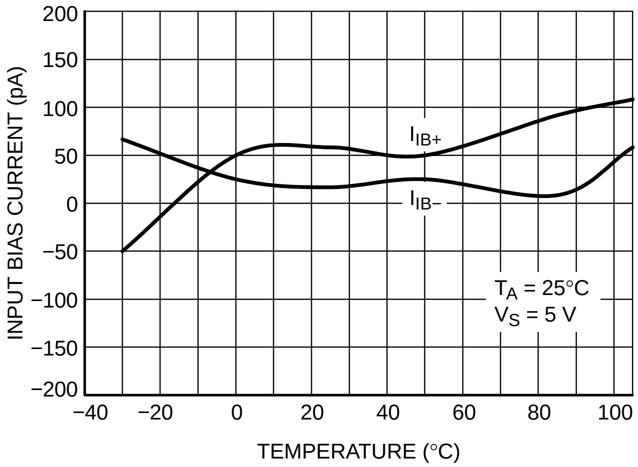


Figure 7. Input Bias Current vs. Temperature

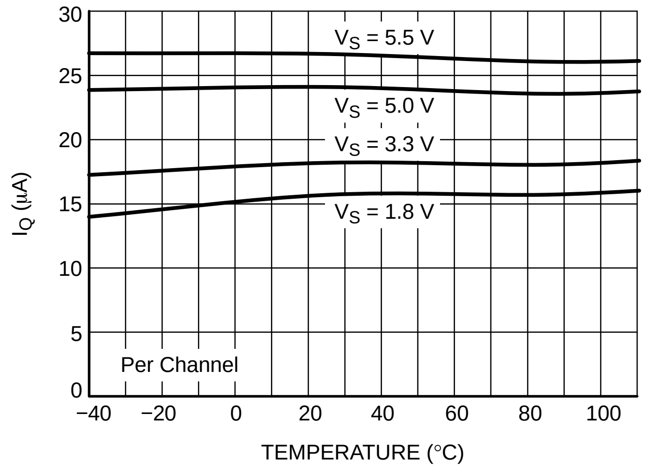


Figure 8. Quiescent Current vs. Temperature

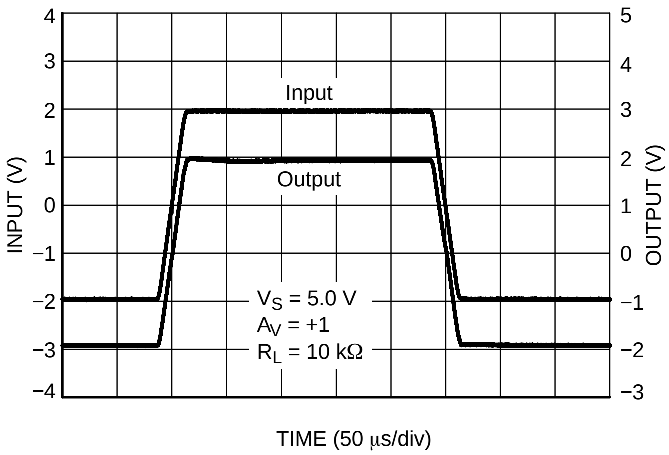


Figure 9. Large Signal Step Response

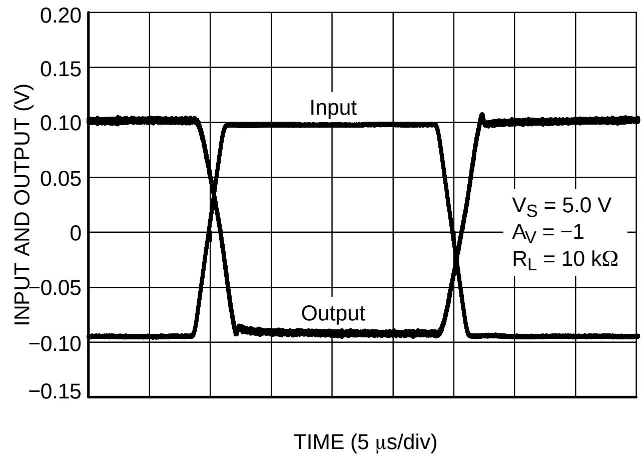


Figure 10. Small Signal Step Response

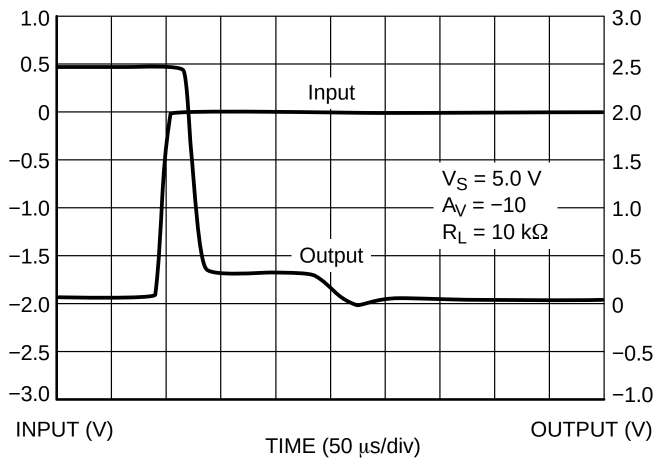


Figure 11. Positive Overvoltage Recovery

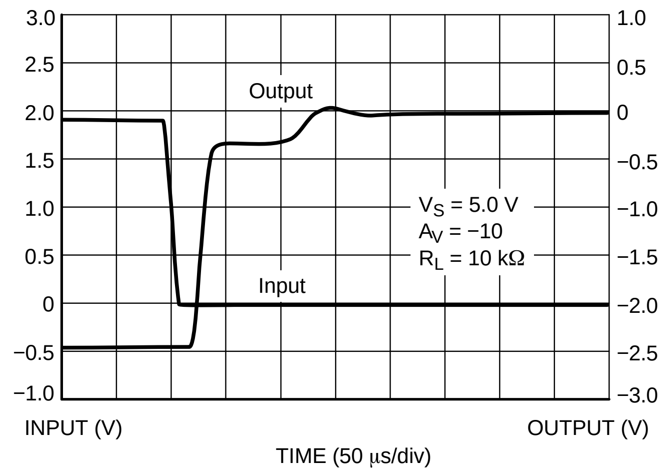


Figure 12. Negative Overvoltage Recovery

TYPICAL CHARACTERISTICS

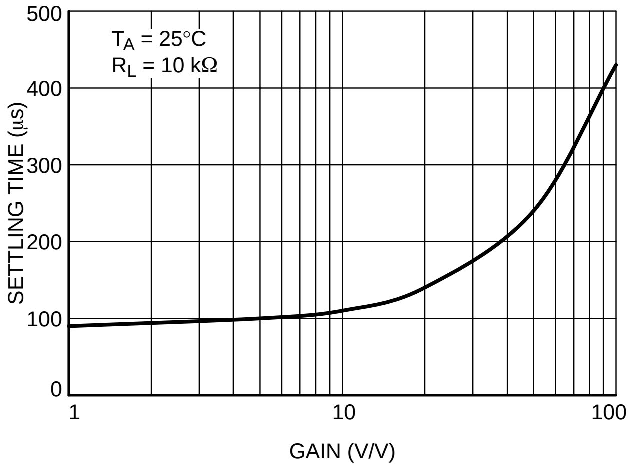


Figure 13. Setting Time to 0.1% vs. Closed−Loop Gain

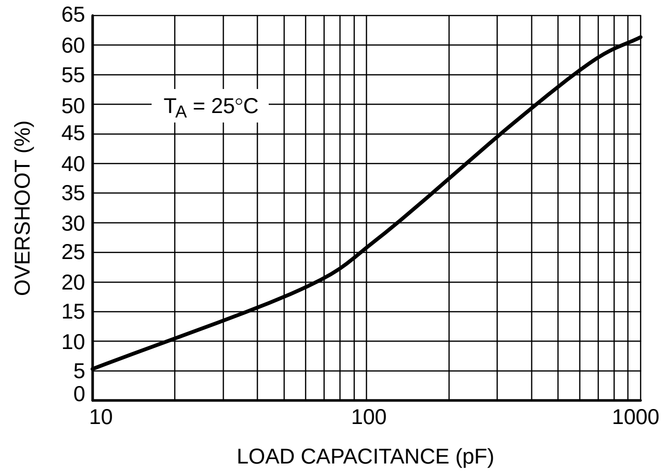


Figure 14. Small−Signal Overshoot vs. Load Capacitance

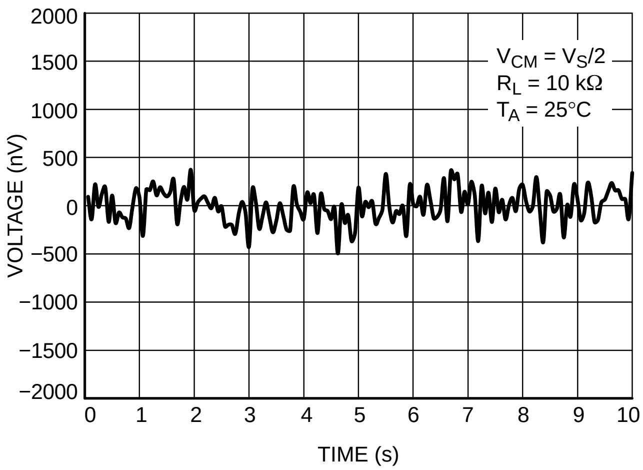


Figure 15. 0.1 Hz to 10 Hz Noise

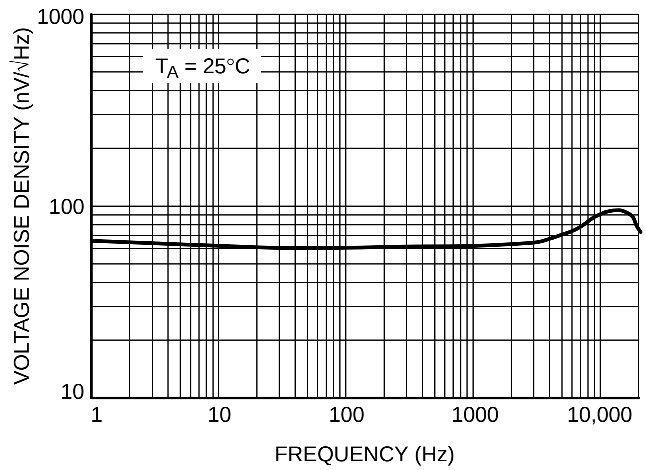


Figure 16. Voltage Noise Density vs. Frequency

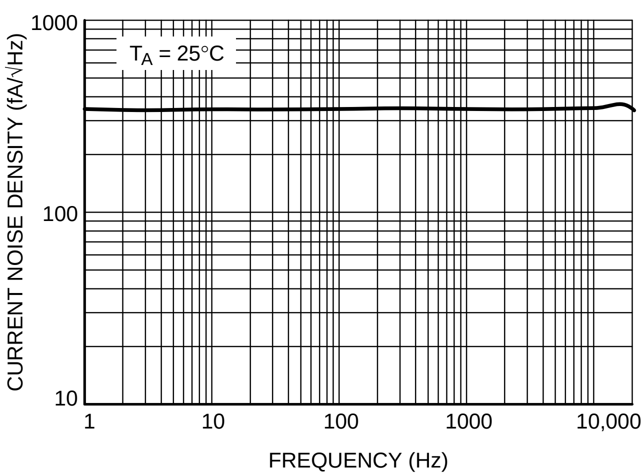


Figure 17. Current Noise Density vs. Frequency

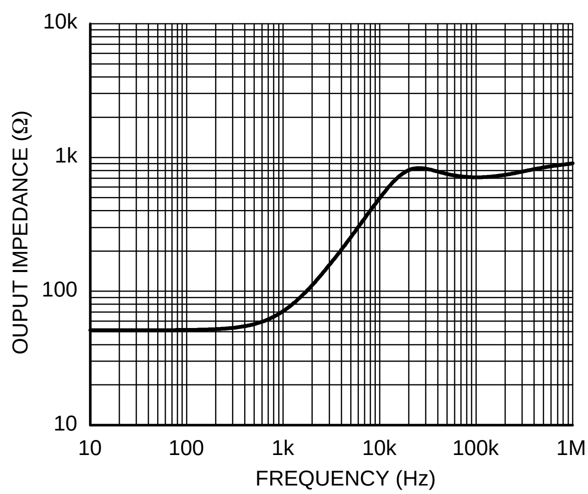


Figure 18. Open Loop Output Impedance vs. Frequency

APPLICATIONS INFORMATION

OVERVIEW

The NCS330, NCS2330, and NCS4330 precision op amps provide low offset voltage and zero drift over temperature. The input common mode voltage range extends 100 mV beyond the supply rails to allow for sensing near ground or VDD. These features make the NCS330 series well−suited for applications where precision is required, such as current sensing and interfacing with sensors.

The NCS330 series of precision op amps uses a chopper−stabilized architecture, which provides the advantage of minimizing offset voltage drift over temperature and time. The simplified block diagram is shown in Figure 19. Unlike the classical chopper architecture, the chopper stabilized architecture has two signal paths.

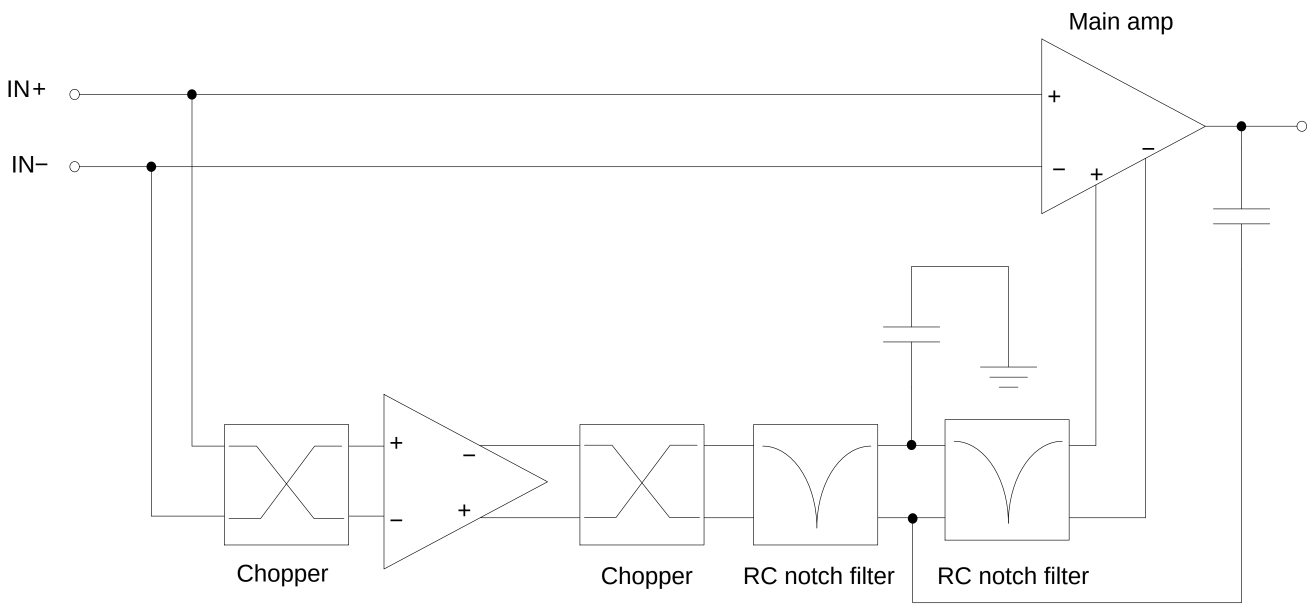


Figure 19. Simplified NCS330 Block Diagram

In Figure 19, the lower signal path is where the chopper samples the input offset voltage, which is then used to correct the offset at the output. The offset correction occurs at a frequency of 125 kHz. The chopper−stabilized architecture is optimized for best performance at frequencies up to the related Nyquist frequency (1/2 of the offset correction frequency). As the signal frequency exceeds the Nyquist frequency, 62.5 kHz, aliasing may occur at the output. This is an inherent limitation of all chopper and chopper−stabilized architectures. Nevertheless, the NCS330 op amps have minimal aliasing up to 125 kHz and low aliasing up to 190 kHz when compared to competitor parts from other manufacturers. ON Semiconductor’s patented approach utilizes two cascaded, symmetrical, RC notch filters tuned to the chopper frequency and its fifth harmonic to reduce aliasing effects.

The chopper−stabilized architecture also benefits from the feed−forward path, which is shown as the upper signal path of the block diagram in Figure 19. This is the high speed signal path that extends the gain bandwidth up to 350 kHz. Not only does this help retain high frequency components of the input signal, but it also improves the loop gain at low frequencies. This is especially useful for low−side current sensing and sensor interface applications where the signal is low frequency and the differential voltage is relatively small.

APPLICATION CIRCUITS

Low−Side Current Sensing

Low−side current sensing is used to monitor the current through a load. This method can be used to detect over−current conditions and is often used in feedback control, as shown in Figure 20. A sense resistor is placed in series with the load to ground. Typically, the value of the sense resistor is less than 100 mΩ to reduce power loss across the resistor. The op amp amplifies the voltage drop across the sense resistor with a gain set by external resistors R1, R2, R3, and R4 (where R1 = R2, R3 = R4). Precision resistors are required for high accuracy, and the gain is set to utilize the full scale of the ADC for the highest resolution.

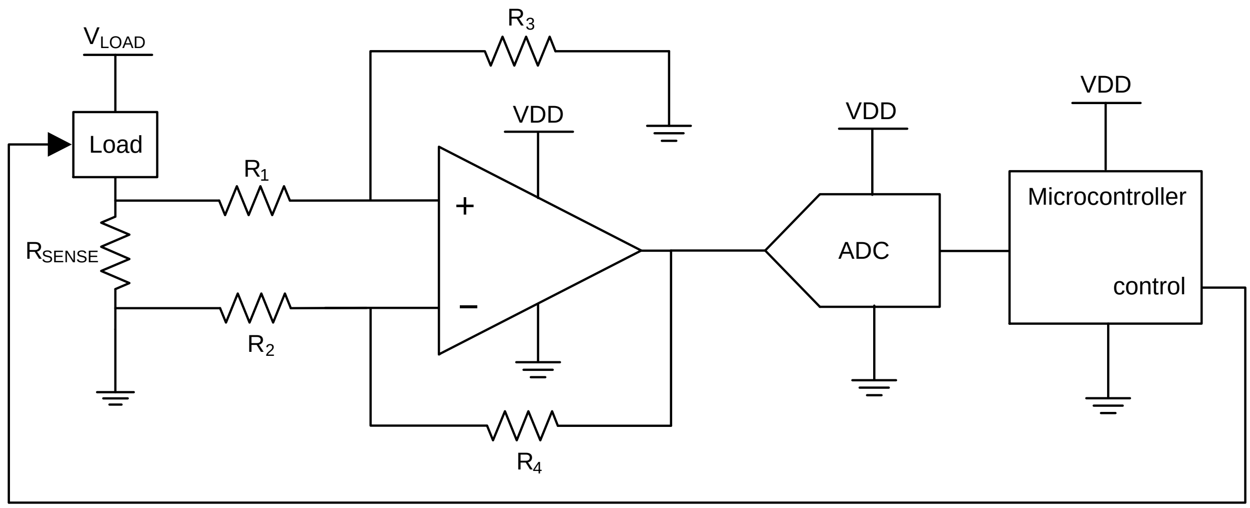


Figure 20. Low−Side Current Sensing

Differential Amplifier for Bridged Circuits

Sensors to measure strain, pressure, and temperature are often configured in a Wheatstone bridge circuit as shown in Figure 21. In the measurement, the voltage change that is produced is relatively small and needs to be amplified before going into an ADC. Precision amplifiers are recommended in these types of applications due to their high gain, low noise, and low offset voltage.

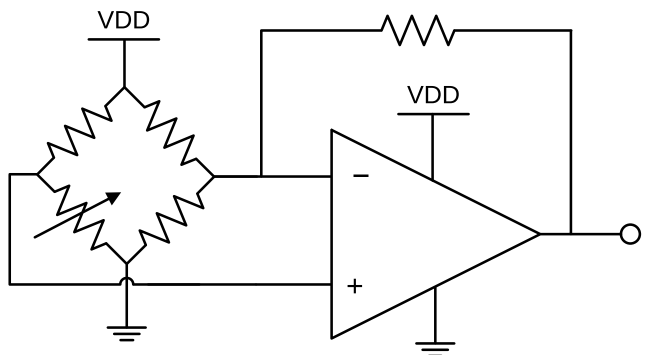


Figure 21. Bridge Circuit Amplification

EMI Susceptibility and Input Filtering

Op amps have varying amounts of EMI susceptibility. Semiconductor junctions can pick up and rectify EMI signals, creating an EMI−induced voltage offset at the output, adding another component to the total error. Input pins are the most sensitive to EMI. The NCS330 op amp family integrates low−pass filters to decrease sensitivity to EMI.

General Layout Guidelines

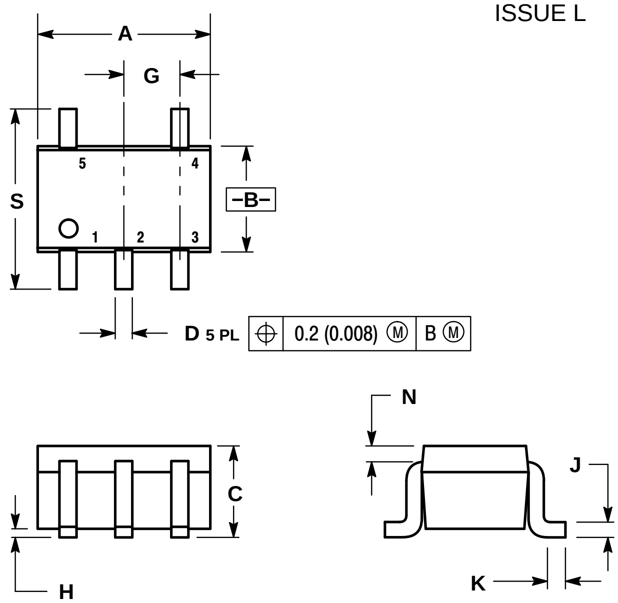
To ensure optimum device performance, it is important to follow good PCB design practices. Place 0.1 μF decoupling capacitors as close as possible to the supply pins. Keep traces short, utilize a ground plane, choose surface−mount components, and place components as close as possible to the device pins. These techniques will reduce susceptibility to electromagnetic interference (EMI). Thermoelectric effects can create an additional temperature dependent offset voltage at the input pins. To reduce these effects, use metals with low thermoelectric−coefficients and prevent temperature gradients from heat sources or cooling fans.

UDFN8 Package Guidelines

The UDFN8 package has an exposed leadframe die pad on the underside of the package. This pad should be soldered to the PCB, as shown in the recommended soldering footprint in the Package Dimensions section of this datasheet. The center pad can be electrically connected to VSS or it may be left floating. When connected to VSS, the center pad acts as a heat sink, improving the thermal resistance of the part.

PACKAGE DIMENSIONS

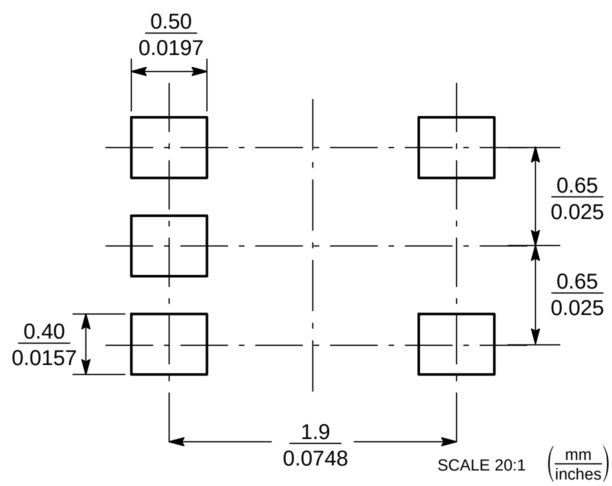
SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

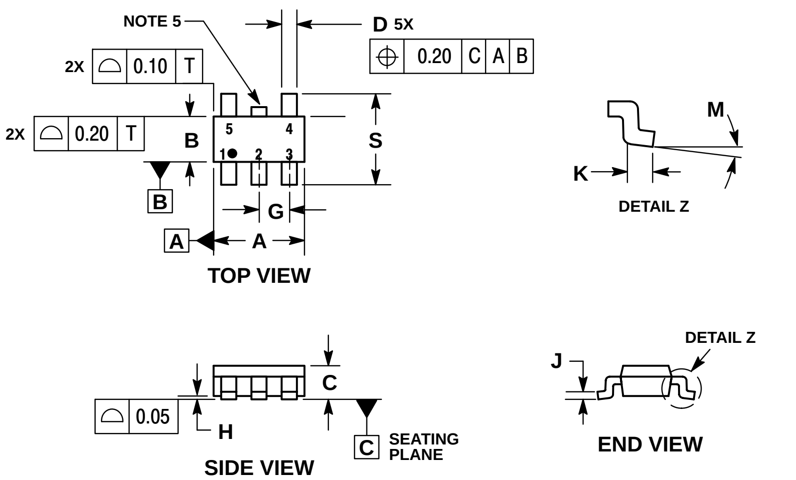
SOLDER FOOTPRINT



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

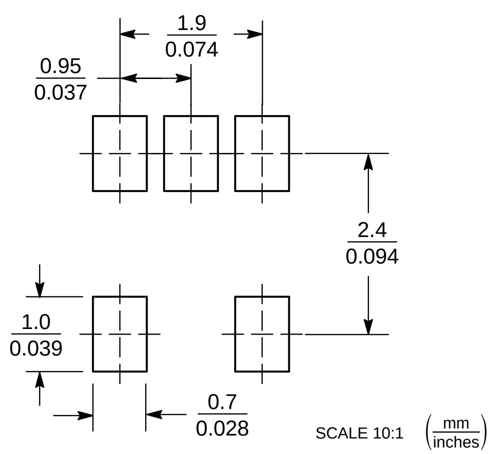
TSOP−5
CASE 483−02
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

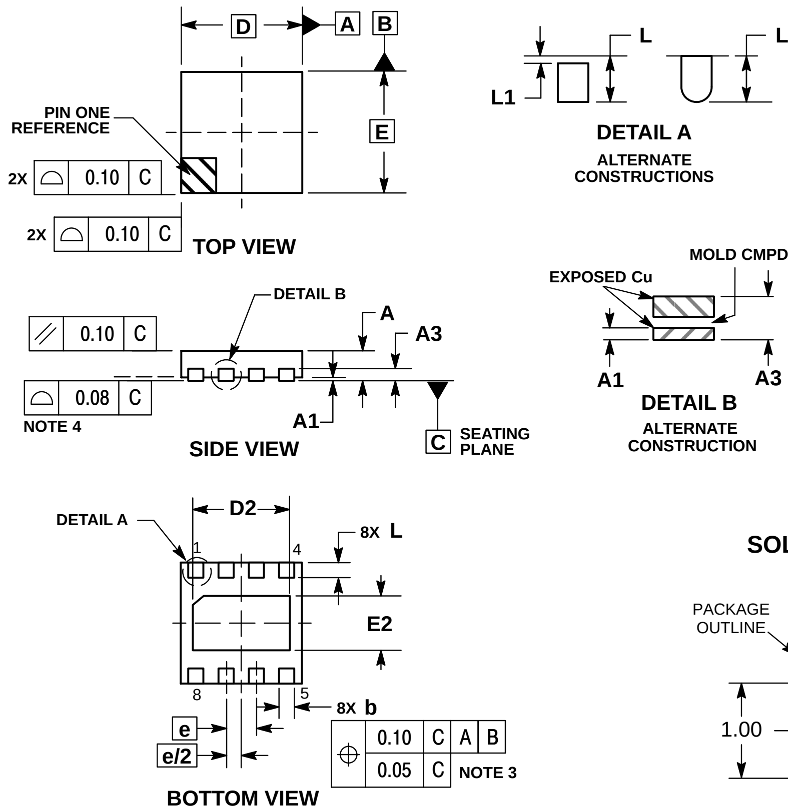
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

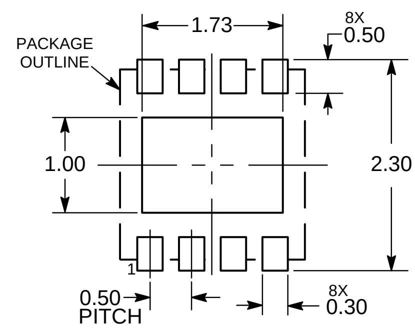
UDFN8, 2x2
CASE 517AW
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.18	0.30
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.50 BSC	
L	0.20	0.45
L1	---	0.15

RECOMMENDED SOLDERING FOOTPRINT*

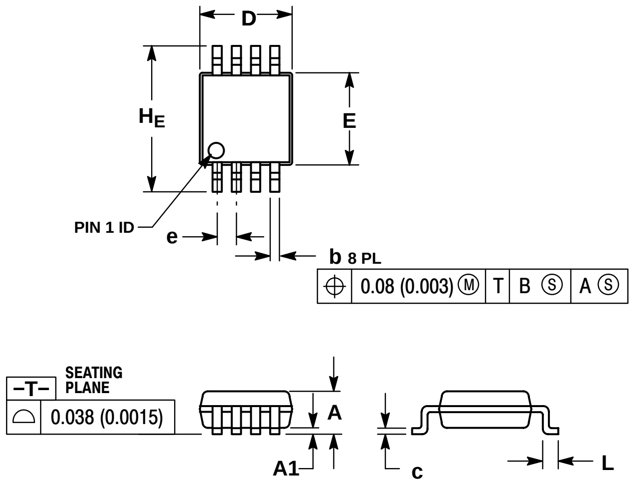


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

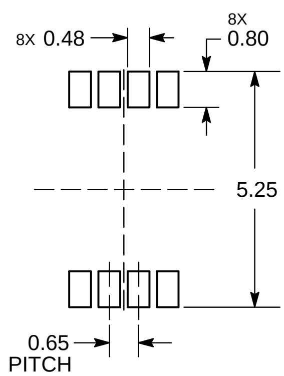
Micro8™
CASE 846A−02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	−−	−−	1.10	−−	−−	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65 BSC			0.026 BSC	
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

RECOMMENDED SOLDERING FOOTPRINT*

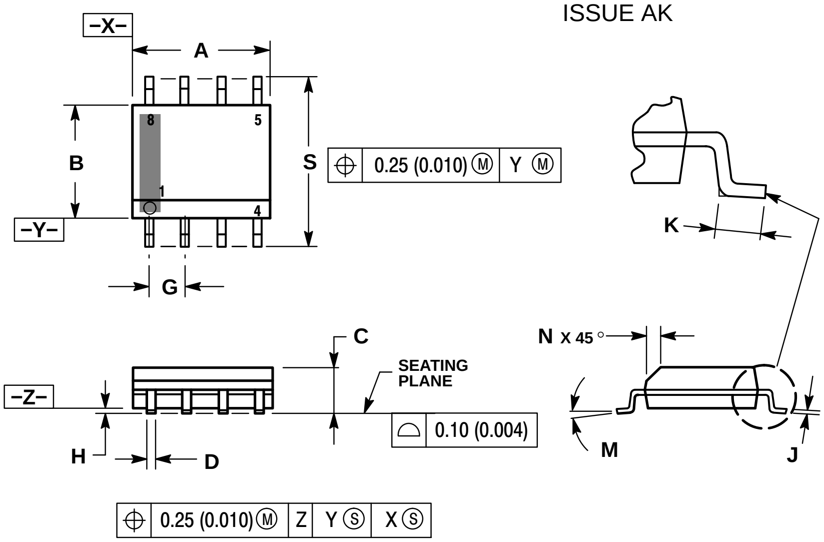


DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

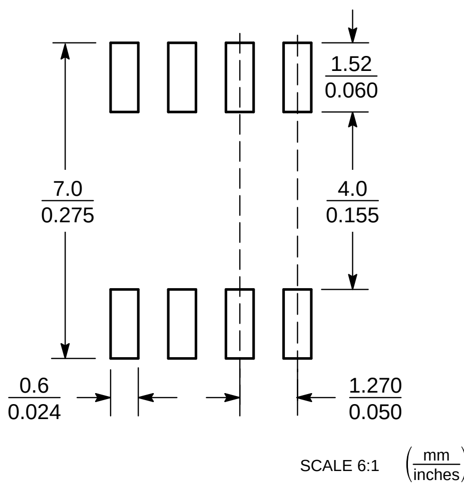
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

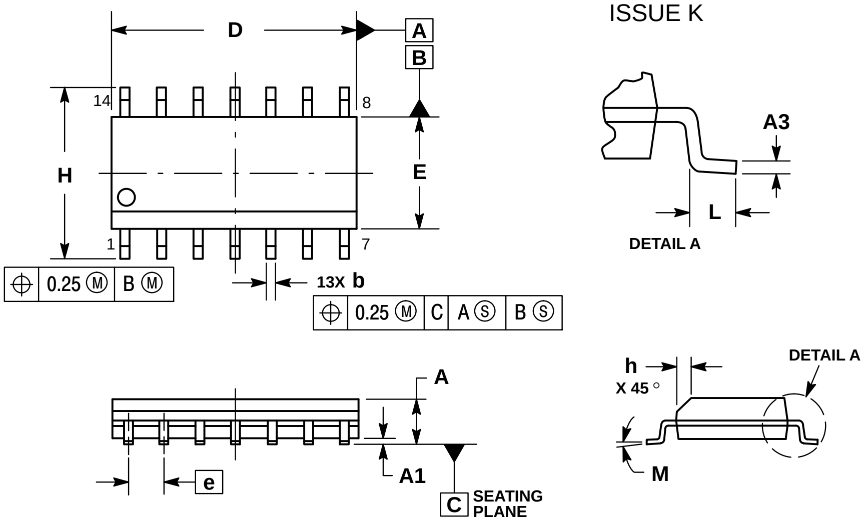
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

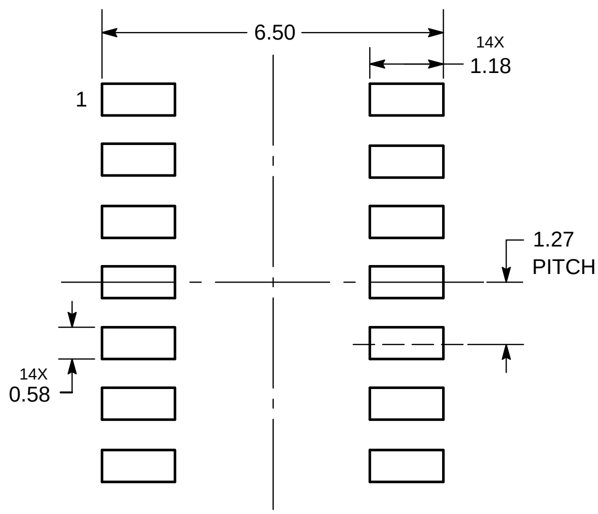
SOIC−14 NB
CASE 751A−03
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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