# NTMFD4902NF

# MOSFET – Power, Dual, N-Channel with Integrated Schottky, SO8FL

## 30 V, High Side 18 A / Low Side 23 A

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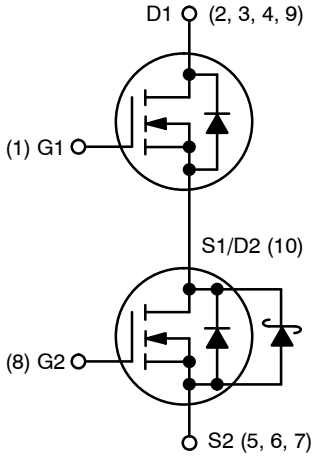
### Features

- Co−Packaged Power Stage Solution to Minimize Board Space
- Low Side MOSFET with Integrated Schottky
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

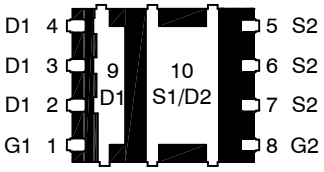
### Applications

- DC−DC Converters
- System Voltage Rails
- Point of Load

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| Q1 Top FET 30 V | 6.5 mΩ @ 10 V | 18 A |
| | 10 mΩ @ 4.5 V | |
| Q2 Bottom FET 30 V | 4.1 mΩ @ 10 V | 23 A |
| | 6.2 mΩ @ 4.5 V | |

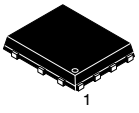



### PIN CONNECTIONS




(Bottom View)

### MARKING DIAGRAM




**DFN8**
**CASE 506BX**


4902NF = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise stated)

| Parameter | | | | Symbol | Value | Unit |
|---|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | Q1 | $V_{DSS}$ | 30 | V |
| Drain−to−Source Voltage | | | Q2 | | | |
| Gate−to−Source Voltage | | | Q1 | $V_{GS}$ | ±20 | V |
| Gate−to−Source Voltage | | | Q2 | | | |
| Continuous Drain Current $R_{\theta JA}$ (Note 1) | Steady State | $T_A$ = 25°C | Q1 | $I_D$ | 13.5 | A |
| | | $T_A$ = 85°C | | | 9.7 | |
| | | $T_A$ = 25°C | Q2 | | 17.5 | |
| | | $T_A$ = 85°C | | | 12.6 | |
| Power Dissipation RθJA (Note 1) | | $T_A$ = 25°C | Q1 | $P_D$ | 1.90 | W |
| | | | Q2 | | 1.99 | |
| Continuous Drain Current $R_{\theta JA} \le 10$ s (Note 1) | | $T_A$ = 25°C | Q1 | $I_D$ | 18.2 | A |
| | | $T_A$ = 85°C | | | 13.1 | |
| | | $T_A$ = 25°C | Q2 | | 23 | |
| | | $T_A$ = 85°C | | | 16.6 | |
| Power Dissipation $R_{\theta JA} \le 10$ s (Note 1) | | $T_A$ = 25°C | Q1 | $P_D$ | 3.45 | W |
| | | | Q2 | | 3.45 | |
| Continuous Drain Current $R_{\theta JA}$ (Note 2) | | $T_A$ = 25°C | Q1 | $I_D$ | 10.3 | A |
| | | $T_A$ = 85°C | | | 7.4 | |
| | | $T_A$ = 25°C | Q2 | | 13.3 | |
| | | $T_A$ = 85°C | | | 9.6 | |
| Power Dissipation $R_{\theta JA}$ (Note 2) | | $T_A$ = 25 °C | Q1 | $P_D$ | 1.10 | W |
| | | | Q2 | | 1.16 | |
| Pulsed Drain Current | | TA = 25°C tp = 10 μs | Q1 | $I_{DM}$ | 60 | A |
| | | | Q2 | | 80 | |
| Operating Junction and Storage Temperature | | | Q1 | $T_J$, $T_{STG}$ | −55 to +150 | °C |
| | | | Q2 | | | |
| Source Current (Body Diode) | | | Q1 | $I_S$ | 3.4 | A |
| | | | Q2 | | 4.9 | |
| Drain to Source dV/dt | | | | dV/dt | 6.0 | V/ns |
| Single Pulse Drain−to−Source Avalanche Energy ($T_J$ = 25C, $V_{DD}$ = 50 V, $V_{GS}$ = 10 V, $I_L$ = XX $A_{pk}$, L = 0.1 mH, $R_G$ = 25 Ω) | | 24 A | Q1 | EAS | 28.8 | mJ |
| | | 27 A | Q2 | EAS | 36.5 | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | | | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 sq−in pad, 2 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size of 100 $mm^2$.

## THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | FET | Symbol | Value | Unit |
|---|---|---|---|---|
| Junction−to−Ambient − Steady State (Note 3) | Q1 | $R_{\theta JA}$ | 65.9 | °C/W |
| | Q2 | | 62.8 | |
| Junction−to−Ambient − Steady State (Note 4) | Q1 | $R_{\theta JA}$ | 113.2 | |
| | Q2 | | 108 | |
| Junction−to−Ambient − (t ≤ 10 s) (Note 3) | Q1 | $R_{\theta JA}$ | 36.2 | |
| | Q2 | | 36.2 | |

3. Surface−mounted on FR4 board using 1 sq−in pad, 2 oz Cu.
4. Surface−mounted on FR4 board using the minimum recommended pad size of 100 $mm^2$.

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise specified)

| Parameter | FET | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | | |
| Drain−to−Source Breakdown Voltage | Q1 | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 30 | | | V |
| | Q2 | | $V_{GS}$ = 0 V, $I_D$ = 1.0 mA | | 30 | | | |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | Q1 | $V_{(BR)DSS}$ / $T_J$ | | | | 18 | | mV / °C |
| | Q2 | | | | | 15 | | |
| Zero Gate Voltage Drain Current | Q1 | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 24 V | $T_J$ = 25°C | | | 1 | μA |
| | | | | $T_J$ = 125°C | | | 10 | |
| | Q2 | | $V_{GS}$ = 0 V, $V_{DS}$ = 24 V | $T_J$ = 25°C | | | 500 | |
| Gate−to−Source Leakage Current | Q1 | $I_{GSS}$ | $V_{GS}$ = 0 V, VDS = ±20 V | | | | ±100 | nA |
| | Q2 | | | | | | ±100 | |
| **ON CHARACTERISTICS** (Note 5) | | | | | | | | |
| Gate Threshold Voltage | Q1 | $V_{GS(TH)}$ | $V_{GS}$ = VDS, $I_D$ = 250 μA | | 1.2 | | 2.2 | V |
| | Q2 | | | | 1.2 | | 2.2 | |
| Negative Threshold Temperature Coefficient | Q1 | $V_{GS(TH)}$ / $T_J$ | | | | 4.5 | | mV / °C |
| | Q2 | | | | | 4.0 | | |
| Drain−to−Source On Resistance | Q1 | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 10 A | | 5.2 | 6.5 | mΩ |
| | | | $V_{GS}$ = 4.5 V | $I_D$ = 10 A | | 8.0 | 10 | |
| | Q2 | | $V_{GS}$ = 10 V | $I_D$ = 15 A | | 3.3 | 4.1 | |
| | | | $V_{GS}$ = 4.5 V | $I_D$ = 15 A | | 5.0 | 6.2 | |
| Forward Transconductance | Q1 | $g_{FS}$ | $V_{DS}$ = 1.5 V, $I_D$ = 10 A | | | 28 | | S |
| | Q2 | | | | | 35 | | |
| **CHARGES, CAPACITANCES & GATE RESISTANCE** | | | | | | | | |
| Input Capacitance | Q1 | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = 15 V | | | 1150 | | pF |
| | Q2 | | | | | 1590 | | |
| Output Capacitance | Q1 | $C_{OSS}$ | | | | 360 | | |
| | Q2 | | | | | 813 | | |
| Reverse Capacitance | Q1 | $C_{RSS}$ | | | | 105 | | |
| | Q2 | | | | | 83 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified)

| Parameter | FET | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **CHARGES, CAPACITANCES & GATE RESISTANCE** | | | | | | | |
| Total Gate Charge | Q1 | $Q_{G(TOT)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V; $I_D$ = 10 A | | 9.7 | | nC |
| | Q2 | | | | 11.5 | | |
| Threshold Gate Charge | Q1 | $Q_{G(TH)}$ | | | 1.1 | | |
| | Q2 | | | | 1.4 | | |
| Gate−to−Source Charge | Q1 | $Q_{GS}$ | | | 3.3 | | |
| | Q2 | | | | 4.2 | | |
| Gate−to−Drain Charge | Q1 | $Q_{GD}$ | | | 3.7 | | |
| | Q2 | | | | 3.4 | | |
| Total Gate Charge | Q1 | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 15 V; $I_D$ = 10 A | | 19.1 | | nC |
| | Q2 | | | | 24.9 | | |
| **SWITCHING CHARACTERISTICS** (Note 6) | | | | | | | |
| Turn−On Delay Time | Q1 | $t_{d(ON)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V, $I_D$ = 10 A, $R_G$ = 3.0 Ω | | 9.0 | | ns |
| | Q2 | | | | 10.5 | | |
| Rise Time | Q1 | $t_r$ | | | 15 | | |
| | Q2 | | | | 15.2 | | |
| Turn−Off Delay Time | Q1 | $t_{d(OFF)}$ | | | 14 | | |
| | Q2 | | | | 17.7 | | |
| Fall Time | Q1 | $t_f$ | | | 4.0 | | |
| | Q2 | | | | 4.7 | | |
| **SWITCHING CHARACTERISTICS** (Note 6) | | | | | | | |
| Turn−On Delay Time | Q1 | $t_{d(ON)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 15 V, $I_D$ = 10 A, $R_G$ = 3.0 Ω | | 6.0 | | ns |
| | Q2 | | | | 7.0 | | |
| Rise Time | Q1 | $t_r$ | | | 14 | | |
| | Q2 | | | | 14 | | |
| Turn−Off Delay Time | Q1 | $t_{d(OFF)}$ | | | 17 | | |
| | Q2 | | | | 22 | | |
| Fall Time | Q1 | $t_f$ | | | 3.0 | | |
| | Q2 | | | | 3.3 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Voltage | Q1 | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 3 A, $T_J$ = 25°C | | 0.75 | 1.0 | V |
| | | | $V_{GS}$ = 0 V, $I_S$ = 3 A, $T_J$ = 125°C | | 0.62 | | |
| | Q2 | | $V_{GS}$ = 0 V, $I_S$ = 2 A, $T_J$ = 25°C | | 0.37 | 0.70 | |
| | | | $V_{GS}$ = 0 V, $I_S$ = 2 A, $T_J$ = 125°C | | 0.31 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified)

| Parameter | FET | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Reverse Recovery Time | Q1 | $t_{RR}$ | $V_{GS}$ = 0 V, $d_{IS}/d_t$ = 100 A/μs, $I_S$ = 3 A | | 23 | | ns |
| | Q2 | | | | 24.5 | | |
| Charge Time | Q1 | ta | | | 12 | | |
| | Q2 | | | | 13 | | |
| Discharge Time | Q1 | tb | | | 11 | | |
| | Q2 | | | | 11.5 | | |
| Reverse Recovery Charge | Q1 | $Q_{RR}$ | | | 12 | | nC |
| | Q2 | | | | 24 | | |
| **PACKAGE PARASITIC VALUES** | | | | | | | |
| Source Inductance | Q1 | $L_S$ | $T_A$ = 25°C | | 0.38 | | nH |
| | Q2 | | | | 0.65 | | |
| Drain Inductance | Q1 | $L_D$ | | | 0.054 | | nH |
| | Q2 | | | | 0.007 | | |
| Gate Inductance | Q1 | $L_G$ | | | 1.5 | | nH |
| | Q2 | | | | 1.5 | | |
| Gate Resistance | Q1 | $R_G$ | | | 0.8 | | Ω |
| | Q2 | | | | 0.8 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NTMFD4902NFT1G | DFN8 (Pb−Free) | 1500 / Tape & Reel |
| NTMFD4902NFT3G | DFN8 (Pb−Free) | 5000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## TYPICAL CHARACTERISTICS – Q1

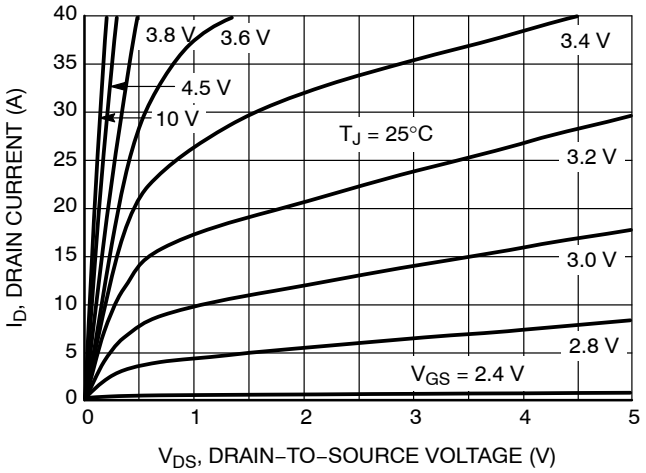



**Figure 1. On−Region Characteristics**

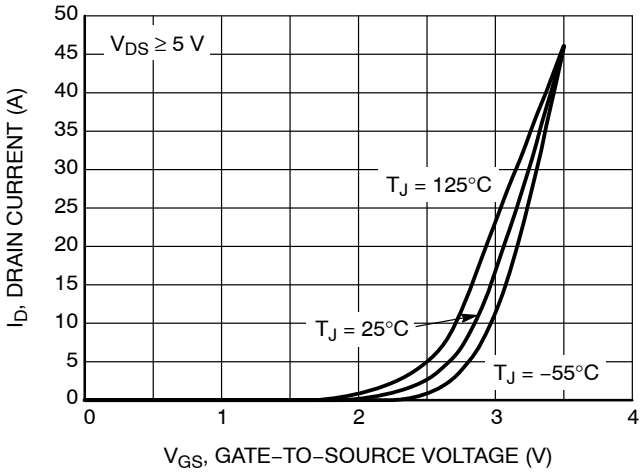



**Figure 2. Transfer Characteristics**

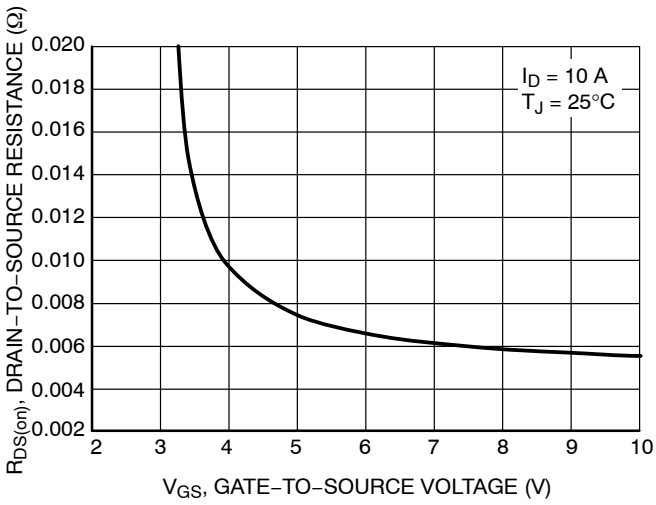



**Figure 3. On−Resistance vs. Gate−to−Source Resistance**

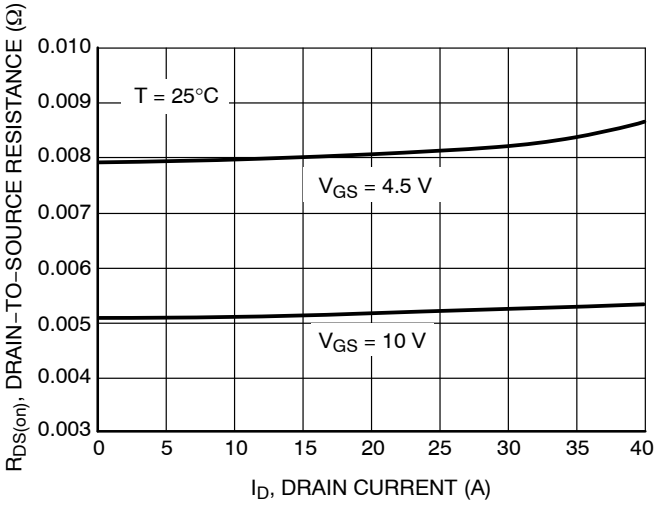



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

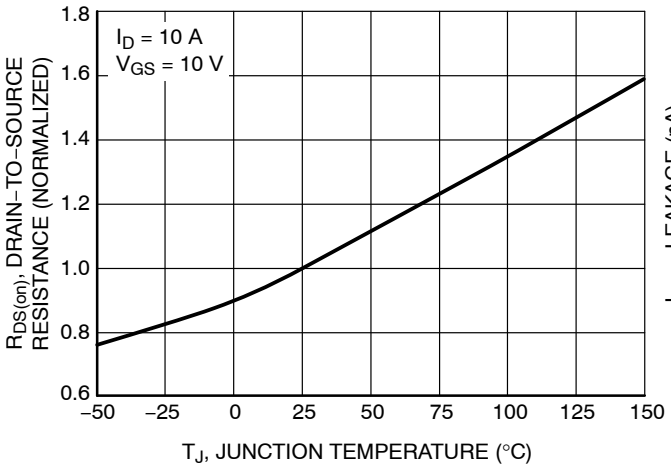



**Figure 5. On−Resistance Variation with Temperature**

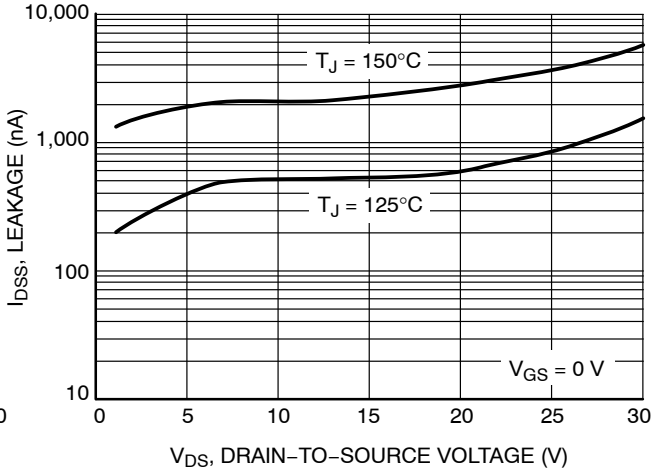



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL CHARACTERISTICS – Q1

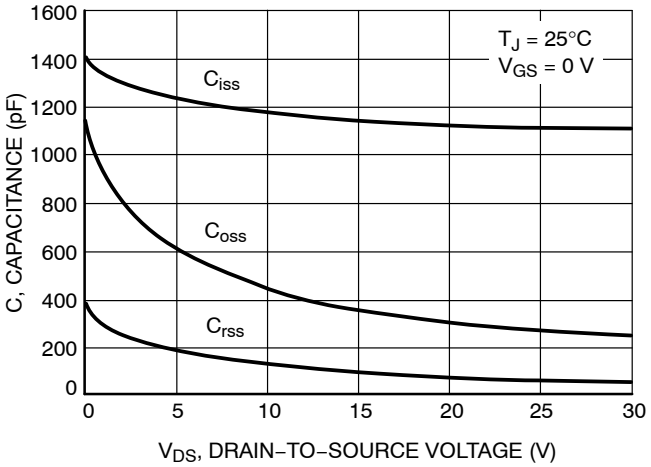



**Figure 7. Capacitance Variation**

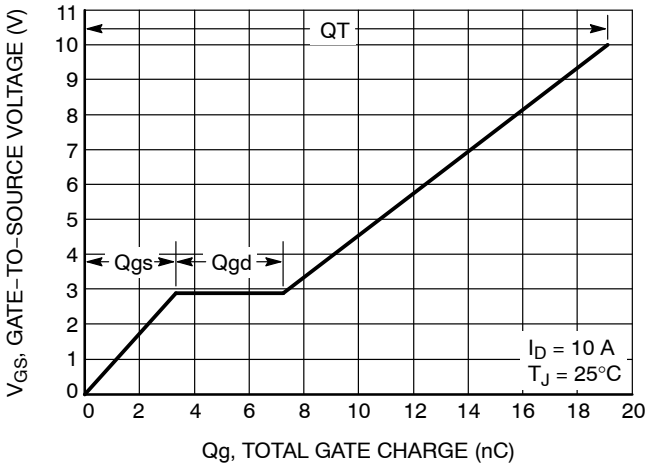



**Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

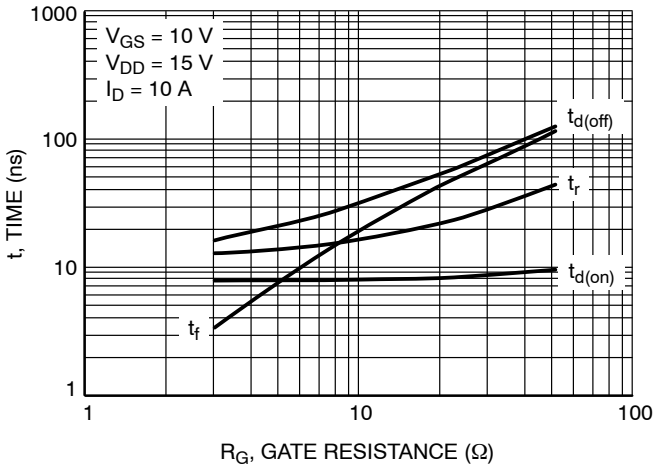



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

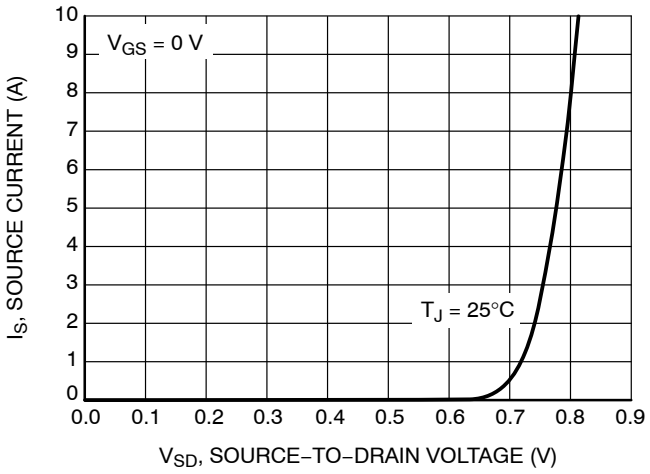



**Figure 10. Diode Forward Voltage vs. Current**

## TYPICAL CHARACTERISTICS – Q2

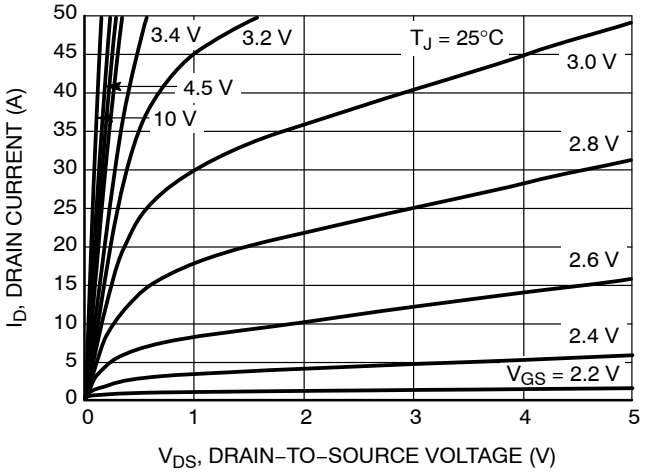



**Figure 11. On−Region Characteristics**

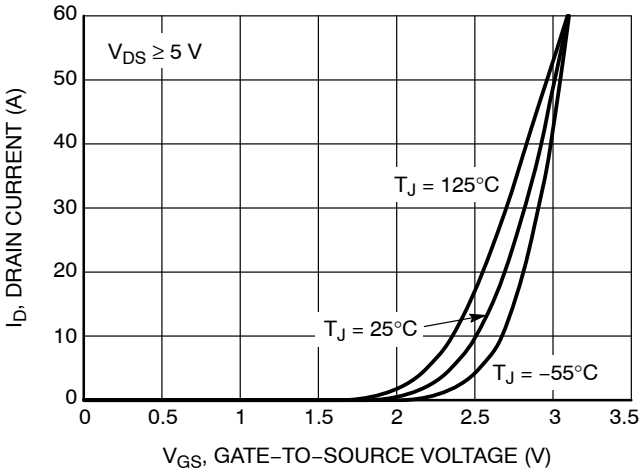



**Figure 12. Transfer Characteristics**

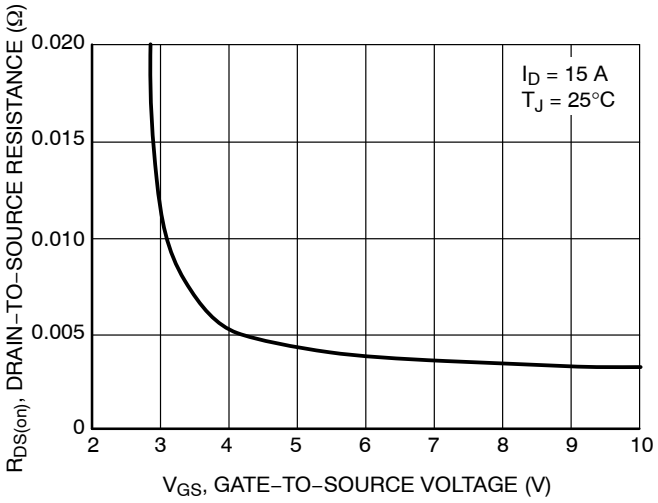



**Figure 13. On−Resistance vs. Gate−to−Source Resistance**

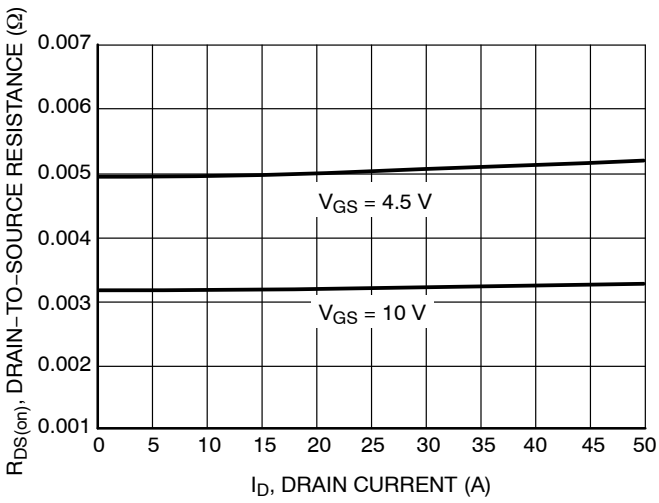



**Figure 14. On−Resistance vs. Drain Current and Gate Voltage**

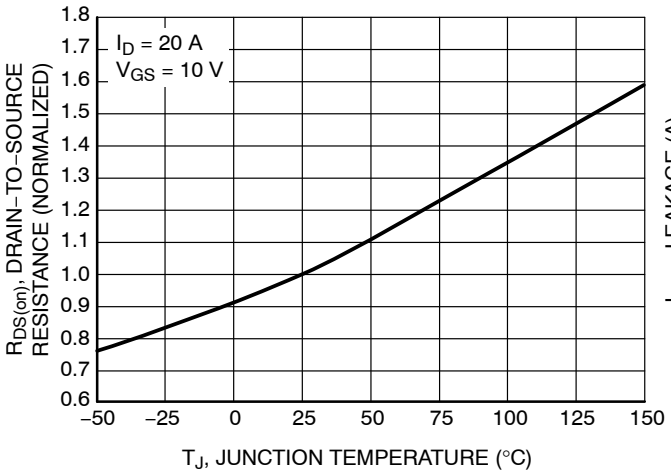



**Figure 15. On−Resistance Variation with Temperature**

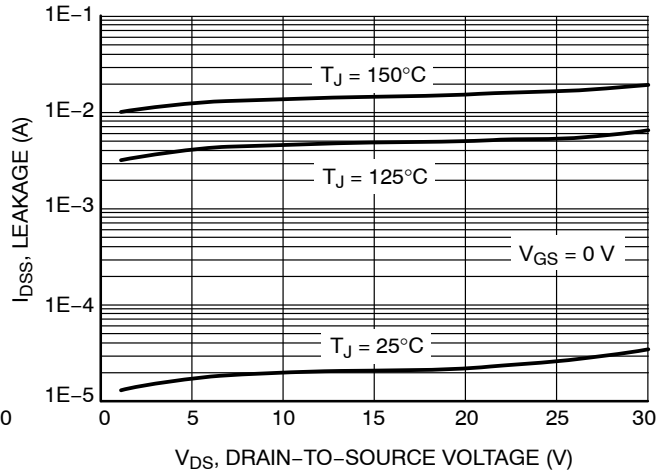



**Figure 16. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL CHARACTERISTICS – Q2

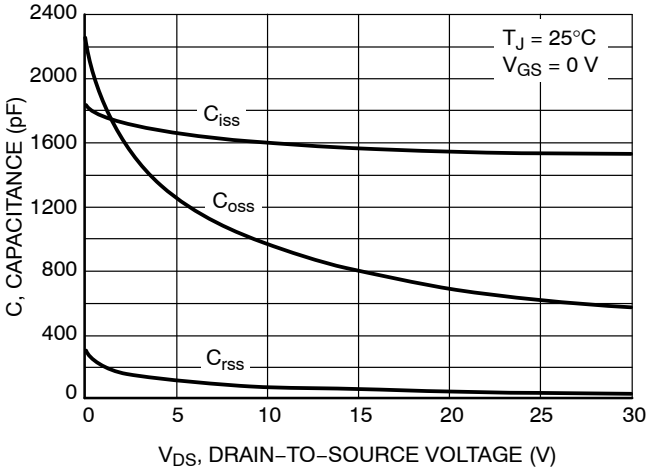



**Figure 17. Capacitance Variation**

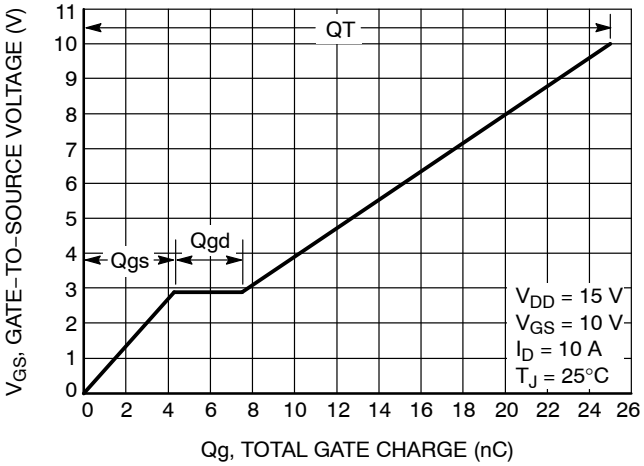



**Figure 18. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

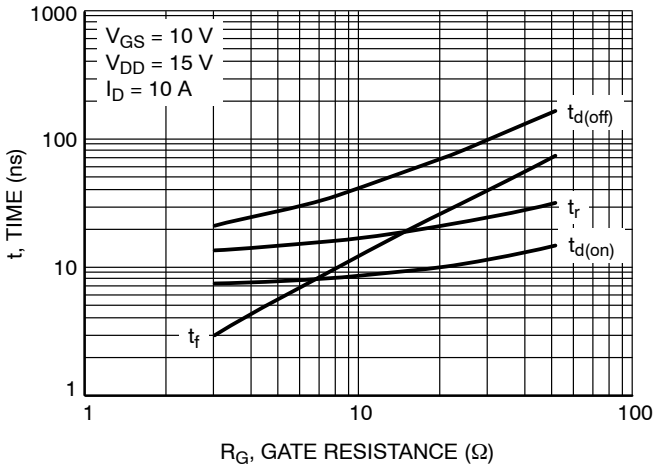



**Figure 19. Resistive Switching Time Variation vs. Gate Resistance**

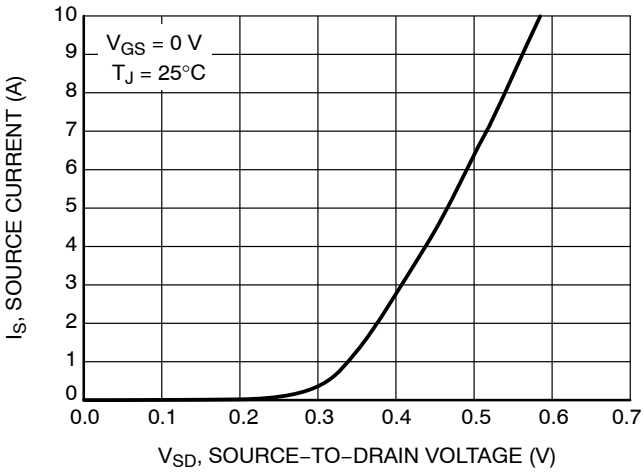
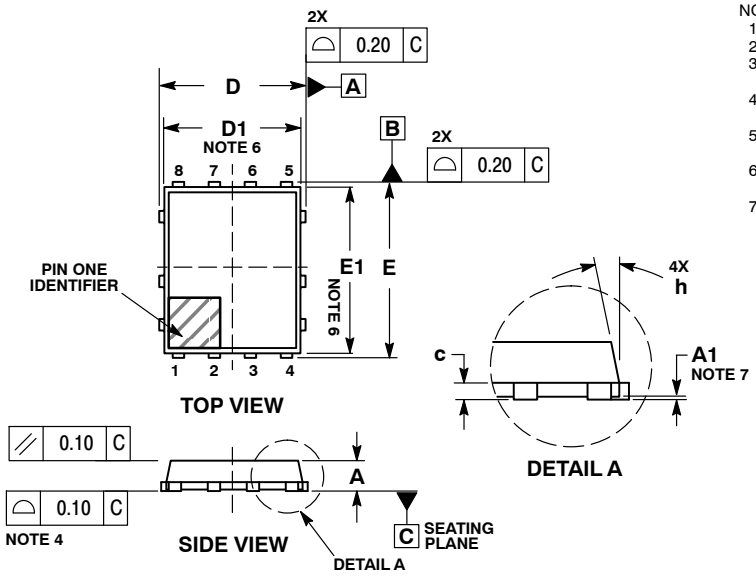
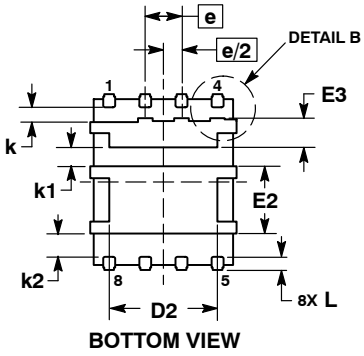


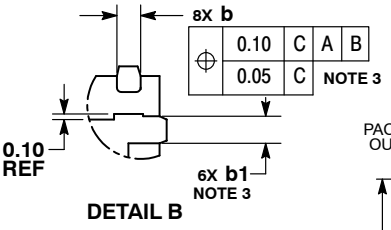

**Figure 20. Diode Forward Voltage vs. Current**

## PACKAGE DIMENSIONS

**DFN8 5x6, 1.27P Dual Flag (SO8FL−Dual−Asymmetrical)**
CASE 506BX
ISSUE D



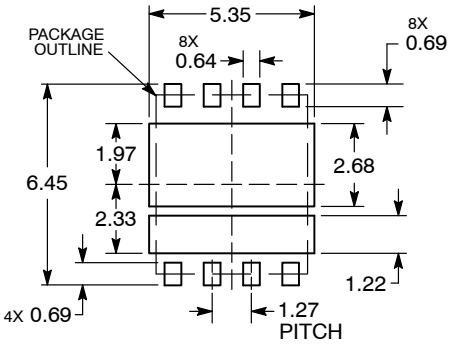




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. DIMENSIONS b AND L ARE MEASURED AT THE PACKAGE SURFACE
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
7. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.90 | 1.10 |
| A1 | 0.00 | 0.05 |
| b | 0.41 | 0.61 |
| b1 | 0.41 | 0.61 |
| c | 0.23 | 0.33 |
| D | 5.00 | 5.30 |
| D1 | 4.50 | 5.10 |
| D2 | 3.50 | 4.22 |
| E | 6.00 | 6.30 |
| E1 | 5.50 | 6.10 |
| E2 | 2.27 | 2.67 |
| E3 | 0.82 | 1.22 |
| e | 1.27 BSC | |
| h | −−− | 12 ° |
| k | 0.39 | 0.59 |
| k1 | 0.56 | 0.76 |
| k2 | 0.73 | 0.93 |
| L | 0.35 | 0.55 |

**RECOMMENDED SOLDERING FOOTPRINT***




DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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