REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add new device types 05-08. - phn	08-11-17	Thomas M. Hess
B	Add case outline N and 4. - phn	09-12-02	Thomas M. Hess
C	Add device type 09 and 10. Add case outline 5 and 6. Update the boilerplate to current requirements as specified in MIL-PRF-38535. - phn	11-06-10	David J. Corbett
D	Add case outline 7. - phn	12-12-03	Thomas M. Hess

REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D												
SHEET	15	16	17	18	19	20	21	22												

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Phu H. Nguyen

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thoma M. Hess

DRAWING APPROVAL DATE
06-07-18

MICROCIRCUIT, DIGITAL, GATE ARRAY, CMOS, ATC18RHA CELL BASED, MONOLITHIC SILICON

REVISION LEVEL
D

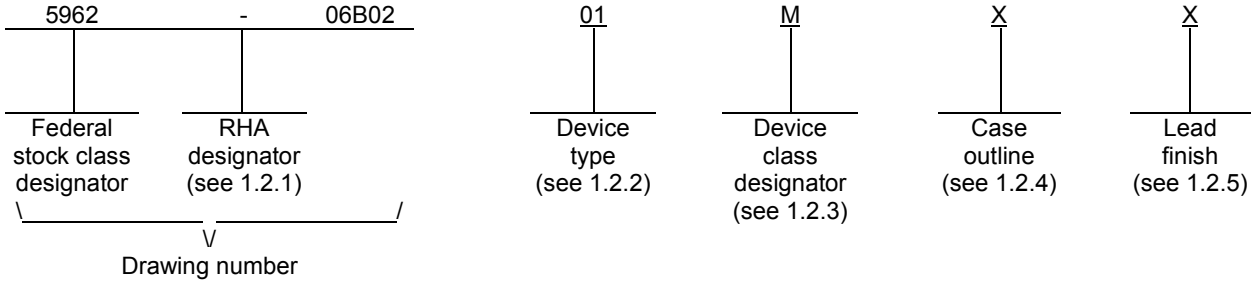
SIZE	CAGE CODE	
A	**67268**	**5962-06B02**

SHEET 1 OF 19

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	ATC18RHA95_216	1.0 Mgates available
02 1/	ATC18RHA95_324	2.2 Mgates available
03 1/	ATC18RHA95_404	3.5 Mgates available
04 1/	ATC18RHA95_504	5.5 Mgates available
05 1/	ATC18RHA95_216	1.0 Mgates available
06 1/	ATC18RHA95_324	2.2 Mgates available
07 1/	ATC18RHA95_404	3.5 Mgates available
08 1/	ATC18RHA95_504	5.5 Mgates available
09 1/	ATC18RHA95_544	6.5 Mgates available
10 1/	ATC18RHA95_544	6.5 Mgates available

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1/ Device types 01-04, 09 will have I/O33 supplied at 3.3 V only and device types 05-08, 10 will have I/O33 supplied at 2.5 V.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	160	Quad flatpack unformed leads
Y	See figure 1	196	Quad flatpack unformed leads
Z	See figure 1	256	Quad flatpack unformed leads
U	See figure 1	352	Quad flatpack with non conductive tie bar
T	See figure 1	349	Column grid array and interposer SCI
M	See figure 1	472	Column grid array and interposer SCI
N	See figure 1	349	Land grid array
4	See figure 1	472	Land grid array
5	See figure 1	625	Land grid array
6	See figure 1	625	Land grid array
7	See figure 1	352	Quad flatpack with non conductive tie bar

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range (V_{DD1}) ..... -0.3 to 2.0 V 4/
Supply voltage range (V_{DD2}) ..... -0.3 to 4.0 V 5/
Input voltage range (V_{IN}) ..... -0.3 to 4.0 V 5/
Input pin current (I_{IN}):
Signal pin ..... -10 mA to 10 mA
Power pin ..... -60 mA to 60 mA
Lead temperature (soldering 10 sec) ..... +300°C 6/
Storage temperature range (TS) ..... -65°C to +150°C
Maximum junction temperature (TJ) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD1}) ..... 1.65 V to 1.95 V 4/
Supply voltage range (V_{DD2}) ..... 3.0 V to 3.6 V or 2.3 V to 2.7 V 5/
Input voltage range (V_{IN}) ..... 0 V to V_{DD2} V 5/
Ambient temperature (T_A) ..... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available (Dose rate = 0.1 Rad(Si)/s) ..... 100 kRads (Si) 7/

2/ This absolute maximum ratings guarantees that the device will not be burned if those maximum voltages are applied during a very limited period of time. This is not a guarantee of functionality or reliability. The users must be warned that if a voltage exceeding the maximum (nominal +10%) and below this absolute maximum rating voltages, is applied to the devices, the reliability of the device will be affected.
3/ All voltages referenced to ground unless otherwise specified.
4/ For core.
5/ For interface, I/O's.
6/ Duration 10 sec maximum at a distance not less than 1.6 mm.
7/ Unless otherwise specified in the AID.

2. APPLICABLE DOCUMENTS

Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.
MIL-PRF-55681 - Capacitor, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and as specified in figure 1.

3.3 AID requirements. All AIDs written against this SMD shall be sent to DLA Land and Maritime -VA. The following items shall be provided to the device manufacturer by the customer as part of an AID. Items 3.3.3 through 3.3.9 form a part of the manufacturer's design database/database archive. These items shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. As such, these items will not appear in the AID in the traditional sense.

3.3.1 Terminal connections and pin assignments.

3.3.2 Package type (see 1.2.4).

3.3.3 Functional block diagram (or equivalent HDL behavioral description).

3.3.4 Logic diagram (or equivalent structural HDL description or mutually agreed to net list).

3.3.5 Pin function description.

3.3.6 Design tape # or Design document name (i.e., net list).

3.3.7 Design functional tape # or name.

3.3.8 Test functional tape # or name.

3.3.9 Switching waveform(s).

3.3.10 Fault coverage. The extent of fault coverage is controlled by the quality of the customers design input, therefore fault coverage shall be specified by the customer.

3.3.11 Burn-in circuit.

3.3.12 ESD class and voltage.

3.3.13 Device electrical performance characteristics (additions to Table I). Device electrical performance characteristics shall include dc parametric, functional, ac parameters and any other data which would be considered required by a design engineer. All electrical performance characteristics apply over the full recommended ambient operating temperature range and specified test load conditions.

3.3.14 Maximum power dissipation. Maximum power dissipation shall be in accordance with the application specific design.

3.3.15 RHA post-irradiated electrical. For RHA devices supplied to this drawing, the RHA post irradiated electrical shall be specified in the AID.

3.3.16 Radiation exposure circuit If applicable, the radiation exposure circuit shall be specified in the AID

3.4 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.6 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A. The AID number shall be added to the marking by the manufacturer.

3.6.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.10 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DD2} \le 3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High-level input voltage	V_{IH}	CMOS buffers	1, 2, 3	All	2		V
		PCI buffers	1, 2, 3	All	$0.5*V_{DD2}$	-	
Low-level input voltage	V_{IL}	CMOS buffers	1, 2, 3	All	-	0.8	
		PCI buffers	1, 2, 3	All	-	$0.3*V_{DD2}$	
High level output voltage	V_{OH}	CMOS buffers I_{OH} =-2, -4, -8, -12, -16 mA	1, 2, 3	All	V_{DD2}-0.4	-	V
Low level output voltage	V_{OL}	CMOS buffers I_{OL} = 2, 4, 8, 12, 16 mA	1, 2, 3	All	-	0.4	
High level input current	I_{IH}	CMOS buffers Vin = V_{DD2} max	1, 2, 3	All	-1	1	µA
High level input current with pull up	I_{IHPU}	CMOS buffers Vin = V_{DD2} max	1, 2, 3	All	-5	5	µA
High level input current with pull down	I_{IHPD}	CMOS buffers Vin = V_{DD2} max	1, 2, 3	All		600	µA
Low level input current	I_{IL}	CMOS buffers Vin = V_{SS}	1, 2, 3	All	-1	1	µA
Low level input current with pull up	I_{ILPU}	CMOS buffers Vin = V_{SS}	1, 2, 3	All	-400		µA
Low level input current with pull down	I_{ILPD}	CMOS buffers Vin = V_{SS}	1, 2, 3	All	-5	5	µA
High impedance state high level output current	I_{OZH}	CMOS buffers Vin = V_{DD2} max	1, 2, 3	All	-1	+1	µA
High impedance state low level output current	I_{OZL}	CMOS buffers Vin = V_{SS}	1, 2, 3	All	-1	+1	µA
Cold sparing Input leakage current	I_{ICS}	V_{DD1} or V_{DD2} = V_{SS} Vin = V_{DD2} max	1, 2, 3	All	-1	+1	µA
Cold sparing Output leakage current	I_{OCS}	V_{DD2} = V_{SS} Vout = V_{DD2} max	1, 2, 3	All	-1	+1	µA
Output short circuit current 2/ 3/	I_{OSN}	CMOS buffers – nn = 1 Vout =V_{DD2}	1, 2, 3	All	-	23	mA
Output short circuit current 2/ 3/	I_{OSP}	CMOS buffers – nn = 1 Vout = Vss	1, 2, 3	All	-	23	mA
High level current	I_{OH}	PCI, V_{OH} = V_{DD2} - 0.4 V	1, 2, 3	All	16	-	mA
Low level current	I_{OL}	PCI, V_{OL} = 0.4 V	1, 2, 3	All	16	-	mA
Differential output voltage	V_{OD}	LVDS PL33 TXZ	1, 2, 3	All	247	454	mV
Common mode output voltage	V_{OS}	LVDS PL33 TXZ	1, 2, 3	All	1125	1375	mV
Input capacitance 2/	C_{I33}	CMOS buffers	4	All		7	pF

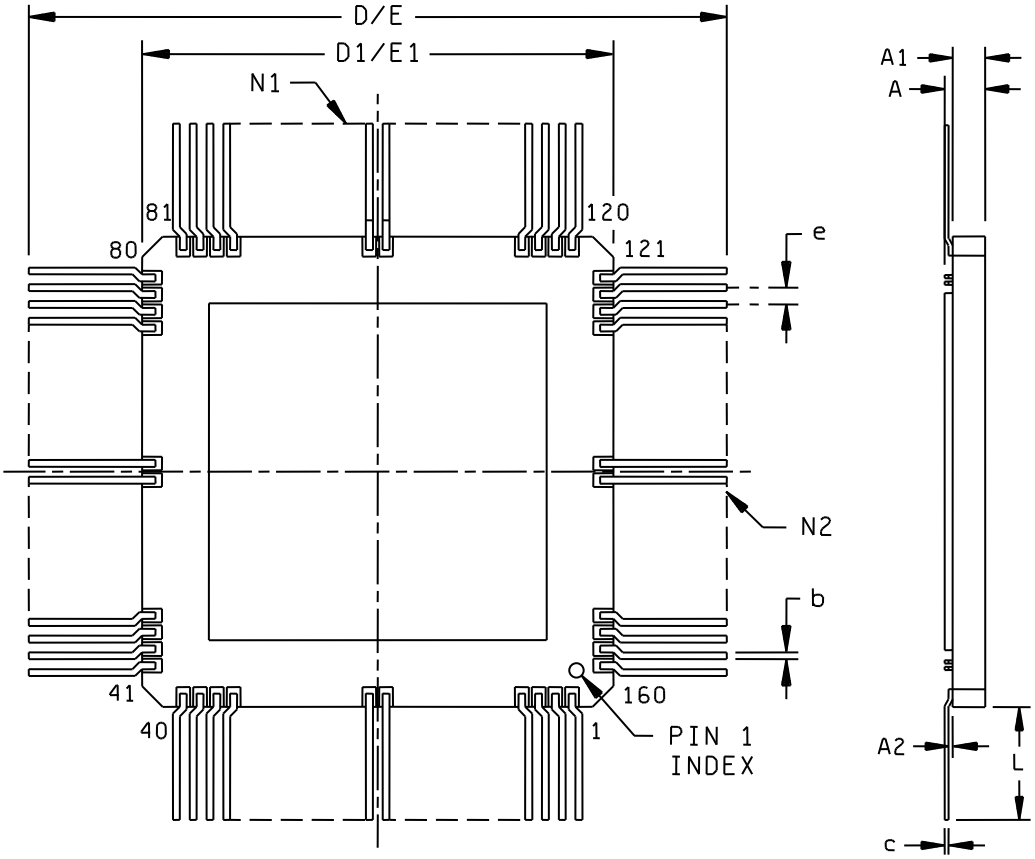
See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $2.3\ V \le V_{DD2} \le 2.7\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High-level input voltage	V_{IH}	CMOS buffers	1, 2, 3	All	2		V
Low-level input voltage	V_{IL}	CMOS buffers	1, 2, 3	All	-	0.7	V
High level output voltage	V_{OH}	CMOS buffers I_{OH} =-1.5, -3, -6, -9, -12 mA	1, 2, 3	All	V_{DD2}-0.4	-	
Low level output voltage	V_{OL}	CMOS buffers I_{OL} = 1.5, 3, 6, 9, 12 mA	1, 2, 3	All	-	0.4	
High level input current	I_{IH}	CMOS buffers Vin = V_{DD2} max	1, 2, 3	All	-1	1	µA
High level input current with pull up	I_{IHPU}	CMOS buffers Vin = V_{DD2} max	1, 2, 3	All	-5	5	µA
High level input current with pull down	I_{IHPD}	CMOS buffers Vin = V_{DD2} max	1, 2, 3	All		360	µA
Low level input current	I_{IL}	CMOS buffers Vin = V_{SS}	1, 2, 3	All	-1	1	µA
Low level input current with pull up	I_{ILPU}	CMOS buffers Vin = V_{SS}	1, 2, 3	All	-260		µA
Low level input current with pull down	I_{ILPD}	CMOS buffers Vin = V_{SS}	1, 2, 3	All	-5	5	µA
High impedance state high level output current	I_{OZH}	CMOS buffers Vin = V_{DD2}	1, 2, 3	All	-1	+1	µA
High impedance state low level output current	I_{OZL}	CMOS buffers Vin = V_{SS}	1, 2, 3	All	-1	+1	µA
Cold sparing Input leakage current	I_{ICS}	$V_{DD2} = V_{SS}$ Vin = V_{DD2} max	1, 2, 3	All	-1	+1	µA
Cold sparing Output leakage current	I_{OCS}	$V_{DD2} = V_{SS}$ Vout = V_{DD2} max	1, 2, 3	All	-1	+1	µA
Output short circuit current 2/ 4/	I_{OSN}	CMOS buffers – nn = 1 Vout =V_{DD2}	1, 2, 3	All	-	14	mA
Output short circuit current 2/ 4/	I_{OSP}	CMOS buffers – nn = 1 Vout = Vss	1, 2, 3	All	-	14	mA
Differential output voltage	V_{OD}	LVDS PL25 TXZ	1, 2, 3	All	247	454	mV
Common mode output voltage	V_{OS}	LVDS PL25 TXZ	1, 2, 3	All	1125	1375	mV
Input capacitance 2/	C_{I33}	CMOS buffers	4	All		7	pF

1/ Devices supplied to this drawing will meet all levels M, D, P, L and R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C. Post irradiation electrical parameters shall be as specified in the AID.
2/ Tested at initial design and after major process changes, otherwise guaranteed
3/ IOSmax = 23, 46, 92, 138, 184 mA for nn = 1, 2, 4, 6, 8.
4/ IOSmax = 14, 28, 56, 84, 112 mA for nn = 1, 2, 4, 6, 8.

Case X

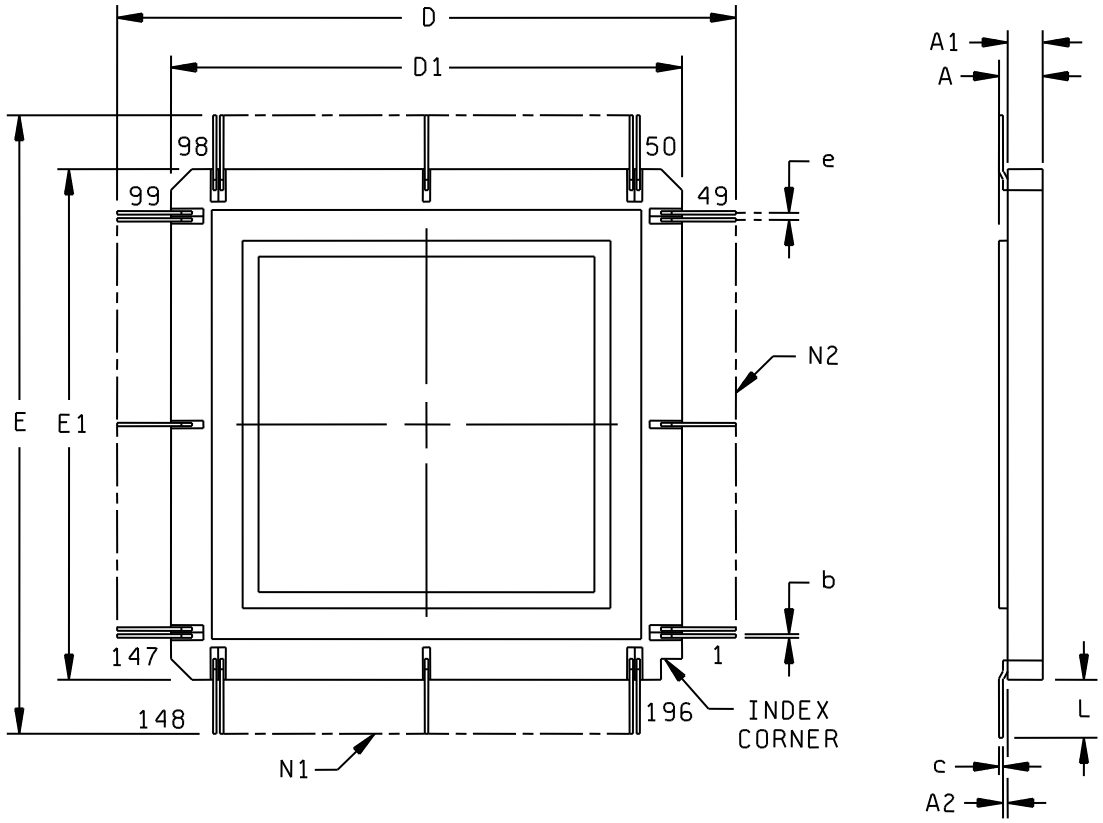


Note: Lid is connected to ground

Dimensions									
Symbol	Millimeter		Inch		Symbol	Millimeter		Inch	
	Min	Max	Min	Max		Min	Max	Min	Max
A	1.96	2.66	.077	.105	E	37.90	39.30	1.492	1.548
A1	1.70	2.10	.067	.083	E1	26.90	27.50	1.059	1.083
A2	0.10	0.30	.004	.012	f	0.25	0.35	.010	.014
C	0.10	0.20	.004	.008	L	5.50	5.90	.216	.232
D	37.90	39.30	1.492	1.548	N1	40		40	
D1	26.90	27.50	1.059	1.083	N2	40		40	
e	0.650 BSC		0.256 BSC						

FIGURE 1. Case outline.

Case Y

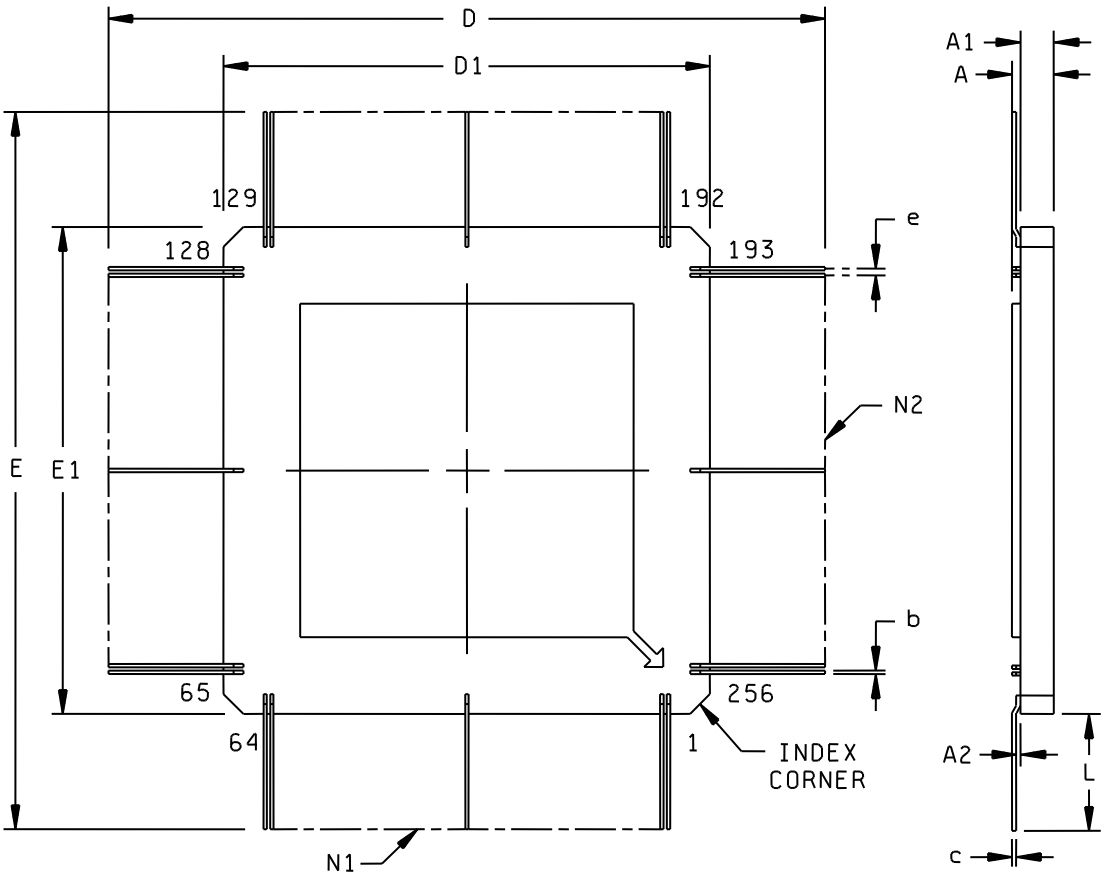


Note: Lid is connected to ground

Dimensions									
Symbol	Millimeter		Inch		Symbol	Millimeter		Inch	
	Min	Max	Min	Max		Min	Max	Min	Max
A	2.13	2.65	.084	.104	e	0.635 BSC		.025 BSC	
A1	1.83	2.24	.072	.088	f	0.20 REF		.008 REF	
A2	0.203 ref		.008 ref		L	6.35	6.70	.250	.264
C	0.102	0.203	.004	.008	N1	49		49	
D/E	46.73	47.94	1.840	1.887	N2	49		49	
D1/E1	34.03	34.54	1.340	1.360					

FIGURE 1. Case outline - Continued.

Case Z

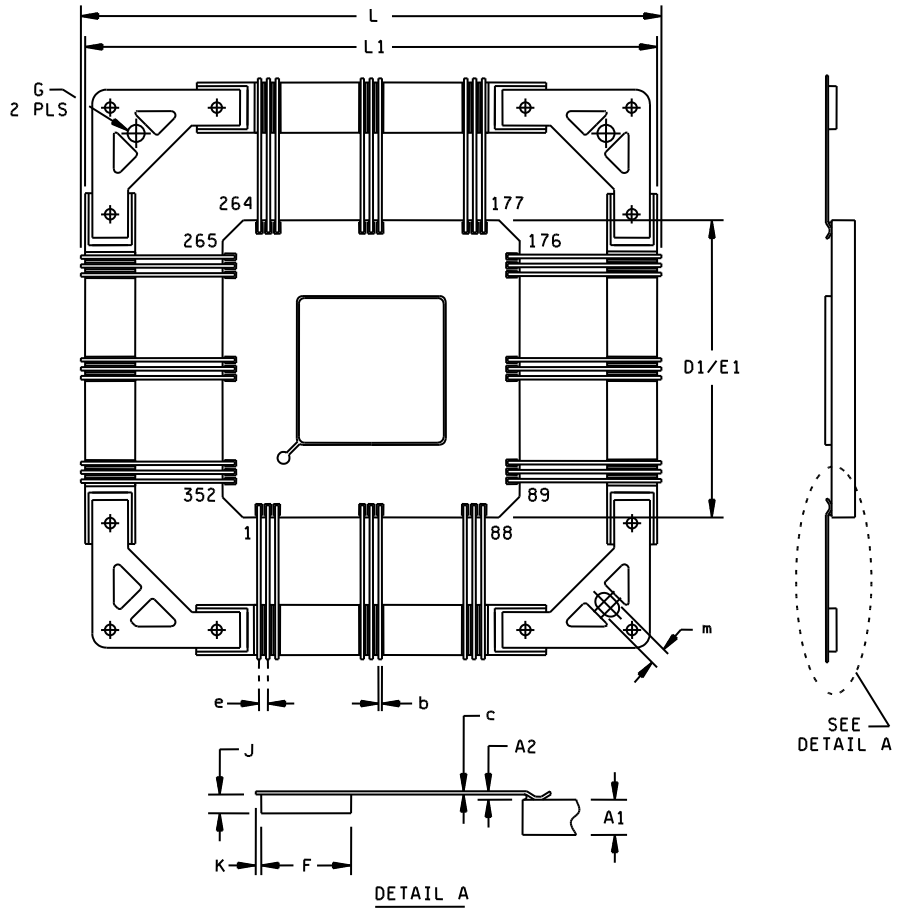


Note: Lid is connected to ground

Dimensions									
Symbol	Millimeter		Inch		Symbol	Millimeter		Inch	
	Min	Max	Min	Max		Min	Max	Min	Max
A	2.41	3.18	.095	.125	E1	36.83	37.34	1.450	1.470
A1	2.06	2.56	.081	.101	e	0.508 bsc		0.20 bsc	
A2	0.05	0.36	.002	.014	f	0.15	0.25	.006	.010
C	0.10	0.20	.004	.008	L	8.20	9.20	.323	.362
D	53.23	55.74	2.095	2.195	N1	64		64	
D1	36.83	37.34	1.450	1.470	N2	64		64	
E	53.23	55.74	2.095	2.195					

FIGURE 1. Case outline - Continued.

Case U

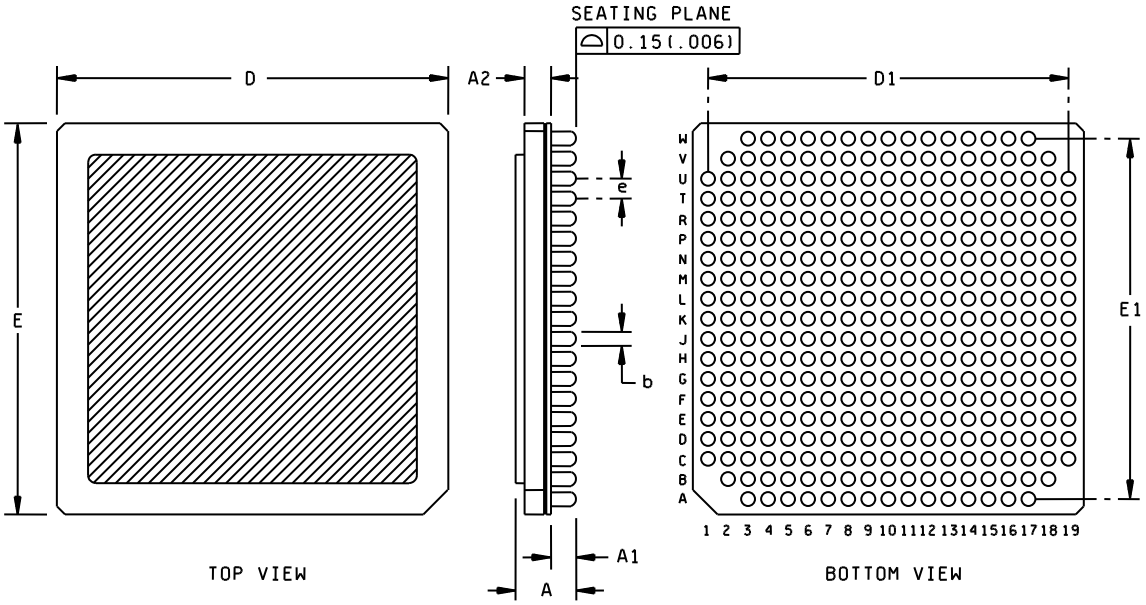


Note: Lid is connected to ground

Dimensions									
Symbol	Millimeter		Inch		Symbol	Millimeter		Inch	
	Min	Max	Min	Max		Min	Max	Min	Max
A	2.75	3.75	.108	.148	F	4.50	5.50	.177	.217
A1	2.35	3.15	.092	.124	G	2.50	2.60	.098	.104
A2	0.05	0.35	.002	.014	J	0.75	1.05	.029	.041
b	0.19	0.25	.007	.010	K		0.50		.020
c	0.11	0.20	.004	.008	L	74.85	76.40	2.947	3.008
D1/E1	47.52	48.48	1.871	1.908	L1	74.60	75.40	2.937	2.968
e	0.50 BASIC		.019 BASIC		m	2.50	2.65	.098	.104

FIGURE 1. Case outline - Continued.

Case T

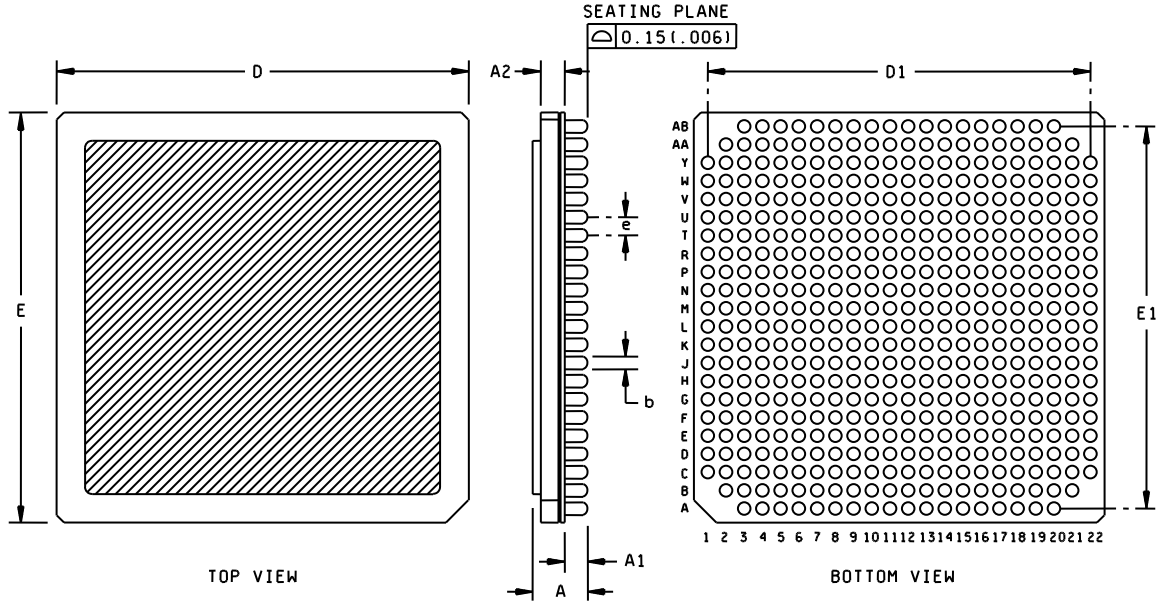


Note: Lid is connected to ground

Dimensions									
Symbol	Millimeter		Inch		Symbol	Millimeter		Inch	
	Min	Max	Min	Max		Min	Max	Min	Max
A	4.30	5.90	.169	.232	D/E	24.80	25.20	.976	.992
A1	1.40	1.85	.055	.073	D1/E1	22.86 TYP		.900 TYP	
A2	2.40	3.45	.094	.136	e	1.27 REF		.050 REF	
b	0.79	0.99	.031	.040					

FIGURE 1. Case outline - Continued.

Case M

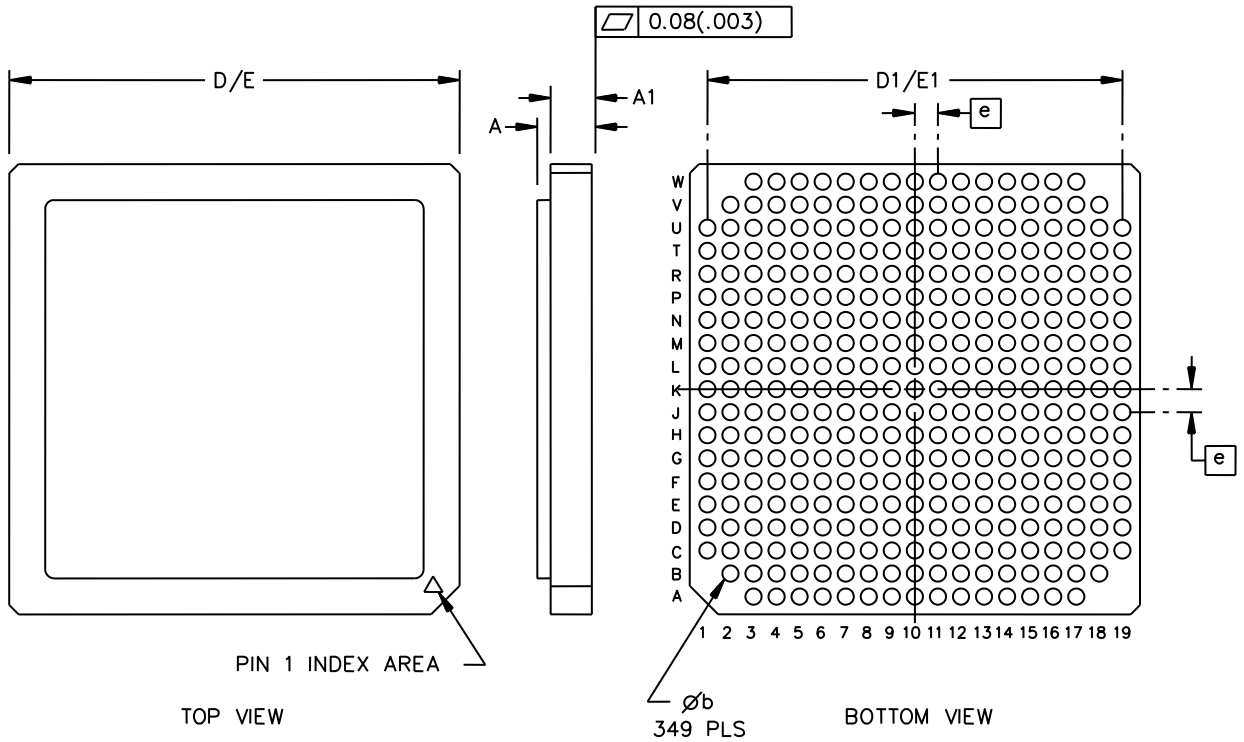


Note: Lid is connected to ground

Dimensions									
Symbol	Millimeter		Inch		Symbol	Millimeter		Inch	
	Min	Max	Min	Max		Min	Max	Min	Max
A	4.30	5.90	.169	.232	D/E	28.77	29.23	1.133	1.151
A1	1.40	1.85	.055	.073	D1/E1	26.67 TYP		1.05 TYP	
A2	2.60	3.45	.102	.136	e	1.27 REF		.050 REF	
b	0.79	0.99	.031	.040					

FIGURE 1. Case outline - Continued.

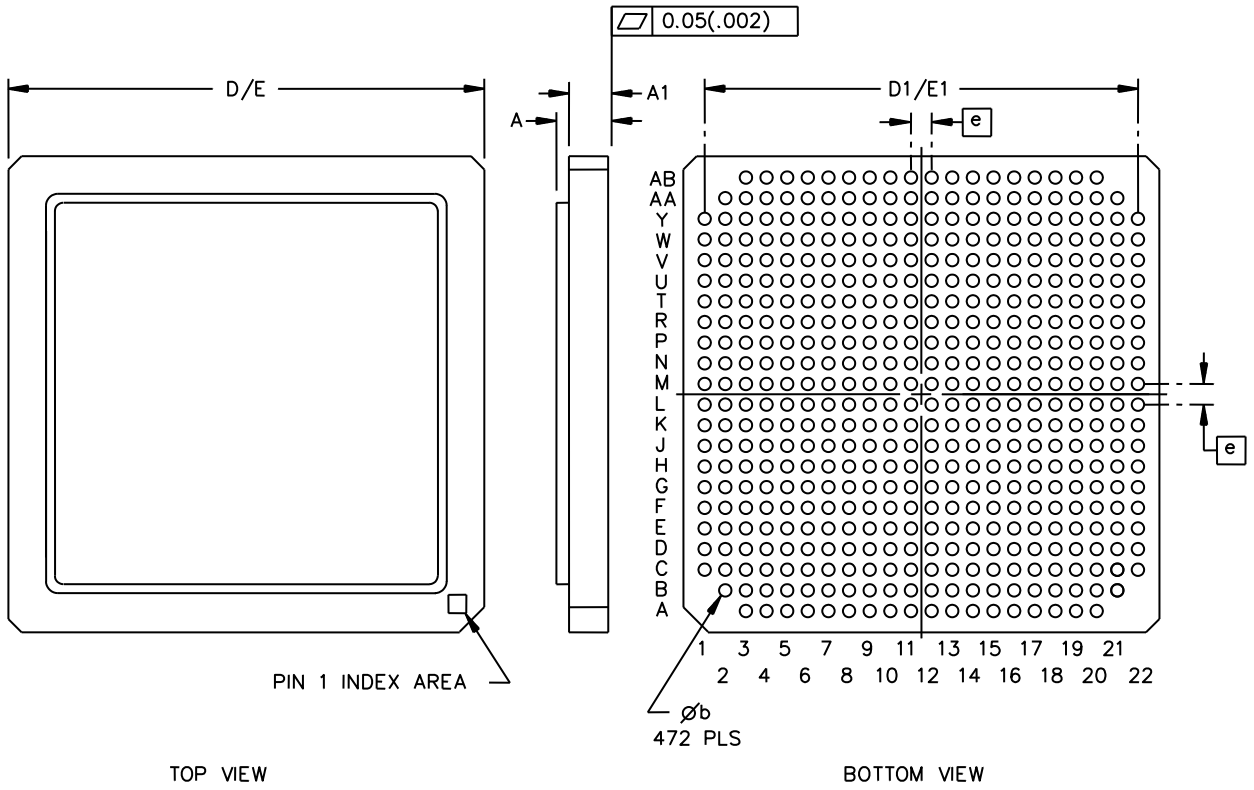
Case N



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		3.40	D1/E1	22.86 TYP	
A1	2.27	2.77	e	1.27 BSC	
D/E	24.85	25.15			

FIGURE 1. Case outline - Continued.

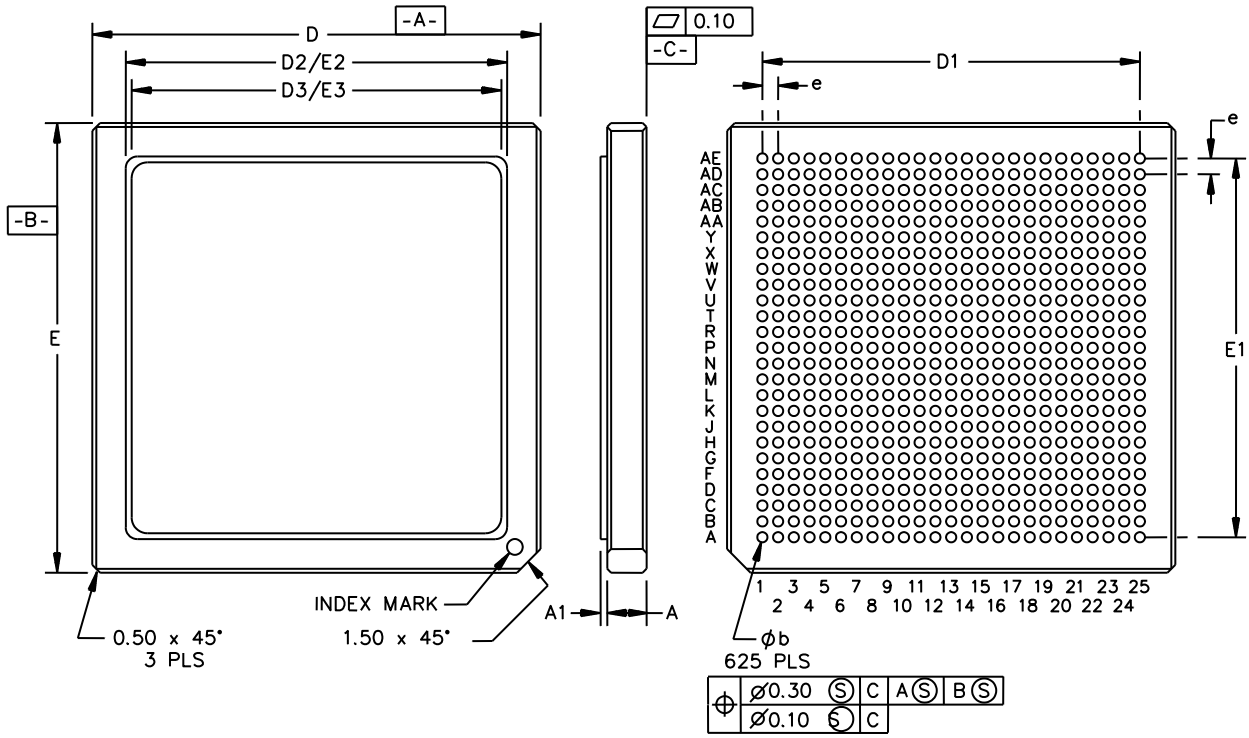
Case 4



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		3.07	D1/E1	26.67 TYP	
A1	2.27	2.77	e	1.27 BSC	
D/E	28.85	29.15			

FIGURE 1. Case outline - Continued.

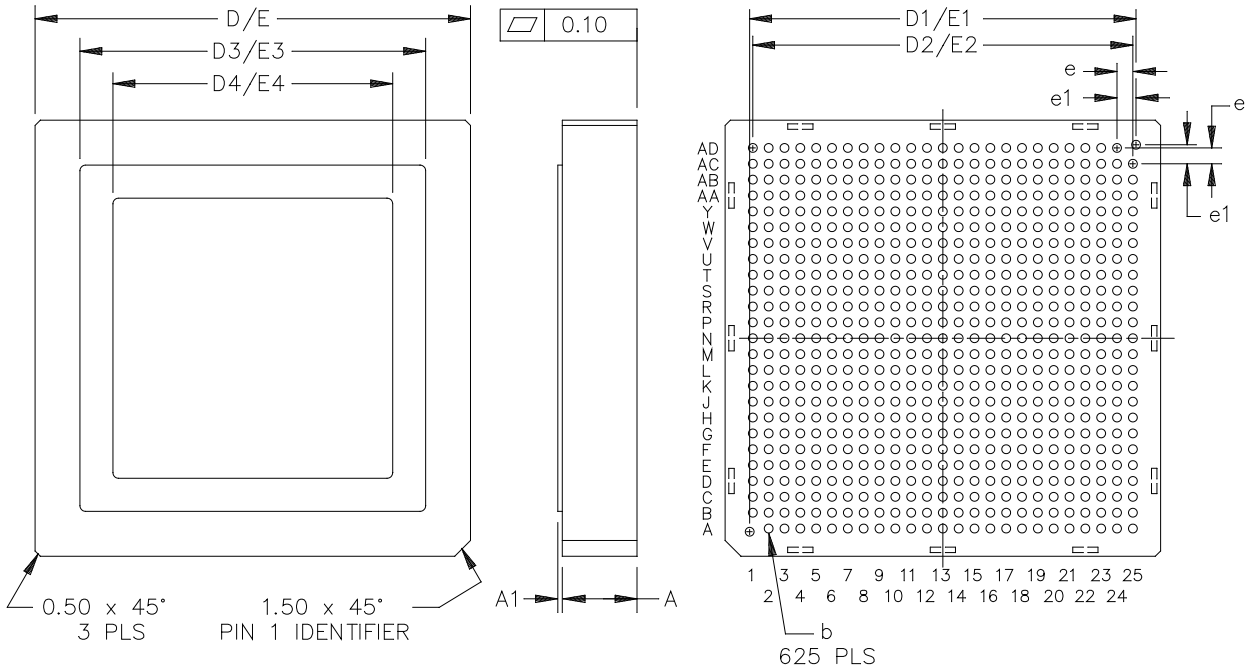
Case 5



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	2.27	2.77	D2/E2	24.39	24.87
A1	0.41	0.47	D3/E3	23.80	23.96
D	28.85	29.15	e	1.00 BSC	
D1/E1	24.00 TYP				

FIGURE 1. Case outline - Continued.

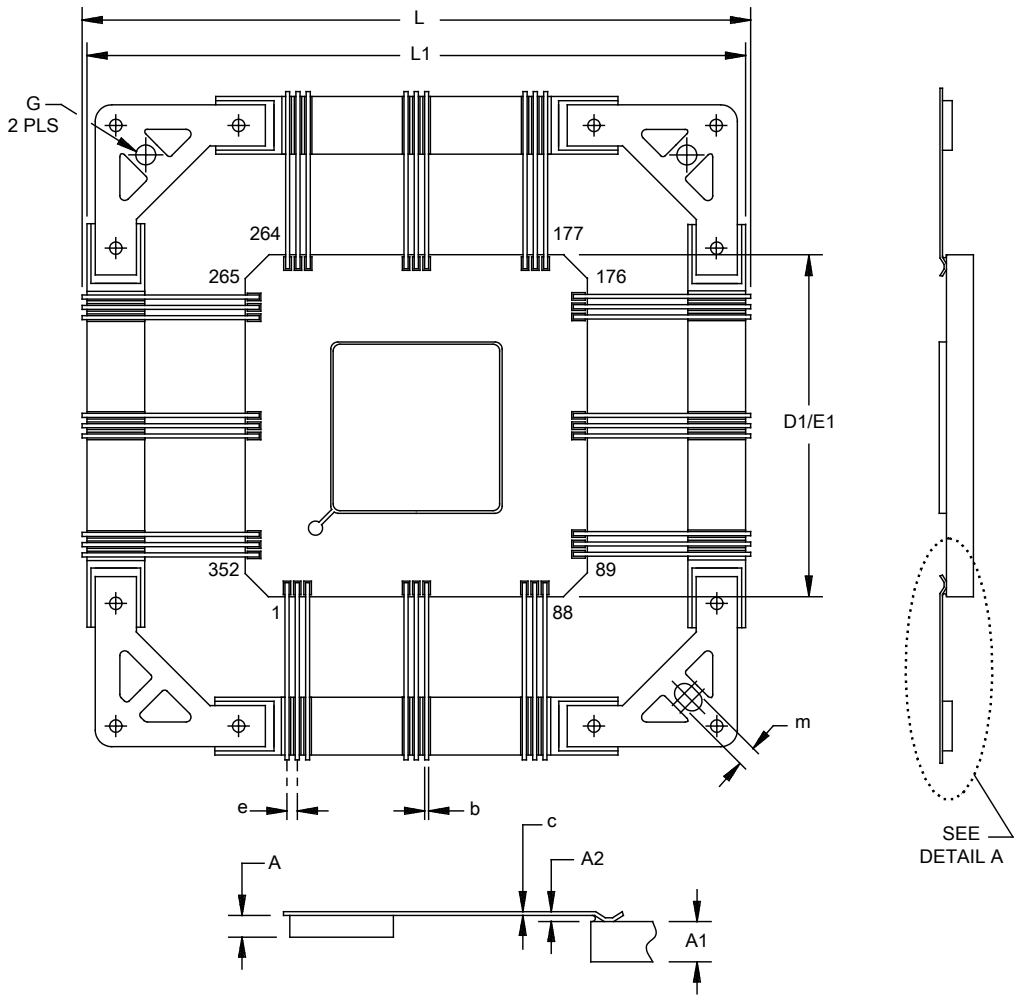
Case 6



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	6.80	7.80	D3/E3	33.07	33.67
A1	0.41	0.47	D4/E4	26.97	27.13
D/E	41.65	42.35	e	1.52 BSC	
D1/E1	36.70	37.70	e1	1.84 BSC	
D2/E2	36.08	37.08			

FIGURE 1. Case outline - Continued.

Case 7



DETAIL A

Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.75	1.05	e	0.50 BSC	
A1	2.49	2.03	G	2.50	2.60
A2	0.19	0.69	L	74.87	76.01
b	0.19	0.25	L1	74.62	75.38
c	0.10	0.17	m	2.50	2.60
D1/E1	47.67	48.33			

FIGURE 1. Case outline - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device class Q and V, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device as described in the AID.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9 3/
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits, as specified in table III, shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE III. Burn-in and operating life test, delta parameter (+25°C)

Parameter 1/	**Symbol**	**Delta limits**
Quiescent supply current delta	ΔI_{CC}	2/
Input current low level	I_{IL}	±100 nA
Input current high level	I_{IH}	±100 nA
High impedance state high level output current	I_{OZH}	±100 nA
High impedance state low level output current	I_{OZL}	±100 nA
Output voltage low level	V_{OL}	±0.10 V
Output voltage high level	V_{OH}	±0.10 V

1/ These parameters shall be recorded before and after required burn-in and life tests to determined delta limits.
2/ Shall be specified in the AID.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

a. End-point electrical parameters shall be as specified in Table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post-irradiation end-point electrical parameter limits as defined in Table I at T_A = +25°C±5°C, after exposure, to the subgroups specified in Table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019.

4.4.4.1.1 Accelerated annealing test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0547.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 12-11-03

Approved sources of supply for SMD 5962-06B02 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962-06B0201QXC	F7400	ATC18R_216KExxx-MQ
5962-06B0201QYC	F7400	ATC18R_216KBxxx-MQ
5962-06B0201QZC	F7400	ATC18R_216KAxxx-MQ
5962-06B0201VXC	F7400	ATC18R_216KExxx-SV
5962-06B0201VYC	F7400	ATC18R_216KBxxx-SV
5962-06B0201VZC	F7400	ATC18R_216KAxxx-SV
5962R06B0201VXC	F7400	ATC18R_216KExxx-SR
5962R06B0201VYC	F7400	ATC18R_216KBxxx-SR
5962R06B0201VZC	F7400	ATC18R_216KAxxx-SR
5962-06B0202QYC	F7400	ATC18R_324KBxxx-MQ
5962-06B0202QZC	F7400	ATC18R_324KAxxx-MQ
5962-06B0202QUC	F7400	ATC18R_324YFxxx-MQ
5962-06B0202QXC	F7400	ATC18R_324KExxx-MQ
5962-06B0202QTB	F7400	ATC18R_3242Hxxx-MQ
5962-06B0202QNC	F7400	ATC18R_3242Uxxx-MQ
5962-06B0202VYC	F7400	ATC18R_324KBxxx-SV
5962-06B0202VZC	F7400	ATC18R_324KAxxx-SV
5962-06B0202VUC	F7400	ATC18R_324YFxxx-SV
5962-06B0202VXC	F7400	ATC18R_324KExxx-SV
5962-06B0202VTB	F7400	ATC18R_3242Hxxx-SV
5962-06B0202VNC	F7400	ATC18R_3242Uxxx-SV
5962R06B0202VYC	F7400	ATC18R_324KBxxx-SR
5962R06B0202VZC	F7400	ATC18R_324KAxxx-SR
5962R06B0202VUC	F7400	ATC18R_324YFxxx-SR
5962R06B0202VXC	F7400	ATC18R_324KExxx-SR
5962R06B0202VTB	F7400	ATC18R_3242Hxxx-SR
5962R06B0202VNC	F7400	ATC18R_3242Uxxx-SR

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962-06B0203QZC	F7400	ATC18R_404KAxxx-MQ
5962-06B0203QUC	F7400	ATC18R_404YFxxx-MQ
5962-06B0203QTB	F7400	ATC18R_4042Hxxx-MQ
5962-06B0203QMB	F7400	ATC18R_4042Gxxx-MQ
5962-06B0203QNC	F7400	ATC18R_4042Uxxx-MQ
5962-06B0203Q4C	F7400	ATC18R_4042Vxxx-MQ
5962-06B0203Q5C	F7400	ATC18R_4042Kxxx-MQ
5962-06B0203Q6C	F7400	ATC18R_4042Wxxx-MQ
5962-06B0203VZC	F7400	ATC18R_404KAxxx-SV
5962-06B0203VUC	F7400	ATC18R_404YFxxx-SV
5962-06B0203VTB	F7400	ATC18R_4042Hxxx-SV
5962-06B0203VMB	F7400	ATC18R_4042Gxxx-SV
5962-06B0203VNC	F7400	ATC18R_4042Uxxx-SV
5962-06B0203V4C	F7400	ATC18R_4042Vxxx-SV
5962-06B0203V5C	F7400	ATC18R_4042Kxxx-SV
5962-06B0203V6C	F7400	ATC18R_4042Wxxx-SV
5962R06B0203VZC	F7400	ATC18R_404KAxxx-SR
5962R06B0203VUC	F7400	ATC18R_404YFxxx-SR
5962R06B0203VTB	F7400	ATC18R_4042Hxxx-SR
5962R06B0203VMB	F7400	ATC18R_4042Gxxx-SR
5962R06B0203VNC	F7400	ATC18R_4042Uxxx-SR
5962R06B0203V4C	F7400	ATC18R_4042Vxxx-SR
5962R06B0203V5C	F7400	ATC18R_4042Kxxx-SR
5962R06B0203V6C	F7400	ATC18R_4042Wxxx-SR
5962-06B0204QZC	F7400	ATC18R_504KAxxx-MQ
5962-06B0204QUC	F7400	ATC18R_504YFxxx-MQ
5962-06B0204QTB	F7400	ATC18R_5042Hxxx-MQ
5962-06B0204QMB	F7400	ATC18R_5042Gxxx-MQ
5962-06B0204QNC	F7400	ATC18R_5042Uxxx-MQ
5962-06B0204Q4C	F7400	ATC18R_5042Vxxx-MQ
5962-06B0204Q5C	F7400	ATC18R_5042Kxxx-MQ
5962-06B0204Q6C	F7400	ATC18R_5042Wxxx-MQ
5962-06B0204VZC	F7400	ATC18R_504KAxxx-SV
5962-06B0204VUC	F7400	ATC18R_504YFxxx-SV
5962-06B0204VTB	F7400	ATC18R_5042Hxxx-SV
5962-06B0204VMB	F7400	ATC18R_5042Gxxx-SV
5962-06B0204VNC	F7400	ATC18R_5042Uxxx-SV
5962-06B0204V4C	F7400	ATC18R_5042Vxxx-SV
5962-06B0204V5C	F7400	ATC18R_5042Kxxx-SV
5962-06B0204V6C	F7400	ATC18R_5042Wxxx-SV

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962R06B0204VZC	F7400	ATC18R_504KAxxx-SR
5962R06B0204VUC	F7400	ATC18R_504YFxxx-SR
5962R06B0204VTB	F7400	ATC18R_5042Hxxx-SR
5962R06B0204VMB	F7400	ATC18R_5042Gxxx-SR
5962R06B0204VNC	F7400	ATC18R_5042Uxxx-SR
5962R06B0204V4C	F7400	ATC18R_5042Vxxx-SR
5962R06B0204V5C	F7400	ATC18R_5042Kxxx-SR
5962R06B0204V6C	F7400	ATC18R_5042Wxxx-SR
5962-06B0205QXC	F7400	ATC18R_216KExxx-MQ
5962-06B0205QYC	F7400	ATC18R_216KBxxx-MQ
5962-06B0205QZC	F7400	ATC18R_216KAabc-MQ
5962-06B0205VXC	F7400	ATC18R_216KExxx-SV
5962-06B0205VYC	F7400	ATC18R_216KBxxx-SV
5962-06B0205VZC	F7400	ATC18R_216KAxxx-SV
5962R06B0205VXC	F7400	ATC18R_216KExxx-SR
5962R06B0205VYC	F7400	ATC18R_216KBxxx-SR
5962R06B0205VZC	F7400	ATC18R_216KAxxx-SR
5962-06B0206QYC	F7400	ATC18R_324KBxxx-MQ
5962-06B0206QZC	F7400	ATC18R_324KAxxx-MQ
5962-06B0206QUC	F7400	ATC18R_324YFxxx-MQ
5962-06B0206QXC	F7400	ATC18R_324KExxx-MQ
5962-06B0206QTB	F7400	ATC18R_3242Hxxx-MQ
5962-06B0206QNC	F7400	ATC18R_3242Uxxx-MQ
5962-06B0206VYC	F7400	ATC18R_324KBxxx-SV
5962-06B0206VZC	F7400	ATC18R_324KAxxx-SV
5962-06B0206VUC	F7400	ATC18R_324YFxxx-SV
5962-06B0206VXC	F7400	ATC18R_324KExxx-SV
5962-06B0206VTB	F7400	ATC18R_3242Hxxx-SV
5962-06B0206VNC	F7400	ATC18R_3242Uxxx-SV
5962R06B0206VYC	F7400	ATC18R_324KBxxx-SR
5962R06B0206VZC	F7400	ATC18R_324KAxxx-SR
5962R06B0206VUC	F7400	ATC18R_324YFxxx-SR
5962R06B0206VXC	F7400	ATC18R_324KExxx-SR
5962R06B0206VTB	F7400	ATC18R_3242Hxxx-SR
5962R06B0206VNC	F7400	ATC18R_3242Uxxx-SR

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962-06B0207QZC	F7400	ATC18R_404KAxxx-MQ
5962-06B0207QUC	F7400	ATC18R_404YFxxx-MQ
5962-06B0207QTB	F7400	ATC18R_4042Hxxx-MQ
5962-06B0207QMB	F7400	ATC18R_4042Gxxx-MQ
5962-06B0207QNC	F7400	ATC18R_4042Uxxx-MQ
5962-06B0207Q4C	F7400	ATC18R_4042Vxxx-MQ
5962-06B0207Q5C	F7400	ATC18R_4042Kxx-MQ
5962-06B0207Q6C	F7400	ATC18R_4042Wxxx-MQ
5962-06B0207VZC	F7400	ATC18R_404KAxxx-SV
5962-06B0207VUC	F7400	ATC18R_404YFxxx-SV
5962-06B0207VTB	F7400	ATC18R_4042Hxxx-SV
5962-06B0207VMB	F7400	ATC18R_4042Gxxx-SV
5962-06B0207VNC	F7400	ATC18R_4042Uxxx-SV
5962-06B0207V4C	F7400	ATC18R_4042Vxxx-SV
5962-06B0207V5C	F7400	ATC18R_4042Kxx-SV
5962-06B0207V6C	F7400	ATC18R_4042Wxxx-SV
5962R06B0207VZC	F7400	ATC18R_404KAxxx-SR
5962R06B0207VUC	F7400	ATC18R_404YFxxx-SR
5962R06B0207VTB	F7400	ATC18R_4042Hxxx-SR
5962R06B0207VMB	F7400	ATC18R_4042Gxxx-SR
5962R06B0207VNC	F7400	ATC18R_4042Uxxx-SR
5962R06B0207V4C	F7400	ATC18R_4042Vxxx-SR
5962R06B0207V5C	F7400	ATC18R_4042Kxx-SR
5962R06B0207V6C	F7400	ATC18R_4042Wxxx-SR
5962-06B0208QZC	F7400	ATC18R_504KAxxx-MQ
5962-06B0208QUC	F7400	ATC18R_504YFxxx-MQ
5962-06B0208QTB	F7400	ATC18R_5042Hxxx-MQ
5962-06B0208QMB	F7400	ATC18R_5042Gxxx-MQ
5962-06B0208QNC	F7400	ATC18R_5042Uxxx-MQ
5962-06B0208Q4C	F7400	ATC18R_5042Vxxx-MQ
5962-06B0208Q5C	F7400	ATC18R_5042Kxxx-MQ
5962-06B0208Q6C	F7400	ATC18R_5042Wxxx-MQ
5962-06B0208VZC	F7400	ATC18R_504KAxxx-SV
5962-06B0208VUC	F7400	ATC18R_504YFxxx-SV
5962-06B0208VTB	F7400	ATC18R_5042Hxxx-SV
5962-06B0208VMB	F7400	ATC18R_5042Gxxx-SV
5962-06B0208VNC	F7400	ATC18R_5042Uxxx-SV
5962-06B0208V4C	F7400	ATC18R_5042Vxxx-SV
5962-06B0208V5C	F7400	ATC18R_5042Kxxx-SV
5962-06B0208V6C	F7400	ATC18R_5042Wxxx-SV

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962R06B0208VZC	F7400	ATC18R_504KAxxx-SR
5962R06B0208VUC	F7400	ATC18R_504YFxxx-SR
5962R06B0208VTB	F7400	ATC18R_5042Hxxx-SR
5962R06B0208VMB	F7400	ATC18R_5042Gxxx-SR
5962R06B0208VNC	F7400	ATC18R_5042Uxxx-SR
5962R06B0208V4C	F7400	ATC18R_5042Vxxx-SR
5962R06B0208V5C	F7400	ATC18R_5042Kxxx-SR
5962R06B0208V6C	F7400	ATC18R_5042Wxxx-SR
5962-06B0209QUC	F7400	ATC18R_544YFxxx-MQ
5962-06B0209Q4C	F7400	ATC18R_5442Vxxx-MQ
5962-06B0209Q5C	F7400	ATC18R_5442Kxxx-MQ
5962-06B0209Q6C	F7400	ATC18R_5442Wxxx-MQ
5962-06B0209VUC	F7400	ATC18R_544YFxxx-SV
5962-06B0209V4C	F7400	ATC18R_5442Vxxx-SV
5962-06B0209V5C	F7400	ATC18R_5442Kxxx-SV
5962-06B0209V6C	F7400	ATC18R_5442Wxxx-SV
5962R06B0209VUC	F7400	ATC18R_544YFxxx-SR
5962R06B0209V4C	F7400	ATC18R_5442Vxxx-SR
5962R06B0209V5C	F7400	ATC18R_5442Kxxx-SR
5962R06B0209V6C	F7400	ATC18R_5442Wxxx-SR
5962-06B0210QUC	F7400	ATC18R_544YFxxx-MQ
5962-06B0210Q4C	F7400	ATC18R_5442Vxxx-MQ
5962-06B0210Q5C	F7400	ATC18R_5442Kxxx-MQ
5962-06B0210Q6C	F7400	ATC18R_5442Wxxx-MQ
5962-06B0210VUC	F7400	ATC18R_544YFxxx-SV
5962-06B0210V4C	F7400	ATC18R_5442Vxxx-SV
5962-06B0210V5C	F7400	ATC18R_5442Kxxx-SV
5962-06B0210V6C	F7400	ATC18R_5442Wxxx-SV
5962R06B0210VUC	F7400	ATC18R_544YFxxx-SR
5962R06B0210V4C	F7400	ATC18R_5442Vxxx-SR
5962R06B0210V5C	F7400	ATC18R_5442Kxxx-SR
5962R06B0210V6C	F7400	ATC18R_5442Wxxx-SR
5962-06B0202Q7C	F7400	ATC18R_324BGxxx-MQ
5962-06B0202V7C	F7400	ATC18R_324BGxxx-SV
5962R06B0202V7C	F7400	ATC18R_324BGxxx-SR

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962-06B0203Q7C	F7400	ATC18R_404BGxxx-MQ
5962-06B0203V7C	F7400	ATC18R_404BGxxx-SV
5962R06B0203V7C	F7400	ATC18R_404BGxxx-SR
5962-06B0206Q7C	F7400	ATC18R_324BGxxx-MQ
5962-06B0206V7C	F7400	ATC18R_324BGxxx-SV
5962R06B0206V7C	F7400	ATC18R_324BGxxx-SR
5962-06B0207Q7C	F7400	ATC18R_404BGxxx-MQ
5962-06B0207V7C	F7400	ATC18R_404BGxxx-SV
5962R06B0207V7C	F7400	ATC18R_404BGxxx-SR

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Due to the nature of this SMD, the standard microcircuit drawing PIN and corresponding vendor similar PIN shall be specified in the AID. The “xxx” is reserved to indicate the customer specific code.
3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
4/ No longer available from an approved source of supplied.

Vendor CAGE number	Vendor name and address
F7400	Atmel Nantes La Chantrerie 44306 Nantes Cedex3 France