PIC18 Q43

PIC18 Q43 Family Product Brief

Description

The PIC18 Q43 microcontroller family is available in 28/40/44/48-pin devices for real-time control applications. This family features a 12-bit ADC with Computation (ADC^2) automating Capacitive Voltage Divider (CVD) techniques for advanced capacitive touch sensing, averaging, filtering, oversampling and threshold comparison. This family showcases a new 16-bit PWM module which provides dual independent outputs on the same timebase. Additional features include Vectored Interrupt Controller with fixed latency for handling interrupts, System Bus Arbiter, Direct Memory Access (DMA) capabilities, UART with support for Asynchronous, DMX, DALI and LIN protocols, SPI, I^2C, memory features like Memory Access Partition (MAP) to support users in data protection and bootloader applications, and Device Information Area (DIA), which stores factory calibration values to help improve temperature sensor accuracy.

PIC18 Q43 Family Types

Table 1. Devices included in this family

Device	Program Memory Flash (bytes)	Data SRAM (bytes)	Data EEPROM (bytes)	Memory Access Partion/ Device Information Area	I/O Pins/Peripheral Pin Select	8-Bit Timer with HLT/16-Bit Timers	16-Bit Dual PWM/CCP	Complimentary Waveform Generator	Signal Measurement Timer	Numerically Controlled Oscillator	Configurable Logic Cell	12-Bit ADC^2 (channels)	8-Bit DAC	Comparator/Zero-Cross Detect	High-Low Voltage Detect	SPI/I^2C	UART/UART with Protocol Support	Direct Memory Access (DMA)	Windowed Watchdog Timer	16-Bit CRC with Scanner	Vectored Interrupts	Peripheral Module Disable	Temperature Indicator
PIC18F25Q43	32k	2048	1024	Y/Y	25/Y	3/4	3/3	3	1	3	8	24	1	2/1	1	2/1	4/1	6	Y	Y	Y	Y	Y
PIC18F26Q43	64k	4096	1024	Y/Y	25/Y	3/4	3/3	3	1	3	8	24	1	2/1	1	2/1	4/1	6	Y	Y	Y	Y	Y
PIC18F27Q43	128k	8192	1024	Y/Y	25/Y	3/4	3/3	3	1	3	8	24	1	2/1	1	2/1	4/1	6	Y	Y	Y	Y	Y
PIC18F45Q43	32k	2048	1024	Y/Y	36/Y	3/4	3/3	3	1	3	8	35	1	2/1	1	2/1	4/1	6	Y	Y	Y	Y	Y
PIC18F46Q43	64k	4096	1024	Y/Y	36/Y	3/4	3/3	3	1	3	8	35	1	2/1	1	2/1	4/1	6	Y	Y	Y	Y	Y
PIC18F47Q43	128k	8192	1024	Y/Y	36/Y	3/4	3/3	3	1	3	8	35	1	2/1	1	2/1	4/1	6	Y	Y	Y	Y	Y
PIC18F55Q43	32k	2048	1024	Y/Y	44/Y	3/4	3/3	3	1	3	8	43	1	2/1	1	2/1	4/1	6	Y	Y	Y	Y	Y
PIC18F56Q43	64k	4096	1024	Y/Y	44/Y	3/4	3/3	3	1	3	8	43	1	2/1	1	2/1	4/1	6	Y	Y	Y	Y	Y
PIC18F57Q43	128k	8192	1024	Y/Y	44/Y	3/4	3/3	3	1	3	8	43	1	2/1	1	2/1	4/1	6	Y	Y	Y	Y	Y

Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC – 64 MHz clock input
  - 62.5 ns minimum instruction cycle
- Six Direct Memory Access (DMA) Controllers:
  - Data transfers to SFR/GPR spaces from either Program Flash Memory, Data EEPROM or SFR/GPR spaces
  - User programmable source and destination sizes
  - Hardware and software triggered data transfers
- Vectored Interrupt Capability:
  - Selectable high/low priority
  - Fixed interrupt latency of three instruction cycles
  - Programmable vector table base address
  - Backwards compatible with previous interrupt capabilities
- 128-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Watchdog Reset on too long or too short interval between watchdog clear events
  - Variable prescaler selection
  - Variable window size selection

Memory

- Up to 128 KB of Program Flash Memory
- Up to 8 KB of Data SRAM Memory
- 1024 Bytes Data EEPROM
- Memory Access Partition: The Program Flash Memory can be partitioned into:
  - Application Block
  - Boot Block
  - Storage Area Flash (SAF) Block
- Programmable Code Protection and Write Protection
- Device Information Area (DIA) Stores:
  - Temperature Indicator factory calibrated data
  - Fixed Voltage Reference measurement data
  - Microchip Unique Identifier
- Device Characteristics Information (DCI) Area Stores:
  - Program/Erase row sizes
  - Pin Count details
  - EEPROM size

- Direct, Indirect and Relative Addressing modes

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 5.5V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality

- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is lower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals
- Low-Power Mode Features:
  - Sleep: < 1µA typical @ 3V
  - Operating Current:
    - 48µA @ 32 kHz, 3V, typical

Digital Peripherals

- Three 16-Bit Pulse-Width Modulators (PWM):
  - Dual outputs for each PWM module
  - Integrated 16-bit timer/counter
  - Double-buffered user registers for duty cycles
  - Right/Left/Center/Variable aligned modes of operation
  - Multiple clock and Reset signal selections
- Four 16-Bit Timers (TMR0/1/3/5)
- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- Eight Configurable Logic Cell (CLC):
  - Integrated combinational and sequential logic
- Three Complimentary Waveform Generators (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
  - Programmable dead band
  - Fault-shutdown input
- Three Capture/Compare/PWM (CCP) modules:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode

- Three Numerically Controlled Oscillators (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input Clock up to 64 MHz
- Signal Measurement Timer (SMT):
  - 24-bit timer/counter with prescaler
  - Several modes of operation like Time-of-Flight, Period and Duty Cycle measurement etc.
- Data Signal Modulator (DSM):
  - Multiplex two carrier clocks, with glitch prevention feature
  - Multiple sources for each carrier
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate 16-bit CRC over any portion of Program Flash Memory
- Five UART modules:
  - One module (UART1) supports LIN master and slave, DMX mode, DALI gear and device protocols
  - Asynchronous UART, RS-232, RS-485 compatible
  - Automatic and user timed BREAK period generation
  - Automatic checksums
  - Programmable 1, 1.5, and two Stop bits
  - Wake-up on BREAK reception
  - DMA compatible
- Two SPI modules:
  - Configurable length bytes
  - Arbitrary length data packets
  - Transmit-without-Receive and Receive-without-transmit option
  - Transfer byte counter
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
- One I^2C module, SMBus, PMBus™ Compatible:
  - 7-bit and 10-bit addressing modes with address masking modes
  - Dedicated address, transmit and receive buffers and DMA capabilities
  - Bus collision detection with arbitration
  - Bus time-out detection and handling
  - I^2C, SMBus 2.0 and SMBus 3.0, and 1.8V input level selections
  - Multi-Master mode, including self-addressing
- Device I/O Port Features:
  - 25 I/O pins (PIC18F25/26/27Q43)
  - 36 I/O pins (PIC18F45/46/47Q43)
  - 44 I/O pins (PIC18F55/56/57Q43)
  - Individually programmable I/O direction, open-drain, slew rate and weak pull-up control
  - Interrupt-on-change on most pins
  - Three programmable external interrupt pins
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

Analog Peripherals

- Analog-to-Digital Converter with Computation (ADC^2):
  - Up to 43 external channels
  - Automated math functions on input signals:
    - Averaging, filter calculations, oversampling and threshold comparison
  - Operates in Sleep
  - Five internal analog channels
  - Hardware Capacitive Voltage Divider (CVD) Support:
    - Adjustable sample and hold capacitor array
    - Guard ring digital output drive
    - Automates touch sampling and reduces software size and CPU usage when touch or proximity sensing is required
- 8-Bit Digital-to-Analog Converter (DAC):
  - Buffered output available on two I/O pins
  - Internal connections to ADC and Comparators
- Two Comparators (CMP):
  - Four external inputs
  - Configurable output polarity
  - External output via Peripheral Pin Select
- Zero-Cross Detect (ZCD):
  - Detect when AC signal on pin crosses ground
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels
  - Internal connections to ADC, Comparator and DAC

Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 64 MHz
  - ±1% at calibration
  - Active Clock Tuning of HFINTOSC for better accuracy
- 32 kHz Low-Power Internal Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External High-frequency Oscillator Block:
  - Three crystal/resonator modes
  - Digital Clock Input mode
  - 4x PLL with external sources
- Fail-Safe Clock Monitor:
  - Allows for operational recovery if external clock stops
- Oscillator Start-up Timer (OST):
  - Ensures stability of crystal oscillator sources

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip

Packages

Table 1. Packages

Device	28-pin SPDIP	28-pin SOIC	28-pin SSOP	28-pin VQFN 4x4x1	40-pin PDIP	40-pin VQFN 5x5x0.9	44-pin TQFP	48-pin TQFP 7x7x1	48-pin VQFN 6x6x0.9
PIC18F25Q43	●	●	●	●					
PIC18F26Q43	●	●	●	●					
PIC18F27Q43	●	●	●	●					
PIC18F45Q43					●	●	●		
PIC18F46Q43					●	●	●		
PIC18F47Q43					●	●	●		
PIC18F55Q43								●	●
PIC18F56Q43								●	●
PIC18F57Q43								●	●

Pin Diagrams

Figure 1. 28-pin SPDIP, SSOP, SOIC

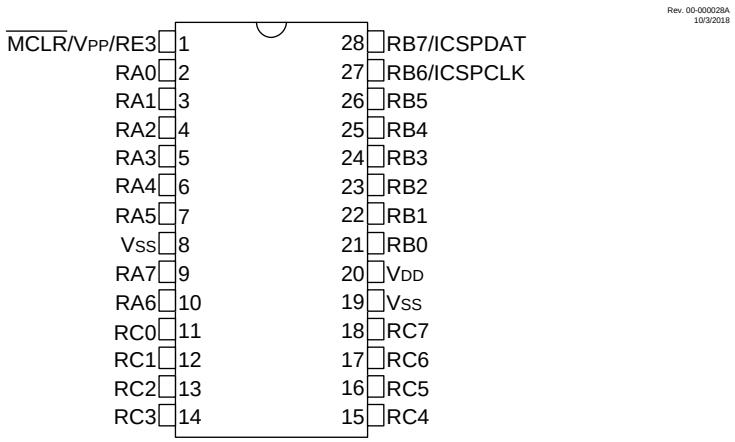
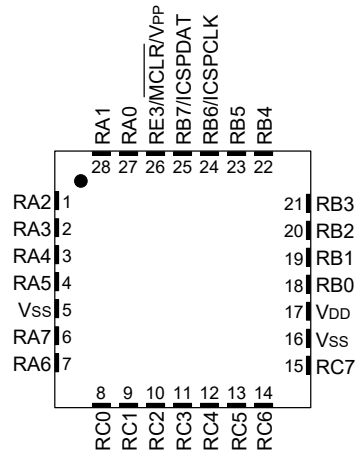


Figure 2. 28-pin , VQFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS}, however it must not be the only V_{SS} connection to the device.

Figure 3. 40-pin PDIP

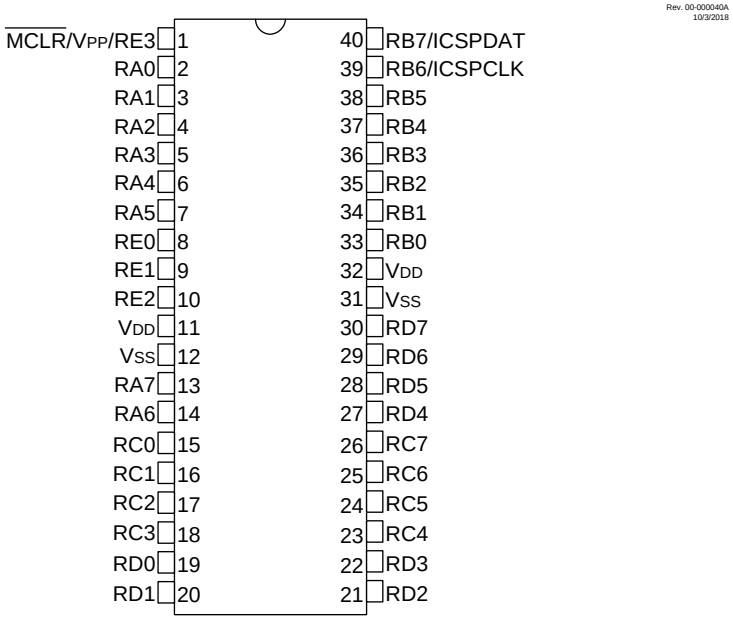
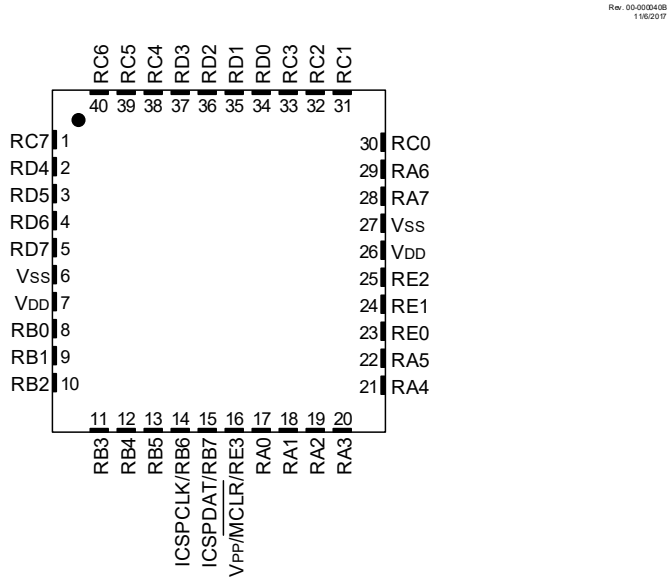


Figure 4. 40-pin, VQFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS}, however it must not be the only V_{SS} connection to the device.

Figure 5. 44-pin TQFP

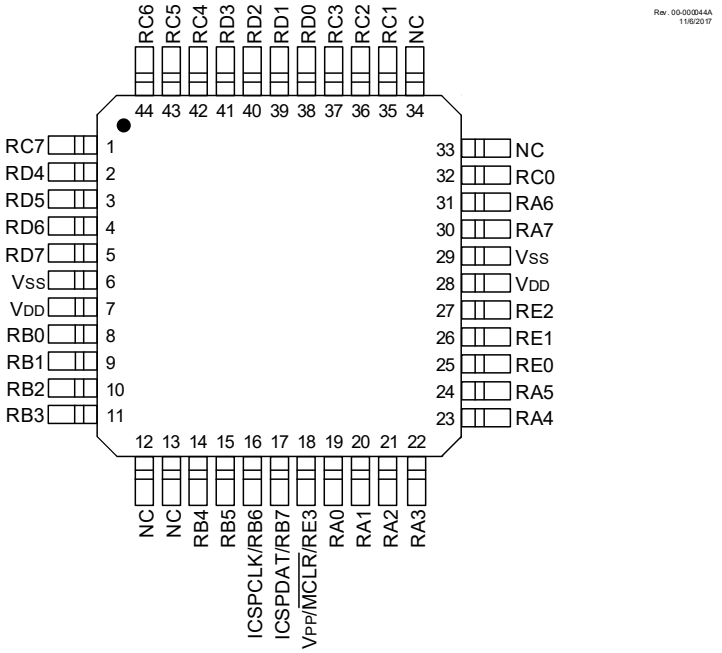


Figure 6. 48-pin TQFP

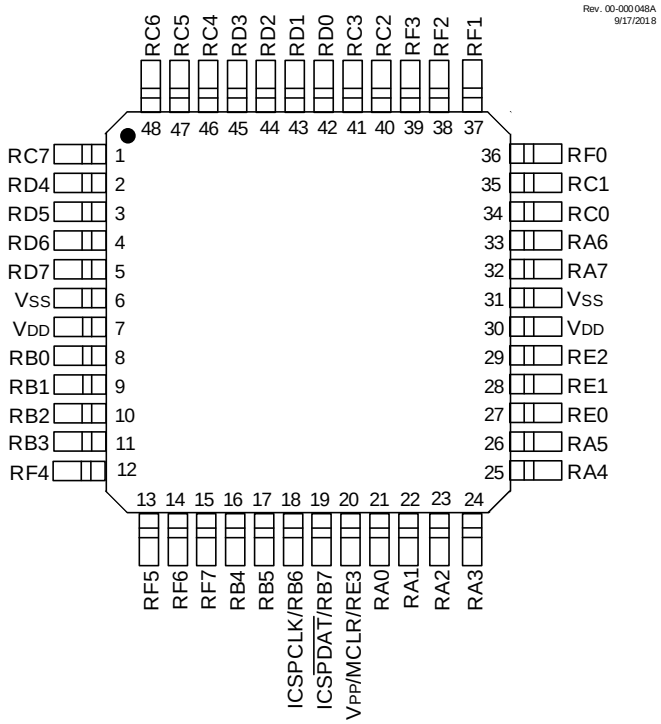


Figure 7. 48-pin VQFN

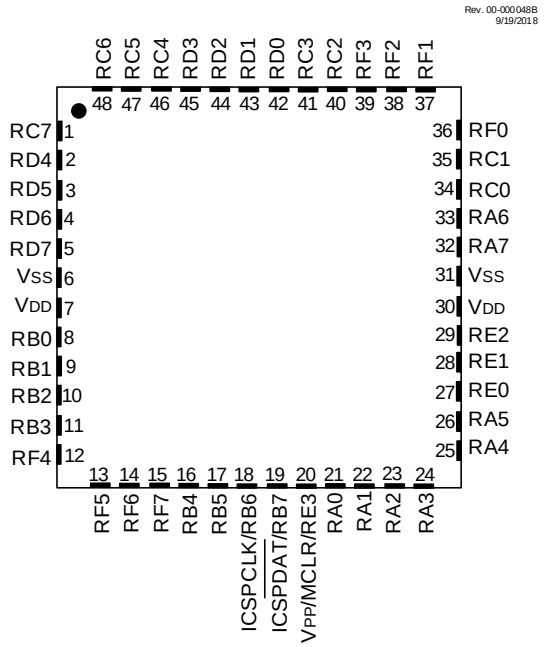


Table 1. 28-Pin Allocation Table

I/O(2)	28-Pin SPDIP, SOIC, SSOP	28-Pin VQFN	A/D	Reference	Comparator	ZCD	Timers/SMT	16-bit PWM/ CCP	CWG	CLC	SPI	I^2C	UART	DSM	IOC	Interrupt	Basic
RA0	2	27	ANA0	—	C1IN0- C2IN0-	—	—	—	—	CLCIN0(1) CLCIN4(1)	—	—	—	—	IOCA0	—	—
RA1	3	28	ANA1	—	C1IN1- C2IN1-	—	—	—	—	CLCIN1(1) CLCIN5(1)	—	—	—	—	IOCA1	—	—
RA2	4	1	ANA2	DAC1OUT1 V_{REF-} (DAC) V_{REF-} (ADC)	C1IN0+ C2IN0+	—	—	—	—	—	—	—	—	—	IOCA2	—	—
RA3	5	2	ANA3	V_{REF+} (DAC) V_{REF+} (ADC)	C1IN1+	—	—	—	—	—	—	—	—	MDCARL(1)	IOCA3	—	—
RA4	6	3	ANA4	—	—	—	T0CKI(1)	—	—	—	SS2(1)	—	CTS5(1)	MDCARH(1)	IOCA4	—	—
RA5	7	4	ANA5	—	—	—	—	—	—	—	SS1(1)	—	RX5(1)	MDSRC(1)	IOCA5	—	—
RA6	10	7	ANA6	—	—	—	—	—	—	—	—	—	CTS3(1)	—	IOCA6	—	CLKOUT OSC2
RA7	9	6	ANA7	—	—	—	—	—	—	—	—	—	RX3(1)	—	IOCA7	—	OSC1 CLKIN
RB0	21	18	ANB0	—	C2IN1+	ZCDIN	—	—	CWG1(1)	—	—	—	—	—	IOCB0	INT0(1)	—
RB1	22	19	ANB1	—	C1IN3- C2IN3-	—	—	—	CWG2(1)	—	—	—(4)	—	—	IOCB1	INT1(1)	—
RB2	23	20	ANB2	—	—	—	—	—	CWG3(1)	—	SDI2(1)	—(4)	—	—	IOCB2	INT2(1)	—
RB3	24	21	ANB3	—	C1IN2- C2IN2-	—	—	—	—	—	SCK2(1)	—	—	—	IOCB3	—	—
RB4	25	22	ANB4 ADACT(1)	—	—	—	T5G(1)	—	—	—	—	—	CTS4(1)	—	IOCB4	—	—
RB5	26	23	ANB5	—	—	—	T1G(1)	CCP3(1)	—	—	—	—	RX4(1)	—	IOCB5	—	—
RB6	27	24	ANB6	—	—	—	—	—	—	CLCIN2(1) CLCIN6(1)		—	CTS2(1)	—	IOCB6	—	ICSPCLK
RB7	28	25	ANB7	DAC1OUT2	—	—	T6IN(1)	PWM3ERS(1)	—	CLCIN3(1) CLCIN7(1)	—	—	RX2(1)	—	IOCB7	—	ICSPDAT
RC0	11	8	ANC0	—	—	—	T1CKI(1) T3CKI(1) T3G(1) SMT1WIN(1)	—	—	—	—	—	—	—	IOCC0	—	SOSCO

.....continued

I/O(2)	28-Pin SPDIP, SOIC, SSOP	28-Pin VQFN	A/D	Reference	Comparator	ZCD	Timers/SMT	16-bit PWM/ CCP	CWG	CLC	SPI	I2C	UART	DSM	IOC	Interrupt	Basic
RC1	12	9	ANC1	—	—	—	SMT1SIG(1)	CCP2(1)	—	—	—	—	—	—	IOCC1	—	SOSCIN SOSCI
RC2	13	10	ANC2	—	—	—	T5CKI(1)	PWMIN0(1) CCP1(1)	—	—	—	—	—	—	IOCC2	—	—
RC3	14	11	ANC3	—	—	—	T2IN(1)	PWM1ERS(1)	—	—	SCK1(1)	SCL1(3,4)	—	—	IOCC3	—	—
RC4	15	12	ANC4	—	—	—	—	—	—	—	SDI1(1)	SDA(3,4)	—	—	IOCC4	—	—
RC5	16	13	ANC5	—	—	—	T4IN(1)	PWM2ERS(1)	—	—	—	—	—	—	IOCC5	—	—
RC6	17	14	ANC6	—	—	—	—	PWMIN1(1)	—	—	—	—	CTS1(1)	—	IOCC6	—	—
RC7	18	15	ANC7	—	—	—	—	—	—	—	—	—	RX1(1)	—	IOCC7	—	—
RE3	1	26	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	—	Vpp/$\overline{MCLR}$
V_{SS}	19	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
V_{DD}(5)	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}(5)
V_{SS}	8	5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	ADGRDA ADGRDB	—	C1OUT C2OUT	—	TMR0	PWM11 PWM12 PWM21 PWM22 PWM31 PWM32 CCP1 CCP2 CCP3	CWG1A CWG1B CWG1C CWG1D CWG2A CWG2B CWG2C CWG2D CWG3A CWG3B CWG3C CWG3D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT CLC5OUT CLC6OUT CLC7OUT CLC8OUT	SS1 SCK1 SDO1 SS2 SCK2 SDO2	SDA1 SCL1	DTR1 RTS1 TX1 DTR2 RTS2 TX2 DTR3 RTS3 TX3 DTR4 RTS4 TX4 DTR5 RTS5 TX5	DSM1	—	—	—

Note:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to the peripheral input selection table for details on which port pins may be used for this signal.
2. All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in the peripheral output selection table.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins are configured for I^2C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RB1) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.
5. A 0.1 uF bypass capacitor to V_{SS} is required on the V_{DD} pin.

Table 2. 40/44/48-Pin Allocation Table

I/O(2)	40 Pin PDIP	40 Pin VQFN	44 Pin TQFP	48 Pin TQFP / VQFN	A/D	Reference	Comparator	ZCD	Timers/SMT	16-bit PWM/ CCP	CWG	CLC	SPI	I^2C	UART	DSM	IOC	Interrupt	Basic
RA0	2	17	19	21	ANA0	—	C1IN0- C2IN0-	—	—	—	—	CLCIN0(1) CLCIN4(1)	—	—	—	—	IOCA0	—	—
RA1	3	18	20	22	ANA1	—	C1IN1- C2IN1-	—	—	—	—	CLCIN1(1) CLCIN5(1)	—	—	—	—	IOCA1	—	—
RA2	4	19	21	23	ANA2	DAC1OUT1 V_{REF-} (DAC) V_{REF-} (ADC)	C1IN0+ C2IN0+	—	—	—	—	—	—	—	—	—	IOCA2	—	—
RA3	5	20	22	24	ANA3	V_{REF+} (DAC) V_{REF+} (ADC)	C1IN1+	—	—	—	—	—	—	—	—	MDCARL(1)	IOCA3	—	—
RA4	6	21	23	25	ANA4	—	—	—	T0CKI(1)	—	—	—	SS2(1)	—	CTS5(1)	MDCARH(1)	IOCA4	—	—
RA5	7	22	24	26	ANA5	—	—	—	—	—	—	—	SS1(1)	—	RX5(1)	MDSRC(1)	IOCA5	—	—
RA6	14	29	31	33	ANA6	—	—	—	—	—	—	—	—	—	CTS3(1)	—	IOCA6	—	CLKOUT OSC2
RA7	13	28	30	32	ANA7	—	—	—	—	—	—	—	—	—	RX3(1)	—	IOCA7	—	OSC1 CLKIN
RB0	33	8	8	8	ANB0	—	C2IN1+	ZCDIN	—	—	CWG1(1)	—	—	—	—	—	IOCB0	INT0(1)	—
RB1	34	9	9	9	ANB1	—	C1IN3- C2IN3-	—	—	—	CWG2(1)	—	—	—(4)	—	—	IOCB1	INT1(1)	—
RB2	35	10	10	10	ANB2	—	—	—	—	—	CWG3(1)	—	SDI2(1)	—(4)	—	—	IOCB2	INT2(1)	—
RB3	36	11	11	11	ANB3	—	C1IN2- C2IN2-	—	—	—	—	—	SCK2(1)	—	—	—	IOCB3	—	—
RB4	37	12	14	16	ANB4 ADACT(1)	—	—	—	T5G(1)	—	—	—	—	—	CTS4(1)	—	IOCB4	—	—
RB5	38	13	15	17	ANB5	—	—	—	T1G(1)	CCP3(1)	—	—	—	—	RX4(1)	—	IOCB5	—	—
RB6	39	14	16	18	ANB6	—	—	—	—	—	—	CLCIN2(1) CLCIN6(1)		—	CTS2(1)	—	IOCB6	—	ICSPCLK
RB7	40	15	17	19	ANB7	DAC1OUT2	—	—	T6IN(1)	PWM3ERS(1)	—	CLCIN3(1) CLCIN7(1)	—	—	RX2(1)	—	IOCB7	—	ICSPDAT

.....continued

I/O(2)	40 Pin PDIP	40 Pin VQFN	44 Pin TQFP	48 Pin TQFP / VQFN	A/D	Reference	Comparator	ZCD	Timers/SMT	16-bit PWM/ CCP	CWG	CLC	SPI	I2C	UART	DSM	IOC	Interrupt	Basic
RC0	15	30	32	34	ANC0	—	—	—	T1CKI(1) T3CKI(1) T3G(1) SMT1WIN(1)	—	—	—	—	—	—	—	IOCC0	—	SOSCO
RC1	16	31	35	35	ANC1	—	—	—	SMT1SIG(1)	CCP2(1)	—	—	—	—	—	—	IOCC1	—	SOSCIN SOSCI
RC2	17	32	36	40	ANC2	—	—	—	T5CKI(1)	PWMIN0(1) CCP1(1)	—	—	—	—	—	—	IOCC2	—	—
RC3	18	33	37	41	ANC3	—	—	—	T2IN(1)	PWM1ERS(1)	—	—	SCK1(1)	SCL1(3,4)	—	—	IOCC3	—	—
RC4	23	38	42	46	ANC4	—	—	—	—	—	—	—	SDI1(1)	SDA(3,4)	—	—	IOCC4	—	—
RC5	24	39	43	47	ANC5	—	—	—	T4IN(1)	PWM2ERS(1)	—	—	—	—	—	—	IOCC5	—	—
RC6	25	40	44	48	ANC6	—	—	—	—	PWMIN1(1)	—	—	—	—	CTS1(1)	—	IOCC6	—	—
RC7	26	1	1	1	ANC7	—	—	—	—	—	—	—	—	—	RX1(1)	—	IOCC7	—	—
RD0	19	34	38	42	AND0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD1	20	35	39	43	AND1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD2	21	36	40	44	AND2	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD3	22	37	41	45	AND3	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD4	27	2	2	2	AND4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD5	28	3	3	3	AND5	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD6	29	4	4	4	AND6	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RD7	30	5	5	5	AND7	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE0	8	23	25	27	ANE0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE1	9	24	26	28	ANE1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE2	10	25	27	29	ANE2	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RE3	1	16	18	20	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	—	Vpp/MCLR
RF0	—	—	—	36	ANF0	—	—	—	—	—	—	—	—	—	—	—		—	—
RF1	—	—	—	37	ANF1	—	—	—	—	—	—	—	—	—	—	—		—	—
RF2	—	—	—	38	ANF2	—	—	—	—	—	—	—	—	—	—	—		—	
RF3	—	—	—	39	ANF3	—	—	—	—	—	—	—	—	—	—	—		—	
RF4	—	—	—	12	ANF4	—	—	—	—	—	—	—	—	—	—	—		—	
RF5	—	—	—	13	ANF5	—	—	—	—	—	—	—	—	—	—	—		—	
RF6	—	—	—	14	ANF6	—	—	—	—	—	—	—	—	—	—	—		—	
RF7	—	—	—	15	ANF7	—	—	—	—	—	—	—	—	—	—	—		—	

.....continued

I/O(2)	40 Pin PDIP	40 Pin VQFN	44 Pin TQFP	48 Pin TQFP / VQFN	A/D	Reference	Comparator	ZCD	Timers/SMT	16-bit PWM/ CCP	CWG	CLC	SPI	I^2C	UART	DSM	IOC	Interrupt	Basic
V_{SS}	12, 31	6, 27	6, 29	6,31	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
V_{DD}(5)	11, 32	7, 26	7, 28	7, 30	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}(5)
OUT(2)					ADGRDA ADGRDB	—	C1OUT C2OUT	—	TMR0	PWM11 PWM12 PWM21 PWM22 PWM31 PWM32 CCP1 CCP2 CCP3	CWG1A CWG1B CWG1C CWG1D CWG2A CWG2B CWG2C CWG2D CWG3A CWG3B CWG3C CWG3D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT CLC5OUT CLC6OUT CLC7OUT CLC8OUT	SS1 SCK1 SDO1 SS2 SCK2 SDO2	SDA1 SCL1	DTR1 RTS1 TX1 DTR2 RTS2 TX2 DTR3 RTS3 TX3 DTR4 RTS4 TX4 DTR5 RTS5 TX5	DSM1	—	—	—

Note:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to the peripheral input selection table for details on which port pins may be used for this signal.
2. All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in the peripheral output selection table.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins are configured for I^2C logic levels; The SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RB1) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.
5. A 0.1 uF bypass capacitor to V_{SS} is required on all V_{DD} pins.

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