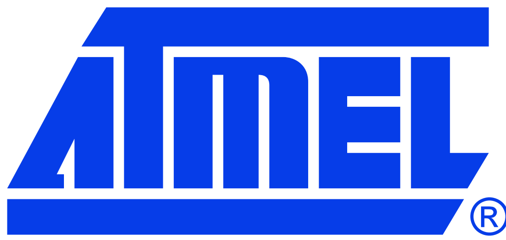

PS-AT28C010

revision C

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 128K x 8-Bit

PARALLEL EEPROM, MONOLITHIC SILICON

Revision	Written by	Approved by	Date
C	S.JAMES	C. FERRE	03/01/08

DOCUMENTATION CHANGE NOTICE

Date of update	Revision letter	modifications
B	28/03/07	Update of table 1 with functional tests
C	03/01/08	Add data retention test description

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1 GENERAL

1.1 Scope

This specification details the ratings, physical and electrical characteristics, tests and inspection data of the 128K x 8-Bit EEPROM named AT28C010. It also defines the specific requirement for space and military applications with high reliability.

1.2 Identification

Part number	Description	Access Time	Case	Level
AT28C010-12DK-MQ	128K x 8-Bit eeprom	120 ns	Flat pack 435 mils 32 leads	Military Level B
AT28C010-12DK-SV	128K x 8-Bit eeprom	120 ns	Flat pack 435 mils 32 leads	Space Level B

1.3 Absolute maximum ratings

Supply voltage range (V_{DD})... -0.6V to 6.25V
Output voltage range (V_{OUT})... -0.6V dc to V_{DD} + 0.6V dc
Power dissipation (Pd).. 0,3W
Storage temperature .... -65°C to 150°C
Maximum junction temperature (T_J).................................. 175°C
Thermal resistance junction to case (Θjc) : .... 6°C/W
Lead temperature (soldering @ 1/16 in, 10 s) .... 300°C
Endurance... 50,000 cycles/byte
Data retention .... 10 years

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})... 4.5 V dc to 5.5 V dc
Ambient operating temperature (T_A) ……………………….. -55°C to 125°C
Storage temperature .... 30°C, 20 to 65% RH, dust free, original packing

1.5 Radiation features

Tested up to a Total Dose of (according to MIL STD 883 Method 1019) :

(dose rate 0.1 rad/s)... 10 kRads (Si) Read Only Mode, when biased
.... 30 kRads (Si) Read Only Mode, when un-biased

No Single Event Latch-up below a LET Threshold of 80 $MeV/mg/cm^2$

1.6 Handling precautions

These components are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacturing, testing, shipment and any handling.
ESD.. 2000 V

2 APPLICABLE DOCUMENTS

MIL-PRF-38535 ....Integrated Circuits, Manufacturing, General Specification for.
MIL-STD-883 ....Test Method Standard Microcircuits.
ASTM Standard F1192-95 ....Standard guide for the measurement of single event phenomena from heavy ion irradiation of semiconductor devices
JEDEC Standard EIA/JESD78..................IC latch-up test
ATMEL Aerospace Products Quality Flows

In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence.

3 REQUIREMENTS

3.1 Design, construction, and physical dimensions.

The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.1.1 Package type.

The package shall be a flat pack 435 mils, 32 leads (figure1). The case shall be hermetically sealed and have a ceramic body. The leads shall be brazed.

3.1.2 Terminal connections.

The terminal connections shall be as specified on figure 2 .

3.1.3 Block diagram.

The block diagram and the truth table shall be as specified on figure 3 .

3.1.4 Timing waveforms.

The timing waveforms shall be as specified on figure 4 .

3.2 Marking

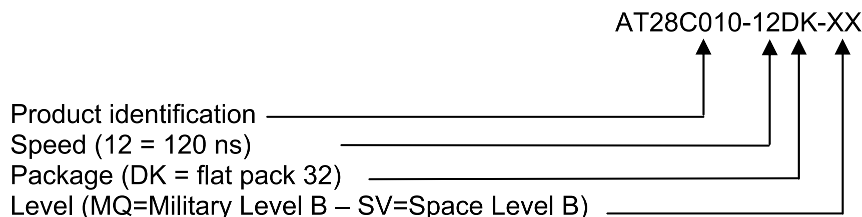
Each component shall be marked in respect of:
(a) Lead Identification
(b) Component Number
(c) Traceability Information
(d) Manufacturer's Component Number

3.2.1 Lead Identification

An index shall be located at the top of the package in the position defined in Figure 1.

3.2.2 Component Number

Each component shall bear the component number which shall be constituted and marked as follows :



3.2.3 Traceability Information

Each component shall be marked in respect of traceability information : lot number and date code.

3.3 Electrical characteristics

The parameters to be measured with respect of electrical characteristics are scheduled in Table 1. The measurements shall be performed at T_{amb}=22 ± 3°C, T_{high}=125 (+0/-5)°C and T_{low} = -55 (+5/-0)°C respectively.

3.4 Burn-in test

3.4.1 Electrical circuit

Circuit for use in performing the power burn-in is shown in figure 5, in accordance with the intent specified in test method 1015 of MIL-STD-883.

3.4.2 Parameters drift value

For space level, the parameter drift values applicable to burn-in are specified in Table 2 of this specification. Unless otherwise stated, measurements shall be performed at + 22 $\pm$ 3 ° C. The parameter drift values (Δ), applicable to the parameters scheduled, shall not be exceeded.
In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 1 shall not be exceeded.
.

3.5 Environmental and Endurance Tests

3.5.1 Electrical Circuit for Operating Life Test

The circuit for operating life testing shall be as specified for power burn in (figure 5).

3.5.2 Electrical Measurements at Completion of Environmental and endurance tests

The parameters to be measured are scheduled in Table 1. Unless otherwise stated, the measurements shall be performed at t_{amb} = 22$\pm$3°C.

3.5.3 Conditions for Operating Life Test

The conditions for operating life testing shall be as specified for power burn in.

3.5.4 Data Retention Screening

An electrical screening is performed during probe in order to guarantee data retention. The Device Under Test is filled with a checker board, then, is configured in margin mode test which allows a linear search of the high or low voltage threshold (high = “1” and low = “0” in the memory cell). The high (or low) recorded threshold voltage represents the fist fail occurring in all the cells. It must be higher than the reference voltage applied on all control gates during normal read operation. To guarantee the reliability of the read operation, a voltage guard band is applied between the reference voltage and the high (or low) threshold voltage.
In a second time, the Device under test performed a bake operation (250 °C / 24 H / without power supply), and is retested with the following flow:

- Read operation in order to check the integrity of the memory.
- Performed a new linear search of the voltage threshold with checking if the valued measure is still higher than the reference voltage, and also, if the drift of the measure before and after the bake do not exceed 0.2V. If one of these two condition is not respected the data retention is failed.

3.6 Total dose irradiation testing

3.6.1 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

3.6.2 Electrical Measurements

The parameters to be measured prior to, during and on completion of irradiation texture are scheduled in Table 1 of this specification.

4 QUALITY ASSURANCE PROVISIONS

4.1 Wafer lot validation

Compliant with ATMEL Quality Management System.

For space level, Wafer Lot is accepted by a SEM performed according to PAQC0016 (PAQC0016 referred to MIL-Std-883 method 2018 and 21400 ESCC specification).

4.2 Sampling and inspection.

Sampling and inspection procedures shall be in accordance with MIL-PRF-38535.

4.3 Screening.

Screening equivalent to MIL-PRF-38535. Screening shall be conducted on all devices prior to qualification and technology conformance inspection

- The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in accordance with MIL-PRF-38535.
- Additional screening for space application devices shall be as specified in MIL-PRF-38535, appendix B.

4.4 Quality conformance inspection

Qualification inspection for high reliability and space level devices shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections.

4.4.1 Group A inspection.

- Tests shall be as specified in table 1 herein.
- Subgroups 5 and 6 of table I of method 5005 of MIL STD 883 shall be omitted.
- Subgroups 7 and 8 of table I of method 5005 of MIL STD 883 shall include verifying the functionality of the device.
- O/V (latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device.
- Capacitance measurement shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failure, and all input and output terminals tested.

4.4.2 Group C inspection.

The group C inspection end-point electrical parameters shall be as specified in table 1 herein.

4.4.3 Group D inspection.

The group D inspection end-point electrical parameters shall be as specified in table 1 herein.

4.5 Delta measurements

Delta measurements, as specified in table 2, shall be made and recorded before and after the required burn-in screens to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table 2. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7 and 9.

5 PACKAGING

5.1 Packaging requirements

The requirements for packaging shall be in accordance with MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test method Mil-Std-883	Conditions $-55°C \leq T_C \leq +125°C$ $+4.5\ V \leq V_{DD} \leq +5.5\ V$ unless otherwise specified	Limits		Unit
				Min	Max	
Functionnal test 1	-	3014	Verify truth table Note 1	-	-	-
Functionnal test 2	-	3014	Verify truth table Note 1	-	-	-
Functionnal test 3	-	3014	Verify truth table Note 1	-	-	-
Functionnal test 4	-	3014	Verify truth table Note 1	-	-	-
High level input current	I_{IH}	3010	VCC= 5.5V, VIN (under test) = 5.5V (VIN remaining inputs = 0V)	-	10	µA
Low level input current	I_{IL}	3010	VCC= 5.5V, VIN (under test) = 0V (VIN remaining inputs = 5.5V)	-10		µA
High impedance output leakage current state, low level	I_{OZL}	-	VIN ($\overline{CE}$)= 0V VIN ($\overline{WE}$, $\overline{OE}$) = 5V VCC = 5.5V VOUT = 0V	-10	-	µA
High impedance output leakage current state, high level	I_{OZH}	-	VIN ($\overline{CE}$)= 0V VIN ($\overline{WE}$, $\overline{OE}$) = 5V VCC = 5.5V VOUT = 5.5V	-	10	µA
Input Low voltage	V_{IL}				0.8	V
Input Low voltage	V_{IH}			2.0		V
High level output voltage TTL	V_{OH1}	3007	VCC =4,5 V, I_{OH} = -400 µA Note 2	2.4		V
High level output voltage CMOS	V_{OH2}	3007	VCC =4,5 V, I_{OH} = -100 µA Note 2	4.2		V
Low level output voltage	V_{OL}	3007	VCC =4.5 V, I_{OL} = 2.1 mA Note 3		0.45	V
Dynamic Operating current	I_{CCOP}	3005	F = $1/T_{AVAV}$ I_{OUT} = 0 mA VCC = 5.5V $\overline{WE}$ = $\overline{OE}$ =VIH		50	mA
Supply current Stand-by mode TTL	I_{CCSB1}	3005	VCC = 5.5V CS ≥ VIH		10	mA
Supply current Standby mode CMOS	I_{CCSB2}	3005	VCC = 5.5V CS ≥ VCC-0.3		10	mA
Input capacitance	C_{IN}	3012	V_{IN} = 0 V T_C = 25°C f_{IN} = 1.0 MHz Note 4		10	pF
Output capacitance	C_{OUT}	3012	V_{OUT} = 0 V T_C = 25°C f_{IN} = 1.0 MHz Note 4		12	pF

Test	Symbol	Test method Mil-Std-883	Conditions $-55°C \leq T_C \leq +125°C$ $+4.5\ V \leq V_{DD} \leq +5.5\ V$ unless otherwise specified	Limits		Unit
				Min	Max	
Read cycle time	T_{AVAV}	3003	VCC = 4.5 & 5.5V Notes 6,5		120	ns
Address access time	T_{AVQV}	3003	VCC = 4.5 & 5.5V Notes 6,5		120	ns
$\overline{CE}$ access time	T_{ELQV}	3003	VCC = 4.5 & 5.5V Notes 6,5		120	ns
$\overline{OE}$ access time	T_{OLQV}	3003	VCC = 4.5 & 5.5V Notes 6,5		50	ns
$\overline{OE}$ or $\overline{CE}$ disable to output in high Z	T_{EHQZ} T_{OHQZ}	3003	VCC = 4.5 & 5.5 V Notes 7,8		50	ns
Output hold from address change	T_{OHQX} T_{AXQX} T_{EHQX}	3003	Note 6	0		ns
Address setup time	T_{AVWL} T_{AVEL}	3003	VCC = 5.5 V Notes 6,9	0		ns
Address hold time	T_{WLAX} T_{ELAX}	3003	Notes 6,9	50		ns
$\overline{CE}$ setup time	T_{ELWL} T_{WLEL}	3003	VCC = 4.5 & 5.5V Note 6	0		ns
$\overline{CE}$ hold time	T_{WHEH} T_{EHWH}	3003	VCC = 4.5 & 5.5V Note,6	0		ns
Write pulse width ($\overline{WE}$ or $\overline{CE}$)	T_{WLWH} T_{ELEH}	3003	VCC = 4.5 V Notes 6, 9	100		ns
Data setup time	T_{DVWH} T_{DVEH}	3003	VCC = 4.5 V Notes 6,9	50		ns
Data hold time	T_{WHDX} T_{EHDX}	3003	Note 6	0		ns
Write cycle time ($\overline{WE}$ or $\overline{CE}$)	T_{WHWL1} T_{EHEL1}	3003	Note 6		10	ms
Byte load cycle	T_{WHWL2}	3003	Note 4		150	µs
Write pulse width High	T_{WPH}	3003	VCC = 4.5 & 5.5V Note 6	50		ns
$\overline{OE}$, $\overline{CE}$ setup time (chip erase)	T_{ELWL2} T_{OHWL2}	3003	VCC = 4.5V Note 6	5		ms
$\overline{WE}$ pulse width (chip erase)	T_{WLWH2}	3003	VCC = 4.5V Note 6	10		ms
$\overline{OE}$, $\overline{CE}$ hold time (chip erase)	T_{WHEH2} T_{WHOL2}	3003	VCC = 4.5V Note 6	10		ms
Data hold time ($\overline{Data}$ Polling)	T_{WHDX}	3003	Note 4	10		ns
$\overline{OE}$ hold time ($\overline{Data}$ Polling)	T_{WHOL}	3003	Note 4	10		ns
Write Recovery Time ($\overline{Data}$ Polling)	T_{WR}	3003	Note 4	0		ns

Test	Symbol	Test method Mil-Std-883	Conditions -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{DD} ≤ +5.5 V unless otherwise specified	Limits		Unit
				Min	Max	
Data hold time (Toggle Bit)	T_{WHDX}	3003	Note 4	10		ns
$\overline{OE}$ hold time (Toggle Bit)	T_{WHOL}	3003	Note 4	10		ns
$\overline{OE}$ High Pulse (Toggle Bit)	T_{OEHP}	3003	Note 4	150		ns
Write Recovery Time (Toggle Bit)	T_{WR}	3003	Note 4	0		ns

Notes

1/ Functional go-no-go test with the following test sequence:

FUNCTIONAL TEST 1

Pattern	Timing (ns) (a)	VCC (V)	VSS (V)	VIL (V)	VIH (V)	IOL (mA)	IOH (mA)	Vout comp (V)
Zeros	300	4.5 and 5.5V	0	0	2	0.5	-0.5	1.5
Ones	300	4.5 and 5.5V	0	0	2	0.5	-0.5	1.5
Checkerboard	300	4.5 and 5.5V	0	0	2	0.5	-0.5	1.5
Inverse Checkerboard	300	4.5 and 5.5V	0	0	2	0.5	-0.5	1.5

FUNCTIONAL TEST 2

Pattern	Timing (ns) (a)	VCC (V)	VSS (V)	VIL (V)	VIH (V)	IOL (mA)	IOH (mA)	Vout comp (V)
Checkerboard	300	5.5	0	-0.3	6	0.5	-0.5	1.5
Inverse Checkerboard	300	4.5	0	-0.3	6	0.5	-0.5	1.5
Checkerboard	300	5.5	0	0	2	0.5	-0.5	(b)
Inverse Checkerboard	300	4.5	0	0.8	3	0.5	-0.5	(b)

FUNCTIONAL TEST 3

Pattern	Timing (ns) (a)	VCC (V)	VSS (V)	VIL (V)	VIH (V)	IOL (mA)	IOH (mA)	Vout comp (V)
Checkerboard	300	4.5	0	0	3	2.1	-0.4	(b)

FUNCTIONAL TEST 4

Pattern	Timing (ns) (a)	VCC (V)	VSS (V)	VIL (V)	VIH (V)	IOL (mA)	IOH (mA)	Vout comp (V)
Zeros	240	4.5 and 5.5V	0	0	3	1.2	-3.0	1.5
Ones	240	4.5 and 5.5V	0	0	3	1.2	-3.0	1.5
Checkerboard	240	4.5 and 5.5V	0	0	3	1.2	-3.0	1.5
Inverse Checkerboard	240	4.5 and 5.5V	0	0	3	1.2	-3.0	1.5

(a) : write cycle is followed by a read cycle.
(b) : 0.45V for low output level, 2.4V for high output level

2/ select address inputs to produce a low level at the pin under test.

3/ select address inputs to produce a high level at the pin under test.

4/ guaranteed but not tested

5/ Parameter measured during functional test 4 using pattern Checker board at 4.5V and 5.5V.

6/ Parameter tested go-no-go during functional test 4.

7/ T_{EHQZ} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (CL = 5 pF).

8/ Guaranteed with output loading 5pF but not tested. Characterized at initial design and after major process changes.

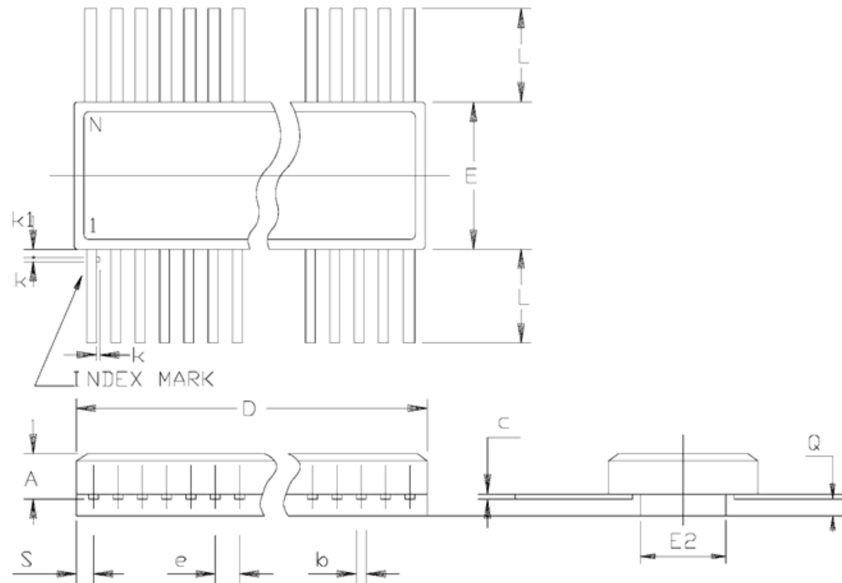
9/ Parameter measured during functional test 4 using pattern Checker board in Vcc worst case.

TABLE 2. Parameter drift values

Test	Symbol	Test method Mil-Std-883	Conditions	Drift limits	Unit
High level output voltage	V_{OH1}	As per table 1	As per table 1	0.1	V
High level output voltage	V_{OH2}	As per table 1	As per table 1	0.1	V
Low level output voltage	V_{OL}	As per table 1	As per table 1	0.1	V
Low level Input current	I_{IL}	As per table 1	As per table 1	1	µA
High level Input current	I_{IH}	As per table 1	As per table 1	1	µA
Output leakage Low current	I_{OZL}	As per table 1	As per table 1	1	µA
Output leakage High current	I_{OZH}	As per table 1	As per table 1	1	µA
Supply current Standby mode TTL	I_{CCSB1}	As per table 1	As per table 1	1	mA
Supply current Standby mode CMOS	I_{CCSB2}	As per table 1	As per table 1	1	mA

Note: the above parameter shall be recorded before and after burn-in to determine the delta.

FIGURE 1. Case outline



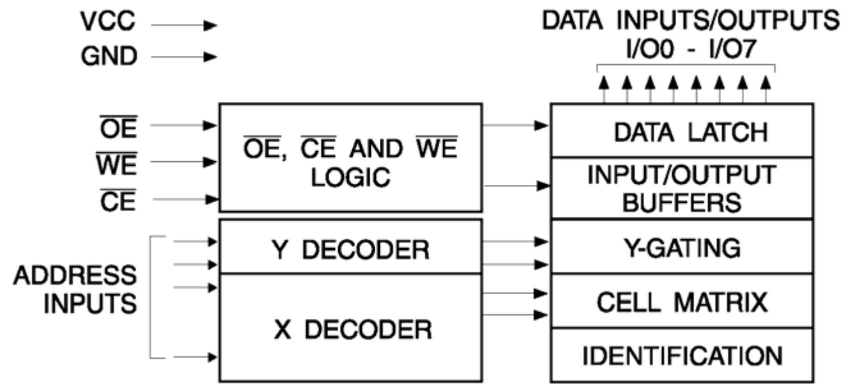
	Mm		inch	
	Min	**Max**	**Min**	**Max**
A	1.78	2.72	0.070	0.107
b	0.38	0.48	0.015	0.019
c	0.076	0.18	0.003	0.007
D	20.62	21.03	0.812	0.828
E	10.92	11.18	0.430	0.440
E2	8.46	80.82	0.333	0.347
K	0.20	0.39	0.008	0.015
K1	0.63 BSC		0.025 BSC	
e	1.27 BSC		0.050 BSC	
L	6.65	8.20	0.262	0.323
Q	0.66	0.91	0.026	0.036
S	---	1.14	---	0.045
N	32			

FIGURE 2. Terminal connections.

Case outline		X	
Pin Number	Name	Pin Number	Name
1	A16	17	I/O3
2	A15	18	I/O4
3	A12	19	I/O5
4	A7	20	I/O6
5	A6	21	I/O7
6	NC	22	$\overline{CE}$
7	A5	23	A10
8	A4	24	$\overline{OE}$
9	A3	25	A11
10	A2	26	A9
11	A1	27	A8
12	A0	28	A13
13	I/O0	29	A14
14	I/O1	30	$\overline{WE}$
15	I/O2	31	NC
16	GND	32	VCC

Name	**Description**
A0 - A16	addresses
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
I/O0 – I/O7	Data inputs/Outputs
NC	Not connected
VCC	Power
GND	Ground

FIGURE 3. Block diagram and the truth table



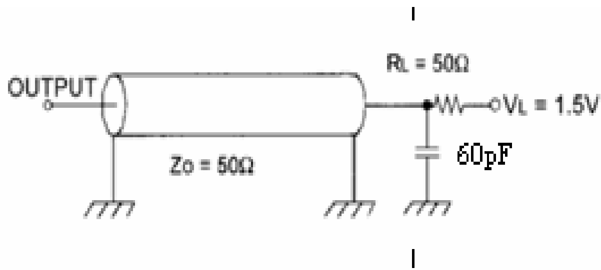
The truth table is as follow:

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	**Inputs/Outputs**	**Mode**
H	**X**	**X**	**Z**	**Stand-by/ Write Inhibit**
L	**H**	**L**	**Data out**	**Read**
L	**L**	**H**	**Data in**	**Write**
X	**H**	**X**	**Z or Data out**	**Write inhibit**
X	**X**	**L**	**Z or Data out**	**Write inhibit**
L	**L**	**L**	**No operation**	**Write inhibit**

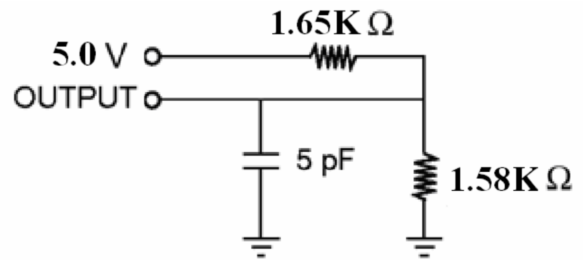
Note: L=low, H=high, X=low or high, Z=high impedance

AC Characteristics:

Temperature Range: …………………………………………………. -55 +125°C
Supply Voltage: ………………………………………………………. 5.0 ± 0.5 V
Input Pulse Levels…………………………………………………….. GND to 3.0 V
Input Timing reference levels…………………………………………. 1.5V
Output level detection ……………………………………………..…. 1.5 ± 0.05V



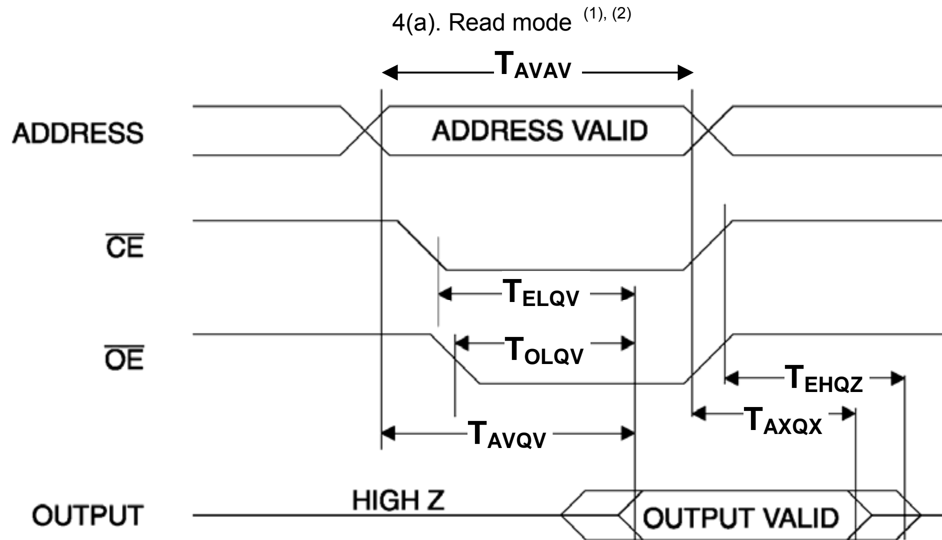
General



Specific (Tehqz, Tohqz)

FIGURE 4. Timing waveforms.

4(a). Read mode [(1), (2)]

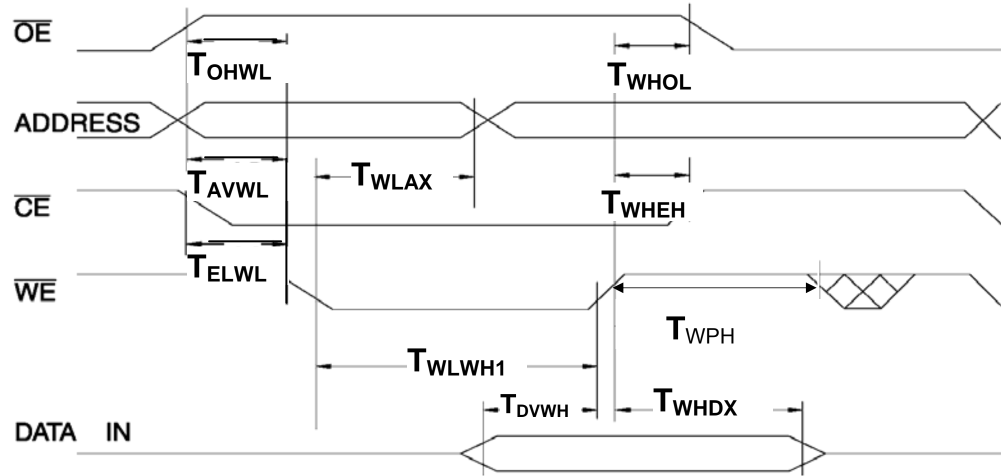


Note:

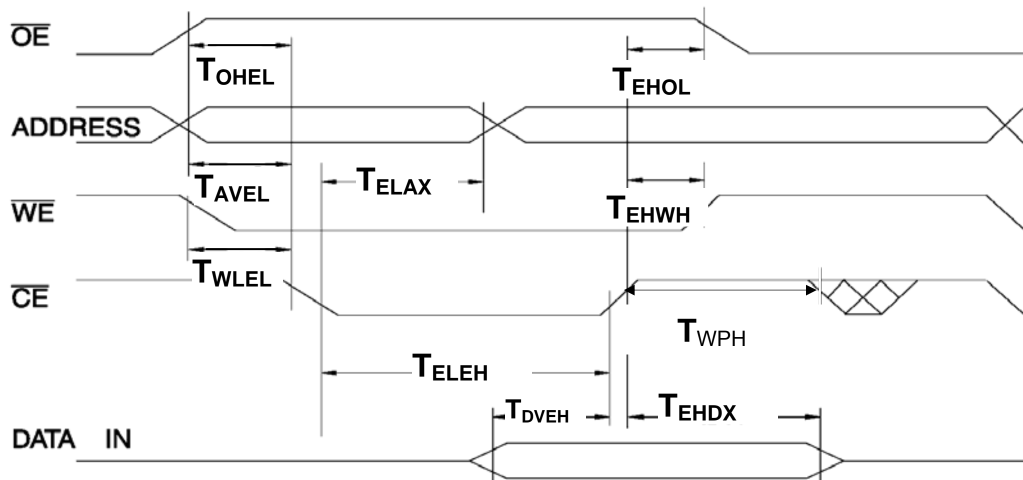
(1) $\overline{CE}$ may be delayed up to T_{AVQV} - T_{ELQV} after the address transition without impact on T_{AVQV}.

(2) $\overline{OE}$ may be delayed up to T_{ELQV} - T_{OLQV} after the falling edge of $\overline{CE}$ without impact on T_{ELQV} or by T_{AVQV} - T_{OLQV} after an address change without impact in T_{AVQV}.

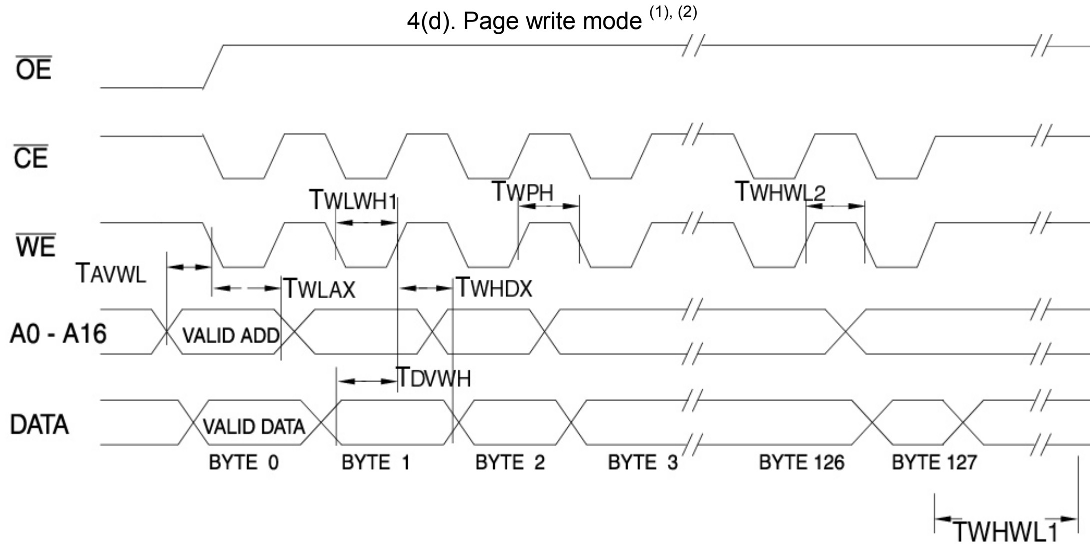
4(b). $\overline{WE}$ controlled byte write mode



4(c). $\overline{CE}$ controlled byte write mode



4(d). Page write mode (1), (2)

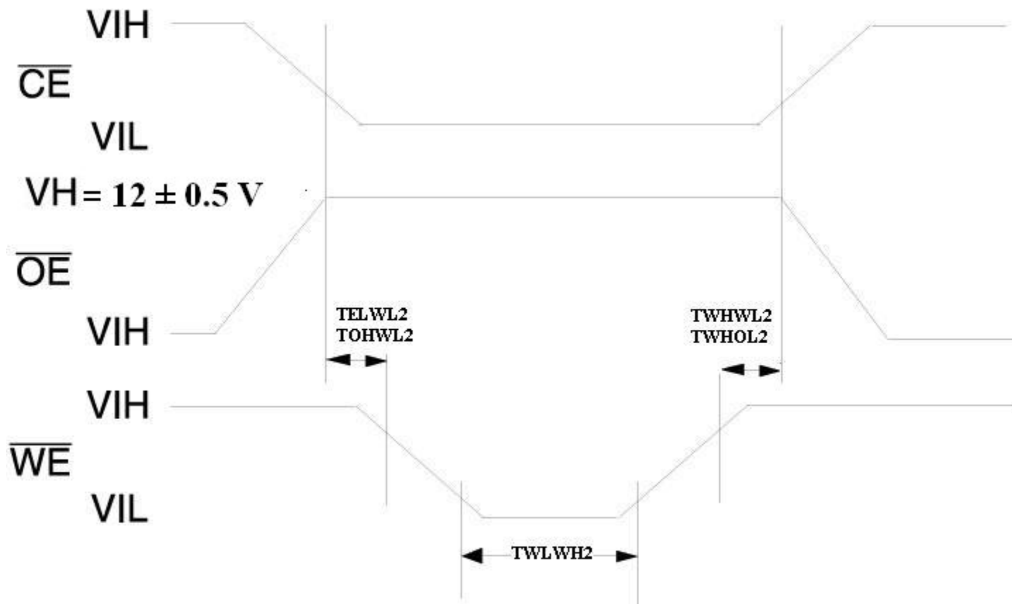


Notes:

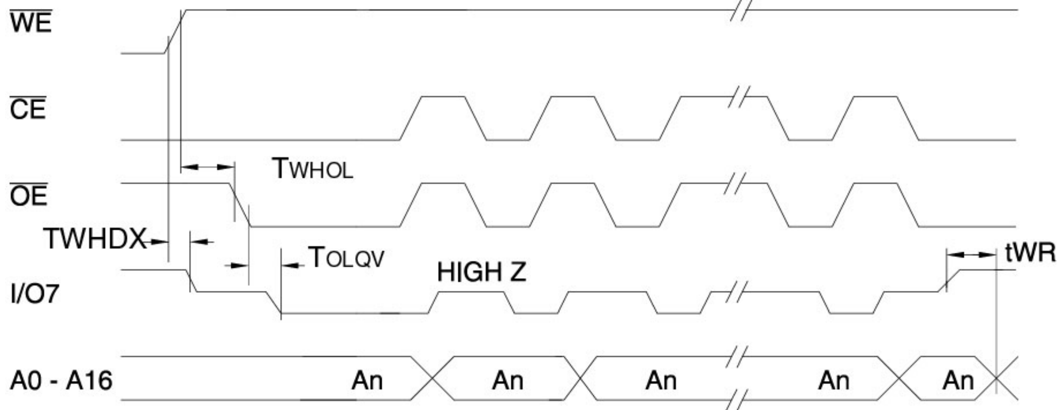
(1) Addresses A7 through A16 must specify the page address during each high to low transition of $\overline{\text{WE}}$ (or $\overline{\text{CE}}$)

(2) $\overline{\text{OE}}$ must be high only when $\overline{\text{WE}}$ and $\overline{\text{CE}}$ are both low

4(e). Chip Erase mode



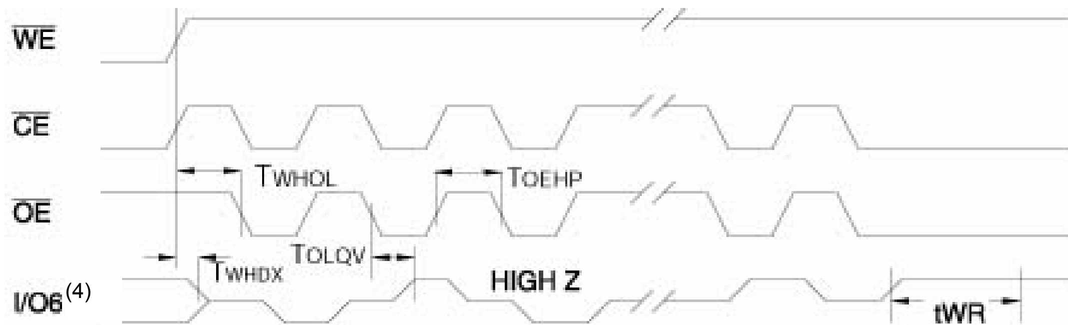
4(f). $\overline{Data}$ Polling Mode [1]



Note:

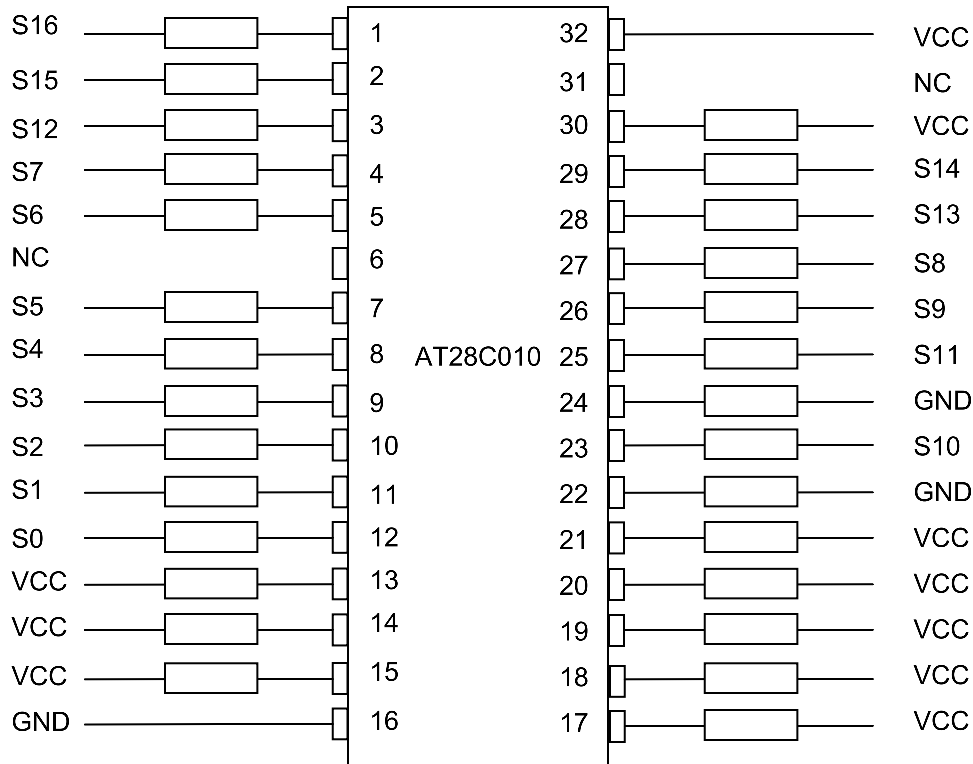
(1) Parameters guaranteed but not tested in this case

4(g). Toggle Bit Mode [1], [2], [3], [4]



Notes
(1) Parameters guaranteed but not tested in this mode
(2) Toggling either OE or CE or both OE and CE will operate toggle bit
(3) Beginning and ending state of I/O6 will vary
(4) Any address location may be used but the address should not vary

FIGURE 5. Electrical circuit for power burn-in and operating life test



Characteristics	Symbol	Conditions	Unit
Ambient Temperature	Tamb	125 (+0/-5)	°C
Address inputs	Vin	S0 to S16 (note 1)	Vac
Select pins	CS	0	V
Control inputs	WE	VCC	V
Control inputs	OE	0	V
Pulse frequency	F_0	1.65 +/- 20%	MHz
Positive Supply Voltage	VCC	5.7V (+0.1 /-0.1)	V
Negative Supply Voltage	GND	0	V

Notes:

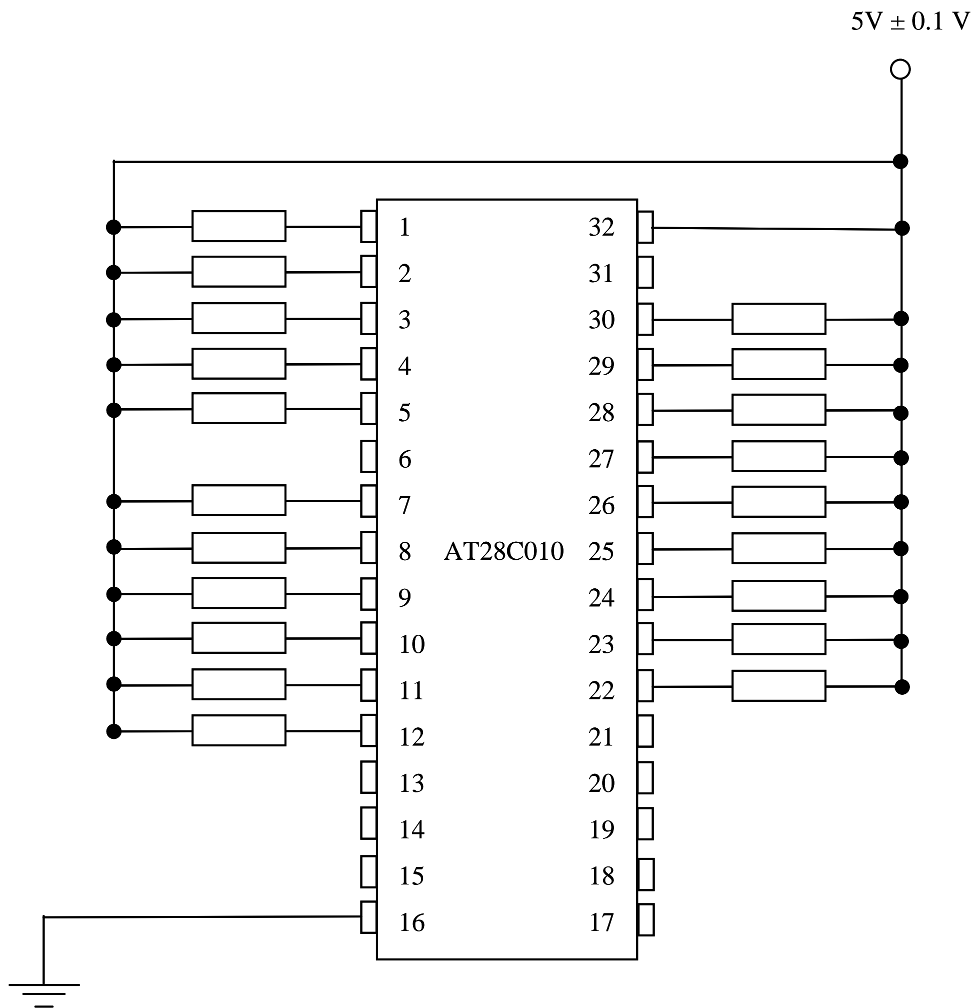
(1) S0 TO S16 are droved signals with the following frequency :

S_0 frequency = F_0

S_N frequency = $F_n = \frac{1}{2}.F_{n-1}$ for n>=1

Resistors = 1 KΩ

FIGURE 6. Electrical circuit for total dose radiation test.



Input protection resistors = 512 ohm