REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline Y. - phn	08-11-04	Thomas M. Hess
B	Removed “ground lid” note for case outline X in section 1.2.4 and in figure 1. - phn	09-01-14	Charles F. Saffle
C	Add case outline Z. - phn	10-07-12	Thomas M. Hess

REV																				
SHEET																				
REV																				
SHEET																				
REV	C	C	C	C																
SHEET	15	16	17	18																

REV STATUS	REV	C	A	C	A	A	A	A	A	A	A	A	A	A	B	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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Thomas M. Hess

DRAWING APPROVAL DATE
08-07-01

REVISION LEVEL
C

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, DIGITAL, CMOS, MH1, GATE ARRAY, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-08B01**

SHEET 1 OF 18

DSCC FORM 2233
APR 97

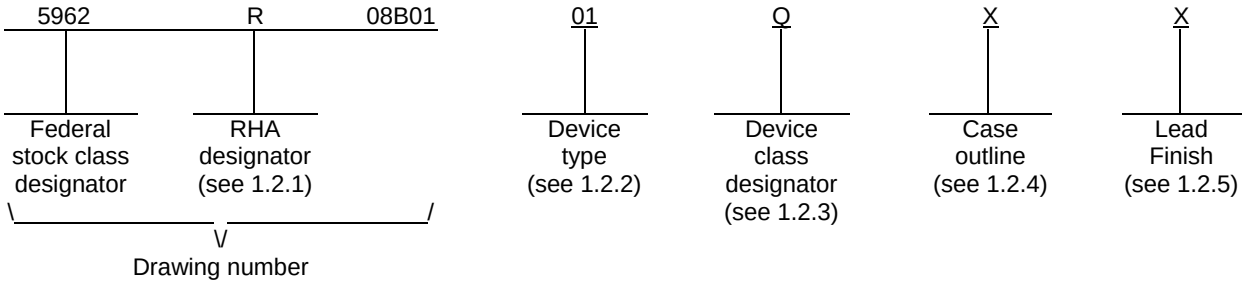
5962-E397-10

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN) in the applicable Altered Item Drawing (AID). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

Customizations (personalizations) for each design, including circuit organization, electrical performance characteristics, and test conditions, shall be specified in an Altered Item Drawing (AID) (see 3.3 herein).

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number			Circuit function
01	TH1099ER	1/	3/	988,000 sites available MH1RT
02	TH1156ER	1/	3/	1,558,000 sites available MH1RT
03	TH1242ER	1/	3/	2,422,000 sites available MH1RT
04	TH1332ER	1/	3/	3,319,000 sites available MH1RT
05	TH1099ES	2/	3/	988,000 sites available MH1RT
06	TH1156ES	2/	3/	1,558,000 sites available MH1RT
07	TH1242ES	2/	3/	2,422,000 sites available MH1RT
08	TH1332ES	2/	3/	3,319,000 sites available MH1RT
09	TH1M099ER	1/	4/	composite 988,000 sites MH1RT
10	TH1M156ER	1/	4/	composite 1,558,000 sites MH1RT
11	TH1M242ER	1/	4/	composite 2,422,000 sites MH1RT
12	TH1M332ER	1/	4/	composite 3,319,000 sites MH1RT
13	TH1M099ES	2/	4/	composite 988,000 sites MH1RT
14	TH1M156ES	2/	4/	composite 1,558,000 sites MH1RT
15	TH1M242ES	2/	4/	composite 2,422,000 sites MH1RT
16	TH1M332ES	2/	4/	composite 3,319,000 sites MH1RT

Device type	Generic number			Circuit function
17	TH1099R	1/	3/	988,000 sites available MH1
18	TH1156R	1/	3/	1,558,000 sites available MH1
19	TH1242R	1/	3/	2,422,000 sites available MH1
20	TH1332R	1/	3/	3,319,000 sites available MH1
21	TH1099S	2/	3/	988,000 sites available MH1
22	TH1156S	2/	3/	1,558,000 sites available MH1
23	TH1242S	2/	3/	2,422,000 sites available MH1
24	TH1332S	2/	3/	3,319,000 sites available MH1
25	TH1M099R	1/	4/	composite 988,000 sites MH1
26	TH1M156R	1/	4/	composite 1,558,000 sites MH1
27	TH1M242R	1/	4/	composite 2,422,000 sites MH1
28	TH1M332R	1/	4/	composite 3,319,000 sites MH1
29	TH1M099S	2/	4/	composite 988,000 sites MH1
30	TH1M156S	2/	4/	composite 1,558,000 sites MH1
31	TH1M242S	2/	4/	composite 2,422,000 sites MH1
32	TH1M332S	2/	4/	composite 3,319,000 sites MH1
33	TH1256A			FPGA conversion

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835, and as follows:

Outline letter 5/	Descriptive designator	Terminals	Package style
X	See figure 1a	132	Quad flat pack unformed leads
Y	See figure 1b	472	Land grid array – grounded lid
Z	See figure 1c	349	Land grid array – grounded lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ These devices are capable of operating at 2.5, 3.0, 3.3 V. See table I for limits.
2/ These devices are capable of operating at 2.5, 3.0, 3.3 V and I/O are Tolerant/Compliant 5.0 V. See table I for limits.
3/ Device will be customized at metal levels.
4/ Device will be customized at base wafer and metal levels.
5/ Additional packages are available on SMD 5962-01B01

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{DD}) ..... -0.5 V to 4.0 V
Supply voltage range (V_{CC}) ..... -0.5 V to 6.0 V 3/
Input voltage range
Low voltage range (V_{IN}) ..... -0.5 V to V_{DD} + 0.5 V
5 V compliant (V_{IN})..... -0.5 V to V_{CC} + 0.5 V
5 V tolerance (V_{IN}) ..... -0.5 V to 6.0 V
Input pin current (I_{IN})
Signal pin..... -10.0 mA to 10.0 mA
Power pin ..... -60 mA to 60 mA
Lead temperature (soldering 10 sec) ..... +300°C 4/
Storage temperature range (T_s) ..... -65°C to +150°C
Maximum junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage range 1(V_{DD}) ..... 2.7 V to 3.3 V
Supply voltage range 2(V_{DD}) ..... 2.3 V to 2.7 V
Supply voltage range 3(V_{DD}) ..... 3.0 V to 3.6 V
Supply voltage range – interface I_O (V_{CC}) ..... 4.5 V to 5.5 V 3/
Ambient temperature (T_A) ..... -55°C to 125°C

1.5 Radiation features.

Maximum total dose available..... 100 Krads 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. . Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltages referenced to ground unless otherwise specified.
3/ V_{CC} range is applicable to the inner peripheral interface when compliant buffers are used.
4/ Duration 10 sec maximum at a distance not less than 1.6 mm.
5/ Unless otherwise specified in the AID.

2.2 Non Government Publications. The following document(s) form a part of this document to the extent specified herin. Unless otherwise specified, the issues of the documents(s) which are DOD adopted are those listed in the DODISS cited in the solicitation

JEDEC PUB 95-1 – Design Requirements for Generic matrix Trays.

(Applications for copies should be addressed to the Electronic Industry Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or at http://www.jedec.org)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.3 AID requirements. All AIDs written against this SMD shall be sent to DSCC-VA. The following items shall be provided to the device manufacturer by the customer as part of an AID. Items 3.3.3 through 3.3.9 form a part of the manufacturer's design database/database archive. These items shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. As such, these items will not appear in the AID in the traditional sense.

3.3.1 Terminal connections and pin assignments.

3.3.2 Package type (see 1.2.4).

3.3.3 Functional block diagram (or equivalent VHDL behavioral description).

3.3.4 Logic diagram (or equivalent structural VHDL description).

3.3.5 Pin function description.

3.3.6 Design tape # or design document name (i.e., net list).

3.3.7 Design functional tape # or name.

3.3.8 Test functional tape # or name.

3.3.9 Switching waveform(s).

3.3.10 Fault coverage. The extent of fault coverage is controlled by the quality of the customers design input, therefore fault coverage shall be specified by the customer.

3.3.11 Device electrical performance characteristics. Device electrical performance characteristics shall include dc parametric (see table I herein for minimum requirements), functional, input to output ac parameters and any other data which would be considered required by a design engineer. All electrical performance characteristics apply over the full recommended case operating temperature range and specified test load conditions.

3.3.12 Maximum power dissipation. Maximum power dissipation shall be in accordance with the application specific design.

3.3.13 RHA post-irradiated electricals. For RHA devices supplied to this drawing, the RHA post irradiated electricals shall be specified in the AID.

3.4 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.6 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A. The AID number shall be added to the marking by the manufacturer.

3.6.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.10 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device class M. Device classes M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le 125°C$ $3.0\ V \le V_{DD} \le 3.6\ V$ unless otherwise specified for device operate at $V_{DD} = 3.3\ V$	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Low level input current (w/o pull-up or pull-down resistor)	I_{IL}	$V_{IN} = V_{SS}$, CMOS buffers	1,2,3	All	-1	1	µA
Low level input current Pull-up resistor PRU1 2/	I_{ILPU}	$V_{IN} = V_{SS}$, CMOS buffers	1,2,3	All	70	230	µA
Low level input current Pull-down resistor PRD1	I_{ILPD}	$V_{IN} = V_{SS}$, CMOS buffers	1,2,3	All	-5	5	µA
High level input current (w/o pull-up or pull-down resistor)	I_{IH}	$V_{IN} = V_{DD}$, CMOS buffers	1,2,3	All	-1	1	µA
High level input current Pull-up resistor PRU1	I_{IHPU}	$V_{IN} = V_{DD}$, CMOS buffers	1,2,3	All	-5	5	µA
High level input current Pull-down resistor PRD1 3/	I_{IHPD}	$V_{IN} = V_{DD}$, CMOS buffers	1,2,3	All	70	540	µA
High impedance state output current	I_{OZ}	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD}$ max, All buffers	1,2,3	All	-1	1	µA
Low level input voltage	V_{IL}	CMOS buffers	1,2,3	All		0.3 V_{DD}	V
High level input voltage	V_{IH}	CMOS buffers	1,2,3	All	0.7 V_{DD}		V
Input leakage current cold sparing	I_{ICS}	$V_{DD} = V_{SS} = 0\ V$, $V_{IN} = 0$ to V_{DD} max, PICZ buffers	1,2,3	All	-2	2	µA
Output leakage current cold sparing	I_{OCS}	$V_{DD} = V_{SS} = 0\ V$, $V_{OUT} = 0$ to V_{DD} max, PO11Z buffers	1,2,3	All	-2	2	µA
Output low voltage 4/	V_{OL}	$I_{OL} = 0.8\ mA$, $V_{DD} = V_{DD}$ min, PO11 buffers	1,2,3	All		0.4	V
Output high voltage 5/	V_{OH}	$I_{OH} = -0.6\ mA$, $V_{DD} = V_{DD}$ min, PO11 buffers	1,2,3	All	2.0		V
Output short circuit current 6/	I_{OSN}	PO11 output at low level shortened to V_{DD}	1,2,3	All		15	mA
Output short circuit current 6/	I_{OSP}	PO11 output at high level shortened to V_{SS}	1,2,3	All		8	mA
Input capacitance 6/	C_{IN}		4	All		2.4	pF
Output capacitance 6/	C_{OUT}		4	All		5.6	pF
I/O capacitance 6/	$C_{I/O}$		4	All		6.6	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le 125°C$ $2.7\ V \le V_{DD} \le 3.3\ V$ unless otherwise specified for device operate at V_{DD} = 3.0 V	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Low level input current (w/o pull-up or pull-down resistor)	I_{IL}	$V_{IN} = V_{SS}$, CMOS buffers	1,2,3	All	-1	1	µA
Low level input current Pull-up resistor PRU1 2/	I_{ILPU}	$V_{IN} = V_{SS}$, CMOS buffers	1,2,3	All	108	330	µA
Low level input current Pull-down resistor PRD1	I_{ILPD}	$V_{IN} = V_{SS}$, CMOS buffers	1,2,3	All	-5	5	µA
High level input current (w/o pull-up or pull-down resistor)	I_{IH}	$V_{IN} = V_{DD}$, CMOS buffers	1,2,3	All	-1	1	µA
High level input current Pull-up resistor PRU1	I_{IHPU}	$V_{IN} = V_{DD}$, CMOS buffers	1,2,3	All	-5	5	µA
High level input current Pull-down resistor PRD1 3/	I_{IHPD}	$V_{IN} = V_{DD}$, CMOS buffers	1,2,3	All	108	825	µA
High impedance state output current	I_{OZ}	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD}$ max, All buffers, no pull resistor	1,2,3	All	-1	1	µA
Low level input voltage	V_{IL}	CMOS buffers	1,2,3	All		0.8	V
High level input voltage	V_{IH}	CMOS buffers	1,2,3	All	2.0		V
Input leakage current cold sparing	I_{ICS}	$V_{DD} = V_{SS} = 0$ V, $V_{IN} = 0$ to V_{DD} max, PICZ buffers	1,2,3	All	-2	2	µA
Output leakage current cold sparing	I_{OCS}	$V_{DD} = V_{SS} = 0$ V, $V_{OUT} = 0$ to V_{DD} max, PO11Z buffers	1,2,3	All	-2	2	µA
Output low voltage 4/	V_{OL}	I_{OL} = 1 mA, $V_{DD} = V_{DD}$ min, PO11 buffers	1,2,3	All		0.4	V
Output high voltage 5/	V_{OH}	I_{OH} = -0.8 mA, $V_{DD} = V_{DD}$ min, PO11 buffers	1,2,3	All	2.4		V
Output short circuit current 6/	I_{OSN}	PO11 output at low level shortened to V_{DD}	1,2,3	All		21	mA
Output short circuit current 6/	I_{OSP}	PO11 output at high level shortened to V_{SS}	1,2,3	All		12	mA
Input capacitance 6/	C_{IN}		4	All		2.4	pF
Output capacitance 6/	C_{OUT}		4	All		5.6	pF
I/O capacitance 6/	$C_{I/O}$		4	All		6.6	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le 125°C$ $3.0\ V \le V_{DD} \le 3.6\ V$ unless otherwise specified for device operate at $V_{DD} = 3.3\ V$	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Low level input current (w/o pull-up or pull-down resistor)	I_{IL}	$V_{IN} = V_{SS}$, CMOS buffers	1,2,3	All	-1	1	µA
Low level input current Pull-up resistor PRU1 2/	I_{ILPU}	$V_{IN} = V_{SS}$, CMOS buffers	1,2,3	All	120	400	µA
Low level input current Pull-down resistor PRD1	I_{ILPD}	$V_{IN} = V_{SS}$, CMOS buffers	1,2,3	All	-5	5	µA
High level input current (w/o pull-up or pull-down resistor)	I_{IH}	$V_{IN} = V_{DD}$, CMOS buffers	1,2,3	All	-1	1	µA
High level input current Pull-up resistor PRU1	I_{IHPU}	$V_{IN} = V_{DD}$, CMOS buffers	1,2,3	All	-5	5	µA
High level input current Pull-down resistor PRD1 3/	I_{IHPD}	$V_{IN} = V_{DD}$, CMOS buffers	1,2,3	All	150	900	µA
High impedance state output current	I_{OZ}	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD}$ max, All buffers	1,2,3	All	-1	1	µA
Low level input voltage	V_{IL}	CMOS buffers	1,2,3	All		0.8	V
High level input voltage	V_{IH}	CMOS buffers	1,2,3	All	2.0		V
Input leakage current cold sparing	I_{ICS}	$V_{DD} = V_{SS} = 0\ V$, $V_{IN} = 0$ to V_{DD} max, PICZ buffers	1,2,3	All	-2	2	µA
Output leakage current cold sparing	I_{OCS}	$V_{DD} = V_{SS} = 0\ V$, $V_{OUT} = 0$ to V_{DD} max, PO11Z buffers	1,2,3	All	-2	2	µA
Output low voltage 4/	V_{OL}	$I_{OL} = 2\ mA$, $V_{DD} = V_{DD}$ min, PO11 buffers	1,2,3	All		0.4	V
Output high voltage 5/	V_{OH}	$I_{OH} = -1.8\ mA$, $V_{DD} = V_{DD}$ min, PO11 buffers	1,2,3	All	2.4		V
Output short circuit current 6/	I_{OSN}	PO11 output at low level shortened to V_{DD}	1,2,3	All		23	mA
Output short circuit current 6/	I_{OSP}	PO11 output at high level shortened to V_{SS}	1,2,3	All		13	mA
Input capacitance 6/	C_{IN}		4	All		2.4	pF
Output capacitance 6/	C_{OUT}		4	All		5.6	pF
I/O capacitance 6/	$C_{I/O}$		4	All		6.6	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le 125°C$ $2.3\ V \le V_{DD} \le 3.6\ V$ 7/ $4.5\ V \le V_{CC} \le 5.5\ V$ 8/ unless otherwise specified for bi-voltage operating devices	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Low level input current (w/o pull-up or pull-down resistor)	I_{IL}	$V_{IN} = V_{SS}$, CMOS buffers	1,2,3	9/	-1	1	µA
Low level input current Pull-up resistor PRU1 2/	I_{ILPU}	$V_{IN} = V_{SS}$, CMOS buffers	1,2,3	9/	180	690	µA
Low level input current Pull-down resistor PRD1	I_{ILPD}	$V_{IN} = V_{SS}$, CMOS buffers	1,2,3	9/	-5	5	µA
High level input current (w/o pull-up or pull-down resistor)	I_{IH}	$V_{IN} = V_{CC}$, $V_{DD} = V_{DD}$ max, $V_{CC} = V_{CC}$ max, CMOS buffers	1,2,3	9/	-1	1	µA
High level input current Pull-up resistor PRU1	I_{IHPU}	$V_{IN} = V_{CC}$, $V_{DD} = V_{DD}$ max, $V_{CC} = V_{CC}$ max, CMOS buffers	1,2,3	9/	-5	5	µA
High level input current Pull-down resistor PRD1 3/	I_{IHPD}	$V_{IN} = V_{CC}$, $V_{DD} = V_{DD}$ max, $V_{CC} = V_{CC}$ max, CMOS buffers	1,2,3	9/	30	400	µA
High impedance state output current	I_{OZ}	$V_{IN} = V_{CC}$ or V_{SS}, $V_{DD} = V_{DD}$ max, $V_{CC} = V_{CC}$ max, All buffers	1,2,3	9/	-1	1	µA
Low level input voltage	V_{IL}	CMOS buffers	1,2,3	9/		0.8	V
High level input voltage	V_{IH}	CMOS buffers	1,2,3	9/	2.0		V
Input leakage current cold sparing	I_{ICS}	$V_{CC} = V_{SS} = 0$ V, $V_{IN} = 0$ to V_{DD} max, PICZ buffers	1,2,3	9/	-2	2	µA
Output leakage current cold sparing	I_{OCS}	$V_{DD} = V_{SS} = 0$ V, $V_{OUT} = 0$ to V_{DD} max, PO11Z buffers	1,2,3	9/	-2	2	µA
Output low voltage 4/	V_{OL}	$V_{DD} = V_{DD}$ min, $V_{CC} = V_{CC}$ min,	1,2,3	9/		0.4	V
Output high voltage 5/	V_{OH}	$V_{DD} = V_{DD}$ min (3.0 V / 3.3 V), $V_{CC} = V_{CC}$ min	1,2,3	9/	2.4		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le 125°C$ $2.3\ V \le V_{DD} \le 3.6\ V$ 7/ $4.5\ V \le V_{CC} \le 5.5\ V$ 8/ unless otherwise specified for bi-voltage operating devices	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage 5/	V_{OH}	$V_{DD} = V_{DD}$ min (2.5 V), $V_{CC} = V_{CC}$ min	1,2,3	9/	2.0		V
Output short circuit current 6/	I_{OSN}	PO11 output at low level shortened to V_{CC}	1,2,3	9/		28	mA
Output short circuit current 6/	I_{OSP}	PO11 output at high level shortened to V_{SS}	1,2,3	9/		17	mA
Threshold trigger input voltage 6/	V_{T+}			9/	2.0		V
Threshold trigger input voltage 6/	V_{T-}			9/		0.8	V
Input capacitance 6/	C_{IN}		4	9/		2.4	pF
Output capacitance 6/	C_{OUT}		4	9/		5.6	pF
I/O capacitance 6/	$C_{I/O}$		4	9/		6.6	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Notes:

1/ Devices supplied to this drawing will meet all levels M, D, P, L and R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25 C. Post irradiation electrical parameters shall be as specified in the AID.

2/ Standard pull-ups: PRU# where # = [1-31] index for Ron:
Ron = # x R0 = 19 kΩ typ (12 to 30 kΩ) in 2.5 V range.
Ron = # x R0 = 15 kΩ typ (10 to 25 kΩ) in 3.0 V range.
Ron = # x R0 = 14 kΩ typ (9 to 25 kΩ) in 3.3 V range.
5 V tolerant/compliant pull-ups: PRU# where # = [1-31] index for Ron:
Ron = # x R0 = 14 kΩ typ (8 to 25kΩ) in each range.

3/ Standard pull-downs: PRD# where # = [1-31] index for Ron:
Ron = # x R0 = 11 kΩ typ (5 to 30 kΩ) in 2.5 V range.
Ron = # x R0 = 9 kΩ typ (4 to 25 kΩ) in 3.0 V range.
Ron = # x R0 = 8 kΩ typ (4 to 20 kΩ) in 3.3 V range.
5 V tolerant/compliant pull-downs: PRD# where # = [1-31] index for Ron:
Ron = # x R0 = 36 kΩ typ (17 to 80 kΩ) in 2.5 V range.
Ron = # x R0 = 23 kΩ typ (11 to 55 kΩ) in 3.0 V range.
Ron = # x R0 = 19 kΩ typ (9 to 45 kΩ) in 3.3 V range.

4/ Output buffers: PO$# where
$ = [1-12] quantity of output driving capability of p-channels.
# = [1-12] quantity of output driving capability of n-channels.
Standard buffers (including cold sparing)
IO = 1.6, 1.8, 2.0 mA measured at V_{OL} = 0.4, 0.4, 0.4 V in 2.5, 3.0, 3.3 V range respectively.
Tolerance buffers (including cold sparing)
IO = 1.0, 1.3, 1.4 mA measured at V_{OL} = 0.4, 0.4, 0.4 V in 2.5, 3.0, 3.3 V range respectively.
Compliant buffers (V_{CC} = 4.5 V)
IO = 1.1, 1.4, 1.6 mA measured at V_{OL} = 0.4, 0.4, 0.4 V in 2.5, 3.0, 3.3 V range respectively.

5/ Output buffers: PO$# where
$ = [1-12] quantity of output driving capability of p-channels.
# = [1-12] quantity of output driving capability of n-channels.
Standard buffers (including cold sparing)
IO = -1.6, -1.8, -2.0 mA measured at V_{OH} = 2.0, 2.4, 2.4 V in 2.5, 3.0, 3.3 V range respectively.
Tolerance buffers (including cold sparing)
IO = -1.0, -1.3, -1.4 mA measured at V_{OH} = 2.0, 2.4, 2.4 V in 2.5, 3.0, 3.3 V range respectively.
Compliant buffers (V_{CC} = 4.5 V)
IO = -1.1, -1.4, -1.6 mA measured at V_{OH} = 2.0, 2.4, 2.4 V in 2.5, 3.0, 3.3 V range respectively.

6/ Tested at initial design and after major process changes, otherwise guaranteed.

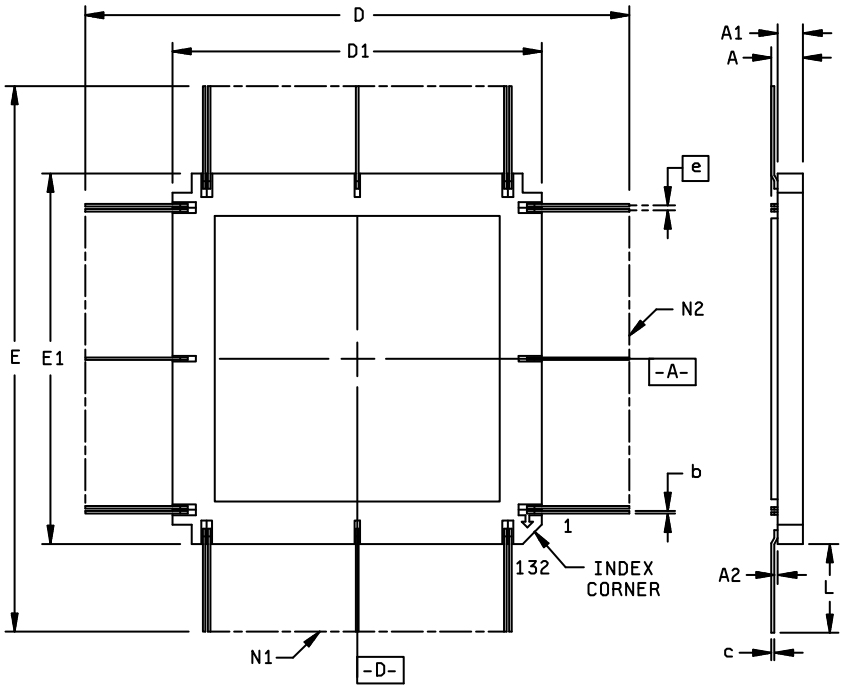
7/ 5 V tolerant buffers.

8/ 5 V compliant buffers.

9/ Device types 5-8, 13-16,21-24, 29-32.

Case X

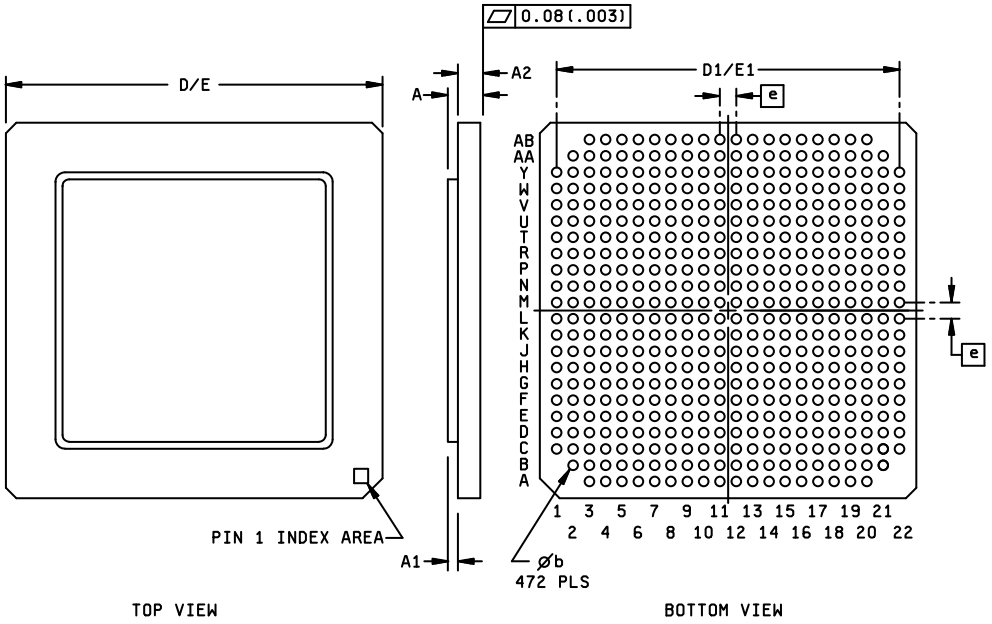
132 Leads unformed quad flat pack



	Millimeters		Inches	
	Min	Max	Min	Max
A	2.36	2.82	.093	.111
A1	1.47	1.83	.058	0.072
A2	0.203 REF		.008 REF	
b	0.200 REF		.008 REF	
C	0.152 TYP		.006 TYP	
D/E	37.00	39.38	1.457	1.550
D1/E1	24.00	24.38	.945	.960
e	0.635 BSC		.025 BSC	
L	6.50	7.50	.256	.295
N1/N2	33		33	

Figure 1a. Case outline – Continued.

Case Y

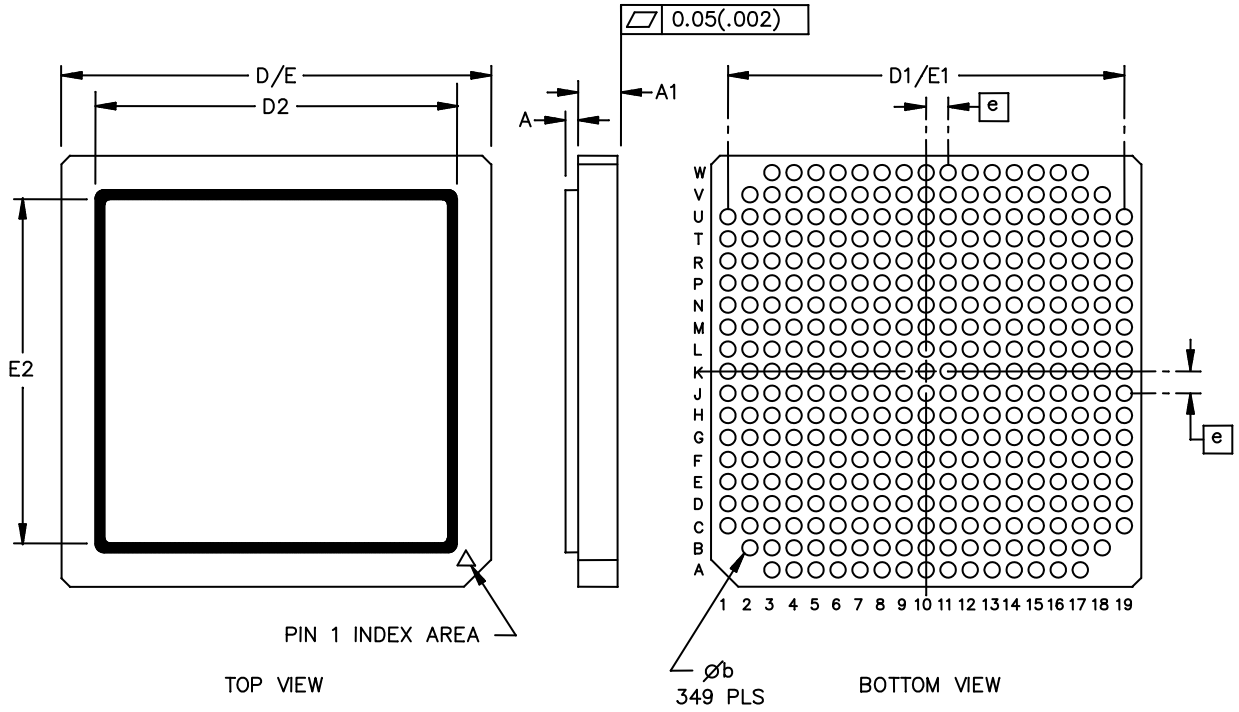


Millimeters					
Symbol	Min	Max	Symbol	Min	Max
A		3.22	D/E	28.85	29.15
A1		0.45	D1/E1	26.67 TYP	
A2	2.27	2.77	e	1.27 BSC	
b	0.81	0.91			

Note:
1. Finish plating: LGA pad: electrolytic gold 0.03 – 0.10 µm; Other pads: electrolytic gold 1.5 µm min.
2. Under plating: LGA pad: electrolytic nickel 3.2 µm min.; Other pads: electrolytic nickel 3.2 µm min.
3. Die attach pad not to be metalized. Seal ring to be electrically connected to VSS.

Figure 1b. Case outline – Continued.

Case Z



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.41	0.47	D2	20.36	20.78
A1	2.26	2.78	E2	19.74	19.90
D/E	24.85	25.15	e	1.27 BSC	
D1/E1	22.86 TYP				

Figure 1c. Case outline – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535 appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9 1/	1,2,3,7,8,9 1/	1,2,3,7,8,9 2/
Group A test requirements (see 4.4)	1,2,3,7,8,9,10,11	1,2,3,7,8,9, 10,11	1,2,3,7,8,9, 10,11
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q, and V shall be as specified in MIL-I-38535.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^oC \pm 5^oC$, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition "B" unless otherwise specified in the AID.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q will replace device class M.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-07-12

Approved sources of supply for SMD 5962-08B01 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962-08B0101QXC	F7400	TH1099ERHabcKNMQ
5962-08B0101VXC	F7400	TH1099ERHabcKNSV
5962R08B0101VXC	F7400	TH1099ERHabcKNSR
5962-08B0101QZC	F7400	TH1099ERHabc2UMQ
5962-08B0101VZC	F7400	TH1099ERHabc2USV
5962R08B0101VZC	F7400	TH1099ERHabc2USR
5962-08B0102QYC	F7400	TH1156ERHabc2VMQ
5962-08B0102VYC	F7400	TH1156ERHabc2VSV
5962R08B0102VYC	F7400	TH1156ERHabc2VSR
5962-08B0102QXC	F7400	TH1156ERHabcKNMQ
5962-08B0102VXC	F7400	TH1156ERHabcKNSV
5962R08B0102VXC	F7400	TH1156ERHabcKNSR
5962-08B0102QZC	F7400	TH1156ERHabc2UMQ
5962-08B0102VZC	F7400	TH1156ERHabc2USV
5962R08B0102VZC	F7400	TH1156ERHabc2USR
5962-08B0103QYC	F7400	TH1242ERHabc2VMQ
5962-08B0103VYC	F7400	TH1242ERHabc2VSV
5962R08B0103VYC	F7400	TH1242ERHabc2VSR
5962-08B0103QZC	F7400	TH1242ERHabc2UMQ
5962-08B0103VZC	F7400	TH1242ERHabc2USV
5962R08B0103VZC	F7400	TH1242ERHabc2USR
5962-08B0104QYC	F7400	TH1332ERHabc2VMQ
5962-08B0104VYC	F7400	TH1332ERHabc2VSV
5962R08B0104VYC	F7400	TH1332ERHabc2VSR
5962-08B0105QXC	F7400	TH1099ESHabcKNMQ
5962-08B0105VXC	F7400	TH1099ESHabcKNSV
5962R08B0105VXC	F7400	TH1099ESHabcKNSR
5962-08B0105QZC	F7400	TH1099ESHabc2UMQ
5962-08B0105VZC	F7400	TH1099ESHabc2USV
5962R08B0105VZC	F7400	TH1099ESHabc2USR
5962-08B0106QYC	F7400	TH1156ESHabc2VMQ
5962-08B0106VYC	F7400	TH1156ESHabc2VSV
5962R08B0106VYC	F7400	TH1156ESHabc2VSR

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962-08B0106QXC	F7400	TH1156ESHabcKNMQ
5962-08B0106VXC	F7400	TH1156ESHabcKNSV
5962R08B0106VXC	F7400	TH1156ESHabcKNSR
5962-08B0106QZC	F7400	TH1156ESHabc2UMQ
5962-08B0106VZC	F7400	TH1156ESHabc2USV
5962R08B0106VZC	F7400	TH1156ESHabc2USR
5962-08B0107QYC	F7400	TH1242ESHabc2VMQ
5962-08B0107VYC	F7400	TH1242ESHabc2VSV
5962R08B0107VYC	F7400	TH1242ESHabc2VSR
5962-08B0107QZC	F7400	TH1242ESHabc2UMQ
5962-08B0107VZC	F7400	TH1242ESHabc2USV
5962R08B0107VZC	F7400	TH1242ESHabc2USR
5962-08B0108QYC	F7400	TH1332ESHabc2VMQ
5962-08B0108VYC	F7400	TH1332ESHabc2VSV
5962R08B0108VYC	F7400	TH1332ESHabc2VSR
5962-08B0109QXC	F7400	TH1M099ERHabcKNMQ
5962-08B0109VXC	F7400	TH1M099ERHabcKNSV
5962R08B0109VXC	F7400	TH1M099ERHabcKNSR
5962-08B0109QZC	F7400	TH1M099ERHabc2UMQ
5962-08B0109VZC	F7400	TH1M099ERHabc2USV
5962R08B0109VZC	F7400	TH1M099ERHabc2USR
5962-08B0110QYC	F7400	TH1M156ERHabc2VMQ
5962-08B0110VYC	F7400	TH1M156ERHabc2VSV
5962R08B0110VYC	F7400	TH1M156ERHabc2VSR
5962-08B0110QXC	F7400	TH1M156ERHabcKNMQ
5962-08B0110VXC	F7400	TH1M156ERHabcKNSV
5962R08B0110VXC	F7400	TH1M156ERHabcKNSR
5962-08B0110QZC	F7400	TH1M156ERHabc2UMQ
5962-08B0110VZC	F7400	TH1M156ERHabc2USV
5962R08B0110VZC	F7400	TH1M156ERHabc2USR
5962-08B0111QYC	F7400	TH1M242ERHabc2VMQ
5962-08B0111VYC	F7400	TH1M242ERHabc2VSV
5962R08B0111VYC	F7400	TH1M242ERHabc2VSR
5962-08B0111QZC	F7400	TH1M242ERHabc2UMQ
5962-08B0111VZC	F7400	TH1M242ERHabc2USV
5962R08B0111VZC	F7400	TH1M242ERHabc2USR
5962-08B0112QYC	F7400	TH1M332ERHabc2VMQ
5962-08B0112VYC	F7400	TH1M332ERHabc2VSV
5962R08B01012VYC	F7400	TH1M332ERHabc2VSR

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962-08B0113QXC	F7400	TH1M099ESHabcKNMQ
5962-08B0113VXC	F7400	TH1M099ESHabcKNSV
5962R08B0113VXC	F7400	TH1M099ESHabcKNSR
5962-08B0113QZC	F7400	TH1M099ESHabc2UMQ
5962-08B0113VZC	F7400	TH1M099ESHabc2USV
5962R08B0113VZC	F7400	TH1M099ESHabc2USR
5962-08B0114QYC	F7400	TH1M156ESHabc2VMQ
5962-08B0114VYC	F7400	TH1M156ESHabc2VSV
5962R08B0114VYC	F7400	TH1M156ESHabc2VSR
5962-08B0114QXC	F7400	TH1M156ESHabcKNMQ
5962-08B0114VXC	F7400	TH1M156ESHabcKNSV
5962R08B0114VXC	F7400	TH1M156ESHabcKNSR
5962-08B0114QZC	F7400	TH1M156ESHabc2UMQ
5962-08B0114VZC	F7400	TH1M156ESHabc2USV
5962R08B0114VZC	F7400	TH1M156ESHabc2USR
5962-08B0115QYC	F7400	TH1M242ESHabc2VMQ
5962-08B0115VYC	F7400	TH1M242ESHabc2VSV
5962R08B0115VYC	F7400	TH1M242ESHabc2VSR
5962-08B0115QZC	F7400	TH1M242ESHabc2UMQ
5962-08B0115VZC	F7400	TH1M242ESHabc2USV
5962R08B0115VZC	F7400	TH1M242ESHabc2USR
5962-08B0116QYC	F7400	TH1M332ESHabc2VMQ
5962-08B0116VYC	F7400	TH1M332ESHabc2VSV
5962R08B0116VYC	F7400	TH1M332ESHabc2VSR
5962-08B0117QXC	F7400	TH1099RHabcKNMQ
5962-08B0117QZC	F7400	TH1099RHabc2UMQ
5962-08B0118QYC	F7400	TH1156RHabc2VMQ
5962-08B0118QXC	F7400	TH1156RHabcKNMQ
5962-08B0118QZC	F7400	TH1156RHabc2UMQ
5962-08B0119QYC	F7400	TH1242RHabc2VMQ
5962-08B0119QZC	F7400	TH1242RHabc2UMQ
5962-08B0120QYC	F7400	TH1332RHabc2VMQ
5962-08B0121QXC	F7400	TH1099SHabcKNMQ
5962-08B0121QZC	F7400	TH1099SHabc2UMQ
5962-08B0122QYC	F7400	TH1156SHabc2VMQ
5962-08B0122QXC	F7400	TH1156SHabcKNMQ
5962-08B0122QZC	F7400	TH1156SHabc2UMQ

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962-08B0123QYC	F7400	TH1242SHabc2VMQ
5962-08B0123QZC	F7400	TH1242SHabc2UMQ
5962-08B0124QYC	F7400	TH1332SHabc2VMQ
5962-08B0125QXC	F7400	TH1M099RHabcKNMQ
5962-08B0125QZC	F7400	TH1M099RHabc2UMQ
5962-08B0126QYC	F7400	TH1M156RHabc2VMQ
5962-08B0126QXC	F7400	TH1M156RHabcKNMQ
5962-08B0126QZC	F7400	TH1M156RHabc2UMQ
5962-08B0127QYC	F7400	TH1M242RHabc2VMQ
5962-08B0127QZC	F7400	TH1M242RHabc2UMQ
5962-08B0128QYC	F7400	TH1M332RHabc2VMQ
5962-08B0129QXC	F7400	TH1M099SHabcKNMQ
5962-08B0129QZC	F7400	TH1M099SHabc2UMQ
5962-08B0130QYC	F7400	TH1M156SHabc2VMQ
5962-08B0130QXC	F7400	TH1M156SHabcKNMQ
5962-08B0130QZC	F7400	TH1M156SHabc2UMQ
5962-08B0131QYC	F7400	TH1M242SHabc2VMQ
5962-08B0131QZC	F7400	TH1M242SHabc2UMQ
5962-08B0132QYC	F7400	TH1M332SHabc2VMQ

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ The “abc” is reserved to indicate the customer specific code.

Vendor CAGE number	Vendor name and address
F7400	Atmel Nantes SA. BP 70602 44306 Nantes Cedex 3 France