MC_10B12C
Block Guide
V02.03

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Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
0.7	25-SEP-2000		Hubert Bode	User specification written by Jamie Happ rev 0.5 translated to MSRS2.0 compliant format
0.8	16-OCT-2000		Hubert Bode	Changed behavior in power saving modes.
0.9	20-OCT-2000		Hubert Bode	Additional explanation for dither feature added.Recirc bit is only allowed to be changed when no PWM channel is operated in (dual) full h-bridge mode.
V02.00	18-APR-2001		Hubert Bode	formal updates, clarification on frame frequency
V02.01	24-APR-2001		Hubert Bode	changed OM[1:0] to MCOM[1:0] and AM[1:0] to MCAM[1:0]
V02.02	5-MAR-2002		Hubert Bode	changed order number
V02.03	9-MAR-2004		Harald Luepken	Translated user specification to MSRS3.1.1 compliant format. Improved wording.

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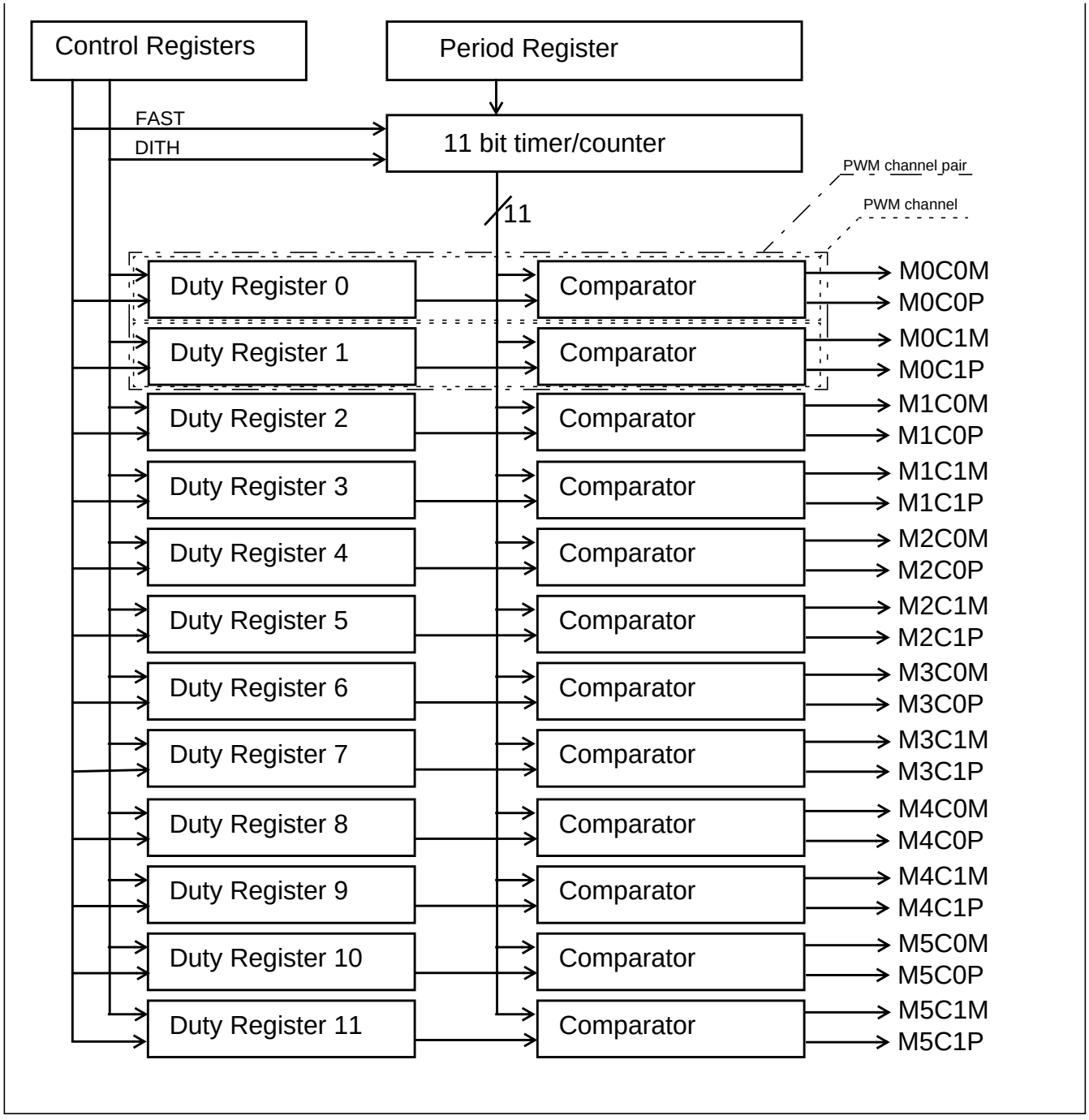
Section 1 Introduction

Figure 1-1 is a block diagram of the MC_10B12C.

Figure 1-1 MC_10B12C - Block Diagram



1.1 Overview

The block MC_10B12C is a PWM motor controller suitable to drive instruments in a cluster configuration or any other loads requiring a PWM signal{-}. The motor controller has 12 PWM channels associated with two pins each (24 pins in total).

1.2 Features

The MC_10B8CMC_10B12C includes the following features:

- 10/11-bit PWM Counter
- 11 bit resolution with selectable PWM dithering function
- 7 bit resolution mode (fast mode): duty cycle can be changed by accessing only 1 byte/output
- Left, right or center aligned PWM
- Output slew rate control
- This module is suited for, but not limited to, driving small stepper and air core motors used in instrumentation applications{-}. This module can be used for other motor control or PWM applications that match the frequency, resolution, and output drive capabilities of the module{-}.
- Control of the recirculation current of the load{vc_1,soc_1}.

1.3 Modes of Operation

1.3.1 Functional Modes

1.3.1.1 PWM Resolution

The motor controller can be configured to either 11 or 7 bits resolution mode by clearing or setting the fast bit{-}. This bit influences all PWM channels{vc_2}. For details, please refer to **4.1.3.1** {-}.

1.3.1.2 Dither Function

Dither function can be selected or deselected by setting or clearing the DITH bit{-}. This bit influences all PWM channels{vc_3}. For details, please refer to **1.3.1.2** {-}.

1.3.2 PWM Channel Configuration Modes

The 12 PWM channels can operate in 3 functional modes{vc_4,soc_4}. Those modes are, with some restrictions, selectable for each channel independently{vc_5}.

1.3.2.1 Dual Full H-bridge mode

This mode is suitable to drive a stepper motor or a 360^{o} air gauge instrument{-}. For details, please refer to **4.1.1.2** {-}. In this mode two adjacent PWM channels are combined, and two PWM channels drive 4 pins{vc_1, soc_1}.

1.3.2.2 Full H-bridge mode

This mode is suitable to drive any load requiring a PWM signal in a h-bridge configuration using 2 pins{-}. For details please refer to **4.1.1.3** {vc_1, soc_1}.

1.3.2.3 Half H-bridge mode

This mode is suitable to drive a 90^{o} instrument driven by one pin{-}. For details, please refer to **1.3.1.1** {vc_1, soc_1}.

1.3.3 PWM Alignment Modes

Each PWM channel can operate independently in three different alignment modes{vc_1, soc_1}. For details, please refer to **4.1.3.3** {-}.

1.3.4 Low Power Modes

The behavior of the motor controller in low power modes is programmable{vc_6, soc_6}. For details, please refer to **4.5** and **4.6** {-}.

Section 2 External Signal Description

2.1 Overview

The motor controller is associated with 24pins. **Table 2-1** lists the relationship between the PWM channels and signal pins as well as PWM channel pair (motor number), coils and nodes they are supposed to drive if all channels are set to dual full H-bridge configuration{vc_4,soc_4}.

Table 2-1 PWM channel and pin assignment

Pin Name	PWM Channel	PWM Channel Pair	Coil	Node
M0C0M	0	0	0	Minus
M0C0P				Plus
M0C1M	1		1	Minus
M0C1P				Plus
M1C0M	2	1	0	Minus
M1C0P				Plus
M1C1M	3		1	Minus
M1C1P				Plus
M2C0M	4	2	0	Minus
M2C0P				Plus
M2C1M	5		1	Minus
M2C1P				Plus
M3C0M	6	3	0	Minus
M3C0P				Plus
M3C1M	7		1	Minus
M3C1P				Plus
M4C0M	8	4	0	Minus
M4C0P				Plus
M4C1M	9		1	Minus
M4C1P				Plus
M5C0M	10	5	0	Minus
M5C0P				Plus
M5C1M	11		1	Minus
M5C1P				Plus

2.2 Detailed Signal Descriptions

2.2.1 M0C0M/M0C0P/M0C1M/M0C1P — PWM Output Pins for Motor 0

High current PWM output pins which can be used for motor drive{-}. These pins interface to the coils of motor 0{-}. PWM output on M0C0M results in a positive current flow through coil 0 when M0C0P is driven to a logic high state{-}. PWM output on M0C1M results in a positive current flow through coil 1 when M0C1P is driven to a logic high state{vc_1, soc_1}.

2.2.2 M1C0M/M1C0P/M1C1M/M1C1P — PWM Output Pins for Motor 1

High current PWM output pins which can be used for motor drive{-}. These pins interface to the coils of motor 1{-}. PWM output on M1C0M results in a positive current flow through coil 0 when M1C0P is driven to a logic high state{-}. PWM output on M1C1M results in a positive current flow through coil 1 when M1C1P is driven to a logic high state{-}.

2.2.3 M2C0M/M2C0P/M2C1M/M2C1P — PWM Output Pins for Motor 2

High current PWM output pins which can be used for motor drive{-}. These pins interface to the coils of motor 2{-}. PWM output on M2C0M results in a positive current flow through coil 0 when M2C0P is driven to a logic high state{-}. PWM output on M2C1M results in a positive current flow through coil 1 when M2C1P is driven to a logic high state{-}.

2.2.4 M3C0M/M3C0P/M3C1M/M3C1P — PWM Output Pins for Motor 3

High current PWM output pins which can be used for motor drive{-}. These pins interface to the coils of motor 2{-}. PWM output on M3C0M results in a positive current flow through coil 0 when M3C0P is driven to a logic high state{-}. PWM output on M3C1M results in a positive current flow through coil 1 when M3C1P is driven to a logic high state{-}.

2.2.5 M4C0M/M4C0P/M4C1M/M4C1P — PWM Output Pins for Motor 4

High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 4. PWM output on M4C0M results in a positive current flow through coil 0 when M4C0P is driven to a logic high state. PWM output on M4C1M results in a positive current flow through coil 1 when M4C1P is driven to a logic high state.

2.2.6 M5C0M/M5C0P/M5C1M/M5C1P — PWM Output Pins for Motor 5

High current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 5. PWM output on M5C0M results in a positive current flow through coil 0 when M5C0P is driven to a logic high state. PWM output on M5C1M results in a positive current flow through coil 1 when M5C1P is driven to a logic high state.

Section 3 Memory Map/Register Definition

3.1 Overview

This section provides a detailed description of all registers of the 10 bit 12 channel Motor Controller module{-}.

3.2 Module Memory Map

Table 3-2 shows the memory map of the the 10 bit 12 channel Motor Controller module.

Table 3-1 MC_10B12C - Memory Map

Address offset	Use	Access
$00	MCCTL0	RW
$01	MCCTL1	RW
$02	MCPER (high byte)	RW
$03	MCPER (low byte)	RW
$04	Reserved	-
$05	Reserved	-
$06	Reserved	-
$07	Reserved	-
$08	Reserved	-
$09	Reserved	-
$0A	Reserved	-
$0B	Reserved	-
$0C	Reserved	-
$0D	Reserved	-
$0E	Reserved	-
$0F	Reserved	-
$10	MCCC0	RW
$11	MCCC1	RW
$12	MCCC2	RW
$13	MCCC3	RW
$14	MCCC4	RW
$15	MCCC5	RW
$16	MCCC6	RW
$17	MCCC7	RW
$18	MCCC8	RW
$19	MCCC9	RW
$1A	MCCC10	RW
$1B	MCCC11	RW
$1C	Reserved	-
$1D	Reserved	-

Table 3-1 MC_10B12C - Memory Map

$1E	Reserved	-
$1F	Reserved	-
$20	MCDC0 (high byte)	RW
$21	MCDC0 (low byte)	RW
$22	MCDC1 (high byte)	RW
$23	MCDC1 (low byte)	RW
$24	MCDC2 (high byte)	RW
$25	MCDC2 (low byte)	RW
$26	MCDC3 (high byte)	RW
$27	MCDC3 (low byte)	RW
$28	MCDC4 (high byte)	RW
$29	MCDC4 (low byte)	RW
$2A	MCDC5 (high byte)	RW
$2B	MCDC5 (low byte)	RW
$2C	MCDC6 (high byte)	RW
$2D	MCDC6 (low byte)	RW
$2E	MCDC7 (high byte)	RW
$2F	MCDC7 (low byte)	RW
$30	MCDC8 (high byte)	RW
$31	MCDC8 (low byte)	RW
$32	MCDC9 (high byte)	RW
$33	MCDC9 (low byte)	RW
$34	MCDC10 (high byte)	RW
$35	MCDC10 (low byte)	RW
$36	MCDC11 (high byte)	RW
$37	MCDC11 (low byte)	RW
$38	Reserved	-
$39	Reserved	-
$3A	Reserved	-
$3B	Reserved	-
$3C	Reserved	-
$3D	Reserved	-
$3E	Reserved	-
$3F	Reserved	-

3.3 Register Descriptions {vc_7}

3.3.1 Motor Controller Control Register 0

This register controls the operating mode of the motor controller module{-}.

Register address offset $00

	7	6	5	4	3	2	1	0
R	0	MCPRE1	MCPRE0	MCSWAI	FAST	DITH	0	MCTOIF
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-1 Motor Controller Control Register 0 (MCCTL0)

MCPRE1, MCPRE0 — Motor Controller Prescaler Select

MCPRE1 and MCPRE0 determine the prescaler value which sets the Motor Controller Timer Counter clock frequency (f_{TC}){vc_8}. The clock source for the prescaler is the peripheral bus clock (f_{BUS}) as shown in **Figure 4-14**{-}. Writes to MCPRE1 or MCPRE0 will not affect the Timer Counter clock frequency f_{TC} until the start of the next PWM period{vc_9}. **Table 3-3** shows the prescaler values that result from the possible combinations of MCPRE1 and MCPRE0{vc_8}.

Table 3-3 Prescaler Values

MCPRE[1:0]	f_{TC}
00	f_{BUS}
01	$f_{BUS}/2$
10	$f_{BUS}/4$
11	$f_{BUS}/8$

MCSWAI — Motor Controller Module Stop in WAIT Mode

1 = Entering WAIT mode will stop the clock of the module and debias the analog circuitry{vc_10}. The module will release the pins{vc_10}.

0 = Entering WAIT mode has no effect on the Motor Controller module and the associated port pins maintain the functionality they had prior to entering WAIT mode both during WAIT mode and after exiting WAIT mode{vc_10}.

FAST — Motor Controller PWM resolution mode

1 = PWM operates in 7 bit resolution (fast) mode, duty cycle registers of all channels are switched to byte mode{vc_2}.

0 = PWM operates in 11 bit resolution mode, duty cycle registers of all channels are switched to word mode{vc_2}.

DITH — Motor Control/Driver dither feature enable (refer to **4.1.3.5**)

1 = Dither feature is enabled{vc_3}.

0 = Dither feature is disabled{vc_3}.

MCTOIF — Motor Controller Timer Counter Overflow Interrupt Flag

This bit is set when a Motor Controller Timer Counter overflow occurs{vc_11}. The bit is cleared by writing a ‘1’ to the bit{vc_11,soc_11}.

This bit can not be set by a write access{vc_12}. The bit is set if a Motor Controller Timer Counter overflow occurs and a ‘1’ is written at the same time{vc_12}. The bit can only be cleared if no overflow occurs at the same time{vc_12}.

1 = A Motor Controller Timer Counter overflow has occurred{vc_11}.
0 = A Motor Controller Timer Counter overflow has not occurred since the last reset or since the bit was cleared{vc_11}.

3.3.2 Motor Controller Control Register 1

This register controls the behavior of the analogue section of the Motor Controller as well as the interrupt enables{-}.

Register address offset $01

	7	6	5	4	3	2	1	0
R	RECIRC	0	0	0	0	0	0	MCTOIE
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-2 Motor Controller Control Register 1 (MCCTL1)

RECIRC — Recirculation in (Dual) Full H-bridge mode (Refer to **4.1.3.3**)
0 = Recirculation on the high side transistors{vc_1,soc_1}. Active state for PWM output is logic low, the static channel will output logic high{vc_1,soc_1}.
1 = Recirculation on the low side transistors{vc_1,soc_1}. Active state for PWM output is logic high, the static channel will output logic low{vc_1,soc_1}.

RECIRC only affects the outputs in (Dual) Full H-bridge modes{vc_1,soc_1}. In Half H-bridge mode, the PWM output is always active low{vc_1,soc_1}. RECIRC = 1 will also invert the effect of the S bits (refer to **4.1.3.2**) in (Dual) Full H-bridge modes{vc_1,soc_1}. RECIRC should only be changed when no PWM channel is operating in (Dual) Full H-bridge mode, otherwise erroneous output pattern may occur{vc_1,soc_1}.

MCTOIE — Motor Controller Timer Counter Overflow Interrupt Enable
1 = Interrupt enabled{-}. An interrupt will be generated when the Motor Controller Timer Counter Overflow Interrupt Flag (MCTOIF) is set{vc_11, soc_11}.
0 = Interrupt disabled{vc_11, soc_11}.

3.3.3 Motor Controller Period Register

The Period Register defines PER, the number of Motor Controller timer counter clocks a PWM period lasts{-}. The Motor Controller timer counter is clocked with the frequency f_{TC}{-}. If dither mode is enabled (DITH = 1, refer to **4.1.3.5**), P0 is ignored and reads as a 0{vc_13}. In this case PER = 2* D[10:1]{vc_3}.

Register address offset $02, $03

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-3 Motor Controller Period Register (MCPER) with DITH = 0

Register address offset $02, $03

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-4 Motor Controller Period Register (MCPER) with DITH = 1

Bit 0 can be set to every value with DITH = 1 but read accesses will always read a ‘0’{vc_13}.

For example programming MCPER to $0022 (PER = 34 decimal) will result in 34 counts for each complete PWM period{vc_14}. Setting MCPER to 0 will shut off all PWM channels as if MCAM[1:0] is set to 0 in all Channel Control registers{-} after the next Period Timer Counter Overflow. In this case, the motor controller releases all pins{vc_15,soc_15}.

This means that the port enable pins (which drive the OBE pins of the motor controller pads) are set to ‘0’ when the next period counter overflow occurs whereas the internal pwm outputs (which drive the DO pins of the motor controller pads) keep their current values{vc_15,soc_15}. The motor controller runs through an initialization phase if the period register is set to a value not equal to 0{vc_15,soc_15}. The value of the pwm outputs will switch to the correct value at the first (internally forced) Timer Counter Overflow{vc_15,soc_15}.

If the motor controller is set to a value not equal zero by a write access and gets cleared by an immediate subsequent write access (next ips clock) one single PWM period will be generated. The motor controller will shut off all PWM channels at the next PWM Timer Counter overlfow if the period register stays cleared.

3.3.4 Motor Controller Channel Control Registers

Each PWM channel has one associated control register to control output delay, PWM alignment and output mode{-}. The registers are named MCCC0 .. MCCC11. In the following, MCCC0 is described as a reference for all 12 registers.

Register address offset $10 .. $1B

	7	6	5	4	3	2	1	0
R	MCOM1	MCOM0	MCAM1	MCAM0	0	0	CD1	CD0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-5 Motor Controller Control Register Channel0 .. 11 (MCCC0 .. MCCC11)

CD1, CD0 — PWM Channel Delay

Each PWM channel can be individually delayed by a programmable number of PWM timer counter clocks{vc_16}. The delay will be n/f_{TC}{vc_16}.

Table 3-4 Channel Delay

CD[1:0]	n [# of PWM clks]
00	0
01	1
10	2
11	3

MCOM1, MCOM0 — Output Mode

MCOM1, MCOM0 control the PWM channel's output mode{vc_1,soc_1}.

Table 3-5 Output Mode

MCOM[1:0]	Output Mode
00	Half H-bridge mode, PWM on MnCxM, MnCxP is released
01	Half H-bridge mode, PWM on MnCxP, MnCxM is released
10	Full H-bridge mode
11	Dual Full H-bridge mode

MCAM1, MCAM0 — PWM Channel Alignment Mode

MCAM1, MCAM0 control the PWM channel's PWM alignment mode and operation{vc_1,soc_1}.

Table 3-6 PWM Alignment Mode

MCAM[1:0]	PWM Alignment Mode
00	Channel disabled

Table 3-6 PWM Alignment Mode

MCAM[1:0]	PWM Alignment Mode
01	left aligned
10	right aligned
11	center aligned

MCAM[1:0] and MCOM[1:0] are double buffered{vc_17}. The values used for the generation of the output waveform will be copied to the working registers either at once (if all PWM channels are disabled or MCPER is set to 0) or if a timer counter overflow occurs{vc_17}. Reads of the register return the most recent written value, which are not necessarily the currently active values{vc_17}.

3.3.5 Motor Controller Duty Cycle Registers

Each Duty Cycle Register sets the sign and duty functionality for the respective PWM Channel{-}.

The contents of the Duty Cycle Registers define DUTY, the number of Motor controller timer counter clocks the corresponding output is driven low (RECIRC = 0) or is driven high (RECIRC = 1){vc_1, soc_1}. Setting all bits to 0 will give a static high output in case of RECIRC = 0, otherwise a static low output{vc_1,soc_1}. Values greater than or equal to the contents of the Period Register will generate a static low output in case of RECIRC = 0, or a static high output if RECIRC = 1{vc_18}. The layout of the Duty Cycle Registers differ dependent upon the state of the FAST bit in the Control Register 0{vc_19}.

Register address offset $20 .. $37

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	S	S	S	S	S	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-6 Motor Controller Duty Cycle Register x (MCDCx) with Fast = 0

Register address offset $20 .. $37

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	S	D8	D7	D6	D5	D4	D3	D2	0	0	0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-7 Motor Controller Duty Cycle Register x (MCDCx) with Fast = 1

Whenever FAST = 1, the bits D10, D9, D1, D0 will be set to 0 if the Duty Cycle Register is written{vc_19}.

For example setting MCDCx = $0158 with FAST = 0 gives the same output waveform as setting MCDCx = $5600 with FAST = 1 (with FAST = 1, the low byte of MCDCx needs not to be written){vc_3}.

The state of the FAST bit has only impact during write and read operations. A change of the FAST bit (set or clear) without writing a new value does not impact the internal interpretation of the duty cycle values{vc_19}.

To prevent the output from inconsistent signals, the duty cycle registers are double buffered{vc_20}. The motor controller module will use working registers to generate the output signals{vc_20}. The working registers are copied from the bus accessible registers at the following conditions:

- MCPER is set to 0 (all channels are disabled in this case)
- MCAM[1:0] of the respective channel is set to 0 (channel is disabled)
- a PWM timer counter overflow occurs when in half H-bridge or full H-bridge mode
- a PWM timer counter overflow occurs and the x of MCDCx of the last written duty cycle register was odd in dual full H-bridge mode{vc_20}.

In this way, the output of the PWM will always be either the old PWM waveform or the new PWM waveform, not some variation in between{vc_20}.

Reads of this register return the most recent value written{vc_20}. Reads do not necessarily return the value of the currently active sign, duty cycle, and dither functionality due to the double buffering scheme{vc_20}.

Section 4 Functional Description

4.1 Modes of Operation

4.1.1 PWM Output Modes

The Motor Controller is configurable between three output modes{vc_1,soc_1}. Dual Full H-bridge mode can be used to control either a stepper motor or a 360° air core instrument{-}. In this case two PWM channels are combined{-}. In Full H-Bridge mode, each PWM channel is updated independently{-}. In Half H-bridge Mode, one pin of the PWM channel can generate a PWM signal to control a 90° air core instrument (or other load requiring a PWM signal) and the other pin is unused{vc_1,soc_1}. The mode of operation for each PWM channel is determined by the corresponding MCOM[1:0] bits in Channel Control Registers{vc_1,soc_1}. After a reset occurs, each PWM channel will be disabled, the corresponding pins are released{vc_21,soc_21}.

Each PWM channel consists of two pins{-}. One output pin will generate a PWM signal{vc_1,soc_1}. The other will operate as logic high or low output depending on the state of the RECIRC bit (refer to **4.1.3.3**), when in (Dual) Full H-bridge mode, or will be released, when in Half H-bridge mode{vc_1,soc_1}. The state of the S bit in the Duty Cycle Register determines the pin where the PWM signal is driven in Full H-bridge mode{vc_1,soc_1}. When in Half H-bridge mode, the state of the released pin is determined by other modules associated with this pin{vc_1,soc_1}.

Associated with each PWM channel pair n are two PWM channels, x and x+1, where x = 2*n and n (0,1,2...5) is the PWM channel pair number{-}. Duty Cycle Register x controls the sign of the PWM signal (which pin drives the PWM signal) and the duty cycle of the PWM signal for Motor Controller Channel x{vc_1,soc_1}. The pins associated with PWM Channel x are MnC0P and MnC0M{-}. Similarly, Duty Cycle Register x+1 controls the sign of the PWM signal and the duty cycle of the PWM signal for channel x+1{vc_1,soc_1}. The pins associated with PWM Channel x+1 are MnC1P and MnC1M{-}. This is summarized in table **Table 4-1** .

Table 4-1 Corresponding Registers and Pin Names for each PWM Channel Pair

PWM Channel Pair Number	PWM Channel Control Register	Duty Cycle Register	Channel Number	Pin Names
n	MCMCx	MCDCx	PWM Channel x, x = 2·n	MnC0M
				MnC0P
	MCMCx+1	MCDCx+1	PWM Channel x+1, x = 2·n	MnC1M
				MnC1P
0	MCMC0	MCDC0	PWM Channel 0	M0C0M
				M0C0P
	MCMC1	MCDC1	PWM Channel 1	M0C1M
				M0C1P

Table 4-1 Corresponding Registers and Pin Names for each PWM Channel Pair

PWM Channel Pair Number	PWM Channel Control Register	Duty Cycle Register	Channel Number	Pin Names
1	MCMC2	MCDC2	PWM Channel 2	M1C0M M1C0P
	MCMC3	MCDC3	PWM Channel 3	M1C1M M1C1P
2	MCMC4	MCDC4	PWM Channel 4	M2C0M M2C0P
	MCMC5	MCDC5	PWM Channel 5	M2C1M M2C1P
3	MCMC6	MCDC6	PWM Channel 6	M3C0M M3C0P
	MCMC7	MCDC7	PWM Channel 7	M3C1M M3C1P
4	MCMC8	MCDC8	PWM Channel 8	M4C0M M4C0P
	MCMC9	MCDC9	PWM Channel 9	M4C1M M4C1P
5	MCMC10	MCDC10	PWM Channel 10	M5C0M M5C0P
	MCMC11	MCDC11	PWM Channel 11	M5C1M M5C1P

4.1.1.1 Startup Procedure

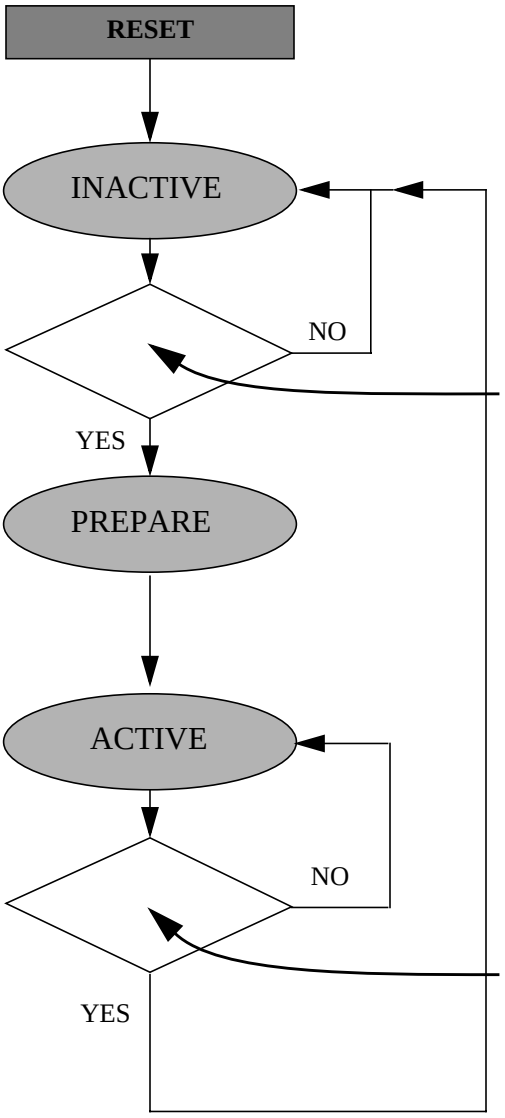
The motor controller traverses a startup procedure if

- the period register is set from zero to a value not equal zero or
- one or more PWM channel is enabled after all PWM channels have been disabled{vc_22}.

The Motor Controller Timer Counter starts to work 2 ipg clock cycles after the period register has been written and at least one channel has been enabled{vc_22}. An Motor Controller Timer Counter overflow is forced at the beginning of the first PWM period (1 ipg clock cycle after the period register or channel control register has been written) used to load all working registers{vc_22}.

The procudedure traverses three states{TBD}.

Figure 4-1 Startup Procedure - States



The motor controller is disabled{vc_22}. The pwm clock and the core clock are disabled{vc_22}. The device is waiting for a proper initialization via the pheriperal bus interface{vc_22}.

Period register not cleared and at least one PWM channel enabled?

Initialization of all buffer and working registers{vc_22}.
The core clock and the pwm clock will be enabled{vc_22}.

The motor controller is generating PWM output on at least one channel{vc_22}.

Motor Controller Timer Counter overflow and period register cleared and all channels disabled{vc_22}*?*

4.1.1.2 Dual Full H-bridge Mode (MCOM = 11)

PWM Channel pairs x and x+1 operate in Dual Full H-bridge mode when both channels have been enabled (MCAM[1:0]=01, 10 or 11) and the corresponding output mode bits MCOM[1:0] in both PWM Channel Control Registers are both set{vc_1,soc_1}.

A typical configuration in Dual Full H-bridge Mode is shown in **Figure 4-2**{-}. PWM Channel x drives the PWM output signal on either MnC0P or MnC0M{-}. If MnC0P drives the PWM signal, MnC0M will be output either high or low depending on the RECIRC bit{vc_1,soc_1}. If MnC0M drives the PWM signal, MnC0P will be an output high or low{vc_1,soc_1}. PWM Channel x+1 drives the PWM output

signal on either MnC1P or MnC1M{vc_1,soc_1}. If MnC1P drives the PWM signal, MnC1M will be an output high or low{vc_1,soc_1}. If MnC1M drives the PWM signal, MnC1P will be an output high or low{vc_1,soc_1}. This results in motor recirculation currents on the high side drivers (RECIRC = 0) when the PWM signal is at a logic high level, or motor recirculation currents on the low side drivers (RECIRC = 1) when the PWM signal is at a logic low level{vc_1,soc_1}. The pin driving the PWM signal is determined by the S (sign) bit in the corresponding Duty Cycle Register and the state of the RECIRC bit{vc_1,soc_1}. The value of the PWM duty cycle is determined by the value of the D[10:0] or D[8:2] bits respectively in the Duty Cycle Register depending on the state of the FAST bit{vc_2}.

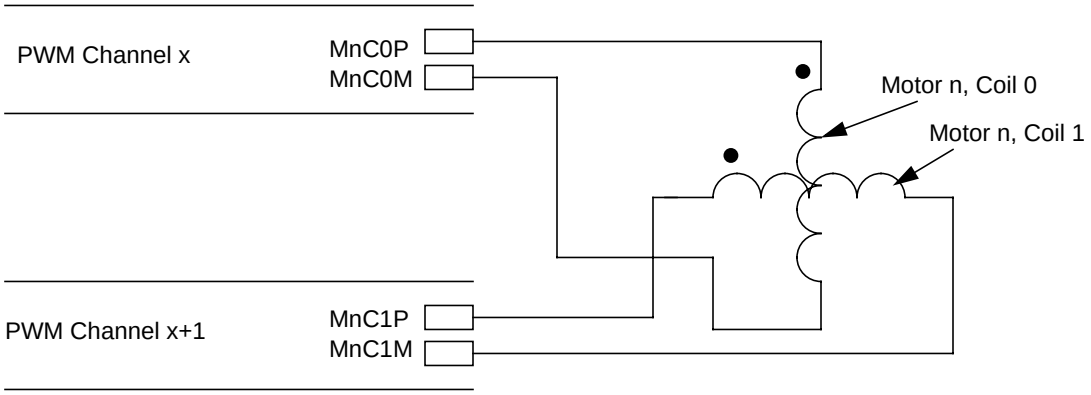


Figure 4-2 Typical Dual Full H-bridge Mode Configuration

Whenever FAST = 0 only 16-bit write accesses to the Duty Cycle Registers are allowed, 8 bit write access can lead to unpredictable duty cycles{vc_2}.

When Fast mode is enabled (FAST = 1), 8 bit write accesses to the high byte of the Duty Cycle Registers are allowed, because only the high byte of the Duty Cycle Register is used to determine the duty cycle{vc_2}.

The following sequence should be used to update the current magnitude and direction for coil 0 and coil 1 of the motor to achieve consistent PWM output:

1. Write to Duty Cycle Register x

2. Write to Duty Cycle Register x+1{-}.

At the next timer counter overflow, the duty cycle registers will be copied to the working duty cycle registers{vc_20}. Sequential writes to the Duty Cycle Register x will result in the previous data being overwritten{vc_20}.

A “pre-sneak” mechanism is applied every Motor Controller Timer Counter overflow to evaluate the content of the duty cycle register on the IP bus side for corner case handling{vc_20}. The effect is that the latest duty cycle register content is used for for the next pwm period even if the working buffers are not

loaded with the new value{vc_20}. This mechanism is disabled as long as Duty Cycle Register x+1 has not been written in Dual Full H-Bridge mode{vc_20}.

A write to Duty Cycle Register x+1 which happens at the same time as a Motor Controller Timer Counter overflow event has priority{vc_21}. The new content of the duty cycle register will be loaded in the duty cycle working register at the next Motor Controller Timer Counter overflow{vc_21}.

4.1.1.3 Full H-bridge Mode (MCOM = 10)

In Full H-Bridge Mode, the PWM Channels x and x+1 operate independently{vc_1,soc_1}. The Duty Cycle Working Registers are updated whenever a Timer Counter overflow occurs{vc_20}.

4.1.1.4 Half H-bridge Mode (MCOM = 00 or 01)

In half H-bridge Mode, the PWM channels x and x+1 operate independently{vc_1,soc_1}. In this mode, each PWM channel can be configured such that one pin is released and the other pin is a PWM output{vc_1,soc_1}. **Figure 4-3** shows a typical configuration in Half H-bridge Mode{-}.

The 2 pins associated with each channel are switchable between released mode and PWM output dependent upon the state of the MCOM[1:0] bits in the MCCCx (Channel Control) register{vc_1,soc_1}. See register description **3.3.4** {-}. In Half H-bridge mode, the state of the S bit has no effect{vc_1,soc_1}.

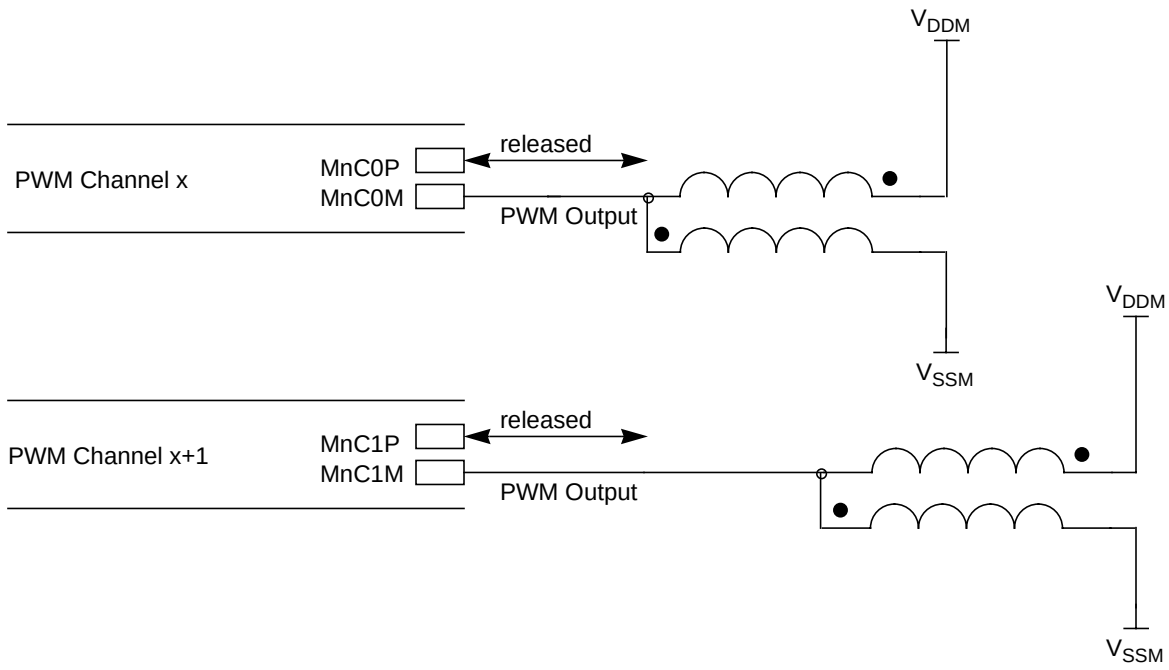


Figure 4-3 Typical Quad Half H-bridge Mode Configuration

4.1.2 Relationship Between PWM Mode and PWM Channel Enable

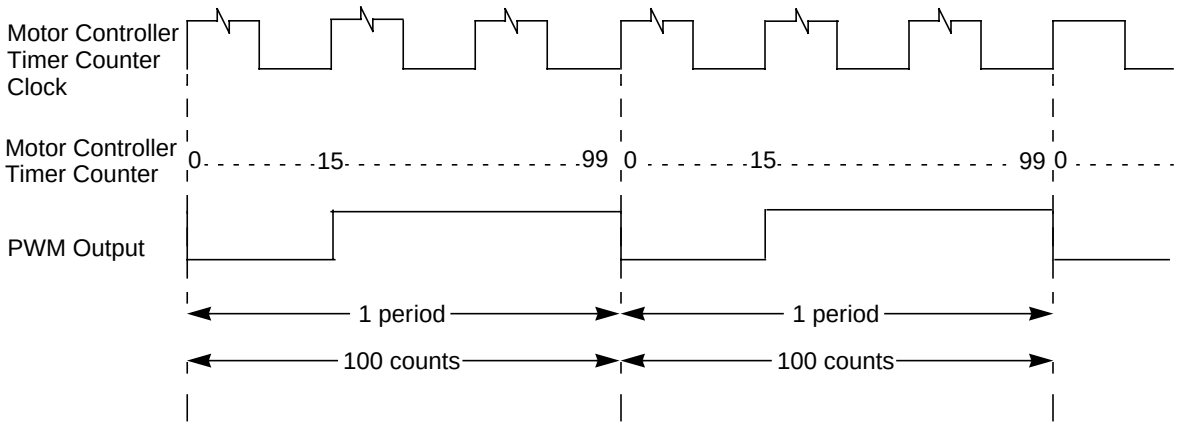
The pair of Motor Controller channels cannot be placed into Dual Full H-bridge mode unless both Motor Controller channels have been enabled (MCAM[1:0] not equal to 00) and Dual Full H-bridge mode is selected for both PWM channels (MCOM[1:0] = 11){vc_1,soc_1}. If only one channel is set to Dual Full H-bridge mode, this channel will operate in Full H-bridge mode, the other as programmed{vc_1,soc_1,vc_22}.

4.1.3 Relationship Between Sign, Duty, Dither, Recirc, Period and PWM Mode Functions

4.1.3.1 PWM Alignment Modes

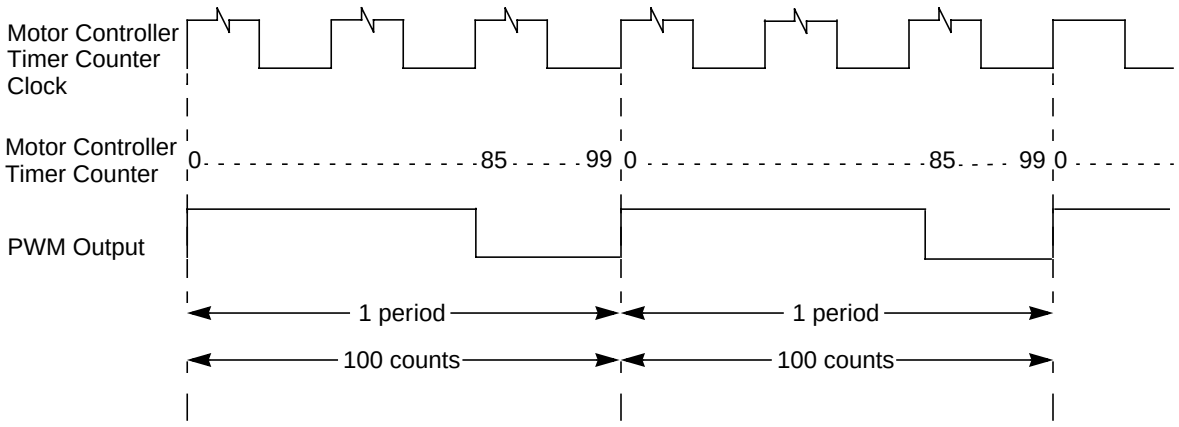
Each PWM channel can be programmed individually to three different alignment modes{-}. The mode is determined by the MCAM[1:0] bits in the corresponding Channel Control Register{-}.

Left aligned (MCAM[1:0] = 01): The output will start active (low if RECIRC = 0 or high if RECIRC = 1) and will turn inactive (high if RECIRC = 0 or low if RECIRC = 1) after the number of counts specified by the corresponding Duty Cycle Register{vc_1,soc_1}.



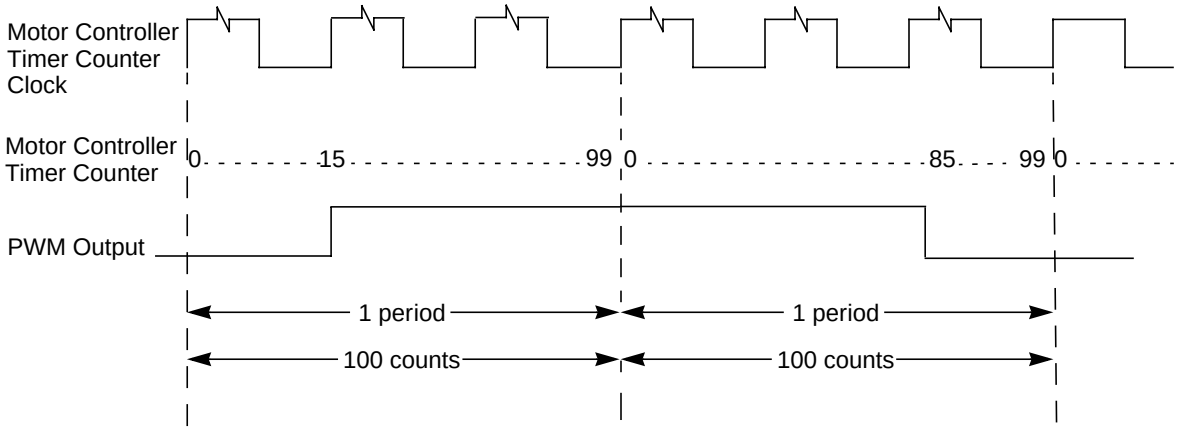
DITH = 0, MCAM[1:0] = 01, MCDCx = 15, MCPER = 100, RECIRC = 0

Right aligned (MCAM[1:0] = 10): The output will start inactive (high if RECIRC = 0 and low if RECIRC = 1) and will turn active after the number of counts specified by the difference of the contents of Period Register and the corresponding Duty Cycle Register{vc_1,soc_1}.



DITH = 0, MCAM[1:0] = 10, MCDCx = 15, MCPER = 100, RECIRC = 0

Center aligned (MCAM[1:0] = 11): Even periods will be output left aligned, odd periods will be output right aligned{vc_1,soc_1}. PWM operation starts with the even period{vc_1,soc_1} after the channel has been enabled. PWM operation might start with the odd period if the channel has not been disabled before changing the alignment mode to center aligned.



DITH = 0, MCAM[1:0] = 11, MCDCx = 15, MCPER = 100, RECIRC = 0

4.1.3.2 Sign Bit (S)

Assuming RECIRC = 0 (the active state of the PWM signal is low), when the S bit for the corresponding channel is cleared, MnC0P (if the PWM channel number is even, n = 0, 1, 2...5, see **Table 4-1**) or MnC1P (if the PWM channel number is odd,n = 0, 1, 2...5, see **Table 4-1**), outputs a logic high when in (Dual) Full H-bridge mode{vc_1,soc_1}. In Half H-bridge Mode the state of the S bit has no effect{vc_1,soc_1}. The PWM output signal is generated on MnC0M (if the PWM channel number is even, n = 0, 1, 2...5, see **Table 4-1**) or MnC1M (if the PWM channel number is odd, n = 0, 1, 2...5){vc_1,soc_1}.

Assuming RECIRC = 0 (the active state of the PWM signal is low), when the S bit for the corresponding channel is set, MnC0M (if the PWM channel number is even, n = 0, 1, 2...5, see table 1-1) or MnC1M (if the PWM channel number is odd, n = 0, 1, 2...5, see **Table 4-1**), outputs a logic high when in (Dual) Full H-bridge mode{vc_1,soc_1}. In Half H-bridge Mode the state of the S bit has no effect{vc_1,soc_1}. The PWM output signal is generated on MnC0P (if the PWM channel number is even, n = 0, 1, 2...5, see **Table 4-1**) or MnC1P (if the PWM channel number is odd, n = 0, 1, 2...5){vc_1,soc_1}.

Setting RECIRC = 1 will also invert the effect of the S bit such that when S = 0, MnC0P or MnC1P will generate the PWM signal and MnC0M or MnC1M will be a static low output{vc_1,soc_1}. When S =1, MnC0M or MnC1M will generate the PWM signal and MnC0P or MnC1P will be a static low output{vc_1,soc_1}. In this case the active state of the PWM signal will be high{vc_1,soc_1}.

See **Table 4-3** for detailed information about the impact of SIGN and RECIRC bit on the PWM output.

Table 4-3 Impact of RECIRC and SIGN bit on the PWM Output

Output Mode	RECIRC	SIGN	Output M	Output P
(Dual) Full H-bridge	0	0	PWM_B[1]	1
(Dual) Full H-bridge	0	1	1	PWM_B
(Dual) Full H-bridge	1	0	0	PWM[2]
(Dual) Full H-bridge	1	1	PWM	1
H-bridge	don't care	0	PWM_B	1
H-bridge	don't care	1	1	PWM_B

NOTES:
1. PWM_B: The PWM signal is low active. E.g. The waveform starts with 0 in left aligned mode. Output M generates the PWM signal. Output P is static high.
2. PWM: The PWM signal is high active. E.g. The waveform starts with 1 in left aligned mode. Output P generates the PWM signal. Output M is static low.

4.1.3.3 RECIRC Bit

The RECIRC bit controls the flow of the recirculation current of the load{-}. Setting RECIRC = 0 will cause recirculation current to flow through the high side transistors, while RECIRC = 1 will cause the recirculation current to flow through the low side transistors{vc_1,soc_1}. The RECIRC bit is only active in (Dual) Full H-bridge modes{vc_1,soc_1}.

Effectively, RECIRC = 0 will cause a static high output on the output terminal not driven by the PWM, RECIRC = 1 will cause a static low output on the output terminals not driven by the PWM{vc_1,soc_1}. To achieve the same current direction, the S bit behavior is inverted if RECIRC = 1{vc_1,soc_1}. **Figure 4-4**, **Figure 4-5**, **Figure 4-6** and **Figure 4-7** illustrate the effect of the RECIRC bit in (Dual) Full H-bridge modes{-}.

RECIRC bit should only be changed, when no PWM channel is operated in (Dual) Full H-bridge mode{-}.

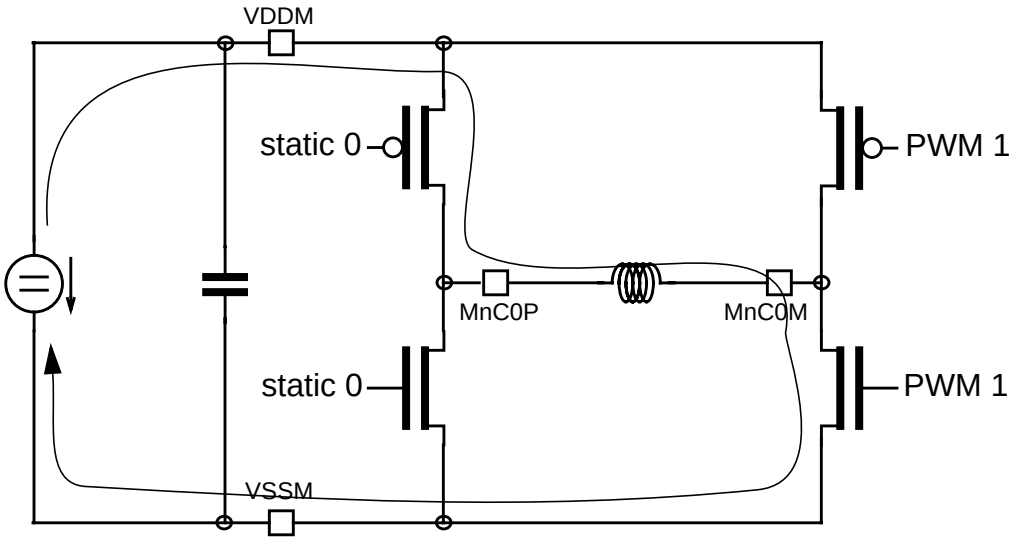


Figure 4-4 PWM active phase, RECIRC = 0, S = 0

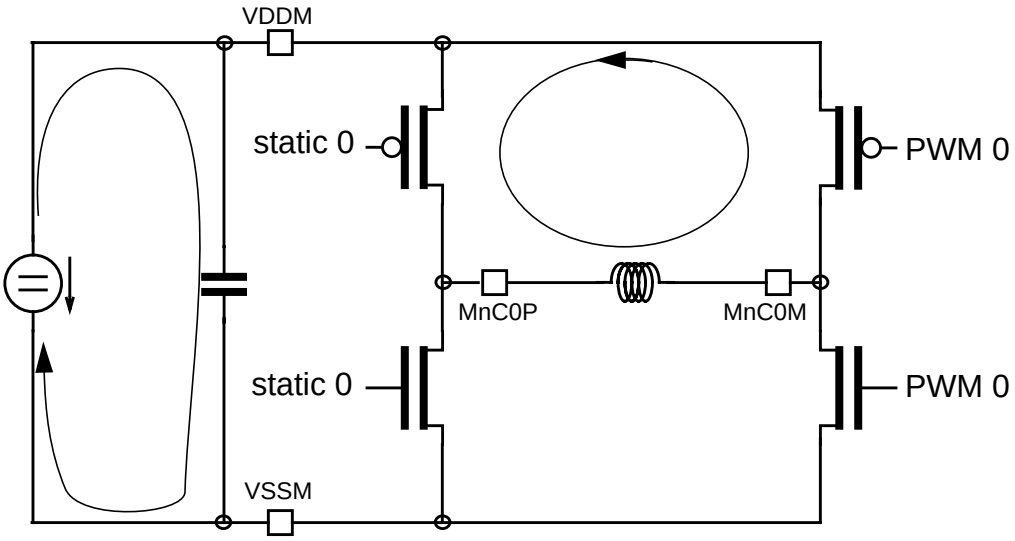


Figure 4-5 PWM passive phase, RECIRC = 0, S = 0

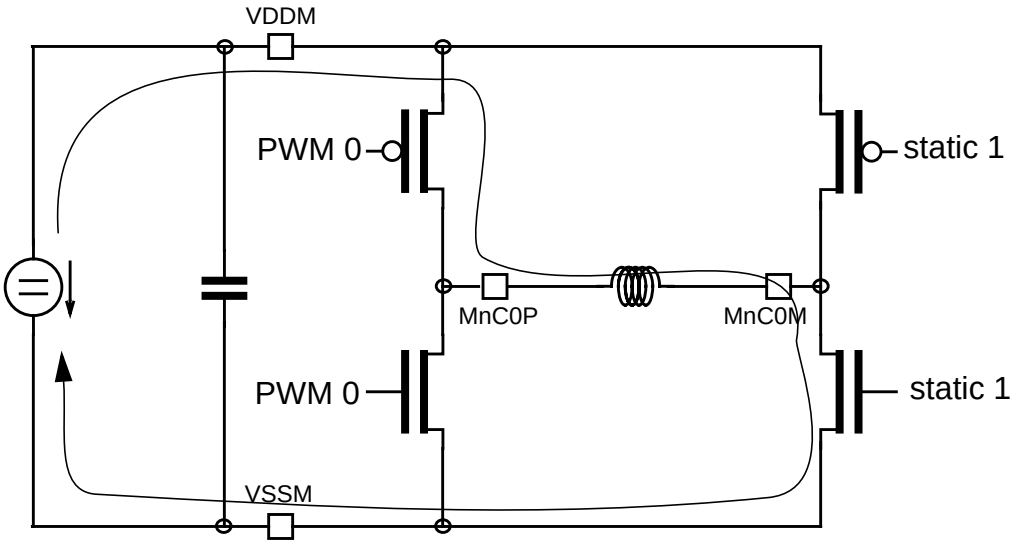


Figure 4-6 PWM active phase, RECIRC = 1, S = 0

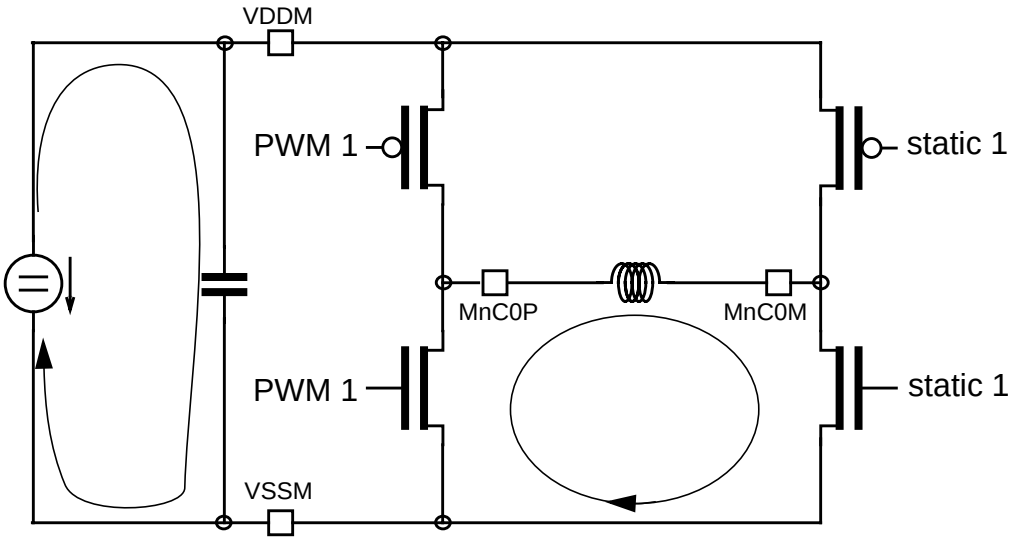


Figure 4-7 PWM passive phase, RECIRC = 1, S = 0

4.1.3.4 Relationship between RECIRC bit, S bit, MCOM bits, PWM state and output transistors

Please refer to **Figure 4-8** for the output transistor assignment:

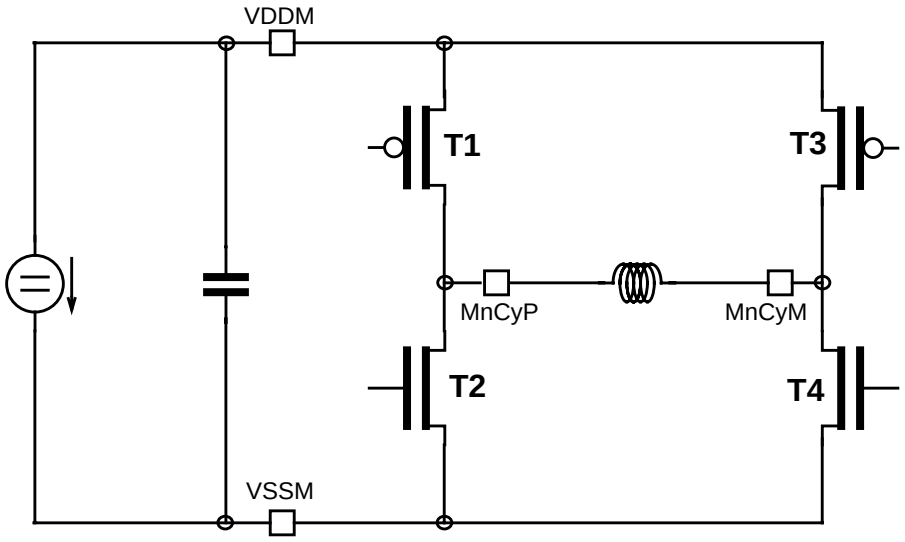


Figure 4-8 Output transistor assignment

Table 4-4 illustrates the state of the output transistors in different states of the PWM Motor Controller module{-}. '–' means that the state of the output transistor is not controlled by the Motor Controller{-}.

Table 4-4 State of output transistors in various modes {vc_1,soc_1}

Mode	MCOM[1:0]	PWM duty	RECIRC	S	T1	T2	T3	T4
off	don't care	–	don't care	don't care	–	–	–	–
Half H-bridge	00	active	don't care	don't care	–	–	OFF	ON
Half H-bridge	00	passive	don't care	don't care	–	–	ON	OFF
Half H-bridge	01	active	don't care	don't care	OFF	ON	–	–
Half H-bridge	01	passive	don't care	don't care	ON	OFF	–	–
(Dual) Full	10 or 11	active	0	0	ON	OFF	OFF	ON
(Dual) Full	10 or 11	passive	0	0	ON	OFF	ON	OFF
(Dual) Full	10 or 11	active	0	1	OFF	ON	ON	OFF

Table 4-4 State of output transistors in various modes {vc_1,soc_1}

Mode	MCOM[1:0]	PWM duty	RECIRC	S	T1	T2	T3	T4
(Dual) Full	10 or 11	passive	0	1	ON	OFF	ON	OFF
(Dual) Full	10 or 11	active	1	0	ON	OFF	OFF	ON
(Dual) Full	10 or 11	passive	1	0	OFF	ON	OFF	ON
(Dual) Full	10 or 11	active	1	1	OFF	ON	ON	OFF
(Dual) Full	10 or 11	passive	1	1	OFF	ON	OFF	ON

4.1.3.5 Dither Bit (DITH)

The purpose of the dither mode is to increase the minimum length of output pulses without decreasing the PWM resolution, in order to limit the pulse distortion introduced by the slewrate control of the outputs{-}. If dither mode is selected the output pattern will repeat after two timer counter overflows{vc_3}. For the same output frequency the shortest output pulse will have twice the length when dither feature is selected{vc_3}. In order to achieve the same output frame frequency, the prescaler of the MC_10B12C module has to be set to twice the division rate if dither mode is selected, e.g. with the same prescaler division rate the repeat rate of the output pattern is the same as well as the shortest output pulse with or without dither mode selected{vc_3}.

The DITH bit in the Control Register 0 enables or disables the dither function{vc_3}.

DITH = 0: dither function is disabled{vc_3}.

When DITH is cleared and assuming left aligned operation and RECIRC = 0, the PWM output will start at a logic low level at the beginning of the PWM period (Motor Controller Timer Counter = $000){vc_3}. The PWM output remains low until the Motor Controller Timer Counter matches the 11 bit PWM duty cycle value, DUTY, contained in D[10:0] in MCDCx{vc_3}. When a match (output compare between Motor Controller Timer Counter and DUTY) occurs, the PWM output will toggle to a logic high level and will remain at a logic high level until the Motor Controller Timer Counter overflows (reaches the contents of MCPER – 1){vc_3}. After the Motor Controller Timer Counter resets to $000, the PWM output will return to a logic low level{vc_3}. This completes one PWM period{vc_3}. The PWM period repeats every P counts (as defined by the bits P[10:0] in the Motor Controller Period Register) of the Motor Controller Timer Counter{vc_3}. If Duty >= P, the output will be static low{vc_3}. If DUTY = $000, the output will be continuously at a logic high level{vc_3}. The relationship between the Motor Controller Timer Counter clock, Motor Controller Timer Counter value, and PWM output when DITH = 0 is shown in **Figure 4-9**{-}.

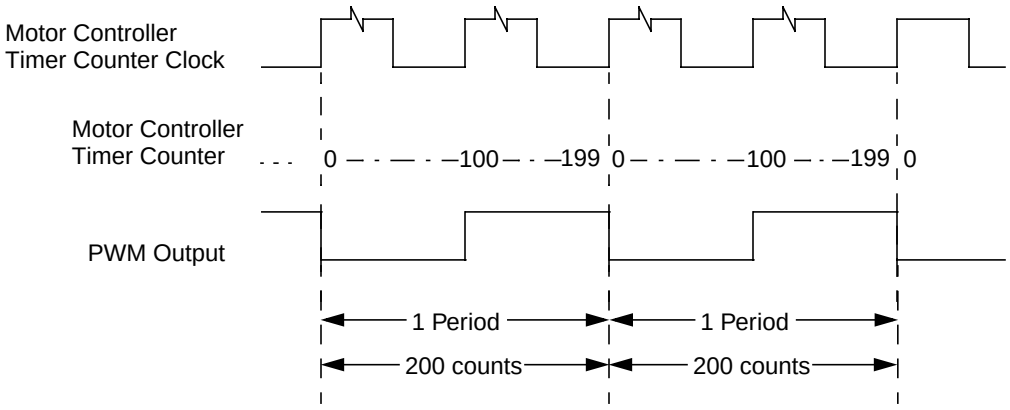


Figure 4-9 PWM Output: DITH = 0, MCAM[1:0] = 01, MCDC = 100 MCPER = 200, RECIRC = 0

DITH = 1: dither function is enabled

Please note if DITH = 1, the bit P0 in the Motor Controller Period Register will be internally forced to 0 and read back always as 0{vc_3}.

When DITH is set and assuming left aligned operation and RECIRC = 0, the PWM output will start at a logic low level at the beginning of the PWM period (when the Motor Controller Timer Counter = $000){vc_3}. The PWM output remains low until the Motor Controller Timer Counter matches the 10 bit PWM duty cycle value, DUTY, contained in D[10:1] in MCDCx{vc_3}. When a match (output compare between Motor Controller Timer Counter and DUTY) occurs, the PWM output will toggle to a logic high level and will remain at a logic high level until the Motor Controller Timer Counter overflows (reaches the value defined by P[10:1] – 1 in MCPER){vc_3}. After the Motor Controller Timer Counter resets to $000, the PWM output will return to a logic low level{vc_3}. This completes the first half of the PWM period{vc_3}. During the second half of the PWM period, the PWM output will remain at a logic low level until either the Motor Controller Timer Counter matches the 10 bit PWM duty cycle value, DUTY, contained in D[10:1] in MCDCx if D0 = 0, or the Motor Controller Timer Counter matches the 10 bit PWM duty cycle value + 1 (the value of D[10:1] in MCDCx is increment by 1 and is compared with the Motor Controller Timer Counter value) if D0 = 1 in the corresponding Duty Cycle Register{vc_3}. When a match occurs, the PWM output will toggle to a logic high level and will remain at a logic high level until the Motor Controller Timer Counter overflows (reaches the value defined by P[10:1] – 1 in MCPER){vc_3}. After the Motor Controller Timer Counter resets to $000, the PWM output will return to a logic low level{vc_3}.

This process will repeat every number of counts of the Motor Controller Timer Counter defined by the Period Register contents (P[10:0]){vc_3}. If the output is neither set to 0% nor to 100% there will be four edges on the PWM output per PWM period in this case{vc_3}. Therefore, the PWM output compare function will alternate between DUTY and DUTY + 1 every half PWM period if D0 in the corresponding Duty Cycle Register is set to 1{vc_3}. The relationship between the Motor Controller Timer Counter clock (f_{TC}), Motor Controller Timer Counter value, and left aligned PWM output when DITH = 1 is shown in **Figure 4-10** and **Figure 4-11**{-}. **Figure 4-12** and **Figure 4-13** show right aligned and center aligned PWM operation respectively, with dither feature enabled and D0 = 1{-}. Please note: In the following examples, the MCPER value is defined by the bits P[10:0], which is, when DITH = 1, always an even number{-}.

NOTE: The DITH bit should only be changed if the motor controller is disabled (all channels disabled or period register cleared) in order to avoid erroneous waveforms.

An erroneous waveform will be generated for one PWM period if DITH bit is set when the motor controller is enabled (at least one channel is generating PWM output).

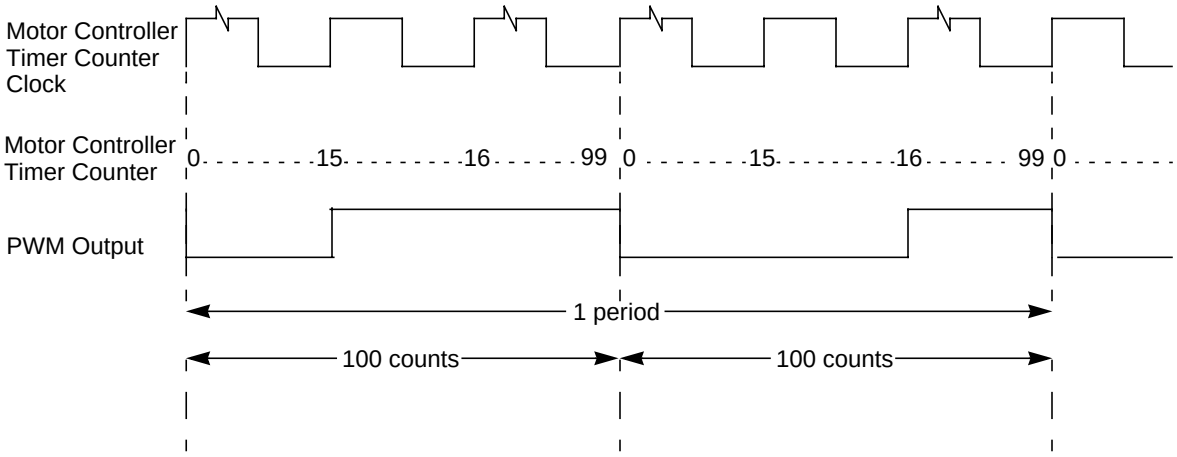


Figure 4-10 PWM Output: DITH = 1, MCAM[1:0] = 01, MCDC = 31, MCPER = 200, RECIRC = 0

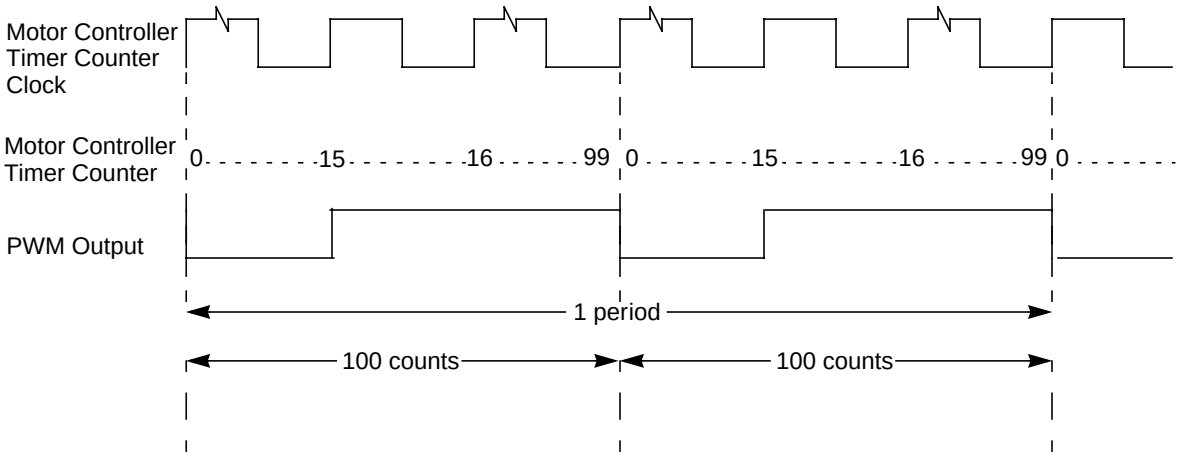


Figure 4-11 PWM Output: DITH = 1, MCAM[1:0] = 01, MCDC = 30, MCPER = 200, RECIRC = 0

A counter overflow will be generated in the middle of the period with DITH = 1{TBD}.

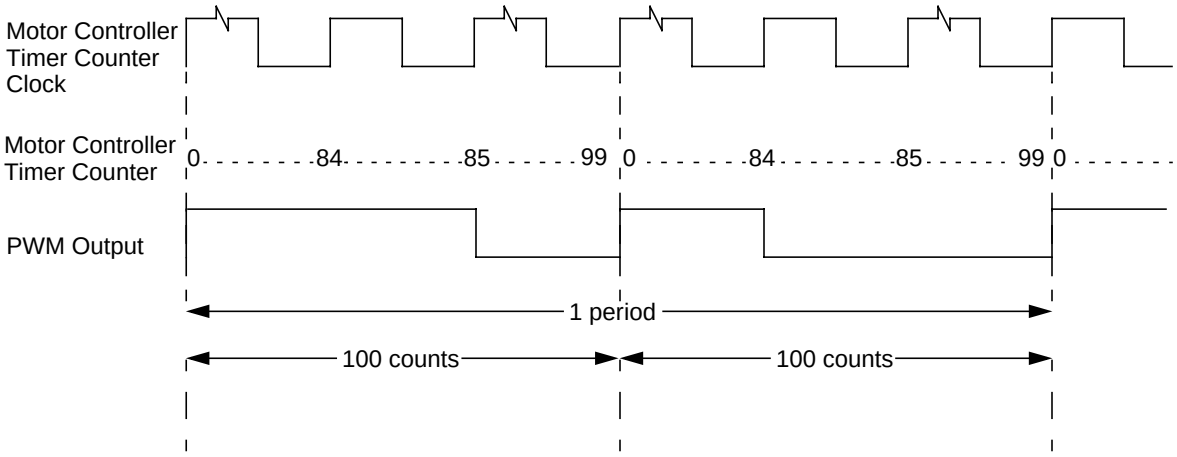


Figure 4-12 PWM Output: DITH = 1, MCAM[1:0] = 10, MCDC = 31, MCPER = 200, RECIRC = 0

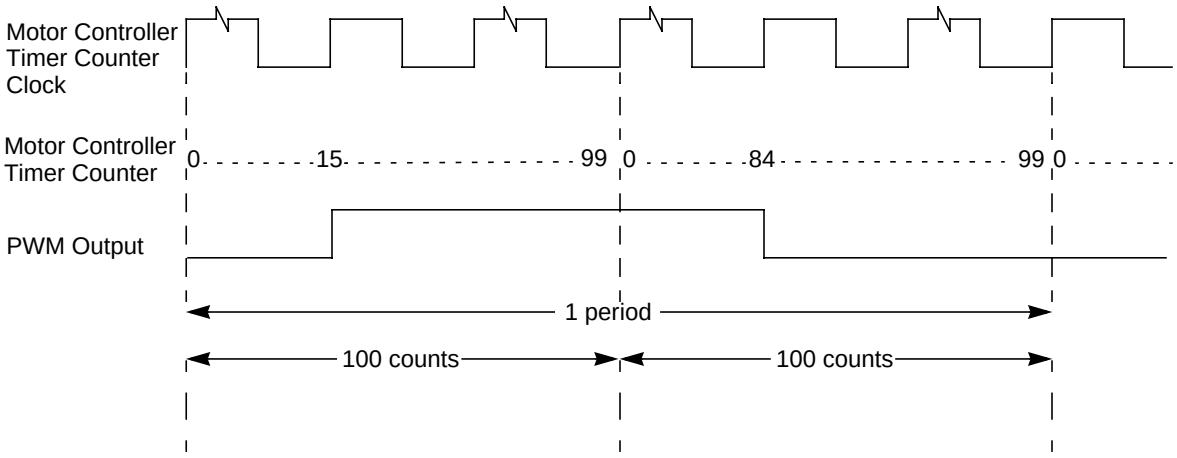


Figure 4-13 PWM Output: DITH = 1, MCAM[1:0] = 11, MCDC = 31, MCPER = 200, RECIRC = 0

4.2 PWM Duty Cycle

The PWM duty cycle for the Motor Controller Channel x can be determined by dividing the decimal representation of bits D[10:0] in MCDCx by the decimal representation of the bits P[10:0] in MCPER and multiplying the result by 100% as shown in the equation below:

$$\text{Effective PWM Channel X \% Duty Cycle} = \frac{\text{DUTY}}{\text{PER}} \cdot 100\%$$

Note: x = PWM Channel Number = 0, 1, 2, 3 ... 11. This equation is only valid if DUTY <= PER and PER is not equal to 0{vc_1}.

Whenever D[10:0] >= P[10:0], a constant low level (RECIRC = 0) or high level (RECIRC = 1) will be output{vc_18}.

4.3 Motor Controller Counter Clock Source

Figure 4-14 shows how the PWM Motor Controller Timer Counter clock source is selected{-}.

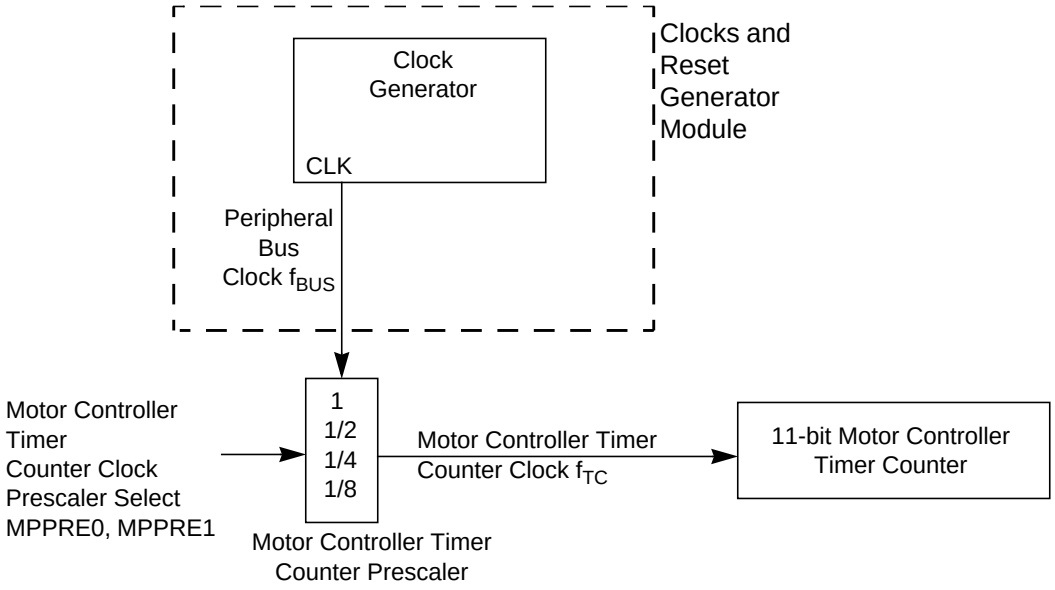


Figure 4-14 Motor Controller Counter Clock Selection

The peripheral bus clock is the source for the Motor Controller Counter Prescaler{-}. The Motor Controller Counter Clock rate f_{TC} is set by selecting the appropriate prescaler value{vc_23}. The prescaler is selected with the MCPRE[1:0] bits in Motor Controller Control Register 0 (MCCTL0){vc_23}. The Motor Controller Channel frequency of operation can be calculated using the following formula if DITH = 0:

$$\text{Motor Channel Frequency (Hz)} = \frac{\text{fTC}}{\text{PERxM}}$$

The Motor Controller Channel frequency of operation can be calculated using the following formula if DITH = 1{vc_23}:

$$\text{Motor Channel Frequency (Hz)} = \frac{fTC}{MCPERxM/2}$$

Note: Both equations are only valid if MCPER is not equal to 0{-}. M=1 for left or right aligned mode, M=2 for center aligned mode{-}.

Table 4-5 shows examples of the Motor Controller channel frequencies that can be generated based on different peripheral bus clock frequencies and the prescaler value{vc_23}.

Table 4-5 Motor Controller Channel Frequencies (Hz), MCPER = 256, DITH = 0, MCAM=10, 01

Prescaler	Peripheral Bus Clock Frequency				
	16 MHz	10 MHz	8 MHz	5 MHz	4 MHz
1	62500	39063	31250	19531	15625
1/2	31250	19531	15625	9766	7813
1/4	15625	9766	7813	4883	3906
1/8	7813	4883	3906	2441	1953

Note: Due to the selectable slewrate control of the outputs, clipping may occur on short output pulses{-}.

4.4 Output Switching Delay

In order to prevent large peak current draw from the motor power supply, selectable delays can be used to stagger the high logic level to low logic level transitions on the Motor Controller outputs{-}. The timing delay, t_d, is determined by the CD[1:0] bits in the corresponding Channel Control Register (MCMCx) and is selectable between 0, 1, 2, or 3 Motor Controller Timer Counter Clock cycles{vc_16}.

The content of the shift register used to generate the delay is cleared by the next pwm clock if the channel gets disabled{vc_16}.

4.5 Operation in WAIT Mode

During WAIT mode, the operation of the Motor Controller pins are selectable between the following two options:

1. MCSWAI = 1:All module clocks are stopped and the associated port pins are set to their inactive state, which is defined by the state of the RECIRC bit during WAIT mode{vc_6}. The Motor Controller module registers stay the same as they were prior to entering WAIT mode{vc_6}. Therefore, after exiting from WAIT mode, the associated port pins will resume to the same functionality they had prior to entering WAIT mode{vc_6}.
2. MCSWAI = 0:The PWM clocks continue to run and the associated port pins maintain the functionality they had prior to entering WAIT mode both during WAIT mode and after exiting WAIT mode{vc_6}.

4.6 Operation in STOP and Pseudo-STOP Modes

All module clocks are stopped and the associated port pins are set to their inactive state, which is defined by the state of the RECIRC bit{vc_6}. The Motor Controller module registers stay the same as they were prior to entering STOP or Pseudo-STOP modes{vc_6}. mode{vc_6}. Therefore, after exiting from STOP or Pseudo-STOP modes, the associated port pins will resume to the same functionality they had prior to entering STOP or Pseudo-STOP modes{vc_6}.

Section 5 Reset

5.1 General

The Motor Controller is reset by system reset{vc_7}. All associated ports are released, all registers of the Motor Controller module will switch to their reset state as defined in the Register Description chapter{vc_7}.

Section 6 Interrupts

6.1 General

The Motor Controller has one interrupt source{-}.

6.1.1 Timer Counter Overflow Interrupt

An interrupt will be requested when the MCTOIE bit in the Motor Controller Control Register 1 is set and the running PWM frame is finished{vc_11,soc_11}. The interrupt is cleared by either setting the MCTOIE bit to 0 or to write a 1 to the MCTOIF bit in the Motor Controller Control Register 0{vc_11,soc_11}.

Section 7 Initialization/Application Information

Provide stepwise instructions for initializing the VC{TBD}. Be as specific as possible{TBD}. Include flow charts and code examples{TBD}. This information is intended for use by the device or SoC customer, and is generally not included in functional verification{TBD}.

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