PIM_9H256
Block User Guide
V01.07

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Motorola, Inc

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
1.0	02 AUG 2000	02 AUG 2000		Initial release of User Guide in SRSv2 document format. Derived from PIM_9DP256 (Barracuda) User Guide V2.0.
1.1	19 FEB 2001	19 FEB 2001		Fixed Reset State of PERT, PPST, PERL, PPSL, PERS Modified sections which did not meet SVSv2 requirements.
1.2	22 MAR 2001	22 MAR 2001		Fixed copy and paste errors. Spec tagged!
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1.7	27 FEB 2004	27 FEB 2004		Minor corrections in **3.3.8**, **3.3.9**, and **3.3.10**

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Section 1 Introduction

1.1 Overview

The Port Integration Module establishes the interface between the peripheral modules and the I/O pins for all ports except for port AD.

This section covers:

- Ports **A**, **B**, **E**, **K**, and the **BKGD** pin, which are shared between the core logic (including the multiplexed bus interface) and the LCD driver,
- Port **T** connected to the timer module and the LCD driver,
- Port **S** which is associated with 2 SCI and 1 SPI modules,
- Port **M** associated with 2 CAN and 1 IIC modules,
- Port **P** connected to the PWM module,
- The standard I/O ports **H** and **J**, which can be used as external interrupt sources,
- Port **L** which is connected to the LCD driver,
- Ports **U**, **V** and **W** associated with the PWM Motor Controller.

The PIM_9H256 offers a set or registers to configure each I/O pin.

1.2 Features

A standard port has the following minimum features:

- Input/output selection
- 5V output drive with two selectable drive strength (or slew rates)
- 5V digital and analog input
- Input with selectable pull-up or pull-down device

Optional features:

- Open drain for wired-or connections
- Interrupt inputs with glitch filtering

1.3 Block Diagram

Figure 1-1 is a block diagram of the PIM_9H256.

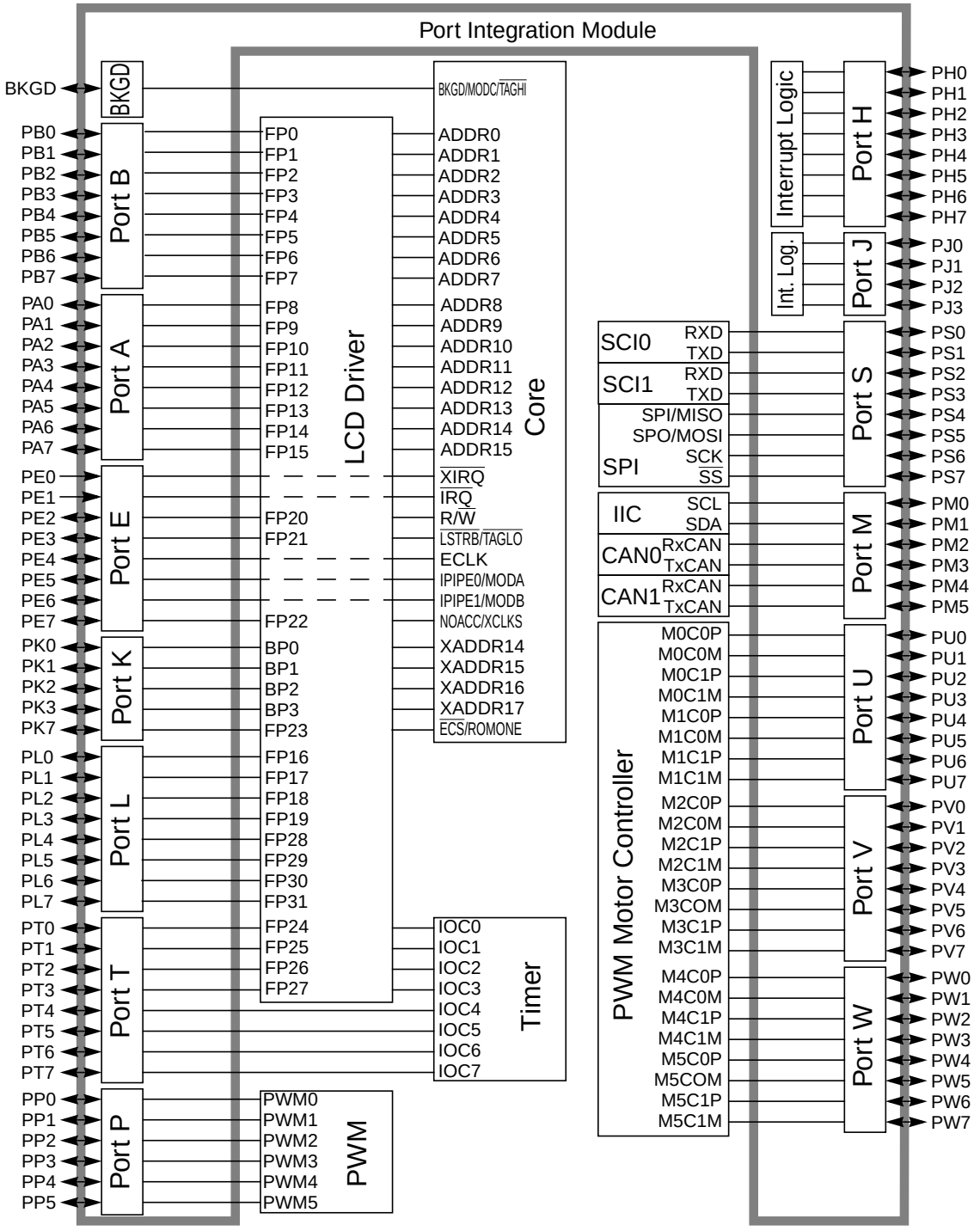

Figure 1-1 PIM_9H256 Block Diagram

Section 2 Signal Description

2.1 Overview

This section lists and describes the signals that do connect off chip.

2.2 Signal properties

Table 2-1 shows all the pins and their functions that are controlled by the PIM_9H256. The order in which the pin functions are listed represents the functions priority (top – highest priority, bottom – lowest priority).

Table 2-1 Signal Properties

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port A	PA7	FP15	LCD Driver interface	S12_mebi
		ADDR15/DATA15/GPIO	Refer to S12_mebi Block User Guide	
	PA6	FP14	LCD Driver interface	
		ADDR14/DATA14/GPIO	Refer to S12_mebi Block User Guide	
	PA5	FP13	LCD Driver interface	
		ADDR13/DATA13/GPIO	Refer to S12_mebi Block User Guide	
	PA4	FP12	LCD Driver interface	
		ADDR12/DATA12/GPIO	Refer to S12_mebi Block User Guide	
	PA3	FP11	LCD Driver interface	
		ADDR11/DATA11/GPIO	Refer to S12_mebi Block User Guide	
	PA2	FP10	LCD Driver interface	
		ADDR10/DATA10/GPIO	Refer to S12_mebi Block User Guide	
	PA1	FP9	LCD Driver interface	
		ADDR9/DATA9/GPIO	Refer to S12_mebi Block User Guide	
	PA0	FP8	LCD Driver interface	
		ADDR8/DATA8/GPIO	Refer to S12_mebi Block User Guide	

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port B	PB7	FP7	LCD Driver interface	S12_mebi
		ADDR7/DATA7/GPIO	Refer to S12_mebi Block User Guide	
	PB6	FP6	LCD Driver interface	
		ADDR6/DATA6/GPIO	Refer to S12_mebi Block User Guide	
	PB5	FP5	LCD Driver interface	
		ADDR5/DATA5/GPIO	Refer to S12_mebi Block User Guide	
	PB4	FP4	LCD Driver interface	
		ADDR4/DATA4/GPIO	Refer to S12_mebi Block User Guide	
	PB3	FP3	LCD Driver interface	
		ADDR3/DATA3/GPIO	Refer to S12_mebi Block User Guide	
	PB2	FP2	LCD Driver interface	
		ADDR2/DATA2/GPIO	Refer to S12_mebi Block User Guide	
	PB1	FP1	LCD Driver interface	
		ADDR1/DATA1/GPIO	Refer to S12_mebi Block User Guide	
	PB0	FP0	LCD Driver interface	
		ADDR0/DATA0/GPIO	Refer to S12_mebi Block User Guide	
Port E	PE7	FP22	LCD Driver interface	S12_mebi
		NOACC/XCLKS/GPIO	Refer to S12_mebi Block User Guide	
	PE6	IPIPE1/MODB/GPIO	Refer to S12_mebi Block User Guide	
	PE5	IPIPE0/MODA/GPIO	Refer to S12_mebi Block User Guide	
	PE4	ECLK/GPIO	Refer to S12_mebi Block User Guide	
	PE3	FP21	LCD Driver interface	
		$\overline{\text{LSTRB}}$/$\overline{\text{TAGLO}}$/GPIO	Refer to S12_mebi Block User Guide	
	PE2	FP20	LCD Driver interface	
		R/$\overline{\text{W}}$/GPIO	Refer to S12_mebi Block User Guide	
	PE1	$\overline{\text{IRQ}}$/GPI	Refer to S12_mebi Block User Guide	
	PE0	$\overline{\text{XIRQ}}$/GPI	Refer to S12_mebi Block User Guide	
Port K	PK7	FP23	LCD Driver interface	S12_mebi
		$\overline{\text{ECS}}$/ROMONE/GPIO	Refer to S12_mebi Block User Guide	
	PK3	BP3	LCD Driver interface	
		XADDR17/GPIO	Refer to S12_mebi Block User Guide	
	PK2	BP2	LCD Driver interface	
		XADDR16/GPIO	Refer to S12_mebi Block User Guide	
	PK1	BP1	LCD Driver interface	
		XADDR15/GPIO	Refer to S12_mebi Block User Guide	
	PK0	BP0	LCD Driver interface	
		XADDR14/GPIO	Refer to S12_mebi Block User Guide	
-	BKGD	BKGD/MODC/$\overline{\text{TAGHI}}$	Refer to S12_mebi Block User Guide and S12_bdm Block User Guide	S12_mebi

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port T	PT7	IOC7	Timer Channel 7	GPIO
		GPIO	General-purpose I/O	
	PT6	IOC6	Timer Channel 6	
		GPIO	General-purpose I/O	
	PT5	IOC5	Timer Channel 5	
		GPIO	General-purpose I/O	
	PT4	IOC4	Timer Channel 4	
		GPIO	General-purpose I/O	
	PT3	FP27	LCD Driver interface	
		IOC3	Timer Channel 3	
		GPIO	General-purpose I/O	
	PT2	FP26	LCD Driver interface	
		IOC2	Timer Channel 2	
		GPIO	General-purpose I/O	
	PT1	FP25	LCD Driver interface	
		IOC1	Timer Channel 1	
		GPIO	General-purpose I/O	
	PT0	FP24	LCD Driver interface	
		IOC0	Timer Channel 0	
		GPIO	General-purpose I/O	
Port S	PS7	$\overline{SS}$	Serial Peripheral Interface slave select output in master mode, input in slave mode or master mode	GPIO
		GPIO	General-purpose I/O	
	PS6	SCK	Serial Peripheral Interface serial clock pin	
		GPIO	General-purpose I/O	
	PS5	MOSI	Serial Peripheral Interface master out/slave in pin	
		GPIO	General-purpose I/O	
	PS4	MISO	Serial Peripheral Interface master in/slave out pin	
		GPIO	General-purpose I/O	
	PS3	TxD1	Serial Communication Interface 1 transmit pin	
		GPIO	General-purpose I/O	
	PS2	RxD1	Serial Communication Interface 1 receive pin	
		GPIO	General-purpose I/O	
	PS1	TxD0	Serial Communication Interface 0 transmit pin	
		GPIO	General-purpose I/O	
	PS0	RxD0	Serial Communication Interface 0 receive pin	
		GPIO	General-purpose I/O	

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port M	PM5	TXCAN1	MSCAN1 transmit pin	GPIO
		GPIO	General-purpose I/O	
	PM4	RXCAN1	MSCAN1 receive pin	
		GPIO	General-purpose I/O	
	PM3	TXCAN0	MSCAN0 transmit pin	
		GPIO	General-purpose I/O	
	PM2	RXCAN0	MSCAN0 receive pin	
		GPIO	General-purpose I/O	
	PM1	SDA	Inter Integrated Circuit serial data line	
		GPIO	General-purpose I/O	
	PM0	SCL	Inter Integrated Circuit serial clock line	
		GPIO	General-purpose I/O	
Port P	PP5	PWM6	Pulse Width Modulator channel 5	GPIO
		GPIO	General-purpose I/O	
	PP4	PWM4	Pulse Width Modulator channel 4	
		GPIO	General-purpose I/O	
	PP3	PWM3	Pulse Width Modulator channel 3	
		GPIO	General-purpose I/O	
	PP2	PWM2	Pulse Width Modulator channel 2	
		GPIO	General-purpose I/O	
	PP1	PWM1	Pulse Width Modulator channel 1	
		GPIO	General-purpose I/O	
	PP0	PWM0	Pulse Width Modulator channel 0	
		GPIO	General-purpose I/O	
Port H	PH7	GPIO/KWH7	General-purpose I/O with interrupt	GPIO
	PH6	GPIO/KWH6	General-purpose I/O with interrupt	
	PH5	GPIO/KWH5	General-purpose I/O with interrupt	
	PH4	GPIO/KWH4	General-purpose I/O with interrupt	
	PH3	GPIO/KWH3	General-purpose I/O with interrupt	
	PH2	GPIO/KWH2	General-purpose I/O with interrupt	
	PH1	GPIO/KWH1	General-purpose I/O with interrupt	
	PH0	GPIO/KWH0	General-purpose I/O with interrupt	
Port J	PJ3	GPIO/KWJ3	General-purpose I/O with interrupt	GPIO
	PJ2	GPIO/KWJ2	General-purpose I/O with interrupt	
	PJ1	GPIO/KWJ1	General-purpose I/O with interrupt	
	PJ0	GPIO/KWJ0	General-purpose I/O with interrupt	

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port L	PL7	FP31	LCD Driver interface	GPIO
		GPIO	General-purpose I/O	
	PL6	FP30	LCD Driver interface	
		GPIO	General-purpose I/O	
	PL5	FP29	LCD Driver interface	
		GPIO	General-purpose I/O	
	PL4	FP28	LCD Driver interface	
		GPIO	General-purpose I/O	
	PL3	FP19	LCD Driver interface	
		GPIO	General-purpose I/O	
	PL2	FP18	LCD Driver interface	
		GPIO	General-purpose I/O	
	PL1	FP17	LCD Driver interface	
		GPIO	General-purpose I/O	
	PL0	FP16	LCD Driver interface	
		GPIO	General-purpose I/O	
Port U	PU7	M1C1M	PWM Motor Controller Channel 3	GPIO
		GPIO	General-purpose I/O	
	PU6	M1C1P	PWM Motor Controller Channel 3	
		GPIO	General-purpose I/O	
	PU5	M1C0M	PWM Motor Controller Channel 2	
		GPIO	General-purpose I/O	
	PU4	M1C0P	PWM Motor Controller Channel 2	
		GPIO	General-purpose I/O	
	PU3	M0C1M	PWM Motor Controller Channel 1	
		GPIO	General-purpose I/O	
	PU2	M0C1P	PWM Motor Controller Channel 1	
		GPIO	General-purpose I/O	
	PU1	M0C0M	PWM Motor Controller Channel 0	
		GPIO	General-purpose I/O	
	PU0	M0C0P	PWM Motor Controller Channel 0	
		GPIO	General-purpose I/O	

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port V	PV7	M3C1M	PWM Motor Controller Channel 7	GPIO
		GPIO	General-purpose I/O	
	PV6	M3C1P	PWM Motor Controller Channel 7	
		GPIO	General-purpose I/O	
	PV5	M3C0M	PWM Motor Controller Channel 6	
		GPIO	General-purpose I/O	
	PV4	M2C0P	PWM Motor Controller Channel 6	
		GPIO	General-purpose I/O	
	PV3	M2C1M	PWM Motor Controller Channel 5	
		GPIO	General-purpose I/O	
	PV2	M2C1P	PWM Motor Controller Channel 5	
		GPIO	General-purpose I/O	
	PV1	M2C0M	PWM Motor Controller Channel 4	
		GPIO	General-purpose I/O	
	PV0	M2C0P	PWM Motor Controller Channel 4	
		GPIO	General-purpose I/O	
Port W	PW7	M5C1M	PWM Motor Controller Channel 11	GPIO
		GPIO	General-purpose I/O	
	PW6	M5C1P	PWM Motor Controller Channel 11	
		GPIO	General-purpose I/O	
	PW5	M5C0M	PWM Motor Controller Channel 10	
		GPIO	General-purpose I/O	
	PW4	M5C0P	PWM Motor Controller Channel 10	
		GPIO	General-purpose I/O	
	PW3	M4C1M	PWM Motor Controller Channel 9	
		GPIO	General-purpose I/O	
	PW2	M4C1P	PWM Motor Controller Channel 9	
		GPIO	General-purpose I/O	
	PW1	M4C0M	PWM Motor Controller Channel 8	
		GPIO	General-purpose I/O	
	PW0	M4C0P	PWM Motor Controller Channel 8	
		GPIO	General-purpose I/O	

Section 3 Memory Map and Registers

3.1 Overview

This section provides a detailed description of all registers.

3.2 Module Memory Map

Table 3-1 shows the register map of the Motor Controller module.

Table 3-1 PIM_9H256 Memory Map

Address offset	Use	Access
$00	Port T I/O Register (PTT)	RW
$01	Port T Input Register (PTIT)	R
$02	Port T Data Direction Register (DDRT)	RW
$03	Port T Reduced Drive Register (RDRT)	RW
$04	Port T Pull Device Enable Register (PERT)	RW
$05	Port T Polarity Select Register (PPST)	RW
$06	Reserved	-
$07	Reserved	-
$08	Port S I/O Register (PTS)	RW
$09	Port S Input Register (PTIS)	R
$0A	Port S Data Direction Register (DDRS)	RW
$0B	Port S Reduced Drive Register (RDRS)	RW
$0C	Port S Pull Device Enable Register (PERS)	RW
$0D	Port S Polarity Select Register (PPSS)	RW
$0E	Port S Wired-Or Mode Register (WOMS)	RW
$0F	Reserved	-
$10	Port M I/O Register (PTM)	RW
$11	Port M Input Register (PTIM)	R
$12	Port M Data Direction Register (DDRM)	RW
$13	Port M Reduced Drive Register (RDRM)	RW
$14	Port M Pull Device Enable Register (PERM)	RW
$15	Port M Polarity Select Register (PPSM)	RW
$16	Port M Wired-Or Mode Register (WOMM)	RW
$17	Reserved	-
$18	Port P I/O Register (PTP)	RW
$19	Port P Input Register (PTIP)	R
$1A	Port P Data Direction Register (DDRP)	RW
$1B	Port P Reduced Drive Register (RDRP)	RW
$1C	Port P Pull Device Enable Register (PERP)	RW
$1D	Port P Polarity Select Register (PPSP)	RW
$1E	Reserved	-

Table 3-1 PIM_9H256 Memory Map

$1F	Reserved	-
$20	Port H I/O Register (PTH)	RW
$21	Port H Input Register (PTIH)	R
$22	Port H Data Direction Register (DDRH)	RW
$23	Port H Reduced Drive Register (RDRH)	RW
$24	Port H Pull Device Enable Register (PERH)	RW
$25	Port H Polarity Select Register (PPSH)	RW
$26	Port H Interrupt Enable Register (PIEH)	RW
$27	Port H Interrupt Flag Register (PIFH)	RW
$28	Port J I/O Register (PTJ)	RW
$29	Port J Input Register (PTIJ)	R
$2A	Port J Data Direction Register (DDRJ)	RW
$2B	Port J Reduced Drive Register (RDRJ)	RW
$2C	Port J Pull Device Enable Register (PERJ)	RW
$2D	Port J Polarity Select Register (PPSJ)	RW
$2E	Port J Interrupt Enable Register (PIEJ)	RW
$2F	Port J Interrupt Flag Register (PIFJ)	RW
$30	Port L I/O Register (PTL)	RW
$31	Port L Input Register (PTIL)	R
$32	Port L Data Direction Register (DDRL)	RW
$33	Port L Reduced Drive Register (RDRL)	RW
$34	Port L Pull Device Enable Register (PERL)	RW
$35	Port L Polarity Select Register (PPSL)	RW
$36	Reserved	-
$37	Reserved	-
$38	Port U I/O Register (PTU)	RW
$39	Port U Input Register (PTIU)	R
$3A	Port U Data Direction Register (DDRU)	RW
$3B	Port U Slew Rate Register (SRRU)	RW
$3C	Port U Pull Device Enable Register (PERU)	RW
$3D	Port U Polarity Select Register (PPSU)	RW
$3E	Reserved	-
$3F	Reserved	-
$40	Port V I/O Register (PTV)	RW
$41	Port V Input Register (PTIV)	R
$42	Port V Data Direction Register (DDRV)	RW
$43	Port V Slew Rate Register (SRRV)	RW
$44	Port V Pull Device Enable Register (PERV)	RW
$45	Port V Polarity Select Register (PPSV)	RW
$46	Reserved	-
$47	Reserved	-
$48	Port W I/O Register (PTW)	RW
$49	Port W Input Register (PTIW)	R
$4A	Port W Data Direction Register (DDRW)	RW

Table 3-1 PIM_9H256 Memory Map

$4B	Port W Slew Rate Register (SRRW)	RW
$4C	Port W Pull Device Enable Register (PERW)	RW
$4D	Port W Polarity Select Register (PPSW)	RW
$4E - $7F	Reserved	-

3.3 Register Descriptions

The following table summarizes the effect on the various configuration bits, data direction (DDR), output level (I/O), reduced drive (RDR), pull enable (PE), pull select (PS) and interrupt enable (IE) for the ports. The configuration bit PS is used for two purposes:

1. Configure the sensitive interrupt edge (rising or falling), if interrupt is enabled.
2. Select either a pull-up or pull-down device if PE is active.

Table 3-2 Pin Configuration Summary

DDR	IO	RDR	PE	PS	IE[1]	Function	Pull Device	Interrupt
0	X	X	0	X	0	Input	Disabled	Disabled
0	X	X	1	0	0	Input	Pull Up	Disabled
0	X	X	1	1	0	Input	Pull Down	Disabled
0	X	X	0	0	1	Input	Disabled	falling edge
0	X	X	0	1	1	Input	Disabled	rising edge
0	X	X	1	0	1	Input	Pull Up	falling edge
0	X	X	1	1	1	Input	Pull Down	rising edge
1	0	0	X	X	0	Output, full drive to 0	Disabled	Disabled
1	1	0	X	X	0	Output, full drive to 1	Disabled	Disabled
1	0	1	X	X	0	Output, reduced drive to 0	Disabled	Disabled
1	1	1	X	X	0	Output, reduced drive to 1	Disabled	Disabled
1	0	0	X	0	1	Output, full drive to 0	Disabled	falling edge
1	1	0	X	1	1	Output, full drive to 1	Disabled	rising edge
1	0	1	X	0	1	Output, reduced drive to 0	Disabled	falling edge
1	1	1	X	1	1	Output, reduced drive to 1	Disabled	rising edge

NOTES:
1. Applicable only on port H and J.

NOTE: *All bits of all registers in this module are completely synchronous to internal clocks during a register read.*

3.3.1 Port T Registers

Port T is shared by the Capture Timer and the LCD Driver. Each pin is assigned to these modules according to the following priority: LCD Driver > Timer > General Purpose IO

Address Offset: $__00

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
TIM:	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
LCD:					1	1	1	1
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-1 Port T I/O Register (PTT)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.
Pins which are used by the LCD driver read 1, if they are configured as inputs.

Address Offset: $__01

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-2 Port T Input Register (PTIT)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to

2 bus cycles.
Pins which are used by the LCD driver read 1.

Address Offset: $__02

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-3 Port T Data Direction Register (DDRT)

Read:Anytime.

Write:Anytime.

This register configures each port T pin as either input or output.
The LCD driver will output an analog signal to each associated pin. The TIM forces the I/O state to be an output for each timer port associated with an enabled output compare. In these cases the data direction bits will not change.
The DDRT bits revert to controlling the I/O direction of a pin when the associated peripheral is disabled. The timer input capture always monitors the state of the pin.

DDRT[7:0] — Data Direction Port T
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTT or PTIT registers, when changing the DDRT register.

Address Offset: $__03

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-4 Port T Reduced Drive Register (RDRT)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port T output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRT[7:0] — Reduced Drive Port T

1 = Associated pin drives at about 1/3 of the full drive strength.

0 = Full drive strength at output.

Address Offset: $__04

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
Reset:	1	1	1	1	1	1	1	1

= Reserved or unimplemented

Figure 3-5 Port T Pull Device Enable Register (PERT)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERT[7:0] — Pull Device Enable Port T

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__05

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
Reset:	1	1	1	1	1	1	1	1

= Reserved or unimplemented

Figure 3-6 Port T Polarity Select Register (PPST)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPST[7:0] — Pull Select Port T

1 = A pull-down device is connected to the associated port T pin, if enabled by the associated bit in register PERT and if the port is used as input.

0 = A pull-up device is connected to the associated port T pin, if enabled by the associated bit in register PERT and if the port is used as input.

3.3.2 Port S Registers

Port S is associated with the Serial Peripheral Interface and both Serial Communication Interfaces.

Address Offset: $__08

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
SPI/SCI	$\overline{SS}$	SCK	MOSI	MISO	TxD1	RxD1	TxD0	RxD0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-7 Port S I/O Register (PTS)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.
The SPI pins (PS[7:4]) configuration is determined by several status bits in the SPI module. *Refer to SPI Block User Guide for details*.
The SCI ports associated with transmit pins 3 and 1 are configured as outputs if the transmitter is enabled.
The SCI pins associated with receive pins 2 and 0 are configured as inputs if the receiver is enabled. *Refer to SPI Block User Guide for details*.

Address Offset: $__09

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-8 Port S Input Register (PTIS)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This also can be used to detect overload or short circuit conditions on output pins.

Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.

Address Offset:$__0A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRS7	DDRS6	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-9 Port S Data Direction Register (DDRS)

Read:Anytime.

Write:Anytime.

This register configures each port S pin as either input or output
If SPI is enabled, the SPI determines the pin direction. *For details see SPI specification.*
If the associated SCI transmit or receive channel is enabled this register has no effect on the pins. The pin is forced to be an output if a SCI transmit channel is enabled, it is forced to be an input if the SCI receive channel is enabled.
The DDRS bits revert to controlling the I/O direction of a pin when the associated channel is disabled.

DDRS[7:0] — Data Direction Port S
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTS or PTIS registers, when changing the DDRS register.

Address Offset: $__0B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-10 Port S Reduced Drive Register (RDRS)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port S output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRS[7:0] — Reduced Drive Port S

1 = Associated pin drives at about 1/3 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__0C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-11 Port S Pull Device Enable Register (PERS)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as output in wired-or (open drain) mode. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled.

PERS[7:0] — Pull Device Enable Port S

1 = Either a pull-up or pull-down device is enabled.
0 = Pull-up or pull-down device is disabled.

Address Offset: $__0D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-12 Port S Polarity Select Register (PPSS)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPSS[7:0] — Pull Select Port S

1 = A pull-down device is connected to the associated port S pin, if enabled by the associated bit in register PERS and if the port is used as input.

0 = A pull-up device is connected to the associated port S pin, if enabled by the associated bit in register PERS and if the port is used as input or as wired-or output.

Address Offset: $__0E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-13 Port S Wired-Or Mode Register (WOMS)

Read:Anytime.

Write:Anytime.

This register configures the output pins as wired-or. If enabled the output is driven active low only (open-drain). A logic level of “1” is not driven. It applies also to the SPI and SCI outputs and allows a multipoint connection of several serial modules. This bit has no influence on pins used as inputs.

WOMS[7:0] — Wired-Or Mode Port S

1 = Output buffers operate as open-drain outputs.
0 = Output buffers operate as push-pull outputs.

3.3.3 Port M Registers

Port M is associated with both MSCAN modules and the IIC Interface.

Address Offset: $__10

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	0	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
CAN/IIC:			TxCAN1	RxCAN1	TxCAN0	RxCAN0	SDA	SCL
Reset	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-14 Port M I/O Register (PTM)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to

2 bus cycles.
The CAN function (TxCAN and RxCAN) takes precedence over the general purpose I/O function if the associated CAN module is enabled. *Refer to MSCAN Block User Guide for details.*
The IIC function takes precedence over the general purpose I/O function associated if enabled. *Refer to IIC Block User Guide for details.*

Address Offset: $__11

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
Write:								
Reset:	0	0	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-15 Port M Input Register (PTIM)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.

Address Offset: $__12

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-16 Port M Data Direction Register (DDRM)

Read:Anytime.

Write:Anytime.

This register configures each port M pin as either input or output.
The CAN forces the I/O state to be an output for each port line associated with an enabled output (TxCAN[1:0]). It also forces the I/O state to be an input for each port line associated with an enabled input (RxCAN[1:0]).
The IIC forces each associated pin to be an open drain output.
In these cases the data direction bits will not change.
The DDRM bits revert to controlling the I/O direction of a pin when the associated peripheral module is disabled.

DDRM[7:0] — Data Direction Port M
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTM or PTIM registers, when changing the DDRM register.

Address Offset: $__13

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-17 Port M Reduced Drive Register (RDRM)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port M output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRM[7:0] — Reduced Drive Port M
1 = Associated pin drives at about 1/3 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__14

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-18 Port M Pull Device Enable Register (PERM)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or wired-or output. This bit has no effect if the port is used as push-pull output. Out of reset no pull device is enabled.

PERM[7:0] — Pull Device Enable Port M
1 = Either a pull-up or pull-down device is enabled.
0 = Pull-up or pull-down device is disabled.

Address Offset: $__15

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-19 Port M Polarity Select Register (PPSM)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin. If CAN is active a pull-up device can be activated on the RxCAN[3:0] inputs, but not a pull-down. If BDLC is active a pull-down device can be activated on the RxBDLC pin but not a pull-up.

PPSM[7:0] — Pull Select Port M

1 = A pull-down device is connected to the associated port M pin, if enabled by the associated bit in register PERM and if the port is used as a general purpose or BDLC input but not as RxCAN.

0 = A pull-up device is connected to the associated port M pin, if enabled by the associated bit in register PERM and if the port is used as general purpose or RxCAN input but not as BDLC.

Address Offset: $__16

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-20 Port M Wired-Or Mode Register (WOMM)

Read:Anytime.

Write:Anytime.

This register configures the output pins as wired-or. If enabled the output is driven active low only (open-drain). A logic level of “1” is not driven. It applies also to the CAN outputs and allows a multipoint connection of several serial modules. Pins associated with the IIC module are always set to wired-or mode. The WOMM bit will not change by activating the IIC. This bit has no influence on pins used as inputs.

3.3.4 Port P Registers

Port M is associated with both MSCAN modules and the Pulse Width Modulator.

Address Offset: $__18

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
Write:								
PWM:			PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-21 Port P I/O Register (PTP)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.
The PWM function takes precedence over the general purpose I/O function if the associated PWM channel is enabled. While channels 4-0 are output only if the respective channel is enabled, channel 5 can be PWM output or input if the shutdown feature is enabled. *Refer to PWM Block User Guide for details.*

Address Offset: $__19

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
Write:								
Reset:	0	0	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-22 Port P Input Register (PTIP)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can be also used to detect overload or short circuit conditions on output pins.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to

2 bus cycles.

Address Offset: $__1A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-23 Port P Data Direction Register (DDRP)

Read:Anytime.

Write:Anytime.

This register configures each port P pin as either input or output.
If the associated PWM channel is enabled this register has no effect on the pins.
The PWM forces the I/O state to be an output for each port line associated with an enabled PWM5-0 channel. Channel 5 can force the pin to input if the shutdown feature is enabled.
The DDRM bits revert to controlling the I/O direction of a pin when the associated PWM channel is disabled.

DDRP[7:0] — Data Direction Port P
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTP or PTIP registers, when changing the DDRP register.

Address Offset: $__1B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-24 Port P Reduced Drive Register (RDRP)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port P output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRP[7:0] — Reduced Drive Port P
1 = Associated pin drives at about 1/3 of the full drive strength.

0 = Full drive strength at output.

Address Offset: $__1C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-25 Port P Pull Device Enable Register (PERP)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERP[7:0] — Pull Device Enable Port P

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__1D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-26 Port P Polarity Select Register (PPSP)

Read:Anytime.

Write:Anytime.

This register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.

PPSP[7:0] — Polarity Select Port P

1 = Rising edge on the associated port P pin sets the associated flag bit in the PIFP register.A pull-down device is connected to the associated port P pin, if enabled by the associated bit in register PERP and if the port is used as input.

0 = Falling edge on the associated port P pin sets the associated flag bit in the PIFP register.A pull-up device is connected to the associated port P pin, if enabled by the associated bit in register PERP and if the port is used as input.

3.3.5 Port H Registers

Address Offset:$__20

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-27 Port H I/O Register (PTH)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.

Address Offset: $__21

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-28 Port H Input Register (PTIH)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to

2 bus cycles.

Address Offset: $__22

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRH7	DDRH6	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-29 Port H Data Direction Register (DDRH)

Read:Anytime.

Write:Anytime.

This register configures each port H pin as either input or output.

DDRH[7:0] — Data Direction Port H

1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTH or PTIH registers, when changing the DDRH register.

Address Offset: $__23

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-30 Port H Reduced Drive Register (RDRH)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port H output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRH[7:0] — Reduced Drive Port H

1 = Associated pin drives at about 1/3 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__24

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-31 Port H Pull Device Enable Register (PERH)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERH[7:0] — Pull Device Enable Port H

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__25

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-32 Port H Polarity Select Register (PPSH)

Read:Anytime.

Write:Anytime.

This register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.

PPSH[7:0] — Polarity Select Port H

1 = Rising edge on the associated port H pin sets the associated flag bit in the PIFH register. A pull-down device is connected to the associated port H pin, if enabled by the associated bit in register PERH and if the port is used as input.

0 = Falling edge on the associated port H pin sets the associated flag bit in the PIFH register. A pull-up device is connected to the associated port H pin, if enabled by the associated bit in register PERH and if the port is used as input.

Address Offset: $__26

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-33 Port H Interrupt Enable Register (PIEH)

Read:Anytime.

Write:Anytime.

This register disables or enables on a per pin basis the edge sensitive external interrupt associated with port H.

PIEH[7:0] — Interrupt Enable Port H

1 = Interrupt is enabled.

0 = Interrupt is disabled (interrupt flag masked).

Address Offset: $__27

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-34 Port H Interrupt Flag Register (PIFH)

Read:Anytime.

Write:Anytime.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSH register. To clear this flag, write “1” to the corresponding bit in the PIFH register. Writing a “0” has no effect.

PIFH[7:0] — Interrupt Flags Port H

1 = Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set).
Writing a “1” clears the associated flag.

0 = No active edge pending.
Writing a “0” has no effect.

3.3.6 Port J Registers

Address Offset: $__28

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PTJ3	PTJ2	PTJ1	PTJ0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-35 Port J I/O Register (PTJ)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.

Address Offset: $__29

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PTIJ3	PTIJ2	PTIJ1	PTIJ0
Write:								
Reset:	0	0	0	0	-	-	-	-

= Reserved or unimplemented

Figure 3-36 Port J Input Register (PTIJ)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can be used to detect overload or short circuit conditions on output pins.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to

2 bus cycles.

Address Offset: $__2A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	DDRJ3	DDRJ2	DDRJ1	DDRJ0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-37 Port J Data Direction Register (DDRJ)

Read:Anytime.

Write:Anytime.

This register configures each port J pin as either input or output.

DDRJ[7:6][1:0] — Data Direction Port J

1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTJ or PTIJ registers, when changing the DDRJ register.

Address Offset: $__2B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	RDRJ3	RDRJ2	RDRJ1	RDRJ0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-38 Port J Reduced Drive Register (RDRJ)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port J output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRJ[7:6][1:0] — Reduced Drive Port J

1 = Associated pin drives at about 1/3 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__2C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PERJ3	PERJ2	PERJ1	PERJ0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-39 Port J Pull Device Enable Register (PERJ)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as wired-or output. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled.

PERJ[7:6][1:0] — Pull Device Enable Port J

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__2D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PPSJ3	PPSJ2	PPSJ1	PPSJ0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-40 Port J Polarity Select Register (PPSJ)

Read:Anytime.

Write:Anytime.

This register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.

PPSJ[7:6][1:0] — Polarity Select Port H

1 = Rising edge on the associated port J pin sets the associated flag bit in the PIFJ register.
A pull-down device is connected to the associated port J pin, if enabled by the associated bit in register PERJ and if the port is used as input.

0 = Falling edge on the associated port J pin sets the associated flag bit in the PIFJ register.
A pull-up device is connected to the associated port J pin, if enabled by the associated bit in register PERJ and if the port is used as general purpose input or as IIC port.

Address Offset: $__2E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PIEJ3	PIEJ2	PIEJ1	PIEJ0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-41 Port J Interrupt Enable Register (PIEJ)

Read:Anytime.

Write:Anytime.

This register disables or enables on a per pin basis the edge sensitive external interrupt associated with port J.

PIEJ[7:6][1:0] — Interrupt Enable Port J

1 = Interrupt is enabled.

0 = Interrupt is disabled (interrupt flag masked).

Address Offset: $__2F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PIFJ3	PIFJ2	PIFJ1	PIFJ0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-42 Port J Interrupt Flag Register (PIFJ)

Read:Anytime.

Write:Anytime.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSJ register. To clear this flag, write “1” to the corresponding bit in the PIFJ register. Writing a “0” has no effect.

PIFJ[7:6][1:0] — Interrupt Flags Port J

1 = Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set).
Writing a “1” clears the associated flag.

0 = No active edge pending.
Writing a “0” has no effect.

3.3.7 Port L Registers

Address Offset: $__30

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PTL7	PTL6	PTL5	PTL4	PTL3	PTL2	PTL1	PTL0
LCD:	1	1	1	1	1	1	1	1
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-43 Port L I/O Register (PTL)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.
Pins which are used by the LCD driver read 1, if they are configured as inputs.

Address Offset: $__31

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIL7	PTIL6	PTIL5	PTIL4	PTIL3	PTIL2	PTIL1	PTIL0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-44 Port L Input Register (PTIL)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.
Pins which are used by the LCD driver read 1. *Refer to LCD driver Block User Guide for details.*
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.

Address Offset: $__32

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRL7	DDRL6	DDRL5	DDRL4	DDRL3	DDRL2	DDRL1	DDRL0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-45 Port L Data Direction Register (DDRL)

Read:Anytime.

Write:Anytime.

This register configures each port L pin as either input or output.

DDRL[7:0] — Data Direction Port L

1 = Associated pin is configured as output.

0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTL or PTIL registers, when changing the DDRT register.

Address Offset: $__33

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRL7	RDRL6	RDRL5	RDRL4	RDRL3	RDRL2	RDRL1	RDRL0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-46 Port L Reduced Drive Register (RDRL)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port L output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRL[7:0] — Reduced Drive Port L

1 = Associated pin drives at about 1/3 of the full drive strength.

0 = Full drive strength at output.

Address Offset: $__34

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERL7	PERL6	PERL5	PERL4	PERL3	PERL2	PERL1	PERL0
Reset:	1	1	1	1	1	1	1	1

= Reserved or unimplemented

Figure 3-47 Port L Pull Device Enable Register (PERL)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERL[7:0] — Pull Device Enable Port L

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__35

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSL7	PPSL6	PPSL5	PPSL4	PPSL3	PPSL2	PPSL1	PPSL0
Reset:	1	1	1	1	1	1	1	1

= Reserved or unimplemented

Figure 3-48 Port L Polarity Select Register (PPSL)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPSL[7:0] — Pull Select Port L

1 = A pull-down device is connected to the associated port L pin, if enabled by the associated bit in register PERT and if the port is used as input.

0 = A pull-up device is connected to the associated port L pin, if enabled by the associated bit in register PERT and if the port is used as input.

3.3.8 Port U Registers

Address Offset: $__38

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PTU7	PTU6	PTU5	PTU4	PTU3	PTU2	PTU1	PTU0
MC:	M1C1M	M1C1P	M1C0M	M1C0P	M0C1M	M0C1P	M0C0M	M0C0P
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-49 Port U I/O Register (PTU)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.
Pins with active slew rate control read 1, if they are configured as inputs.

Address Offset: $__39

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIU7	PTIU6	PTIU5	PTIU4	PTIU3	PTIU2	PTIU1	PTIU0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-50 Port U Input Register (PTIU)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.
The input buffer of a pin becomes deactivated when slew rate control is enabled. These pins will read **1**.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.

Address Offset: $__3A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRU7	DDRU6	DDRU5	DDRU4	DDRU3	DDRU2	DDRU1	DDRU0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-51 Port U Data Direction Register (DDRU)

Read:Anytime.

Write:Anytime.

This register configures each port U pin as either input or output.
The MC forces the I/O state to be an output for each associated pin. In these cases the data direction bits will not change.
The DDRU bits revert to controlling the I/O direction of a pin when the associated motor controler channel is disabled.
The timer input capture always monitors the state of the pin.

DDRU[7:0] — Data Direction Port U
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTU or PTIU registers, when changing the DDRU register.

Address Offset: $__3B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SRRU7	SRRU6	SRRU5	SRRU4	SRRU3	SRRU2	SRRU1	SRRU0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-52 Port U Slew Rate Register (SRRU)

Read:Anytime.

Write:Anytime.

This register enables the slew rate control of each port U output pin. If the port is used as input this bit is ignored.

SRRU[7:0] — Slew Rate Port U
1 = Enable slew rate control.
0 = Disable slew rate control.

Address Offset: $__3C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERU7	PERU6	PERU5	PERU4	PERU3	PERU2	PERU1	PERU0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-53 Port U Pull Device Enable Register (PERU)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERU[7:0] — Pull Device Enable Port U

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__3D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSU7	PPSU6	PPSU5	PPSU4	PPSU3	PPSU2	PPSU1	PPSU0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-54 Port U Polarity Select Register (PPSU)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPSU[7:0] — Pull Select Port U

1 = A pull-down device is connected to the associated port T pin, if enabled by the associated bit in register PERU and if the port is used as input.

0 = A pull-up device is connected to the associated port T pin, if enabled by the associated bit in register PERU and if the port is used as input.

3.3.9 Port V Registers

Address Offset: $__40

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PTV7	PTV6	PTV5	PTV4	PTV3	PTV2	PTV1	PTV0
MC:	M3C1M	M3C1P	M3C0M	M3C0P	M2C1M	M2C1P	M2C0M	M2C0P
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-55 Port V I/O Register (PTV)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.
Pins with active slew rate control read 1, if they are configured as inputs.

Address Offset: $__41

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIV7	PTIV6	PTIV5	PTIV4	PTIV3	PTIV2	PTIV1	PTIV0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-56 Port V Input Register (PTIV)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.
The input buffer of a pin becomes deactivated when slew rate control is enabled. These pins will read **1**.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.

Address Offset: $__42

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRV7	DDRV6	DDRV5	DDRV4	DDRV3	DDRV2	DDRV1	DDRV0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-57 Port V Data Direction Register (DDRV)

Read:Anytime.

Write:Anytime.

This register configures each port V pin as either input or output.
The MC forces the I/O state to be an output for each associated pin. In these cases the data direction bits will not change.
The DDRV bits revert to controlling the I/O direction of a pin when the associated motor controller channel is disabled.
The timer input capture always monitors the state of the pin.

DDRV[7:0] — Data Direction Port V
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTV or PTIV registers, when changing the DDRV register.

Address Offset: $__43

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SRRV7	SRRV6	SRRV5	SRRV4	SRRV3	SRRV2	SRRV1	SRRV0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-58 Port V Slew Rate Register (SRRV)

Read:Anytime.

Write:Anytime.

This register enables the slew rate control of each port V output pin. If the port is used as input this bit is ignored.

SRRV[7:0] — Slew Rate Port V
1 = Enable slew rate control.
0 = Disable slew rate control.

Address Offset: $__44

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERV7	PERV6	PERV5	PERV4	PERV3	PERV2	PERV1	PERV0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-59 Port V Pull Device Enable Register (PERV)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERV[7:0] — Pull Device Enable Port V

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__45

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSV7	PPSV6	PPSV5	PPSV4	PPSV3	PPSV2	PPSV1	PPSV0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-60 Port V Polarity Select Register (PPSV)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPSV[7:0] — Pull Select Port V

1 = A pull-down device is connected to the associated port T pin, if enabled by the associated bit in register PERU and if the port is used as input.

0 = A pull-up device is connected to the associated port T pin, if enabled by the associated bit in register PERU and if the port is used as input.

3.3.10 Port W Registers

Address Offset: $__48

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PTW7	PTW6	PTW5	PTW4	PTW3	PTW2	PTW1	PTW0
MC:	M5C1M	M5C1P	M5C0M	M5C0P	M4C1M	M4C1P	M4C0M	M4C0P
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-61 Port W I/O Register (PTW)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.
Pins with active slew rate control read 1, if they are configured as inputs.

Address Offset: $__49

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIW7	PTIW6	PTIW5	PTIW4	PTIW3	PTIW2	PTIW1	PTIW0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-62 Port W Input Register (PTIW)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.
The input buffer of a pin becomes deactivated when slew rate control is enabled. These pins will read **1**.
Due to internal synchronization circuits, input signal are propagated to this register with a delay of up to 2 bus cycles.

Address Offset: $__4A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRW7	DDRW6	DDRW5	DDRW4	DDRW3	DDRW2	DDRW1	DDRW0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-63 Port W Data Direction Register (DDRW)

Read:Anytime.

Write:Anytime.

This register configures each port W pin as either input or output.
The MC forces the I/O state to be an output for each associated pin. In these cases the data direction bits will not change.
The DDRW bits revert to controlling the I/O direction of a pin when the associated motor controller channel is disabled.
The timer input capture always monitors the state of the pin.

DDRW[7:0] — Data Direction Port W
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTW or PTIW registers, when changing the DDRW register.

Address Offset: $__4B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SRRW7	SRRW6	SRRW5	SRRW4	SRRW3	SRRW2	SRRW1	SRRW0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-64 Port W Slew Rate Register (SRRW)

Read:Anytime.

Write:Anytime.

This register enables the slew rate control of each port W output pin. If the port is used as input this bit is ignored.

SRRW[7:0] — Slew Rate Port W
1 = Enable slew rate control.
0 = Disable slew rate control.

Address Offset: $__4C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERW7	PERW6	PERW5	PERW4	PERW3	PERW2	PERW1	PERW0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-65 Port W Pull Device Enable Register (PERW)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERW[7:0] — Pull Device Enable Port W

1 = Either a pull-up or pull-down device is enabled.
0 = Pull-up or pull-down device is disabled.

Address Offset: $__4D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSW7	PPSW6	PPSW5	PPSW4	PPSW3	PPSW2	PPSW1	PPSW0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-66 Port W Polarity Select Register (PPSW)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPSW[7:0] — Pull Select Port W

1 = A pull-down device is connected to the associated port T pin, if enabled by the associated bit in register PERW and if the port is used as input.
0 = A pull-up device is connected to the associated port T pin, if enabled by the associated bit in register PERW and if the port is used as input.

Section 4 Functional Description

4.1 General

Each pin can act as general purpose I/O. In addition the pin can act as an output from a peripheral module or an input to a peripheral module.

A set of configuration registers is common to all ports. All registers can be written at any time, however a specific configuration might not become active.

Example:

Selecting a pull-up resistor. This resistor does not become active while the port is used as a push-pull output.

4.1.1 I/O register

This register holds the value driven out to the pin if the port is used as a general purpose I/O.

Writing to this register has only an effect on the pin if the port is used as general purpose output. When reading this address, the value of the pins is returned if the data direction register bits are set to 0.

If the data direction register bits are set to 1, the contents of the I/O register is returned. This is independent of any other configuration (see **Figure 4-1**).

4.1.2 Input register

This is a read-only register and always returns the value of the pin (see **Figure 4-1**).

4.1.3 Data direction register

This register defines whether the pin is used as an input or an output.

If a peripheral module controls the pin the contents of the data direction register is ignored (see **Figure 4-1**).

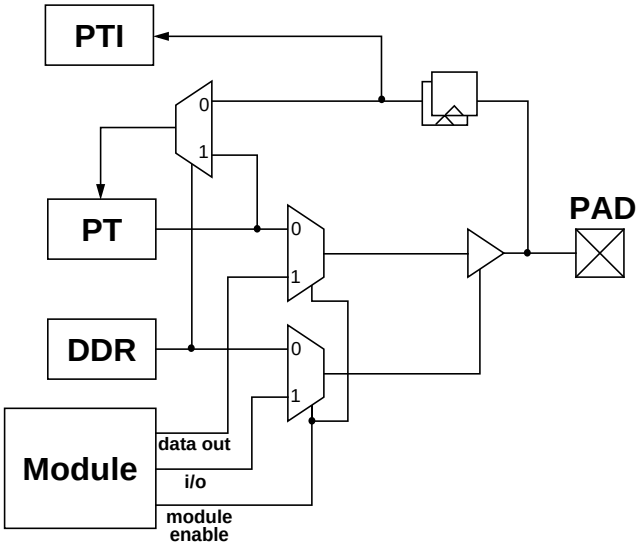

Figure 4-1 Illustration of I/O pin functionality

4.1.4 Reduced drive register

If the port is used as an output the register allows the configuration of the drive strength.

4.1.5 Pull device enable register

This register turns on a pull-up or pull-down device.

It becomes only active if the pin is used as an input or as a wired-or output.

4.1.6 Polarity select register

This register selects either a pull-up or pull-down device if enabled.

It becomes only active if the pin is used as an input. A pull-up device can be activated if the pin is used as a wired-or output.

4.2 Port T

This port is associated with the Capture Timer and the LCD driver module.

In all modes, port T pins PT[7:0] can be used for either general-purpose I/O, for the Capture Timer channels, or for the LCD driver interface.

During reset, port T pins are configured as high-impedance inputs.

4.3 Port S

This port is associated with the serial SCI and SPI modules.

In all modes, port S pins PS[7:0] can be used either for general-purpose I/O, or with the SCI and SPI subsystems.

During reset, port S pins are configured as inputs with pull-up.

4.4 Port M

This port is associated with the IIC and 2 CAN modules.

In all modes, port M pins PM[5:0] can be used for either general purpose I/O, or with the IIC and CAN subsystems.

During reset, port M pins are configured as high-impedance inputs.

4.5 Port P

This port is associated with the PWM module.

In all modes, port P pins PP[5:0] can be used for either general purpose I/O, or with the PWM subsystem. If the PWM is enabled the pins become PWM output channels with the exception of pin 5 which can be PWM input or output.

During reset, port P pins are configured as high-impedance inputs.

4.6 Port H

Port H offers 8 I/O pins with edge triggered interrupt capability in wired-or fashion. The interrupt enable as well as the sensitivity to rising or falling edges can be individually configured on per pin basis. All 8 bits/pins share the same interrupt vector. Interrupts can be used with the pins configured as inputs or outputs.

An interrupt is generated when a bit in the port interrupt flag register and its corresponding port interrupt enable bit are both set.

This external interrupt feature is capable to wake up the CPU when it is in STOP or WAIT mode.

A digital filter on each pin prevents pulses shorter than a specified time from generating an interrupt (see Table 1-2 Pulse Detection Criteria). Four consecutive samples have to be either low or high in order to detect a valid low or high input.

The filters are continuously clocked by the bus clock in RUN and WAIT mode. In STOP mode the clock is generated by a single RC oscillator in the Port Integration Module. To maximize current saving the RC oscillator runs only if the following condition is true on any pin:

Active level at the input as defined by the port polarity select register (PPS) and port interrupt enabled (PIE=1) and port interrupt flag not set (PIF=0).

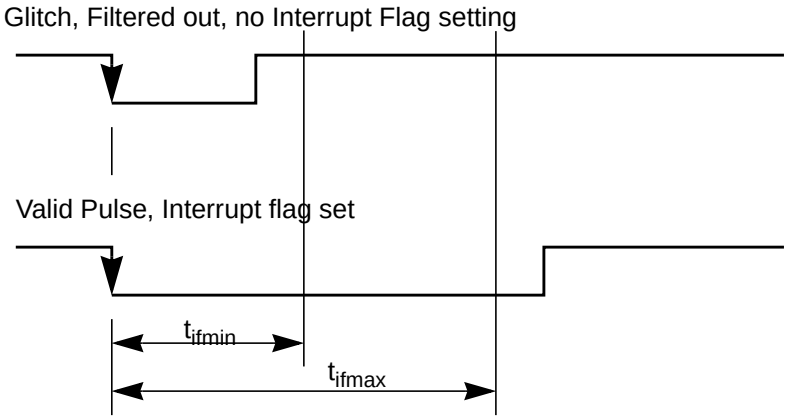

Figure 4-2 Interrupt Glitch Filter on Port P, H and J

Table 4-1 Pulse Detection Criteria

Pulse	Mode			
	$\overline{\text{STOP}}$		STOP[1]	
		Unit		Unit
Ignored	t_{pulse} <= 3	bus clocks	t_{pulse} <= 3.2	µs
Uncertain	3 < t_{pulse} < 4	bus clocks	3.2 < t_{pulse} < 10	µs
Valid	t_{pulse} >= 4	bus clocks	t_{pulse} >= 10	µs

NOTES:
1. These values include the spread of the oscillator frequency over temperature, voltage and process.

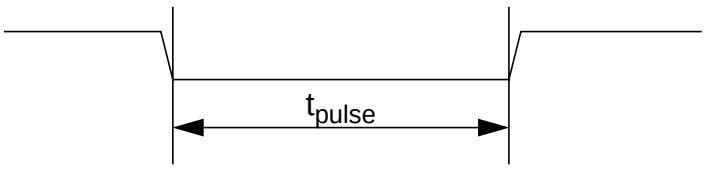

Figure 4-3 Pulse Illustration

4.7 Port J

4.8 Port J offers 4 I/O ports with the same interrupt features as port H.

4.9 Port L

This port is associated with the LCD driver module.

In all modes, port L pins PL[7:0] can be used for either general-purpose I/O or for the LCD driver interface.

During reset, port T pins are configured as high-impedance inputs.

4.10 Port U

This port is associated with the Motor Controller module.

In all modes, port U pins PU[7:0] can be used for either general-purpose I/O or for the Motor Controller.

During reset, port U pins are configured as high-impedance inputs.

4.11 Port V

This port is associated with the Motor Controller module.

In all modes, port V pins PV[7:0] can be used for either general-purpose I/O or for the Motor Controller.

During reset, port V pins are configured as high-impedance inputs.

4.12 Port W

This port is associated with the Motor Controller module.

In all modes, port W pins PW[7:0] can be used for either general-purpose I/O or for the Motor Controller.

During reset, port W pins are configured as high-impedance inputs.

4.13 Port A, B, E, K, and BKGD pin

All port and pin logic is located in the core module *Refer to S12_mebi Block User Guide for details*.

4.14 112 Pin QFP bond-out version

In case the port pins are not bonded out in the chosen package the user should initialize the registers to be inputs with enabled pull resistance to avoid excess current consumption. This applies to the following pins:

- All port J and H.

- Port PS2-3, PM0-1, PP2-5, PL4-7.
- PAD15-8. The A/D converter associated with those pins (ATD) should be disabled.

4.15 External Pin Descriptions

All ports start up as general purpose inputs on reset.

4.16 Low Power Options

4.16.1 Run Mode

No low power options exist for this module in run mode.

4.16.2 Wait Mode

No low power options exist for this module in wait mode.

4.16.3 Stop Mode

All clocks are stopped. There are however asynchronous paths to generate interrupts from STOP on port H and J.

Section 5 Resets

5.1 General

The reset values of all registers are given in the Register Description in section **3.3**.

5.2 Reset Initialization

All registers including the data registers get set/reset asynchronously. **Table 5-1** summarizes the port properties after reset initialization.

Table 5-1 Port Reset State Summary

Port	Reset States				
	Data Direction	Pull Mode	Red. Drive/ Slew Rate	Wired-Or Mode	Interrupt
A	Refer to section Bus Control and Input/Output	pull down	Refer to section Bus Control and Input/Output		
B		pull down			
E		pull down			
K		pull down			
BKGD pin		pull down			
T	input	pull down	disabled	n/a	n/a
S	input	hiz	disabled	disabled	n/a
M	input	hiz	disabled	disabled	n/a
P	input	hiz	disabled	n/a	n/a
H	input	hiz	disabled	n/a	disabled
J	input	hiz	disabled	n/a	disabled
L	input	pull down	disabled	n/a	n/a
U	input	hiz	disabled	n/a	n/a
V	input	hiz	disabled	n/a	n/a
W	input	hiz	disabled	n/a	n/a

Section 6 Interrupts

6.1 General

Port P, H and J generate a separate edge sensitive interrupt if enabled.

6.2 Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Port H	PIFH[7:0]	PIEH[7:0]	I Bit
Port J	PIFJ[7:6][1:0]	PIFJ[7:6][1:0]	I Bit

Table 6-1 Port Integration Module Interrupt Sources

NOTE: *Vector addresses and their relative interrupt priority are determined at the MCU level.*

6.3 Recovery from STOP

The PIM_9H256 can generate wake-up interrupts from STOP on port H and J. For other sources of external interrupts refer to the respective Block User Guides.

User Guide End Sheet

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