LCD32F4B

Block User Guide

V01.07

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Motorola, Inc

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Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
00.00	02-Feb-00			First Pass Release, version was sent to development tools.
00.01	07-Feb-00			Master page format changes. Added LCD Data Register descriptions. Added LCD Frontplane Enable Register Descriptions. Added voltage generation section. Added WAIT and STOP mode behavior section.
00.02	18-Feb-00			Removed contents of LCD voltage generation section due to changing customer requirements (still TBD).
00.03	16-Mar-00			- Added explanation of module during reset in section 1.1. Revised LCD Driver Block Diagram. - Added additional LCD prescaler dividers, 65536 and 131072 to module functionality. - Added the following sections to the document: Port B Frontplane Output, Port B Behavior during MCU Single Chip Modes, Port B Behavior during MCU Expanded Modes, Port A Frontplane Output, Port A Behavior during MCU Single Chip Modes, Port A Behavior during MCU Expanded Modes, Port L Frontplane Output, Port E Frontplane Output, Port E Behavior during MCU Single Chip Modes, Port E Behavior during MCU Expanded Modes, Port K Frontplane and Backplane Output, Port K Behavior during MCU Single Chip Modes, Port K Behavior during MCU Expanded Modes, Port T Frontplane Output, LCD System Enable and Frontplane Enable Sequencing. - Minor document formatting changes.
00.04	17-Apr-00			- Modified LCD RAM and Register map by splitting up the port L, E, and K frontplane enable registers into FPENL, FPENE, and FPENK respectively (previously FPENLEK). - Allowed LCD system to continue running during expanded modes. Modified operational description of ports to incorporate this change.
00.05	28-June-00			-Modified as of now PORT logic will be outside of the module.
01.00	26-Jul-00			- LCD module spec is now independent from Mako - Modified RAM and register locations as well as bit positions in the FPEN registers to ease a future stretch in LCD RAM size. - if the clocks are stopped, enabled frontplane/backplane pins are forced to V_{SSX}. - In expanded mode the frontplane and backplane drivers are disabled by the LCD module. - Added LCD Stop in WAIT mode (LCDSWAI) and LCD Run in Pseudo STOP mode (LCDRPSTP) control bits in a second LCD control register (LCDCR1). - RAM content indeterminate after reset.
01.01	29-Aug-00			- Number of frontplanes increased to 32, inc. FPEN bits and RAM - When LCD is enabled mode switching is not allowed. - Updated and clarified the Electrical Characteristics
01.02	12-Dec-00			- Changed, Figure 6-1, Figure 6-2 and the explanation. - Corrected Table 6-1
01.03	18-Jan-01			-Reformatted for SRS v2.0
01.04	16-Feb-01			- suggestion for improvement
01.05	15-Mar-01			improvements concerning SRS
01.06	13-Aug-01			improvements concerning SRS
01.07	08-Mar-02			Syntax corrections, document order number and formats updated

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Section 1 Introduction

1.1 Overview

The LCD32F4B driver module has 32 frontplane drivers and 4 backplane drivers so that a maximum of 128 LCD segments are controllable. Each segment is controlled by a corresponding bit in the LCD RAM. Four multiplex modes (1/1, 1/2, 1/3, 1/4 duty), and three bias (1/1, 1/2, 1/3) methods are available. The V_0 voltage is the lowest level of the output waveform and V_3 becomes the highest level. All frontplane and backplane pins can be multiplexed with other Port functions.

The LCD32F4B driver system consists of five major sub-modules:

- Timing and Control – consists of registers and control logic for frame clock generation, bias voltage level select, frame duty select, backplane select, and frontplane select/enable to produce the required frame frequency and voltage waveforms.

- LCD RAM – contains the data to be displayed on the LCD. Data can be read from or written to the display RAM at any time.

- Frontplane Drivers – consists of 32 frontplane drivers.

- Backplane Drivers – consists of 4 backplane drivers.

- Voltage Generator – Based on voltage applied to VLCD, it generates the voltage levels for the timing and control logic to produce the frontplane and backplane waveforms.

1.2 Features

The LCD32F4B includes these distinctive features:

- Supports five LCD operation modes
- 32 frontplane drivers
- 4 backplane drivers
  - Each frontplane has an enable bit respectively
- Programmable frame clock generator
- Programmable bias voltage level selector
- On Chip generation of 4 different output voltage levels

1.3 Modes of Operation

- The LCD32F4B module supports five operation modes with different numbers of backplanes and different biasing levels.During Pseudo STOP Mode and Wait Mode the LCD operation can be suspended under software control. Depending on the state of internal bits, the LCD can operate normally or the LCD clock generation can be turned off and the LCD32F4B module enters a power conservation state.

This is a high level description only, detailed descriptions of operating modes are contained in later sections.

1.4 Block Diagram

Figure 1-1 is a block diagram of the LCD32F4B module.
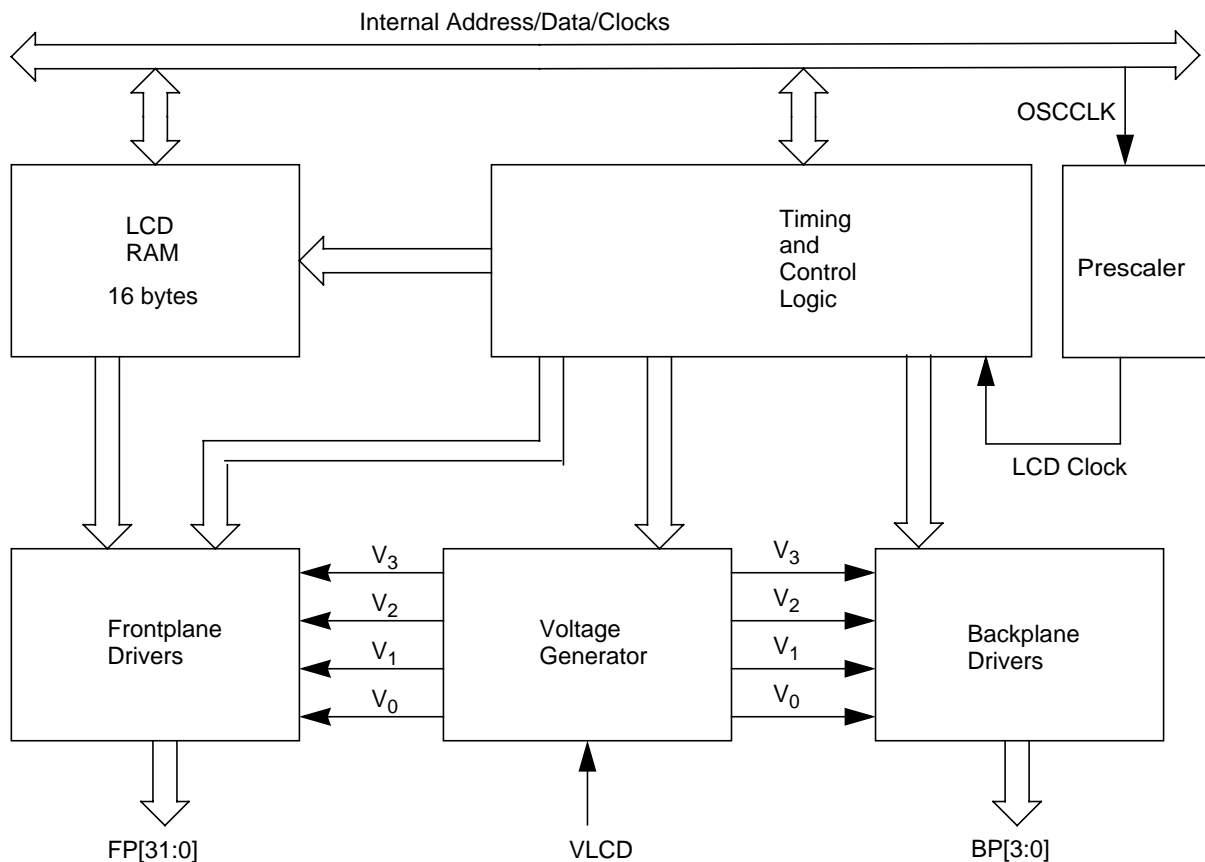
Figure 1-1 LCD32F4B Driver Block Diagram

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Section 2 Signal Description

2.1 Overview

The LCD32F4B module has a total of 37 external pins.

Table 2-1 Signal Properties

Name	Port	Function	Reset State	Pull up
4 Backplane Waveforms	BP[3:0]	Backplane waveform signals that connect directly to the pads	high impedance	
32 Frontplane Waveforms	FP[31:0]	Frontplane waveform signals that connect directly to the pads	high impedance	
LCD Voltage	VLCD	LCD supply voltage		

2.2 Detailed Signal Descriptions

2.2.1 BP[3:0]

This output signal vector represents the analog backplane waveforms of the LCD32F4B module and is connected directly to the corresponding pads.

2.2.2 FP[31:0]

This output signal vector represents the analog frontplane waveforms of the LCD32F4B module and is connected directly to the corresponding pads.

2.2.3 VLCD

Positive supply voltage for the LCD waveform generation.

Section 3 Memory Map and Registers

3.1 Overview

This section provides a detailed description of all memory and registers.

3.2 Module Memory Map

The memory map for the LCD32F4B module is given below in **Table 3-1**. The Address listed for each register is the address offset. The total address for each register is the sum of the base address for the LCD32F4B module and the address offset for each register.

Table 3-1 Module Memory Map

Address	Use	Access
$_00	LCD Control Register 0 (LCDCR0)	Read/Write
$_01	LCD Control Register 1 (LCDCR1)	Read/Write
$_02	LCD Frontplane Enable Register 0 (FPENR0)	Read/Write
$_03	LCD Frontplane Enable Register 1 (FPENR1)	Read/Write
$_04	LCD Frontplane Enable Register 2 (FPENR2)	Read/Write
$_05	LCD Frontplane Enable Register 3 (FPENR3)	Read/Write
$_06	Unimplemented	
$_07	Unimplemented	
$_08	LCDRAM (Location 0)	Read/Write
$_09	LCDRAM (Location 1)	Read/Write
$_0A	LCDRAM (Location 2)	Read/Write
$_0B	LCDRAM (Location 3)	Read/Write
$_0C	LCDRAM (Location 4)	Read/Write
$_0D	LCDRAM (Location 5)	Read/Write
$_0E	LCDRAM (Location 6)	Read/Write
$_0F	LCDRAM (Location 7)	Read/Write
$_10	LCDRAM (Location 8)	Read/Write
$_11	LCDRAM (Location 9)	Read/Write
$_12	LCDRAM (Location 10)	Read/Write
$_13	LCDRAM (Location 11)	Read/Write
$_14	LCDRAM (Location 12)	Read/Write
$_15	LCDRAM (Location 13)	Read/Write
$_16	LCDRAM (Location 14)	Read/Write
$_17	LCDRAM (Location 15)	Read/Write

3.3 Register Descriptions

This section consists of register descriptions. Each description includes a standard register diagram. Details of register bit and field function follow the register diagrams, in bit order.

3.3.1 LCD Control Register 0

$_00

	7	6	5	4	3	2	1	0
R	LCDEN	0	LCLK2	LCLK1	LCLK0	BIAS	DUTY1	DUTY0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented
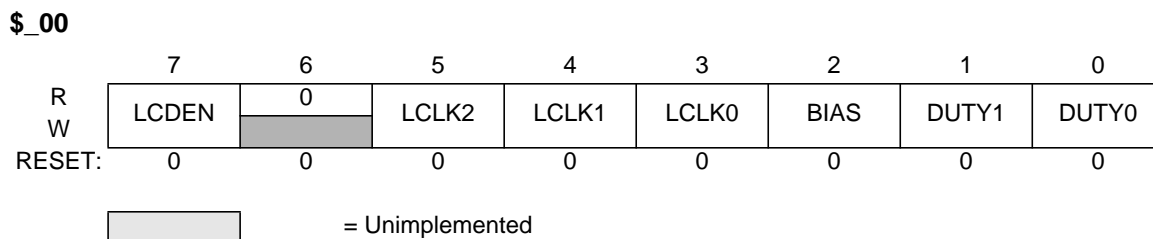
Figure 3-1 LCD Control Register 0 (LCDCR0)

Read: Anytime

Write: LCDEN anytime. To avoid segment flicker the clock prescaler bits, the bias select bit and the duty select bits must not be changed when the LCD is enabled.

LCDEN — LCD32F4B Driver System Enable

The LCDEN bit starts the LCD waveform generator.
  1 = LCD Driver System is enabled. All FP[31:0] pins with FP[31:0]EN set, will output an LCD driver waveform The BP[3:0] pins will output an LCD32F4B driver waveform based on the settings of DUTY0 and DUTY1.
  0 = All frontplane and backplane pins are disabled. In addition, the LCD32F4B system is disabled and all LCD waveform generation clocks are stopped.

LCLK0-2 — LCD Clock Prescaler

The LCD Clock Prescaler bits determine the OSCCLK divider value to produce the LCD Clock Frequency. For detailed description of the correlation between LCD Clock Prescaler bits and the divider value please refer to **Table 4-1**.

BIAS — BIAS Voltage Level Select

This bit selects the bias voltage levels during various LCD operating modes, as shown in table **Table 4-2**.

DUTY1/0 — LCD Duty Select

The DUTY1 and DUTY0 bits select the duty (multiplex mode) of the LCD32F4B driver system, as shown in table **Table 4-2**.

3.3.2 LCD Control Register 1

$_01

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	LCDSWAI	LCDRP-STP
W								
RESET:	0	0	0	0	0	0	0	0

☐ = Unimplemented
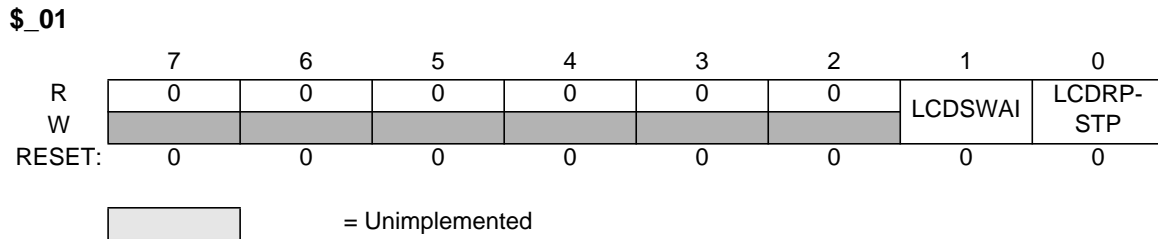
Figure 3-2 LCD Control Register 1 (LCDCR1)

Read and Write: Anytime

LCDRPSTP — LCD Run in Pseudo STOP Mode

This bit controls the LCD operation while in Pseudo STOP mode.
1 = LCD operates normally in Pseudo STOP mode.
0 = Stop LCD32F4B driver system when in Pseudo STOP mode.

LCDSWAI — LCD Stop in Wait Mode

This bit controls the LCD operation while in WAIT mode.
1 = Stop LCD32F4B driver system when in wait mode.
0 = LCD operates normally in wait mode.

3.3.3 LCD Frontplane Enable Register 0 – 3

$_02

	7	6	5	4	3	2	1	0
R	FP7EN	FP6EN	FP5EN	FP4EN	FP3EN	FP2EN	FP1EN	FP0EN
W								
RESET:	0	0	0	0	0	0	0	0

☐ = Unimplemented
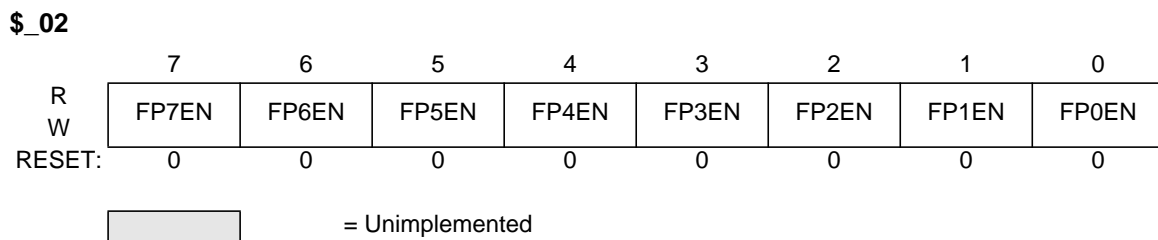
Figure 3-3 LCD Frontplane Enable Register 0 (FPENR0)

$_03

	7	6	5	4	3	2	1	0
R W	FP15EN	FP14EN	FP13EN	FP12EN	FP11EN	FP10EN	FP9EN	FP8EN
RESET:	0	0	0	0	0	0	0	0

☐ = Unimplemented
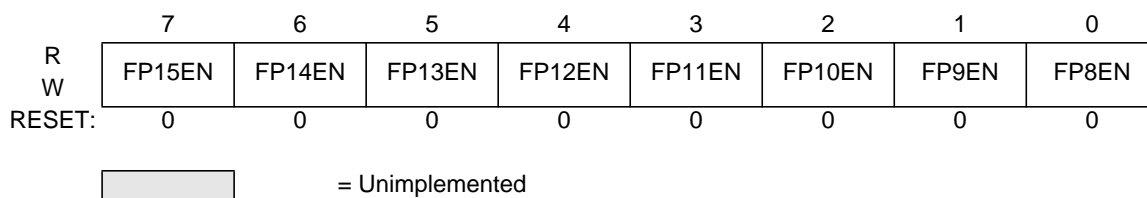
Figure 3-4 LCD Frontplane Enable Register 1 (FPENR1)

$_04

	7	6	5	4	3	2	1	0
R W	FP23EN	FP22EN	FP21EN	FP20EN	FP19EN	FP18EN	FP17EN	FP16EN
RESET:	0	0	0	0	0	0	0	0

☐ = Unimplemented
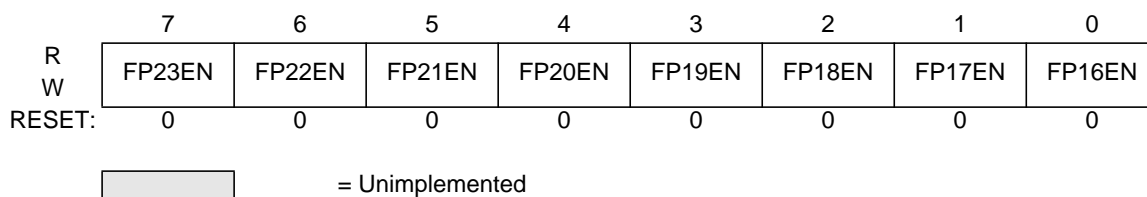
Figure 3-5 LCD Frontplane Enable Register 2 (FPENR2)

$_05

	7	6	5	4	3	2	1	0
R W	FP31EN	FP30EN	FP29EN	FP28EN	FP27EN	FP26EN	FP25EN	FP24EN
RESET:	0	0	0	0	0	0	0	0

☐ = Unimplemented

Figure 3-6 LCD Frontplane Enable Register 3 (FPENR3)

These bits enable the frontplane output waveform on the corresponding frontplane pin when LCDEN = 1.

Read and Write: Anytime

FP[31:0]EN — Frontplane Output Enable

The FP[31:0]EN bit enables the frontplane driver outputs. If LCDEN = 0, these bits have no effect on the state of the I/O pins. It is recommended to set FP[31:0]EN bits before LCDEN is set.
   1 = Frontplane driver output enabled on FP[31:0].
   0 = Frontplane driver output disabled on FP[31:0].

3.3.4 LCD RAM

The LCD RAM consists of 16 bytes. After reset the LCD RAM contents will be indeterminate (I), as indicated by **Table 3-2**.}

	7	6	5	4	3	2	1	0

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$__08 LCDRAM	R W	FP1BP3	FP1BP2	FP1BP1	FP1BP0	FP0BP3	FP0BP2	FP0BP1	FP0BP0
	RESET:	I	I	I	I	I	I	I	I
$__09 LCDRAM	R W	FP3BP3	FP3BP2	FP3BP1	FP3BP0	FP2BP3	FP2BP2	FP2BP1	FP2BP0
	RESET:	I	I	I	I	I	I	I	I
$__0A LCDRAM	R W	FP5BP3	FP5BP2	FP5BP1	FP5BP0	FP4BP3	FP4BP2	FP4BP1	FP4BP0
	RESET:	I	I	I	I	I	I	I	I
$__0B LCDRAM	R W	FP7BP3	FP7BP2	FP7BP1	FP7BP0	FP6BP3	FP6BP2	FP6BP1	FP6BP0
	RESET:	I	I	I	I	I	I	I	I
$__0C LCDRAM	R W	FP9BP3	FP9BP2	FP9BP1	FP9BP0	FP8BP3	FP8BP2	FP8BP1	FP8BP0
	RESET:	I	I	I	I	I	I	I	I
$__0D LCDRAM	R W	FP11BP3	FP11BP2	FP11BP1	FP11BP0	FP10BP3	FP10BP2	FP10BP1	FP10BP0
	RESET:	I	I	I	I	I	I	I	I
$__0E LCDRAM	R W	FP13BP3	FP13BP2	FP13BP1	FP13BP0	FP12BP3	FP12BP2	FP12BP1	FP12BP0
	RESET:	I	I	I	I	I	I	I	I
$__0F LCDRAM	R W	FP15BP3	FP15BP2	FP15BP1	FP15BP0	FP14BP3	FP14BP2	FP14BP1	FP14BP0
	RESET:	I	I	I	I	I	I	I	I
$__10 LCDRAM	R W	FP17BP3	FP17BP2	FP17BP1	FP17BP0	FP16BP3	FP16BP2	FP16BP1	FP16BP0
	RESET:	I	I	I	I	I	I	I	I
$__11 LCDRAM	R W	FP19BP3	FP19BP2	FP19BP1	FP19BP0	FP18BP3	FP18BP2	FP18BP1	FP18BP0
	RESET:	I	I	I	I	I	I	I	I
$__12 LCDRAM	R W	FP21BP3	FP21BP2	FP21BP1	FP21BP0	FP20BP3	FP20BP2	FP20BP1	FP20BP0
	RESET:	I	I	I	I	I	I	I	I
$__13 LCDRAM	R W	FP23BP3	FP23BP2	FP23BP1	FP23BP0	FP22BP3	FP22BP2	FP22BP1	FP22BP0
	RESET:	I	I	I	I	I	I	I	I
$__14 LCDRAM	Read: Write:	FP25BP3	FP25BP2	FP25BP1	FP25BP0	FP24BP3	FP24BP2	FP24BP1	FP24BP0
	RESET:	I	I	I	I	I	I	I	I
$__15 LCDRAM	Read: Write:	FP27BP3	FP27BP2	FP27BP1	FP27BP0	FP26BP3	FP26BP2	FP26BP1	FP26BP0
	RESET:	I	I	I	I	I	I	I	I
$__16 LCDRAM	Read: Write:	FP29BP3	FP29BP2	FP29BP1	FP29BP0	FP28BP3	FP28BP2	FP28BP1	FP28BP0
	RESET:	I	I	I	I	I	I	I	I
$__17 LCDRAM	Read: Write:	FP31BP3	FP31BP2	FP31BP1	FP31BP0	FP30BP3	FP30BP2	FP30BP1	FP30BP0
	RESET:	I	I	I	I	I	I	I	I

I = value is indeterminate

Table 3-2 LCD RAM

Read and Write: Anytime

FP[31:0]BP[3:0] — LCD Segment ON

The FP[31:0]BP[3:0] bit displays (turns on) the LCD Segment connected between FP[31:0] and BP[3:0].

1 – LCD Segment ON.

0 – LCD Segment OFF.

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Section 4 Functional Description

4.1 General

This section provides a complete functional description of the LCD32F4B block, detailing the operation of the design from the end user perspective in a number of subsections.

4.1.1 LCD Driver Description

4.1.1.1 Frontplane, Backplane, and LCD System During Reset

During a reset the following conditions exist:

- The LCD32F4B system is configured in the default mode, 1/4 duty and 1/3 bias, that means all backplanes are used.

- All frontplane enable bits, FP[31:0]EN are cleared and the ON/OFF control for the display, the LCDEN bit is cleared, thereby forcing all frontplane and backplane driver outputs to the high impedance state. The MCU pin state during reset is defined by the port integration module (PIM).

4.1.1.2 LCD Clock and Frame Frequency

The frequency of the oscillator clock (OSCCLK) and divider determine the LCD Clock Frequency. The divider is set by the LCD Clock Prescaler bits, LCLK[2:0], in the LCD Control Register 0 (LCDCR0). Table **Table 4-1** shows the LCD clock and frame frequency for some multiplexed mode at OSCCLK = 16*MHz*, 8*MHz*, 4*MHz*, 2*MHz*, 1*MHz*, and 0.5*MHz*.

Table 4-1 LCD Clock and Frame Frequency

Oscillator frequency in MHz	LCD Clock Prescaler			Divider	LCD Clock Frequency [*Hz*]	Frame Frequency [*Hz*]			
	LCLK2	LCLK1	LCLK0			1/1 Duty	1/2 Duty	1/3 Duty	1/4 Duty
OSCCLK = 0.5	0	0	0	1024	488	488	244	163	122
	0	0	1	2048	244	244	122	81	61
OSCCLK = 1.0	0	0	1	2048	488	488	244	163	122
	0	1	0	4096	244	244	122	81	61
OSCCLK = 2.0	0	1	0	4096	488	488	244	163	122
	0	1	1	8192	244	244	122	81	61
OSCCLK = 4.0	0	1	1	8192	488	488	244	163	122
	1	0	0	16384	244	244	122	81	61
OSCCLK = 8.0	1	0	0	16384	488	488	244	163	122
	1	0	1	32768	244	244	122	81	61
OSCCLK = 16.0	1	1	0	65536	244	244	122	81	61
	1	1	1	131072	122	122	61	40	31

For other combinations of OSCCLK and Divider not shown in table **Table 4-1**, the following formula may be used to calculate the LCD frame frequency for each multiplex mode:

$$\text{LCD Frame Frequency (Hz)} = \left\lceil \frac{\text{OSCCLK (Hz)}}{\text{Divider}} \right\rceil \cdot \text{Duty}$$

The possible divider values are shown in **Table 4-1**.

4.1.1.3 LCD RAM

For a segment on the LCD to be displayed, data must be written to the LCD RAM which is shown in **Section 3** in this book. The 128 bits in the LCD RAM correspond to the 128 segments that are driven by the frontplane and backplane drivers. Writing a '1' to a given location will result in the corresponding display segment being driven with a differential RMS voltage necessary to turn the segment ON when the LCDEN bit is set and the corresponding FP[31:0]EN bit is set. Writing a '0' to a given location will result in the corresponding display segment being driven with a differential RMS voltage necessary to turn the segment OFF. The LCD RAM is a dual port RAM that interfaces with the internal address and data buses of the MCU. It is possible to read from LCD RAM locations for scrolling purposes. When LCDEN = 0, the LCD RAM can be used as on-chip RAM. Writing or reading of the LCDEN bit does not change the contents of the LCD RAM. After a reset, the LCD RAM contents will be indeterminate.

4.1.1.4 LCD Driver System Enable and Frontplane Enable Sequencing

If LCDEN = 0 (LCD32F4B Driver System disabled) and the frontplane enable bit, FP[31:0]EN, is set, the frontplane driver waveform will not appear on the output until LCDEN is set. If LCDEN = 1 (LCD32F4B Driver System enabled), the frontplane driver waveform will appear on the output as soon as the corresponding frontplane enable bit, FP[31:0]EN, in the registers FPENR0 – FPENR3 is set.

4.1.1.5 LCD Bias and Modes of Operation

The LCD32F4B driver has 5 modes of operation:

- 1/1 Duty (1 backplane), 1/1 Bias (2 voltage levels)
- 1/2 Duty (2 backplanes), 1/2 Bias (3 voltage levels)
- 1/2 Duty (2 backplanes), 1/3 Bias (4 voltage levels)
- 1/3 Duty (3 backplanes), 1/3 Bias (4 voltage levels)
- 1/4 Duty (4 backplanes), 1/3 Bias (4 voltage levels)

The voltage levels required for the different operating modes are generated internally based on VLCD. Changing VLCD alters the differential RMS voltage across the segments in the ON and OFF states, thereby setting the display contrast.

The backplane waveforms are continuous and repetitive every frame. They are fixed within each operating mode and are not affected by the data in the LCD RAM.

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The frontplane waveforms generated are dependent on the state (ON or OFF) of the LCD segments as defined in the LCD RAM. The LCD32F4B driver hardware uses the data in the LCD RAM to construct the frontplane waveform to create a differential RMS voltage necessary to turn the segment ON or OFF.

The LCD duty is decided by the DUTY1 and DUTY0 bits in the LCD Control Register 0 (LCDCR0). The number of bias voltage levels is determined by the BIAS bit in the LCDCR0. **Table 4-2** summarizes the Multiplex modes (duties) and the bias voltage levels that can be selected for each multiplex mode (duty). The backplane pins have their corresponding backplane waveform output BP[3:0] in high impedance state when in the OFF state as indicated in **Table 4-2**. In the OFF state the corresponding pins BP[3:0]can be used for other functionality, for example as general purpose I/O ports.

Table 4-2 LCD Duty and Bias

Duty	LCDCR0 Reg.		Backplanes				Bias (BIAS=0)			Bias (BIAS=1)		
	DUTY1	DUTY0	BP3	BP2	BP1	BP0	1/1	1/2	1/3	1/1	1/2	1/3
1/1	0	1	OFF	OFF	OFF	BP0	YES	NA	NA	YES	NA	NA
1/2	1	0	OFF	OFF	BP1	BP0	NA	YES	NA	NA	NA	YES
1/3	1	1	OFF	BP2	BP1	BP0	NA	NA	YES	NA	NA	YES
1/4	0	0	BP3	BP2	BP1	BP0	NA	NA	YES	NA	NA	YES

4.1.2 Operation in WAIT Mode

The LCD32F4B driver system operation during WAIT mode is controlled by the *LCD Stop in WAIT* (LCDSWAI) bit in the LCD Control Register 1 (LCDCR1). If LCDSWAI is reset, the LCD32F4B driver system continues to operate during WAIT mode. If LCDSWAI is set, the LCD32F4B driver system is turned off during WAIT mode. In this case the LCD waveform generation clocks are stopped and the LCD32F4B drivers pull down to VSSX those frontplane and backplane pins that were enabled before entering WAIT mode.The contents of the LCD RAM and the LCD registers retain the values they had prior to entering WAIT mode.

4.1.3 Operation in Pseudo STOP Mode

The LCD32F4B driver system operation during Pseudo STOP mode is controlled by the *LCD Run in Pseudo STOP* (LCDRPSTP) bit in the LCD Control Register 1 (LCDCR1). If LCDRPSTP is reset, the LCD32F4B driver system is turned off during Pseudo STOP mode. In this case the LCD waveform generation clocks are stopped and the LCD32F4B drivers pull down to VSSX those frontplane and backplane pins that were enabled before entering Pseudo Stop mode. If LCDRPSTP is set, the LCD32F4B driver system continues to operate during Pseudo STOP mode. The contents of the LCD RAM and the LCD registers retain the values they had prior to entering Pseudo STOP mode.

4.1.4 Operation in STOP Mode

All LCD32F4B driver system clocks are stopped, the LCD32F4B driver system pulls down to VSSX those frontplane and backplane pins that were enabled before entering STOP mode. Also, during STOP mode, the contents of the LCD RAM and the LCD registers retain the values they had prior to entering STOP

mode. As a result, after exiting from STOP mode, the LCD32F4B driver system clocks will run (if LCDEN = 1) and the frontplane and backplane pins retain the functionality they had prior to entering STOP mode.

4.1.5 LCD Waveform Examples

The following figures show the timing examples of the LCD output waveforms for the available modes of operation.

4.1.5.1 1/1 Duty Multiplexed with 1/1 Bias Mode

Duty = 1/1: DUTY1 = 0, DUTY0 = 1
Bias = 1/1: BIAS = 0 or BIAS = 1
$V_0 = V_1 = VSSX, V_2 = V_3 = VLCD$
- BP1, BP2, and BP3 are not used, a maximum of 32 segments are displayed.
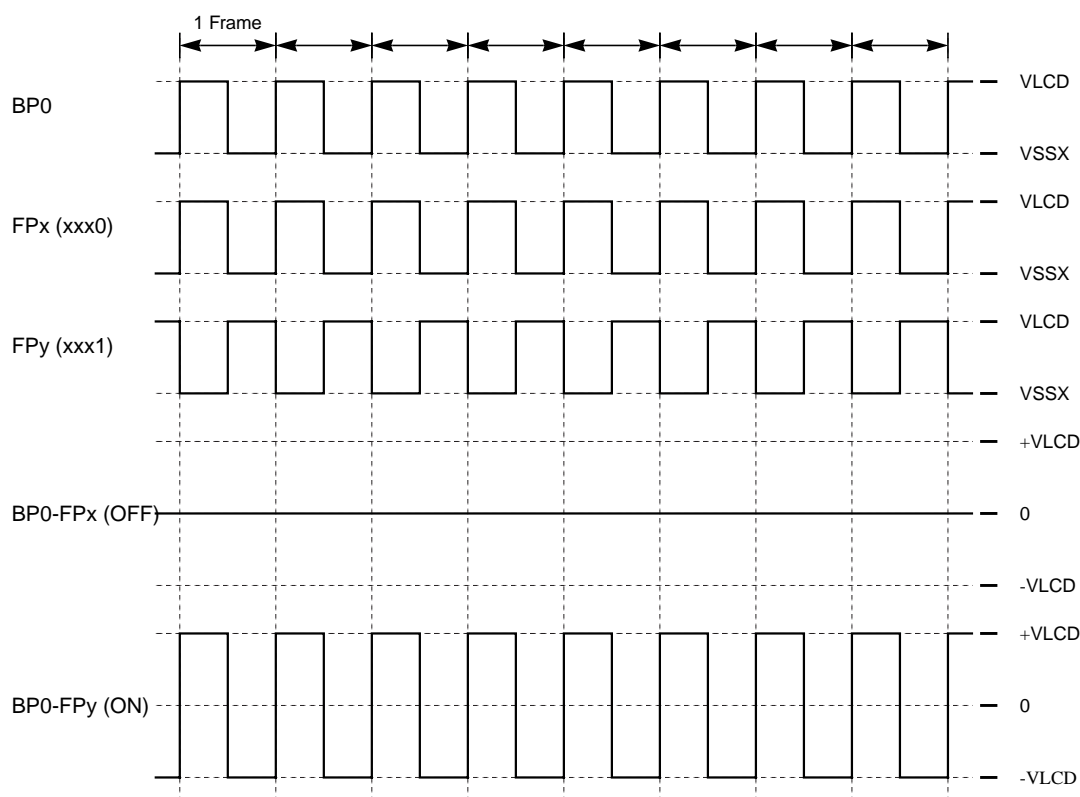
Figure 4-1 1/1 Duty and 1/1 Bias

4.1.5.2 1/2 Duty Multiplexed with 1/2 Bias Mode

Duty = 1/2: DUTY1 = 1, DUTY0 = 0

Bias = 1/2: BIAS = 0

V_0 = VSSX, V_1 = V_2 = VLCD * 1/2, V_3 = VLCD

- BP2 and BP3 are not used, a maximum of 64 segments are displayed.
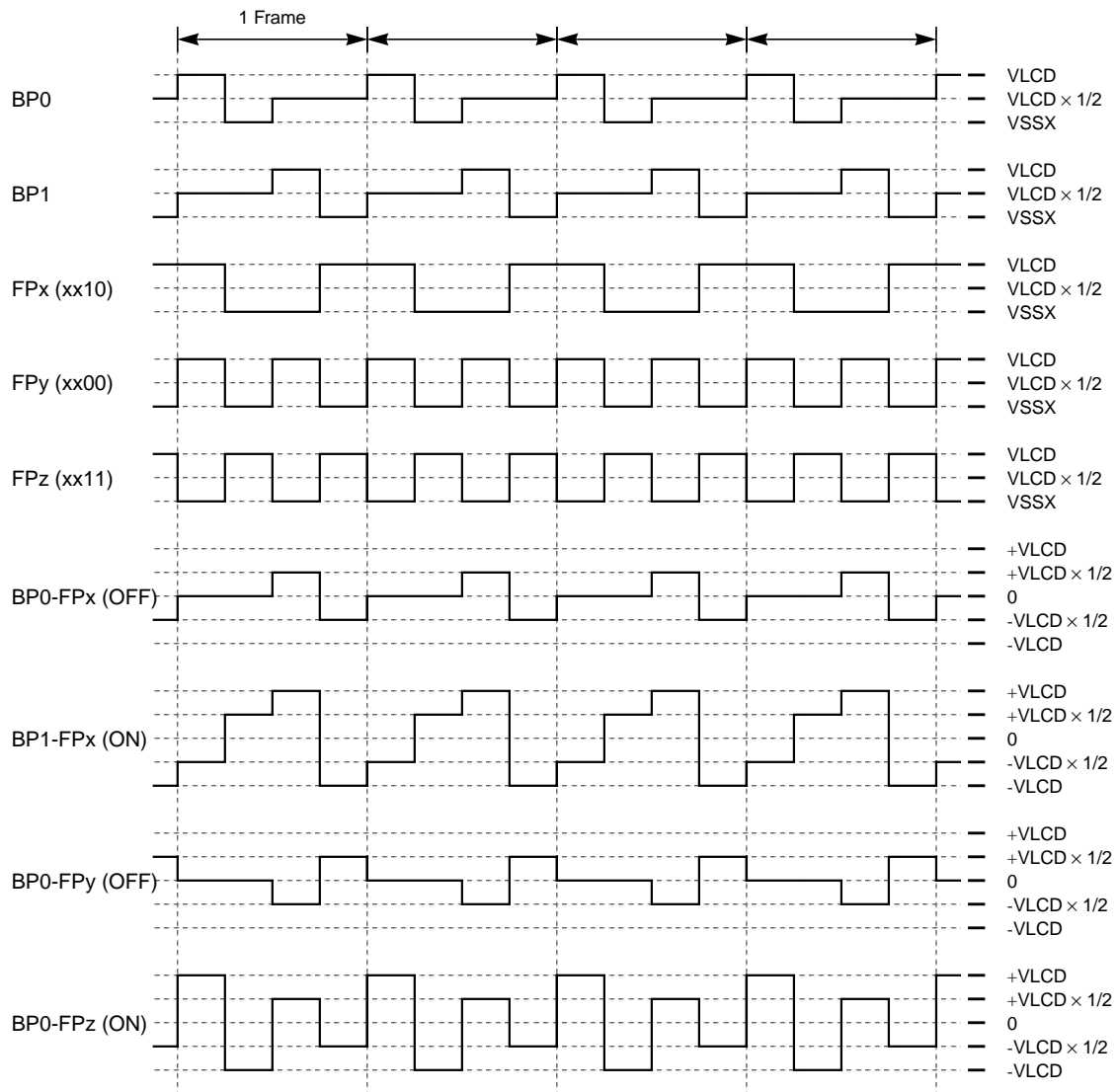

Figure 4-2 1/2 Duty and 1/2 Bias

4.1.5.3 1/2 Duty Multiplexed with 1/3 Bias Mode

Duty = 1/2: DUTY1 = 1, DUTY0 = 0

Bias = 1/3: BIAS = 1

V_0 = VSSX, V_1 = VLCD * 1/3, V_2 = VLCD * 2/3, V_3 = VLCD

- BP2 and BP3 are not used, a maximum of 64 segments are displayed.

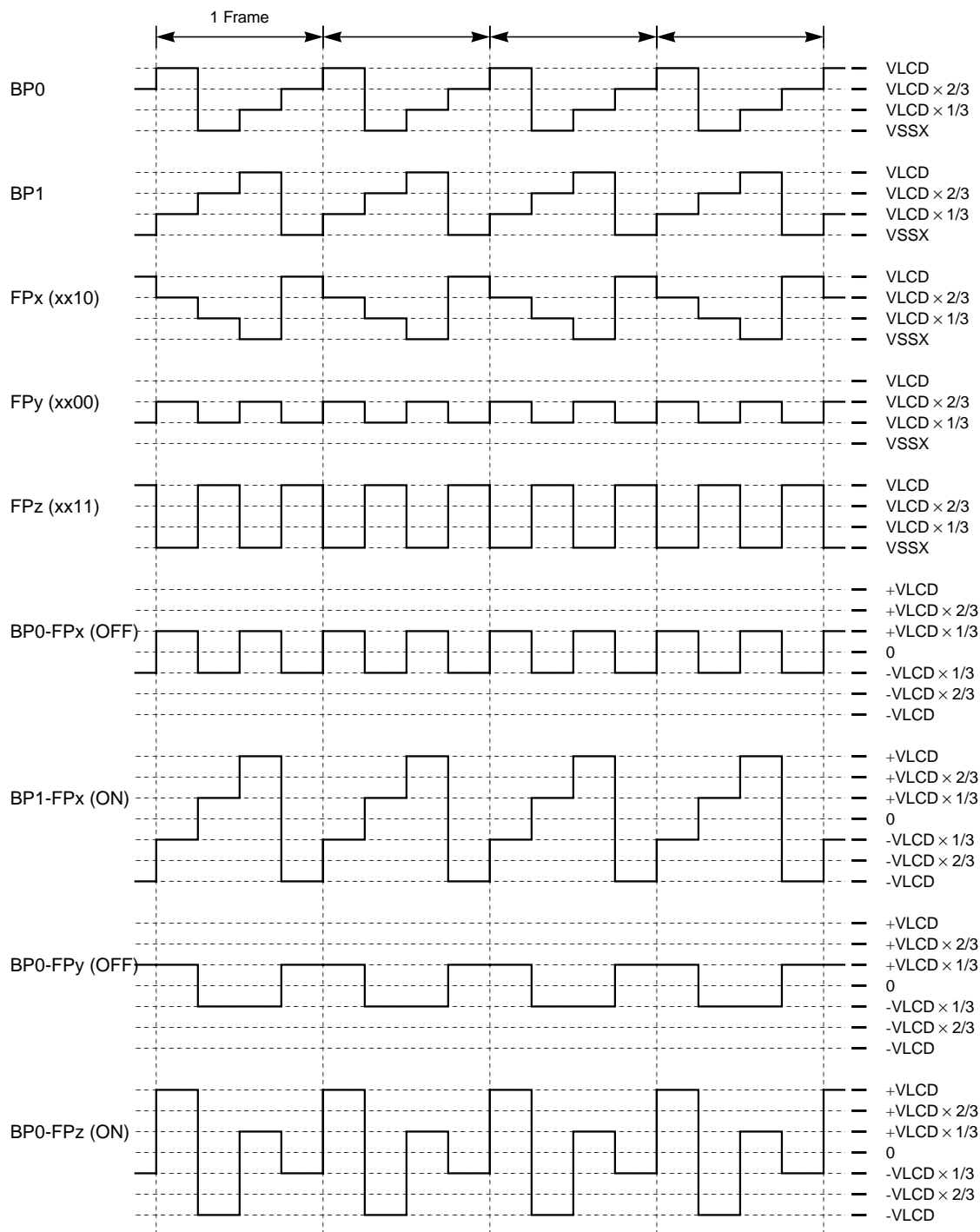**Figure 4-3 1/2 Duty and 1/3 Bias**

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4.1.5.4 1/3 Duty multiplexed with 1/3 Bias mode

Duty = 1/3: DUTY1 = 1, DUTY0 = 1

Bias = 1/3: BIAS = 0 or BIAS = 1

V_0 = VSSX, V_1 = VLCD * 1/3, V_2 = VLCD * 2/3, V_3 = VLCD

- BP3 is not used, a maximum of 96 segments are displayed.
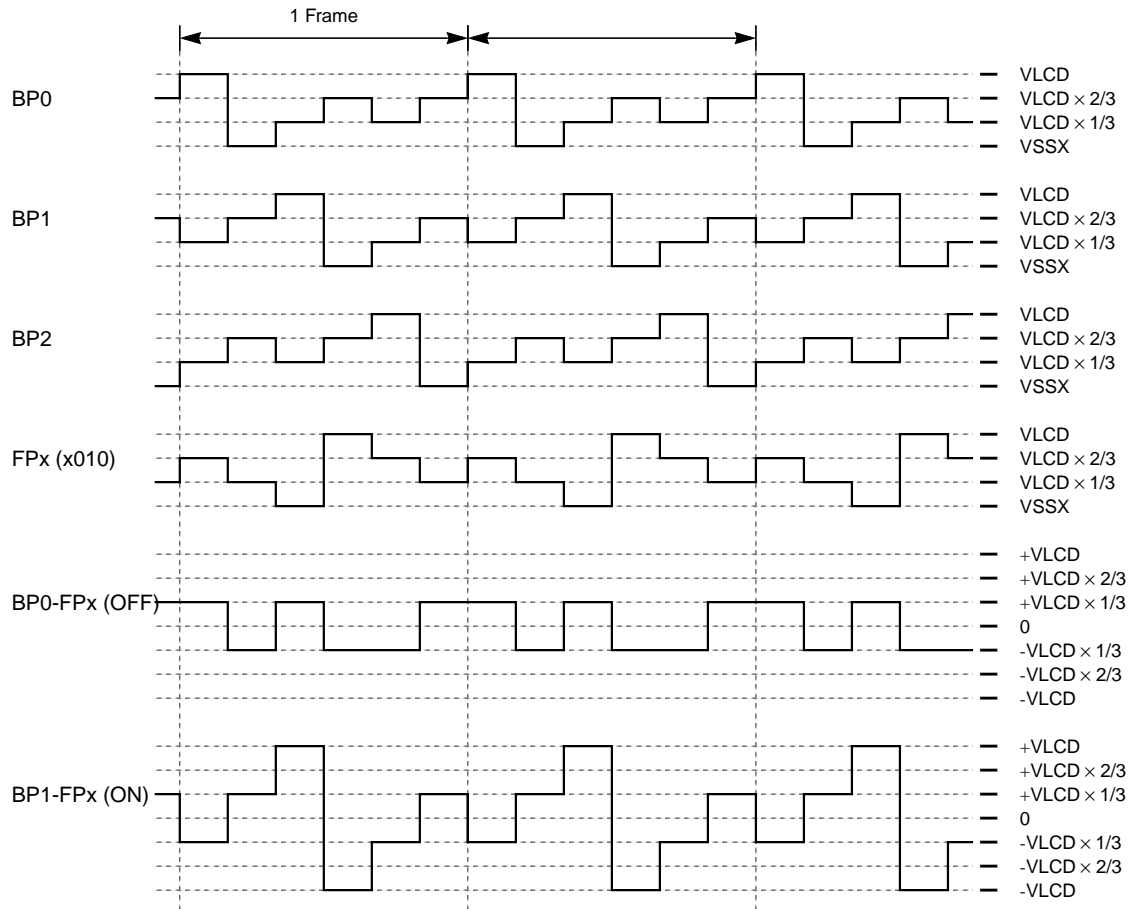

Figure 4-4 1/3 Duty and 1/3 Bias

4.1.5.5 1/4 Duty multiplexed with 1/3 Bias mode

Duty = 1/4: DUTY1 = 0, DUTY0 = 0
Bias = 1/3: BIAS = 0 or BIAS = 1
$\qquad$ V_0 = VSSX, V_1 = VLCD * 1/3, V_2 = VLCD * 2/3, V_3 = VLCD
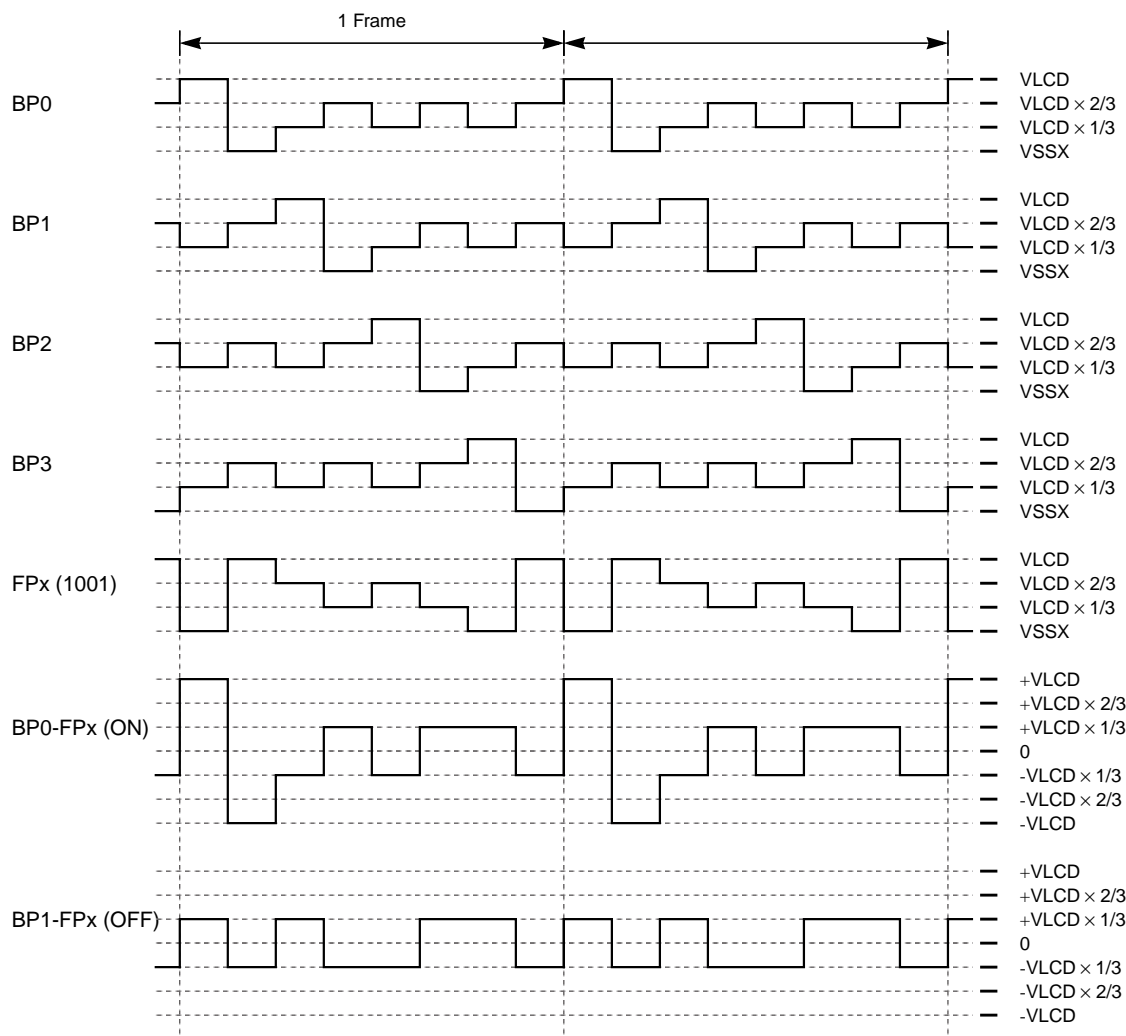- A maximum of 128 segments are displayed.

Figure 4-5 1/4 Duty and 1/3 Bias

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Section 5 Resets

5.1 General

The reset values of registers and signals are described in **Section 3 Memory Map and Registers**. The behavior of the LCD32F4B system during reset is described in **4.1.1 LCD Driver Description**.

Section 6 Interrupts

6.1 General

This module does not generate any interrupts.

User Guide End Sheet

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