HCS12 Compact Flash Host Controller (CFHC) Block Guide V01.09

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TSPG 8/16 Bit MCU
Freescale Semiconductor, Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V00.01	28 Nov., 2001	28 Nov., 2001	Todd Hung, Robin Then	Section 3 and 4.5 were initialized by Robin Then (R51557). Other sections were initialized by Todd Huang (R45781). At Suzhou design center.
V00.02	29 Nov., 2001	29 Nov., 2001	Todd Huang, Robin Chen	Updated the Section 3, and the 4.1.
V00.03	04 Dec., 2001	04 Dec., 2001	Todd Huang, Robin Chen	Updated after the BUG review with system/project team.
V01.00	17 Dec., 2001	17 Dec., 2001	Todd Huang, Robin Chen	1. Added the wait assertion error and programmable wait time out interrupt as system team required in. 2. Added the register to control the individual port enable signals of CA4~10 as system team required. 3. Removed the port information in table2-1 as integration team required. 4. Simplified the pin function description in table2-1. 5. Added the description of No $\overline{\text{IOIS16}}$ Assertion during Word Accesses. 6. Added the CDRS bit for selecting corresponding port for Card data bus routing as system team required. 7. Removed CRESET pin from the CFOE bit controlling list.
V01.01	18 Dec., 2001	18 Dec., 2001	Todd Huang, Robin Chen	1. Updated the **Table 4-6**. 2. In **4.1**, described valid byte for IPBI byte operation (P33). 3. In **4.2**, described valid byte at QUEUE bus for byte operation (P38).
V01.02	24 Dec., 2001	24 Dec., 2001	Todd Huang, Robin Chen	1. In **3.3.10**, made CIF writable, and updated CIF clearing method. 2. In **Section 2**, added the CVCC pin.
V01.03	8 Jan., 2002	8 Jan., 2002	Todd Huang, Robin Chen	1. In **3.3.4**, removed CDRS bit. 2. In **3.3.10**, added CHGIF bit will be reset when com=0.
V01.04	12 Mar., 2002	12 Mar., 2002	Todd Huang, Robin Chen	1. Updated the document number. 2, In **3.3.5**, revised description of the STOP bit and BSY bit. 3. In **3.3.10**, revised the reset description of the CFTEIF bit. 4. In **4.5**, updated **Table 4-8**,**Table 4-9**,**Table 4-10**,and **Figure 4-8**.
V01.05	10 May., 2002	10 May., 2002	Todd Huang, Robin Chen	1. In **3.3.1**, added "only sample card pins when CFHC is enabled and not in power saving mode". 2, In **3.3.5**, added "The bit HIS, STOP, INVOKE and RWB are only writable when CFHC is enabled and not in power saving mode". 3. In **3.3.6**, **3.3.7**, added "Only be writable when CFHC is enabled and not in power saving mode". 4. In **3.3.10**, added "The bit CIF is only writable when CFHC is enabled and not in power saving mode". 5. In **3.3.5**, added "No operation can be invoked during CF card in standby mode (both CE2B and CE1B are high)". 6. In **3.3.3** , removed **CF Interface Status Register (CFISR)** from CFE disable reset list. 7. Initialized application note in **5.2**.

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.06	14 April, 2003	18 April, 2003	Robin Chen	1. In **3.3.2** , added "In byte operation mode, the transmit byte must be stored at the MSB of CFDR. And receive byte can be read from MSB or LSB of CFDR. In word operation mode, the MSB of CFDR has even address and the LSB of CFDR has odd address." 2. In **Table 3-2**, added two columns "IDATA[15:8]" and "IDATA[7:0]". 3. In **Table 4-12**, changed the value of thREG(IORD) to 2. 4. In **Table 4-13**, changed the value of thREG(IOWR) to 2.
V01.07	6 May, 2003		Robin Chen	1. In **Table 4-10**, changed the value of tv(WT-OE) to 4. 2. In **Table 4-11**, changed the value of tv(WT-WE) to 4. 3. In **Table 4-12**, changed the value of tdfIOIS16(ADR) to 4, tdWT(IORD) to 4. 4. In **Table 4-13**, changed the value of tdfIOIS16(ADR) to 4, tdWT(IOWR) to 4.
V01.08	25 SEP 2003		Daniel Yu	Removed NDA message and POPI info
V01.09	05 NOV 2004		Wai-On Law	1. In **Table 2-1**,added corresponding CF interface names. 2. Replaced company logo.

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Preface

Content of the Block Guide is intended for re-use as reference material in customer documentation. This Block Guide must contain sufficient detail for an end customer to understand and use the block within a final System-on-a-Chip design.

Terminology

IP BUS: Semiconductor Reuse Standard Intellectual Proprietary Standard Bus (see SRS V3.0 IP Interface)

CF: Compact Flash

CFHC: Compact Flash Host Controller

INTF: Interface

CTRL: Controller

INT: Interrupt

GEN: Generator

FIFO: First In First Out Shift Register

QUEUE: A BUS Interface for Block Data Transfer between peripheral modules without intervention from CPU, some similar to DMA.

Conditional Text

No conditional text.

Section 1 Introduction

The block diagram of the CFHC module is shown in **Figure 1-1**

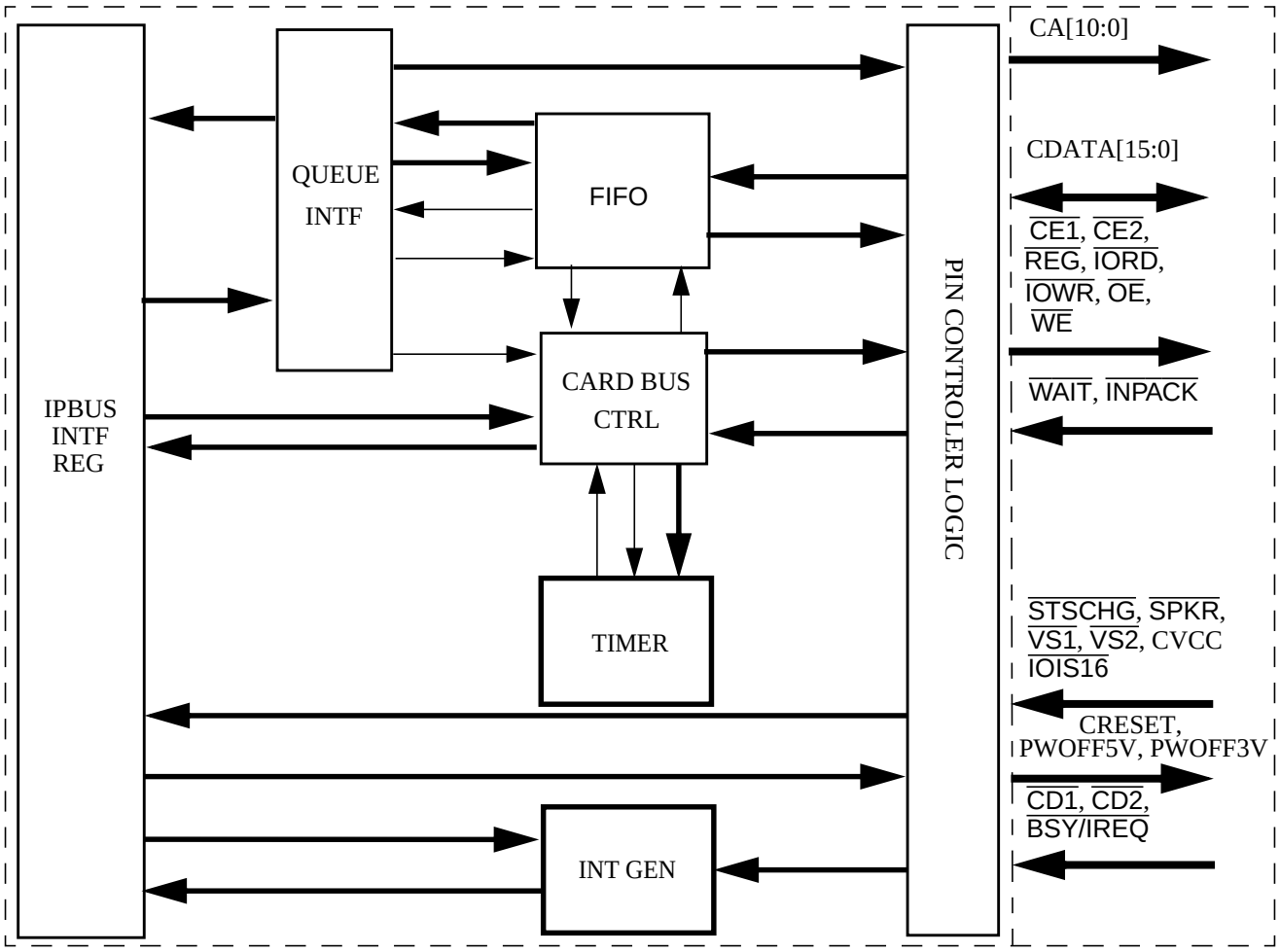

Figure 1-1 CFHC Block Diagram

1.1 Overview

This Compact Flash Host Controller module processes the data transfer between IPBI/Integrated Queue and CF/CF+ card.

1.2 Features

The CFHC module includes these distinctive features:

- Support PC Card Memory mode and PC Card IO mode (no ATA mode)
- Has QUEUE interface to support fast direct data transfer with other peripherals

- Has one 16 bits x 4 FIFO.
- Block data operation with block size up to 512 bytes.
- Software controlled power up/down sequence.
- Interrupts of Card detect/remove, card ready and IREQ.
- Card access timing/pins compatible with CF Spec v1.4.
- Up to 1K words (2K bytes) card address access.
- Two data paths (QUEUE and IP BUS) controllable by software.

1.3 Modes of Operation

The CFHC functions the same in normal, special, freeze, and emulation modes. It has three low power modes: disable mode in run mode, wait and stop modes.

- System Run Mode

  This is the basic mode of operation

  In run mode with the CFHC system enable (CFE) bit in the CFHC control register cleared, the CFHC system is in a low-power, disabled state. CFHC registers can still be accessed (not all can be written, please see **3.3 Register Descriptions** for detail information of each register), but clocks to the core of this module are disabled.

- System Wait Mode

  CFHC operation in wait mode depends upon the state of the CFSWAI bit in CFHC control register

  – If CFSWAI is cleared, the CFHC operates normally when the CPU is in system wait mode.

  – If CFSWAI is set, CFHC clock generation ceases and the CFHC module enters a power conservation state when the CPU is in wait mode. If CFSWAI is set, any card access in progress stops at wait mode entry. The transmission and reception resumes when the CFHC exits system wait mode.

- System Stop Mode

  The CFHC is inactive in system stop mode for reduced power consumption. The STOP instruction does not affect CFHC register states.

Section 2 External Signal Description

2.1 Overview

The CFHC has the following external signals, please See **Table 2-1**.

Table 2-1 Signal Properties

Name	Compact Flash Interface Names	Function	Reset State	Pull up
$\overline{\text{BSY/IREQ}}$	$\overline{\text{RDY/BSY}}$ $\overline{\text{IREQ}}$	Active Low input Card busy signal (PC Card Memory Mode), or Interrupt Request (PC Card I/O Mode)	—	Passive
CA[10:0]	A[10:0]	Card Address bus output	11'h000	—
$\overline{\text{CD1}}$, $\overline{\text{CD2}}$	-CD1, -CD2	Active Low input Card detect signals	—	Passive
CDATA[15:0]	D[15:0]	Bi-directional CF/CF+ card Data bus	—	—
$\overline{\text{CE1}}$, $\overline{\text{CE2}}$	-CE1, -CE2	Active Low output Card enable and byte select signals	2'b11	—
CRESET	RESET	Active High output Card reset signal	1'b1	—
CVCC	VCC	Active high input Socket powered up indication signal	—	Passive
$\overline{\text{INPACK}}$	-INPACK	Active Low input Input Acknowledge signal (PC Card I/O Mode)	—	Passive
$\overline{\text{IOIS16}}$	-IOIS16	Active Low input 16 bit indication signal (PC Card I/O Mode)	—	Passive
$\overline{\text{IORD}}$	-IORD	Active Low output I/O Read strobe signal (PC Card I/O Mode)	1'b1	—
$\overline{\text{IOWR}}$	-IOWR	Active Low output I/O Write strobe pulse (PC Card I/O Mode)	1'b1	—
$\overline{\text{OE}}$	-OE	Active Low output Output Enable strobe signal	1'b1	—
PWOFF5V		Active High output 5V Card power supply switch off signal	1'b1	—
PWOFF3V		Active High output 3.3V Card power supply switch off signal	1'b1	—
$\overline{\text{REG}}$	-REG	Active Low output. Attribute memory select signal (PC Card Memory Mode)	1'b1	—
$\overline{\text{SPKR}}$	-SPKR	Active Low input Binary Audio signal (PC Card I/O Mode)	—	Passive
$\overline{\text{STSCHG}}$	-STSCHG	Active Low input Card status change signal (PC Card I/O Mode)	—	Passive

Table 2-1 Signal Properties

Name	Compact Flash Interface Names	Function	Reset State	Pull up
$\overline{VS1}$, $\overline{VS2}$	-VS1, -VS2	Active Low input Voltage sense signals	—	Passive
$\overline{WAIT}$	-WAIT	Active Low input Card wait signal	—	Passive
$\overline{WE}$	-WE	Active Low output Card write enable signal	1’b1	—

2.2 Detailed Signal Descriptions

2.2.1 $\overline{BSY/IREQ}$

Active Low input.

In PC Card Memory Mode this signal is set high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up registor .

At power up and at Reset, the $\overline{BSY/IREQ}$ signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time. The $\overline{BSY/IREQ}$ signal is held high (disabled from being busy) whenever the following condition is true: The CompactFlash Storage Card or CF+ Card has been powered up with CRESET continuously disconnected or asserted.

In PC Card I/O Mode, after the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as Interrupt Request.This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. The pulse width must be wider than two QUEUE clock cycles.

2.2.2 CA[10:0]

Address bus output to CF/CF+ card.

In both PC Card Memory Mode and PC Card I/O Mode, these address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card, a byte in the card’s information structure and its configuration control and status registers.

In PC Card I/O Mode, this signal is the same as the PC Card Memory Mode signal.

The reset status are 11’h000.

2.2.3 $\overline{\text{CD1}}$, $\overline{\text{CD2}}$

Active Low input.

In both PC Card Memory Mode and PC Card I/O Mode, these Card Detect pins are connected to ground on the CompactFlash Storage Card or CF+ Card.They are used by the host to determine that the CompactFlash Storage Card or CF+ Card is fully inserted into its socket.

2.2.4 CDATA[15:0]

Bi-directional CF/CF+ card Data bus.

In both PC Card Memory Mode and PC Card I/O Mode, these lines carry the Data, Commands and Status information between the host and the controller. CDATA[0] is the LSB of the Even Byte of the Word. CDATA[8] is the LSB of the Odd Byte of the Word.

2.2.5 $\overline{\text{CE1}}$, $\overline{\text{CE2}}$

Active Low output.

In both PC Card Memory Mode and PC Card I/O Mode, these two output signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. $\overline{\text{CE2}}$ always accesses the odd byte of the word. $\overline{\text{CE1}}$ accesses the even byte or the odd byte of the word depending on CA[0] and $\overline{\text{CE2}}$. A multiplexing scheme based on CA[0], $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ allows 8 bit hosts to access all data on CDATA[7:0].

The reset status is 2’b11.

2.2.6 CRESET

Active High output.

In both PC Card Memory Mode and PC Card I/O Mode, when the pin is high, this signal resets the CompactFlash Storage Card or CF+ Card The CompactFlash Storage Card or CF+ Card is reset only at power up if this pin is left high or open from power-up.

The reset status is 1’b1.

2.2.7 CVCC

Active high input.

When high, indicate the CF/CF+ card socket has been powered up.

2.2.8 $\overline{\text{INPACK}}$

Active Low input.

In PC Card Memory Mode, this signal is asserted high.

In PC Card I/O Mode, the Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus.This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF+ Card and the CPU.

2.2.9 $\overline{\text{IOIS16}}$

Active Low input.

In PC Card Memory Mode, this signal is asserted high.

In PC Card I/O Mode, a Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.

2.2.10 $\overline{\text{IORD}}$

Active Low output.

This signal is not used in the PC Card Memory Mode.

In PC Card I/O Mode, this is an I/O Read strobe signal. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF+ Card when the card is configured to use the I/O interface.

The reset status is 1’b1.

2.2.11 $\overline{\text{IOWR}}$

Active Low output.

This signal is not used in the PC Card Memory Mode.

In PC Card I/O Mode, this I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is configured to use the I/O interface.

The reset value is 1’b1.

2.2.12 $\overline{\text{OE}}$

Active Low output.

This is an Output Enable strobe signal. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers.

The reset value is 1’b1.

2.2.13 PWOFF5V

Active High output.

Switch off 5V CompactFlash Storage Card or CF+ Card power supply.

The reset value is 1’b1.

2.2.14 PWOFF3V

Active High output.

Switch off 3.3V CompactFlash Storage Card or CF+ Card power supply.

The reset value is 1’b1.

2.2.15 $\overline{\text{REG}}$

Active Low output.

In PC Card Memory Mode, this signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.

In PC Card I/O Mode, this signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.

The reset value is 1’b1.

2.2.16 $\overline{\text{SPKR}}$

Active Low input.

In PC Card Memory Mode, this signal is asserted high.

In PC Card I/O Mode, this signal is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.

2.2.17 $\overline{\text{STSCHG}}$

Active Low input.

In PC Card Memory Mode, this signal is asserted high.

In PC Card I/O Mode, this signal is asserted low to alert the host to changes in the RDY/$\overline{\text{BSY}}$ and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Configure and Status Register.

2.2.18 $\overline{\text{VS1}}$, $\overline{\text{VS2}}$

Active Low input.

The $\overline{\text{VS1}}$ is grounded so that the CompactFlash Storage Card or CF+ Card CIS can be read at 3.3 volts and $\overline{\text{VS2}}$ is reserved by PCMCIA for a secondary voltage.

2.2.19 $\overline{\text{WAIT}}$

Active Low input.

In both PC Card Memory Mode and PC Card I/O Mode, this signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.

2.2.20 $\overline{\text{WE}}$

Active Low output.

In the PC Card Memory Mode, this is used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ Card when the card is configured in the memory interface mode.It is also used for writing the configuration registers.

In PC Card I/O Mode, this signal is used for writing the configuration registers.

The reset status is 1’b1.

Section 3 Memory Map and Registers

3.1 Overview

This section provides a detailed description of all memory and registers for the CFHC module.

3.2 Module Memory Map

The memory map for the CFHC module is given below in **Table 3-1**. The Address listed for each register is the address offset.The actual address for each register is the sum of the base address for the CFHC module and the address offset for each register.

Table 3-1 Module Memory Map

Address	Use	Access
Base Address + $00	**CF Interface Status Register (CFISR)**	Read
Base Address + $02	**CF Card Configuration Register (CFCCR)**	Read/Write
Base Address + $04	**CF Status and Control Register 1 (CFSCR1)**	Read/Write
Base Address + $06	**CF Status and Control Register 2 (CFSCR2)**	Read/Write
Base Address + $08	**CF Command Register (CFCR)**	Read/Write
Base Address + $0A	**CF Block Base Address Register (CFBBAR)**	Read/Write
Base Address + $0C	**CF Block Size Register (CFBSR)**	Read/Write
Base Address + $0E	**CF Power Management Register (CFPMR)**	Read/Write
Base Address + $10	**CF Data Register (CFDR)**	Read/Write
Base Address + $12	**CF Interrupt Flag Register (CFIFR)**	Read

3.3 Register Descriptions

This section consists of register descriptions in address orderEach description includes a standard register diagram with an associated figure number Details of register bit and field function follow the register diagrams, in bit order.

3.3.1 CF Interface Status Register

Register address: Base Address + $00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	VCC	CWAIT	INPACK	VS	RDY	IOIS16	CD2	CD1	SPKRB	CHG
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

= Unimplemented or Reserved

Figure 3-1 CF Interface Status Register (CFISR)

Read only register, only sample card pins when CFHC is enabled and not in power saving mode.

CHG — State Change

Complement of the logic level of CF/CF+ card pin46 ($\overline{\text{STSCHG}}$).

1 = Alert the changes in $\overline{\text{STSCHG}}$ and write protect states in I/O mode.

0 = Card is in memory mode or states of $\overline{\text{STSCHG}}$ and write protect are not changed in I/O mode.

SPKRB — Binary Audio Output

This bit presents the logic level of CF/CF+ card pin45 ($\overline{\text{SPKR}}$). For memory card this bit is high. For I/O card, this bit is the Binary Audio Output from card If the card does not support the Binary Audio function, this bit will be low

CD1 — Card Detect 1

Complement of the logic level of the $\overline{\text{CD1}}$ signal.

1 = Card is detected in socket.

0 = Card is not detected in socket.

CD2 — Card Detect 2

Complement of the logic level of the $\overline{\text{CD2}}$ signal.

1 = Card is detected in socket.

0 = Card is not detected in socket.

IOIS16 — 16 bit I/O Port Select

Complement of the logic level of CF/CF+ card pin24 ($\overline{\text{IOIS16}}$) when COM bit of **CF Card Configuration Register (CFCCR)** is high. If COM bit of **CF Card Configuration Register (CFCCR)** is low, this bit will be cleared.

1 = Card is in memory mode or permits 16 bit I/O port function in I/O mode.

0 = 16 bit I/O port function is not allowed.

RDY — Card Ready

This bit presents the logic level of CF pin37 ($\overline{\text{BSY/IREQ}}$) when COM bit of **CF Card Configuration Register (CFCCR)** is low. If COM bit of **CF Card Configuration Register (CFCCR)** is high, this bit will be cleared.

1 = Card is ready.
0 = Card is busy.

VS — Voltage Sense

Complement of the logic value of CF/CF+ card pin33 ($\overline{\text{VS1}}$).

1 = CF/CF+ card CIS can be read at 3.3 volts.
0 = CF/CF+ card CIS can't be read at 3.3 volts.

INPACK — Input Acknowledge

Not valid in memory mode. Complement of the logic level of CF/CF+ card pin43 ($\overline{\text{INPACK}}$).

1 = Card is select and responding to an I/O read cycle.
0 = I/O read cycle is not acknowledged.

CWAIT — Bus Cycle Wait

This bit is used to delay completion of the memory or I/O cycle in progress Complement of the logic level of CF/CF+ card pin42 ($\overline{\text{WAIT}}$).

1 = Host must extends the length of an input cycle.
0 = No cycle extension needed.

VCC — Card Power Supply

This bit is used to indicate whether socket has powered up or not.

1 = Socket is powered up.
0 = Socket is not powered up.

3.3.2 CF Card Configuration Register

Register address: Base Address + $02

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	0	CE2B	CE1B	REGB	COM
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

= Unimplemented or Reserved

Figure 3-2 CF Card Configuration Register (CFCCR)

Read at any time. Can be written only when BSY bit of **CF Command Register (CFCR)** is low.

COM — Card Operation Mode

The bit is used to determine the card operation mode: Memory mode or I/O mode.

1 = Card operated in I/O mode.

0 = Card operated in memory mode.

REGB — Attribute Memory Select

This bit is used during memory cycles to distinguish between common memory and register (Attribute) memory accesses. This bit must also be cleared during I/O cycles when the I/O address is on the bus.

1 = Common memory accesses during memory cycles.

0 = Register accesses during memory cycles or card accesses during I/O cycles.

CE2B~CE1B — Card Enable

These bits are used both to select the card and to indicate the card whether a byte or a word operation is being performed CE2B always accesses the odd byte of the word CE1B accesses the even byte or the odd byte of the word depending on CA0(LSB of address bus to card) and CE2B. A multiplexing scheme based on CA0, CE1B, CE2B allows host to access all data on CDATA[15:0]. See **Table 3-2**.

Table 3-2 Multiplexing Scheme

Function Code	CE2B	CE1B	CA0	CDATA[15:8]	CDATA[7:0]	IDATA[15:8]	IDATA[7:0]
Standby Mode	1	1	X	High Z	High Z	Not Valid	Not Valid
Byte Read	1	0	0	High Z	Even Byte	Even Byte	Even Byte
	1	0	1	High Z	Odd Byte	Odd Byte	Odd Byte
	0	1	X	Odd Byte	High Z	Odd Byte	Odd Byte
Byte Write	1	0	0	Don’t Care	Even Byte	Even Byte	Don’t Care
	1	0	1	Don’t Care	Odd Byte	Odd Byte	Don’t Care
	0	1	X	Odd Byte	Don’t Care	Odd Byte	Don’t Care
Word Read*	0	0	X	Odd Byte	Even Byte	Even Byte	Odd Byte
Word Write*	0	0	X	Odd Byte	Even Byte	Even Byte	Odd Byte

**Attribute memory is limited to 8-bit wide accesses only at even addresses, so in 16-bit accesses the odd byte is not valid.*

Note: Where the CDATA[15:0] means CF/CF+ Card Data Bus. Where IDATA[15:0] means **CF Data Register (CFDR)** or QUEUE INTF Data Bus depending on HIS bit of **CF Command Register (CFCR)**.

3.3.3 CF Status and Control Register 1

Register address: Base Address + $04

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	CFE	CFOE	CRST	DIS-INC	CF-SWAI	IEDGE	WERRIE	TER-RIE	CFR-FIE	CFTEIE	OOIE	CIE	VSIE	RDYIE	CHGIE	CDIE
RESET:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-3 CF Status and Control Register 1 (CFSCR1)

Can be read and written at any time.

CDIE — Card Detect Interrupt Enable

This read/write bit enables the CPU interrupt generated by CDIF bit of **CF Interrupt Flag Register (CFIFR)**.

1 = Interrupt from $\overline{CD1}$ or $\overline{CD2}$ is enabled.
0 = Interrupt from $\overline{CD1}$ or $\overline{CD2}$ is disabled.

CHGIE — Card State Change Interrupt Enable

This read/write bit enables the CPU interrupt generated by CHGIF bit of **CF Interrupt Flag Register (CFIFR)**.

1 = Interrupt from the $\overline{STSCHG}$ is enabled.
0 = Interrupt from the $\overline{STSCHG}$ is disabled.

RDYIE — Card RDY/$\overline{BSY}$ Interrupt Enable

This read/write bit enables the CPU interrupt generated by RDYIF bit of **CF Interrupt Flag Register (CFIFR)**.

1 = Interrupt from $\overline{BSY/IREQ}$ is enabled.
0 = Interrupt from the $\overline{BSY/IREQ}$ is disabled.

VSIE — Voltage Sense Interrupt Enable

This read/write bit enables the CPU interrupt generated by VSIF bit of **CF Interrupt Flag Register (CFIFR)**.

1 = Interrupt from VSIF is enabled.
0 = Interrupt from VSIF is disabled.

CIE — Card Interrupt Enable

This read/write bit enables the CPU interrupt generated by CIF bit of **CF Interrupt Flag Register (CFIFR)**.

1 = Interrupt from the CF/CF+ card is enabled.

0 = Interrupt from the CF/CF+ card is disabled.

OOIE — Operation Over Interrupt Enable

This read/write bit enables the CPU interrupt generated by OOIF bit of **CF Interrupt Flag Register (CFIFR)**.

1 = OOIF interrupt is enabled.
0 = OOIF interrupt is disabled.

CFTEIE — CF Transmit Interrupt Enable

This read/write bit enables CPU interrupt requests generated by the CFTEIF bit of **CF Interrupt Flag Register (CFIFR)**.

1 = CFTEIF interrupt is enabled.
0 = CFTEIF interrupt is disabled.

CFRFIE — CF Receive Interrupt Enable

This read/write bit enables CPU interrupt requests generated by the CFRFIF bit of **CF Interrupt Flag Register (CFIFR)**.

1 = CFRFIF interrupt is enabled.
0 = CFRFIF interrupt is disabled.

TERRIE — Time-out Error Interrupt Enable

This read/write bit enables CPU interrupt requests generated by the TERRIF bit of **CF Interrupt Flag Register (CFIFR)**.

1 = TERRIF interrupt is enabled.
0 = TERRIF interrupt is disabled.

WERRIE — Wait Assertion Error Interrupt Enable

This read/write bit enables CPU interrupt requests generated by the WERRIF bit of **CF Interrupt Flag Register (CFIFR)**.

1 = WERRIF interrupt is enabled.
0 = WERRIF interrupt is disabled.

IEDGE — Interrupt Edge Select

This bit specifies the triggering edge of card $\overline{\text{BSY/IREQ}}$ pin for interrupt generation when COM bit of **CF Card Configuration Register (CFCCR)** is cleared.

1 = RDYIF bit will be set by rising edge of $\overline{\text{BSY/IREQ}}$ pin when COM bit of **CF Card Configuration Register (CFCCR)** is cleared.
0 = RDYIF bit will be set by falling edge of $\overline{\text{BSY/IREQ}}$ pin when COM bit of **CF Card Configuration Register (CFCCR)** is cleared.

CFSWAI — CF Module Stop in Wait Mode

This bit is used for power conservation in wait mode. When CF module is stopped, the I/O registers can be accessed by CPU, but any data transfer between Queue controller and CF/CF+ card will be paused.Any other registers in CF module will freeze.

1 = CF module is stopped when in system wait mode.
0 = CF module operates normally in system wait mode.

DISINC — Disable increase of **CF Block Base Address Register (CFBBAR)**

This read/write is used to control the increase of the register **CF Block Base Address Register (CFBBAR)**.When this bit is set, the register CFBBAR will not be increased every card read/write cycle.

1 = Disable increase of the register CFBBAR.
0 = Enable increase of the register CFBBAR.

CRST — Card Reset

This bit resets CF/CF+ card.

1 = Hard reset to Card.
0 = No reset to Card.

CFOE — CF Output Enable

This bit only affect the output signals, but not internal state.

1 = Output to CF/CF+ card is enabled.
0 = Output to CF/CF+ card is disabled. $\overline{CE1}$, $\overline{CE2}$, $\overline{REG}$, $\overline{IORD}$, $\overline{IOWR}$, $\overline{OE}$, $\overline{WE}$, and CA[10:0] are tri-stated.

CFE — CFHC system Enable

This bit enables the CFHC system and dedicates the CFHC port pins to CFHC system functions.

1 = The CF module is enabled.
0 = The module is disabled. The interface is held in reset but registers can still be accessed. BSY, STOP, TQ, RQ and INVOKE bit of**CF Command Register (CFCR)**, **CF Block Size Register (CFBSR)**, **CF Interrupt Flag Register (CFIFR)** and internal state machine, timer and FIFO will be reset and idled. Multi functional I/O ports will be released from the CFHC for other function.

3.3.4 CF Status and Control Register 2

Register address: Base Address + $06

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CA10E	CA9E	CA8E	CA7E	CA6E	CA5E	CA4E	0	0	0	TPS5-TPS0					
W																
RESET:	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1	1

= Unimplemented or Reserved

Figure 3-4 CF Status and Control Register 2 (CFSCR2)

Can be read and written at any time.

TPS5-TPS0 — Time-out Period Select

These six bits are used to select the period of wait time out in 50ns(3 periods of QUEUE clock) steps when CFHC accesses common memory or I/O port of CF/CF+ card.The max period of wait time out is 3000ns (180 periods of QUEUE clock). The min period of wait time out is 50ns. Detailed values are shown in **Table 3-3**.

Table 3-3 TPS Values

Values of TPS (TPS5-TPS0)	The Width of Wait Time Out (ns)
000000	50
000001	100
000010	150
000011	200
...	...
111000	2850
111001	2900
111010	2950
111011	3000
1111xx	3000

CA4E — Card Address Bit 4 Port Enable

This read/write is used to enable the port for card address bit 4.

1 = Port for card address bit 4 is enabled when CFOE and CFE of **CF Status and Control Register 1 (CFSCR1)** is set.

0 = Port for card address bit 4 is disabled.

CA5E — Card Address Bit 5 Port Enable

This read/write is used to enable the port for card address bit 5.

1 = Port for card address bit 5 is enabled when CFOE and CFE of **CF Status and Control Register 1 (CFSCR1)** is set.

0 = Port for card address bit 5 is disabled.

CA6E — Card Address Bit 6 Port Enable

This read/write is used to enable the port for card address bit 6.

1 = Port for card address bit 6 is enabled when CFOE and CFE of **CF Status and Control Register 1 (CFSCR1)** is set.

0 = Port for card address bit 6 is disabled.

CA7E — Card Address Bit 7 Port Enable

This read/write is used to enable the port for card address bit 7.

1 = Port for card address bit 7 is enabled when CFOE and CFE of **CF Status and Control Register 1 (CFSCR1)** is set.

0 = Port for card address bit 7 is disabled.

CA8E — Card Address Bit 8 Port Enable

This read/write is used to enable the port for card address bit 8.

1 = Port for card address bit 8 is enabled when CFOE and CFE of **CF Status and Control Register 1 (CFSCR1)** is set.
0 = Port for card address bit 8 is disabled.

CA9E — Card Address Bit 9 Port Enable

This read/write is used to enable the port for card address bit 9.
1 = Port for card address bit 9 is enabled when CFOE and CFE of **CF Status and Control Register 1 (CFSCR1)** is set.
0 = Port for card address bit 9 is disabled.

CA10E — Card Address Bit 10 Port Enable

This read/write is used to enable the port for card address bit 10.
1 = Port for card address bit 10 is enabled when CFOE and CFE of **CF Status and Control Register 1 (CFSCR1)** is set.
0 = Port for card address bit 10 is disabled.

3.3.5 CF Command Register

Register address: Base Address + $08

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	HIS	BSY	0	TQ	RQ	STOP	0	RWB
W															INVOKE	
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-5 CF Command Register (CFCR)

Read at any time. The bit of HIS, STOP, INVOKE and RWB are only writable when CFHC is enabled and not in power saving mode with the restriction of the BSY bit status.

RWB — Read Operation or Write Operation

This bit indicates the operation to be performed is reading data from card or writing data to card. This bit can only be written when BSY = 0.
1 = Read accesses.
0 = Write accesses.

INVOKE — Operation Invoked

No operation can be invoked during CF card in standby mode (both CE2B and CE1B are high). This bit is used to start a read or write operation.This bit can only be set when BSY = 0, and will be cleared after the BSY bit is set, no operation can be invoked during CF card in standby mode (both CE2B and CE1B is high). Writing one to the INVOKE bit as the BSY bit is set will be ignored. This bit will be always read back as 0.

1 = Invoke operation.
0 = Not invoke new operation.

STOP — STOP Operation

Setting this bit will reset the BSY (after STOP operation), TQ and RQ of **CF Command Register (CFCR)**, reset the CFTEIF and CFRFIF of **CF Interrupt Flag Register (CFIFR)**, and **CF Block Size Register (CFBSR)**, and the internal state machine, timer and FIFO will be reset and idled after the current CF/CF+ Card read/writing cycle has been completed. This bit only can be set when BSY =1. This bit will be cleared after STOP operation completed, also software can clear this bit.

1 = Operation disabled.
0 = Operation enabled.

RQ — Reception Request (reserved bit for internal use)

When CFHC module is ready to receive data from Queue Controller, this bit will be set to indicate a reception request to the Queue Controller is generated.

1 = A new reception request generated.
0 = No new reception request.

TQ — Transmission Request (reserved bit for internal use)

When CF module is ready to transmit data to Queue Controller, this bit will be set to indicate a transmission request to the Queue Controller is generated.

1 = A new transmission request generated.
0 = No new transmission request.

BSY — CF Module Busy

This bit is used to indicate card accesses are in progress. Whenever a new operation is invoked, this bit will be set, and will be cleared when operation is completed or operation is stopped, or CFE of **CF Status and Control Register 1 (CFSCR1)** is cleared.

1 = Card access is in progress in CF module.
0 = No card access in CF module.

HIS — Host Interface Select

This bit is used to select the host interface that talks with CF/CF+ card. This bit can only be written when BSY = 0.

1 = Queue Controller.
0 = IPBUS.

3.3.6 CF Block Base Address Register

Register address: Base Address + $0A

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	BBA10-BBA0										
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-6 CF Block Base Address Register (CFBBAR)

Read at any time.

BBA10-BBA0 — Block Base Address

These eleven bits present the starting address of a block space to be accessed. This register must be initialized before a new operation is invoked. During a read or write operation this register is increased by 1 (byte operation) or by 2 (word operation or Attribute memory access) every read or write cycle. This register will be cleared when system reset. In word operation mode, the LSB (BBA0) of this register is ignored. This register can only be written when BSY bit of the **CF Command Register (CFCR)** is low, while CFHC is enabled and not in power saving mode.

3.3.7 CF Block Size Register

Register address: Base Address + $0C

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W								BS8-BS0								
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-7 CF Block Size Register (CFBSR)

BS8-BS0 — Block Size in byte

These nine bits present the size of a block space in byte (block size = CFBSR + 1 for byte operation, block size = CFBSR + 2 for word operation) to be accessed. BS0 will be ignored for word operation. During a read or write operation this register is decreased by 1 (byte operation) or by 2 (word operation

or Attribute memory access) in every read or write cycle until last read/write cycle completed (CFBSR=0). This Register will be cleared when system is reset, CF module is disabled, STOP is set, or a read/write operation is completed. This register can only be written when BSY of the **CF Command Register (CFCR)** = 0 while CFHC is enabled and not in power saving mode, and will be always read back as 0.

3.3.8 CF Power Management Register

Register address: Base Address + $0E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CPE	CVS
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-8 CF Power Management Register (CFPMR)

Can be read at any time.CPE bit can be written at any time.

CVS — Card Voltage Select

This bit is used to switch the power supply of socket. This bit can only be written when CPE=0.
1 = VCC for CF/CF+ card is 5v.
0 = VCC for CF/CF+ card is 3.3v.

CPE — Card Power Enable

This bit is used to enable the power of socket.
1 = Power to the socket is enabled.
0 = Power to the socket is disabled.

3.3.9 CF Data Register

Register address: Base Address + $10

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	RD15-RD0															
W	TD15-TD0															
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-9 CF Data Register (CFDR)

RD15-RD0/TD15-TD0 — Receive/Transmit Data Bit

Should be accessed properly together with the CFRFIF and CFTEIF bit of **CF Interrupt Flag Register (CFIFR)**. The CF data register consists of the read-only receive data register and the write-only transmit data register. Writing to the CF data register writes data into the transmit data register. Reading the CF data register reads data from the receive data register. The transmit data and receive data registers are separate registers that can contain different values. In byte operation mode, the transmit byte must be stored at the MSB of **CF Data Register (CFDR)**. And receive byte can be read from MSB or LSB of **CF Data Register (CFDR)**. In word operation mode, the MSB of **CF Data Register (CFDR)** has even address and the LSB of **CF Data Register (CFDR)** has odd address. When HIS of the **CF Command Register (CFCR)** is high, writing to this address is ignored, reading this address will get unexpected value.

3.3.10 CF Interrupt Flag Register

Register address: Base Address + $12

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	WERRIF	TERRIF	CFRFIF	CFTEIF	OOIF	CIF	VSIF	RDYIF	CHGIF	CDIF
W												0				
RESET:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-10 CF Interrupt Flag Register (CFIFR)

Can be read at any time.

CDIF — Card Detect Interrupt Flag

State change in $\overline{CD1}$ or $\overline{CD2}$ will set this bit. That is, the rising edge or falling edge of $\overline{CD1}$ or $\overline{CD2}$ will set this bit. This bit is cleared 1) by reading the CFIFR register with this bit set followed by reading the CFISR; 2) by reset; or 3) when CFE = 0. Setting this bit will generate an interrupt when CDIE of **CF Status and Control Register 1 (CFSCR1)** is high.

1 = State change in $\overline{CD1}$ or $\overline{CD2}$.
0 = No state change in $\overline{CD1}$ or $\overline{CD2}$.

CHGIF — Card State Change Interrupt Flag

Falling edge of $\overline{STSCHG}$ will set this bit. This bit is cleared 1) by reading the CFIFR register with this bit set followed by reading the CFISR register; 2) by reset; 3) COM = 0; or 4) when CFE = 0. Setting this bit will generate an interrupt when CHGIE of **CF Status and Control Register 1 (CFSCR1)** is high.

1 = $\overline{STSCHG}$ states change when COM = 1.
0 = $\overline{STSCHG}$ states do not change or when COM = 1.

RDYIF — Card Ready Interrupt Flag

This bit is set by the falling edge or rising edge (configured by the IEDGE bit of CFSCR1) of the signal $\overline{\text{BSY/IREQ}}$ when memory mode is configured (COM = 0). This bit is cleared 1) by reading the CFIFR register with this bit set, followed by read the CFISR register; 2) by reset; 3) COM = 1; or 4) when CFE = 0. Setting this bit will generate an interrupt when RDYIE of **CF Status and Control Register 1 (CFSCR1)** is high.

1 = State changes in $\overline{\text{BSY/IREQ}}$ when COM = 0.
0 = No state changes in $\overline{\text{BSY/IREQ}}$ or when COM = 0.

VSIF — Voltage Sense Interrupt Flag

This bit is set by the falling edge or rising edge of the signal $\overline{\text{VS1}}$. This bit is cleared 1) by reading the CFIFR register with this bit set, followed by reading the CFISR; 2) by reset; or 3) when CFE = 0. Setting this bit will generate an interrupt when VSIE of **CF Status and Control Register 1 (CFSCR1)** is high.

1 = State changes in $\overline{\text{VS1}}$.
0 = No state changes in $\overline{\text{VS1}}$.

OOIF — Operation Over Interrupt Flag

This bit will be set when a reading/writing operation completed. This bit is cleared 1) by reading the CFIFR register with this bit set, followed by reading the CFCR register; 2) by reset; or 3) when CFE = 0. Setting this bit will generate an interrupt when OOIE of **CF Status and Control Register 1 (CFSCR1)** is high.

1 = Operation completes.
0 = Operation does not complete or there is no operation.

CIF — Card Hard Interrupt Flag

The CIF bit is only writable when CFHC is enabled and not in power saving mode with value of zero.

This bit will be set while interrupt is asserted from the $\overline{\text{BSY/IREQ}}$ pin when COM = 1. This bit is cleared 1) by writing 0 to CIF bit; 2) by reset; 3) COM = 0; or 4) when CFE = 0. Setting this bit will generate an interrupt when CIE of **CF Status and Control Register 1 (CFSCR1)** is high.

1 = Card Hard Interrupt by $\overline{\text{BSY/IREQ}}$ pin when COM = 1.
0 = No Card Hard Interrupt by $\overline{\text{BSY/IREQ}}$ pin or when COM = 1.

CFTEIF — CF Transmit Data Register Empty Interrupt Flag

This bit is set when there is room in the transmit data register (**CF Data Register (CFDR)**). CFIFR must be read with CFTEIF=1 before writing data to CFDR or the CFDR write will be ignored. CFTEIF is automatically set when a data word transfers from the transmit data register into the CF/CF+ card through the FIFO. If no new data is waiting in the transmit data register, CFTEIF simply remains set and no data moves from the transmit data register to CF/CF+ card. This bit can only be set when BSY = 1 and HIS = 0. It is cleared by reading CFIFR with CFTEIF set, followed by writing a data value to the transmit data register at CFDR; and is reset to default value 1) by reset; 2) when CFE=0; 3) STOP bit is set. Setting this bit will generates an interrupt request if the CFTEIE bit of the CFSCR1 is also set.

1 = Transmit data register empty.
0 = Transmit data register not empty.

CFRFIF — CF Receive Data Register Full Interrupt Flag

This bit is set when there is valid data in the receive data register (**CF Data Register (CFDR)**). CFIFR must be read with CFRFIF=1 before reading data from CFDR or the CFDR read will get unexpected value. This bit is automatically set when a data word transfers from CF/CF+ card into the receive data register through the FIFO. This bit can only be set when BSY = 1 and HIS = 0. It is cleared 1) by reading CFIFR with CFRFIF set, followed by reading a data value from the receive data register at CFDR; 2) by reset; 3) when CFE=0; 4) STOP bit is set. Setting this bit will generate an interrupt request if the CFRFIE bit of the CFSCR1 is also set.

1 = Receive data register full.
0 = Receive data register not full.

TERRIF — Time-out Error Interrupt Flag

This bit is set if wait width time of CF/CF+ card is greater than the time specified by the TPS5-TPS0 bits of the register **CF Status and Control Register 2 (CFSCR2)** during common memory or I/O port accesses. It is cleared 1) by reading CFIFR with TERRIF set, followed by reading CFISR; 2) by reset; 3) when CFE=0. Setting this bit will generate an interrupt request when TERRIE bit of the CFSCR1 is also set.

1 = Time-out error occurs in read/write cycles.
0 = No time-out error occurs.

WERRIF — Wait Assertion Error Interrupt Flag

This bit is set if there is no $\overline{\text{WAIT}}$ signal assertion at the beginning of a read/write cycle during common memory or I/O port accesses. It is cleared 1) by reading CFIFR with WERRIF set, followed by reading CFISR; 2) by reset; 3) when CFE=0. Setting this bit will generate an interrupt request when WERRIE bit of the CFSCR1 is also set.

1 = Wait assertion error occurs.
0 = No wait assertion error occurs.

Section 4 Functional Description

This section provides a complete functional description of the Compact Flash Host Controller (CFHC) module. Please refer to the detailed CFHC block diagram **Figure 1-1**.

The IP BUS runs at 30/15/7.5 Mhz, and the QUEUE bus runs at 60 Mhz.

The CFHC includes the two interfaces with the IPBUS and QUEUE BUS.

4.1 IPBUS INTF REG

The IPBUS INTF REG is the IPBUS interface and register sub-module. It includes the standard IP bus interface and register block. The CPU can read/write the CFHC registers and data buffers through the IP bus. It will decode the CFHC register address and compose the read/write data bus.Also it has the register block inside it.

The CPU can read and write the CFHC registers through IP BUS. The **Figure 4-1** and **Figure 4-2** show the read and write operation separately.

The CPU may configure the CFHC as enabled (by setting CFE high) or disabled (by setting CFE low). When CFHC is enabled and the BSY bit of CFCR is low, the CPU can invoke the CFHC to read or write the card data by setting the INVOKE bit of CFCR high. The CFHC supports both block data operation and single word/byte operation.

For block data operation, when BSY=0, according to (**Table 4-1, Table 4-2, Table 4-3**, **Table 4-4**, **Table 4-5**, **Table 4-6**, **Table 4-7**), configure the CE1B, CE2B, the COM and REG of CFCCR for reg/memory/IO access, the CFBBAR for the starting address, and the CFBSR for the block size (bk size = CFBSR + 1 for byte operation, or CFBSR + 2 for word operation, or operation to configuration registers and attribute memory), and then configure the RWB, HIS of CFCR (select QUEUE or IPBI as host interface) and set INVOKE. The CFHC will set the BSY high, and transfer the block data between the CF/CF+ card reg/memory and the internal FIFO, the CFBBAR will count up the address by 1 (for byte operation) or 2 (for word operation, or operation to configuration registers and attribute memory) when the DISINC bit of CFSCR1 is cleared or keep the original value when the DISINC bit is set, and the CFBSR will count down the block size by 1 (for byte operation) or 2 (for word operation, or operation to configuration registers and attribute memory). After the QUEUE (HIS=1) or CPU (HIS=0) has succeeded reading/writing all the block data through CFHC, the BSY bit of CFCR will be cleared. During block data operation, CPU can end the current block data transfer by setting the STOP bit of CFCR with the current write/read cycle at the CF/CF+ card interface is completed (to prevent the damage to the card), it will set or reset the BSY, TQ, RQ bits of CFCR, the CFTEIF, CFRFIF, TERRIF and WERRIF bits of CFIFR, and the CFBSR registers when CFHC finishing the current handshake with the CF/CF+ card.The CFHC will clear the FIFO data and status. The STOP bit will be cleared after the BSY bit goes down. The CF/CF+ card pin will be in standby status.

For single word/byte data operation, it’s similar to the block data operation. CPU may either write 0 to CFBSR or do no operation to this register to configure a single word/byte data operation (the default value of CFBSR is always 0 after previous operation whether is completely finished or stopped).

CPU will access the data through IPBUS when HIS bit is cleared. For each word/byte read, the CFRFIF bit of CFIFR will be set when the data read from CF/CF+ card is ready in the CFDR. After CPU reads the CFIFR followed by reading the CFDR, the CFRFIF bit of CFIFR will be cleared if no data is ready in the CFDR from the FIFO. For each word/byte write, the CFTEIF bit of CFIFR will be set when the CFDR is empty to accept the data to be written to the CF/CF+ card. After CPU reads the CFIFR followed by writing the CFDR, the CFTEIF bit of will be cleared, and it will be set again when the CFDR is ready for next byte/word writing. When HIS bit of CFCR is set, QUEUE INTF will access the card data (refer to **4.2** in detail), and it's invalid for CPU to read/write the CFDR through IPBUS.

For byte operation at IPBUS, the valid byte data in CFDR is defined in **Table 4-1**, **Table 4-3**, **Table 4-5**, **Table 4-6**, **Table 4-7**.

Table 4-1 CF Storage Card Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	0	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bits D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bits D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 bits D15-D0)
X	0	0	1	0	0	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bits D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bits D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 bits D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access

Table 4-2 CF Storage Card Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Reg Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Reg Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Reg Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Reg Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Reg Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Reg Write

Table 4-3 CF+ Card Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10-A1	A0	SELECTED SPACE
1	1	X	X	X	XX	X	Standby
X	0	0	0	1	XX	0	Configuration Registers Read
1	0	1	0	1	XX	X	Common Memory Read (8 bits D7-D0)
0	1	1	0	1	XX	X	Common Memory Read (8 bits D15-D8)
0	0	1	0	1	XX	0	Common Memory Read (16 bits D15-D0)
X	0	0	1	0	XX	0	Configuration Registers Write
1	0	1	1	0	XX	X	Common Memory Write (8 bits D7-D0)
0	1	1	1	0	XX	X	Common Memory Write (8 bits D15-D8)
0	0	1	1	0	XX	0	Common Memory Write (16 bits D15-D0)
X	0	0	0	1	XX	0	Card Information Structure Read
1	0	0	1	0	XX	0	Invalid Access
1	0	0	0	1	XX	1	Invalid Access
1	0	0	1	0	XX	1	Invalid Access
0	1	0	0	1	XX	X	Invalid Access
0	1	0	1	0	XX	X	Invalid Access

Table 4-4 CF+ Card Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A8-A5	A4	A3	A2	A1	A0	SELECTED SPACE
X	0	0	0	1	XX	0	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	XX	0	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	XX	0	0	0	1	0	Card Status Reg Read
X	0	0	1	0	XX	0	0	0	1	0	Card Status Reg Write
X	0	0	0	1	XX	0	0	1	0	0	Pin Replacement Reg Read
X	0	0	1	0	XX	0	0	1	0	0	Pin Replacement Reg Write
X	0	0	0	1	XX	0	0	1	1	0	Socket and Copy Reg Read
X	0	0	1	0	XX	0	0	1	1	0	Socket and Copy Reg Write
X	0	0	0	1	XX	0	1	0	0	0	Reserved
X	0	0	1	0	XX	0	1	0	1	0	I/O Base 0
X	0	0	0	1	XX	0	1	1	0	0	I/O Base 1
X	0	0	1	0	XX	0	1	1	1	0	Reserved
X	0	0	0	1	XX	1	0	0	0	0	Reserved
X	0	0	1	0	XX	1	0	0	1	0	I/O Limit
X	0	0	0	1	XX	1	0	1	0	0	Reserved

Table 4-5 Attribute Memory Function

Function Mode	-REG	-CE2	-CE1	A10	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	L	H	L	L	L	L	L	H	High Z	Even Byte
Write Byte Access CIS ROM (8 bits) (invalid)	L	H	L	L	L	L	H	L	Don’t Care	Even Byte
Read Byte Access Configuration CF Storage (8 bits)	L	H	L	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration CF Storage (8 bits)	L	H	L	L	H	L	H	L	Don’t Care	Even Byte
Read Byte Access Configuration CF+ (8 bits)	L	H	L	X	X	L	L	H	High Z	Even Byte
Write Byte Access Configuration CF+ (8 bits)	L	H	L	X	X	L	H	L	Don’t Care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS ROM (16 bits) (invalid)	L	L	L	L	L	X	H	L	Don’t Care	Even Byte
Read Word Access Configuration CF Storage (16 bits)	L	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration CF Storage (16 bits)	L	L	L	L	H	X	H	L	Don’t Care	Even Byte
Read Word Access Configuration CF+ (16 bits)	L	L	L	X	X	X	L	H	Not Valid	Even Byte
Write Word Access Configuration CF+ (16 bits)	L	L	L	X	X	X	H	L	Don’t Care	Even Byte

Table 4-6 I/O Function

Function Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L	H	L	L	L	H	High Z	Even Byte
	L	H	L	H	L	H	High Z	Odd Byte
Byte Output Access (8 bits)	L	H	L	L	H	L	Don’t Care	Even Byte
	L	H	L	H	H	L	Don’t Care	Odd Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd Byte	Even Byte

Table 4-6 I/O Function

Function Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Word Output Access (16 bits)	L	L	L	L	H	L	Odd Byte	Even Byte
IO Read Inhibit	H	X	X	X	L	H	High Z	High Z
IO Write Inhibit	H	X	X	X	H	L	Don’t Care	Don’t Care
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd Byte	Don’t Care

Table 4-7 Common Memory Function

Function Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Read Access (8 bits)	H	H	L	L	L	H	High Z	Even Byte
	H	H	L	H	L	H	High Z	Odd Byte
Byte Write Access (8 bits)	H	H	L	L	H	L	Don’t Care	Even Byte
	H	H	L	H	H	L	Don’t Care	Odd Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd Byte	Even Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd Byte	Even Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd Byte	Don’t Care

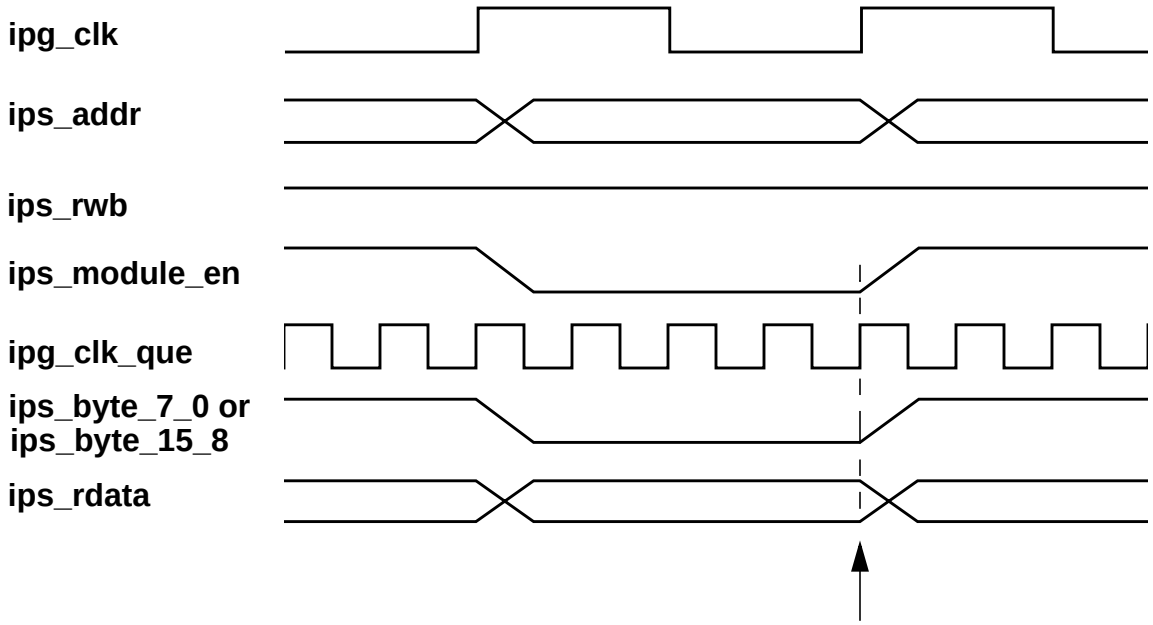

Figure 4-1 IPBUS INTF Read Timing

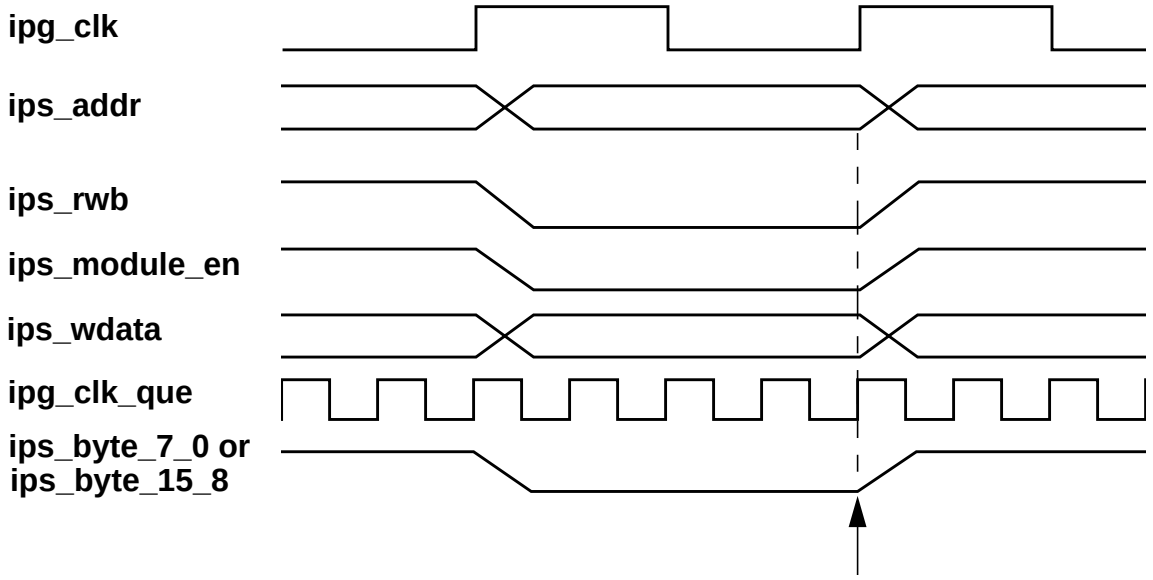

Figure 4-2 IPBUS INTF Write Timing

4.2 QUEUE INTF

When HIS bit of CFCR is cleared, QUEUE INTF will be disabled, no transmit or receive request will be send to the QUEUE controller.

When HIS bit of CFCR is set, QUEUE INTF will access the card data. When an operation is invoked (INVOKE bit is set), the BSY bit will be set. For card reading, when the FIFO gets the card data, the data will be put on the QUEUE bus, and QUEUE INTF will send a request to the QUEUE Controller to receive the data. When the QUEUE Controller gets the data from the QUEUE INTF, it will give an acknowledgement to CFHC, the request will be removed if the FIFO is empty (see **Figure 4-3**), or still asserted if there is remaining data in the FIFO (see **Figure 4-4**). For card data writing, the QUEUE INTF will send a request to the QUEUE Controller to require transmitting the data when the FIFO isn't full. When the QUEUE Controller puts the writing data onto the QUEUE bus together with an acknowledgement, the CFHC will put the data into the FIFO. The request will be removed if the FIFO is full or there is no further data write operation (see **Figure 4-5**); or will be still asserted if the block data write operation hasn't been completed and the FIFO isn't full (see **Figure 4-6**). When HIS bit is set, any operation by the IPBUS to the CFDR register, or the CFTEIF/CFRFIF bits of the CFCR, won't affect the QUEUE INTF and the FIFO status.

For byte operation at QUEUE bus, all byte will be put into high byte.

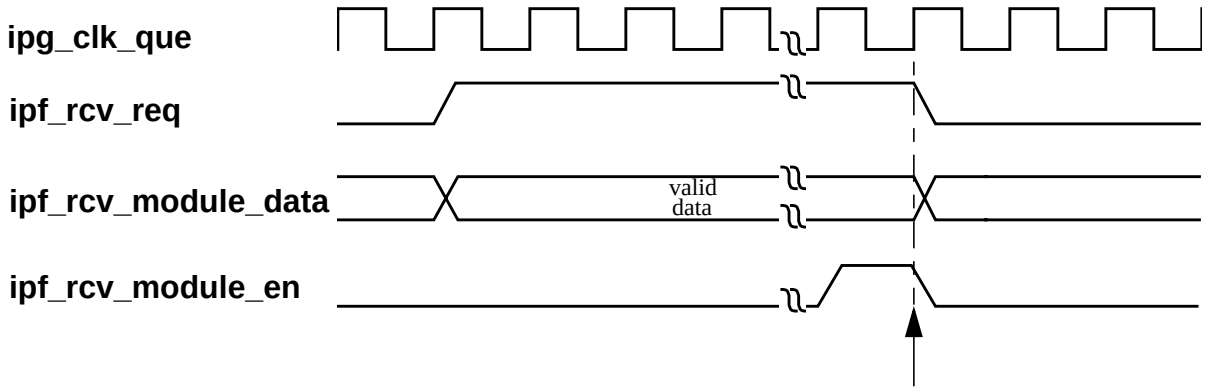

Figure 4-3 QUEUE INTF Single Word Read Timing

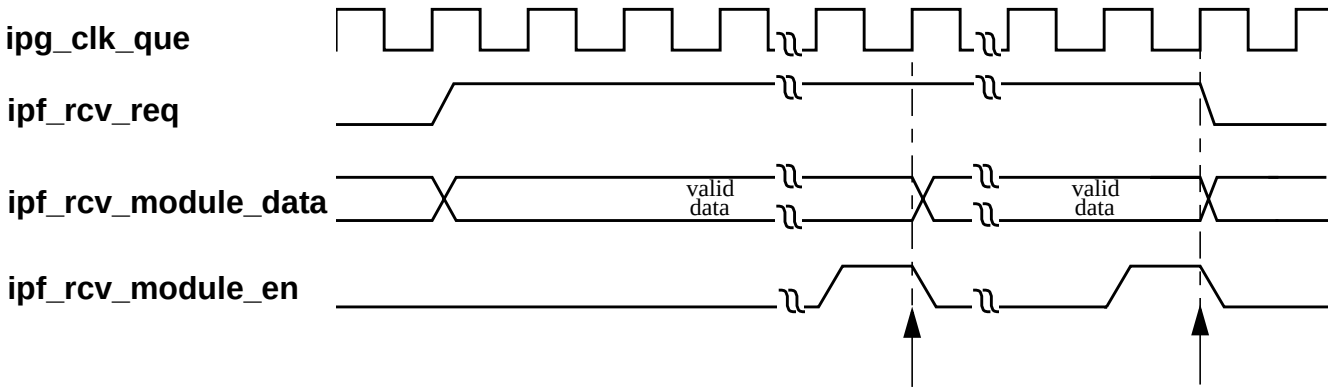

Figure 4-4 QUEUE INTF Multi Word Read Timing

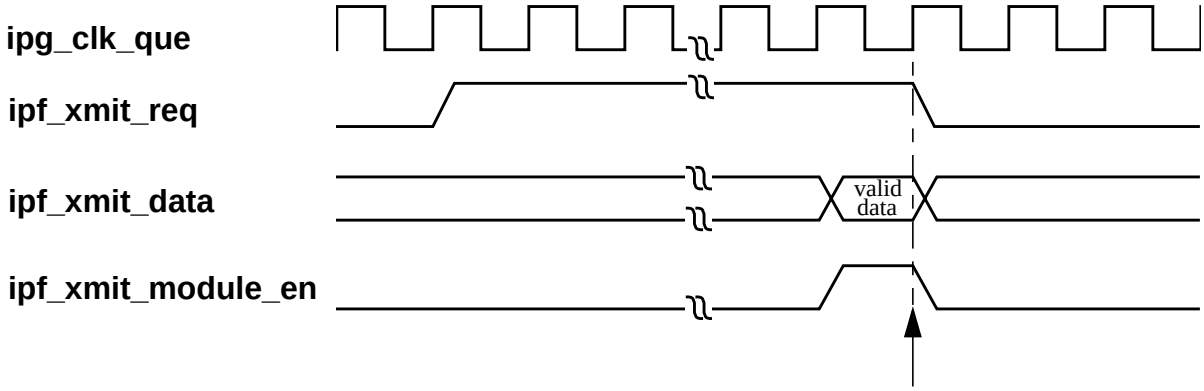

Figure 4-5 QUEUE INTF Single Word Write Timing

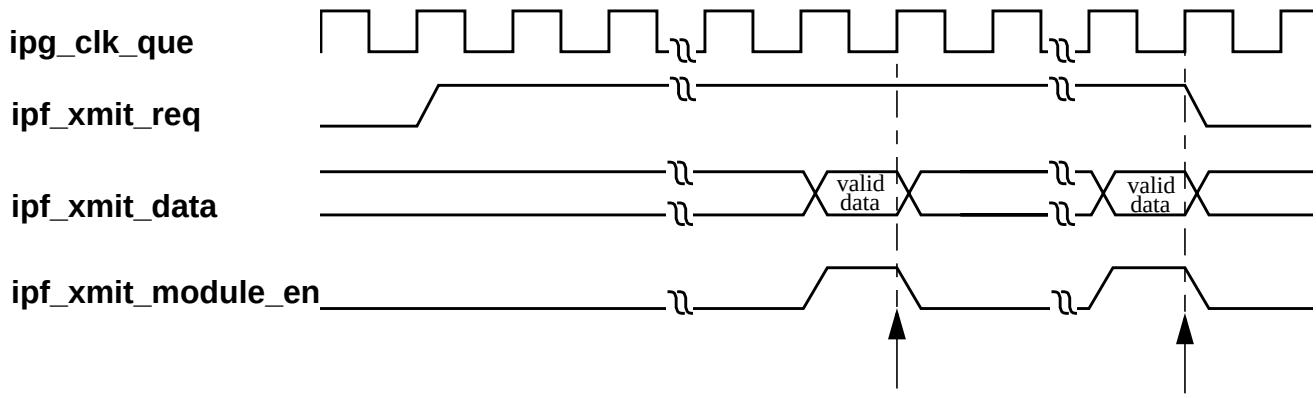

Figure 4-6 QUEUE INTF Multi Word Write Timing

4.3 FIFO

This is a four word deep FIFO used by both card read and write. The transmission and reception operation from the IPBUS and QUEUE-BUS share the same single FIFO buffer.The FIFO is configured as transmission (write from IPBUS/QUEUE-BUS) status after reset, and will be configured as transmission or reception according to the RWB bit of CFCR every when invoking.

For card data reading, the CARD BUS CTRL will read the data from CF/CF+ card with hand shaking and write to the FIFO when it's not full. The IPBUS INTF REG (when HIS=0) or QUEUE INTF (when HIS=1) will read the data from the FIFO when it's not empty.

For card data writing, the IPBUS INTF REG (when HIS=0) or QUEUE INTF sub-block (when HIS=1) will write the received data to FIFO when FIFO isn't full. The CARD BUS CTRL will read the data from the FIFO when it's not empty and write to the CF/CF+ card with hand shaking.

4.4 INT GEN

There are 10 interrupt sources provided by CFHC:

WERRI, TERRI, CFRFI, CFTEI, CI, OOI, VSI, RDYI, CHGI, CDI.

There are two interrupt vectors: one for CI, and one for the other interrupt sources.

(Please refer to **3.3.3** and **3.3.10** in detail for condition and configuration.)

The pulse width of $\overline{\text{IREQ}}$ pin must be wider than two QUEUE clock cycles.

4.5 CARD BUS CTRL

This block implements the signals to communicate with CF/CF+ card. There are two types of bus cycles and timing sequences that occur in the CF/CF+ card interface: direct mapped I/O transfer and memory access. Here six types of timing sequences are detailed: attribute memory read/write, common memory read/write and I/O read/write.

If CFHC is in standby mode, all the interface signals are in their reset status. Detailed status descriptions are shown in **Table 2-1**.

After the power up sequence, CFHC and CF/CF+ card are ready. The **CF Card Configuration Register (CFCCR)** should be initialized first for selecting the access mode (Attribute Memory Read/Write, Common Memory Read/Write and I/O Read/Write).

For common memory read/write and I/O read/write there is a time-out error interrupt to prevent system hang-up. If the wait width time of CF/CF+ card is greater than the time specified by the TPS5-TPS0 bits of the register **CF Status and Control Register 2 (CFSCR2)**, the time-out error interrupt flag (TERRIF of **CF Interrupt Flag Register (CFIFR)**) will be set, and an interrupt will be generated if TERRIE of **CF Status and Control Register 1 (CFSCR1)** is also set. CARD BUS CTRL will complete the current read/write cycle after the TERRIF bit of **CF Interrupt Flag Register (CFIFR)** is set, and current read/write block operation will go on without being interrupted.

CF/CF+ card may request the CARD BUS CTRL to extend the length of read/write cycle by asserting the $\overline{\text{WAIT}}$ signal at the start of the cycle. The CARD BUS CTRL will monitor the $\overline{\text{WAIT}}$ signal after the $\overline{\text{WAIT}}$ signal asserted and use this signal to indicate when the data is ready. After the data is latched, the CARD BUS CTRL will not monitor the $\overline{\text{WAIT}}$ signal. If there is no $\overline{\text{WAIT}}$ signal assertion from the CF/CF+ card, the CARD BUS CTRL will also complete the cycle with the minimum cycle time according to the **Table 4-10**, **Table 4-11**, **Table 4-12** and **Table 4-13**, and current read/write block operation will go on without interrupted.

The I/O transfer to or from the CF/CF+ Card can be either 8 or 16 bits. When a 16-bit accessible port is addressed, the signal $\overline{\text{IOIS16}}$ is asserted by the CF/CF+ Card.Otherwise, the $\overline{\text{IOIS16}}$ signal is de-asserted. When a 16 bit transfer is attempted, and the $\overline{\text{IOIS16}}$ signal is not asserted by the CF/CF+ Card, the CARD BUS CTRL will generate a pair of 8-bit references to access the word's even byte and odd byte. The CARD BUS CTRL will merge the even byte and odd byte into a word. See **Figure 4-7**.

For Attribute Memory Read/Write Operation, COM, REGB and CE1B are cleared. The LSB (BA0) of **CF Block Base Address Register (CFBBAR)** will be ignored (taken as zero) and data are always accessed in the lower byte (CDATA[7:0]) of card data bus. Attribute Memory access time is defined as 300ns. Detailed timing specs are shown in **Table 4-8**.

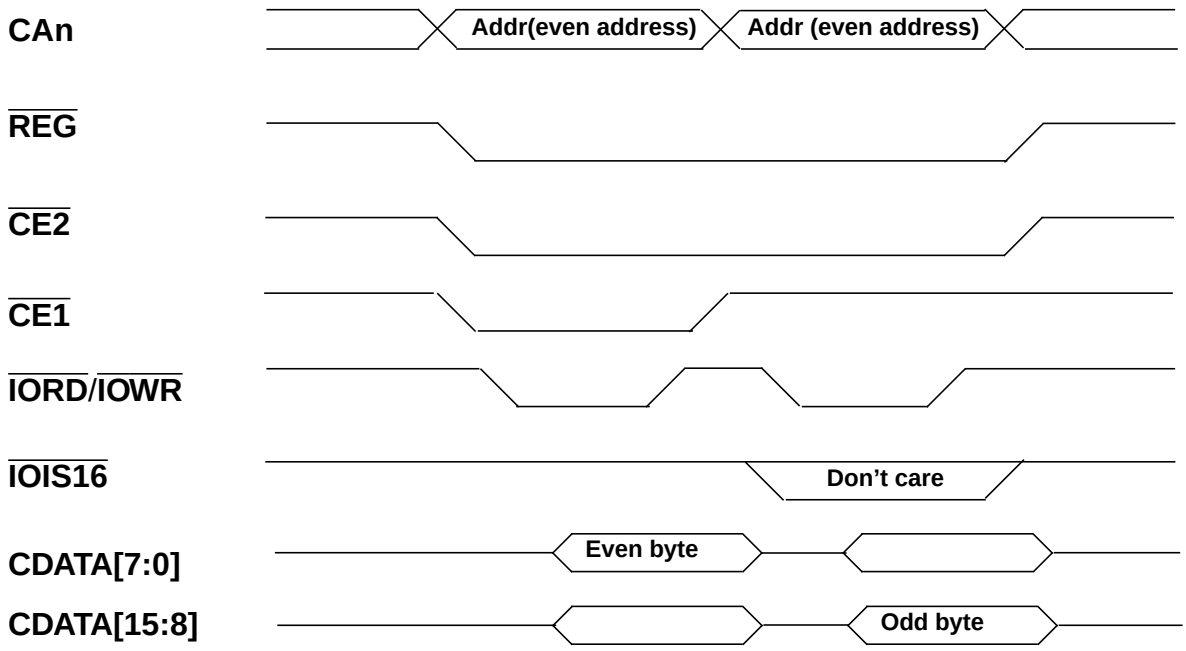

Figure 4-7 Timing Diagram of No IOIS16 Assertion in Word Accesses

Table 4-8 Attribute Memory Read Timing

Speed Version			300 ns	
Item	Symbol	IEEE Symbol	Min no. of ipg_clk_que*	Max no. of ipg_clk_que
Read Cycle Time	tc(R)	tAVAV	22	22
Address Access Time	ta(A)	tAVQV	22	22
Card Enable Access Time	ta(CE)	tELQV	18	18
Output Enable Acces Time	ta(OE)	tGLQV	9	9
Output Disable Time from CE	tdis(CE)	tEHQZ	6	6
Output Disable Time from OE	tdis(OE)	tGHQZ	6	6
Address Setup Time	tsu(A)	tAVGL	2	2
Output Enable Time from CE	ten(CE)	tELQNZ	1	1
Output Enable Time from OE	ten(OE)	tGLQNZ	1	1
Data Valid from Address Change	tv(A)	tAXQX	0	0

* The frequency of the clock ipg_clk_que is 60MHz.

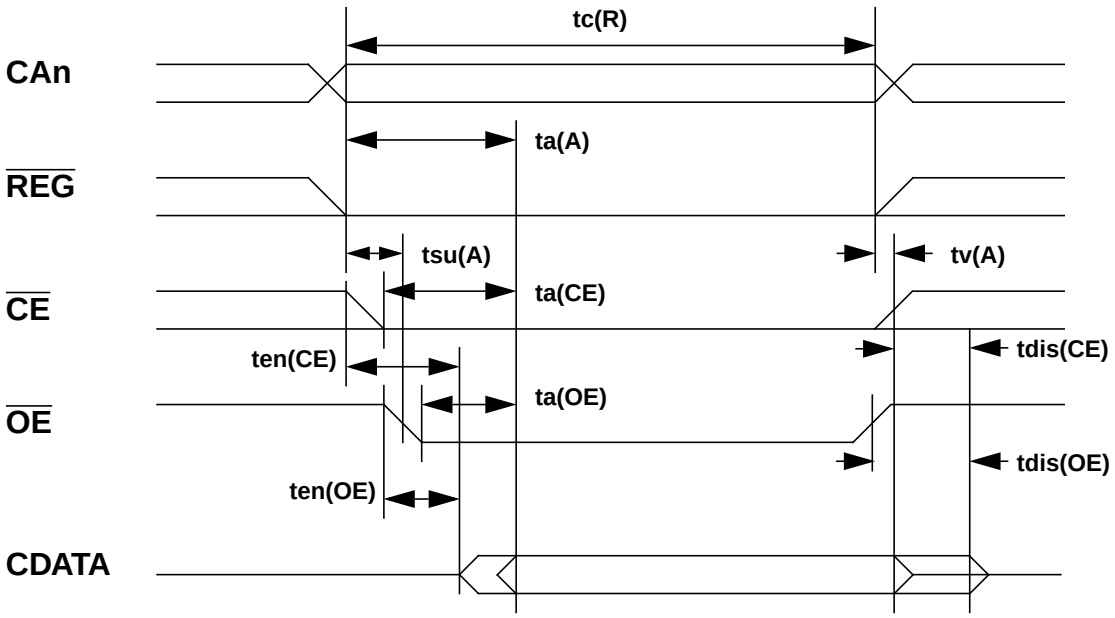

Figure 4-8 Attribute Memory Read Timing Diagram

The CF/CF+ Card Configuration Register (Attribute Memory) Write access time is defined as 250ns. Detailed timing specifications are shown in **Table 4-9**.

Table 4-9 Configuration Register (Attribute Memory) Write Timing

Speed Version			250 ns	
Item	Symbol	IEEE Symbol	Min no. of ipg_clk_que	Max no. of ipg_clk_que
Write Cycle Time	tc(W)	tAVAV	15	15
Write Pulse Width	tw(WE)	tWLWH	11	11
Address Setup Time	tsu(A)	tAVWL	2	2
Write Recovery Time	trec(WE)	tWMAX	2	2
Data Setup Time for WE	tsu(D-WEH)	tDVWH	5	5
Data Hold Time	th(D)	tWMDX	2	2

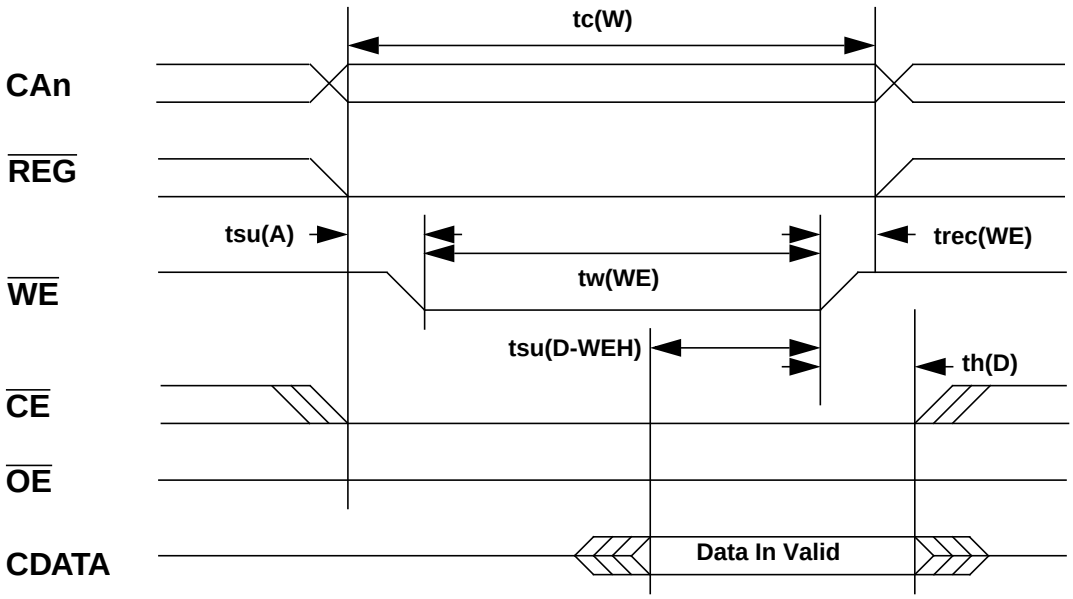

Figure 4-9 Configuration Register (Attribute Memory) Write Timing Diagram

For Common Memory Read or Write Operation, COM is cleared with REGB set. $\overline{OE}$ or $\overline{WE}$ signal will be de-asserted separately for one cycle of QUEUE clock after $\overline{WAIT}$ signal is de-asserted. Detailed timing specifications are shown in **Table 4-10** (Read) and **Table 4-11** (Write).

Table 4-10 Common Memory Read Timing

Item	Symbol	IEEE Symbol	Min no. of ipg_clk_que	Max no. of ipg_clk_que
Output Enable Access Time	ta(OE)	tGLQV	9	9
Output Disable Time from OE	tdis(OE)	tGHQZ	6	6
Address Setup Time	tsu(A)	tAVGL	2	2
Address Hold Time	th(A)	tGHZX	2	2
CE Setup before OE	tsu(CE)	tELGL	0	0
CE Hold following OE	th(CE)	tGHEH	2	2
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV	4	4
Data Setup for Wait Release	tv(WT)	tQVWTH	0	0
Wait Width Time	tw(WT)	tWTLWTH	0	21(180 for CF+ Card)

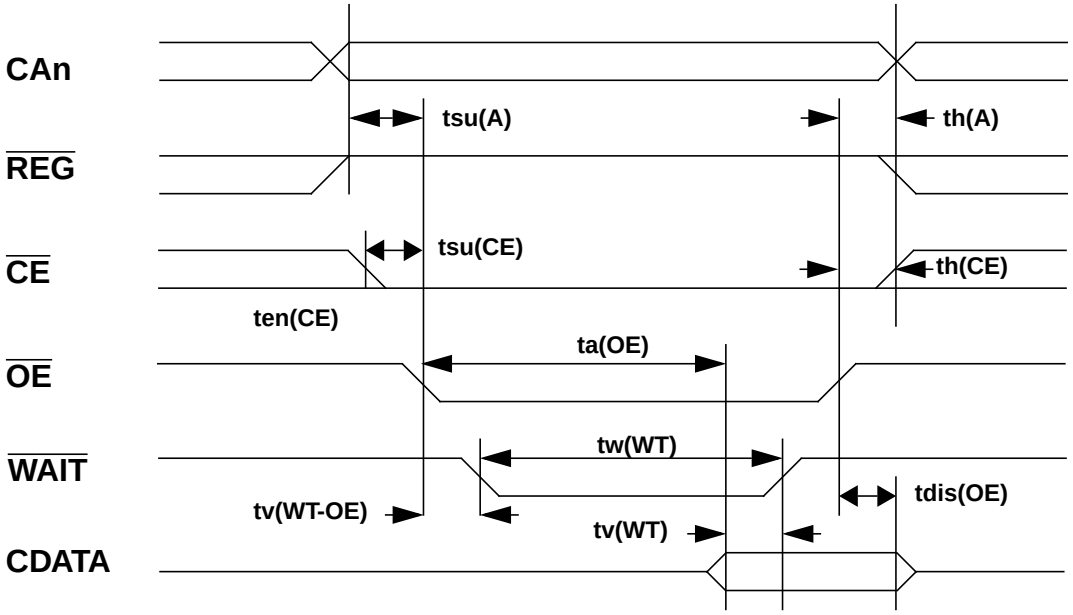

Figure 4-10 Common Memory Read Timing Diagram

Table 4-11 Common Memory Write Timing

Item	Symbol	IEEE Symbol	Min no. of ipg_clk_que	Max no. of ipg_clk_que
Data Setup before WE	tsu(D-WEH)	tDVWH	5	5
Data Hold Following WE	th(D)	tWMDX	2	2
WE Pulse Width	tw(WE)	tWLWH	9	9
Address Setup Time	tsu(A)	tAVWL	2	2
CE Setup before WE	tsu(CE)	tWMAX	2	2
Address Hold Time	th(A)	tGHAX	2	2
CE Hold following WE	th(CE)	tGHEH	2	2
Wati Delay Falling from WE	tv(WT-WE)	tWLWTV	4	4
WE High from Wait Release	tv(WT)	tWTHWH	0	0
Wait Width Time	tw(WT)	tWTLWTH	0	21(180 for CF+ Card)

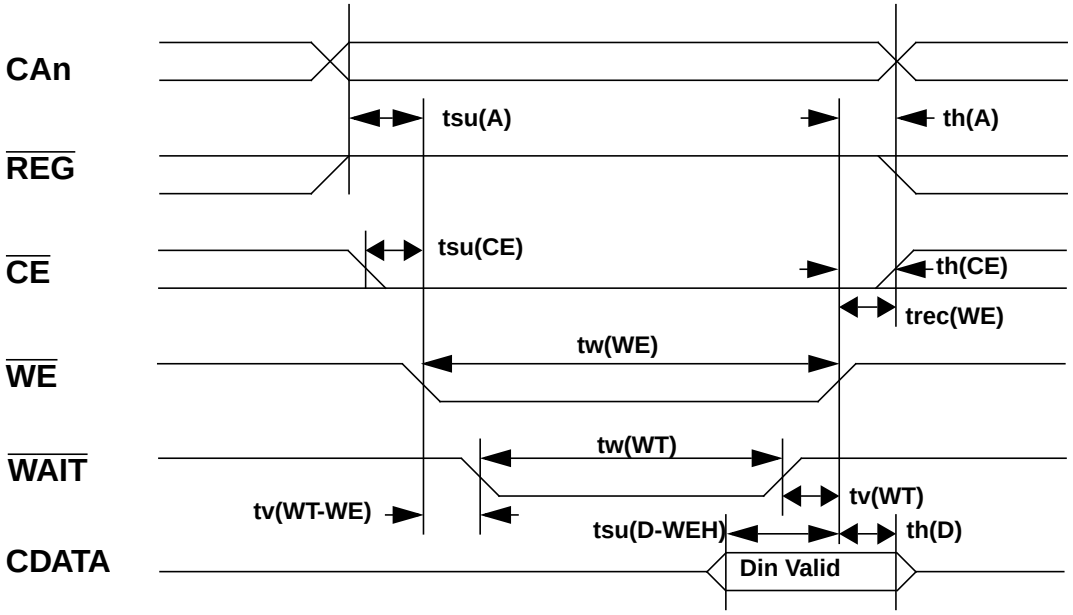

Figure 4-11 Common Memory Write Timing Diagram

For I/O Read/Write Operation, COM is set with REGB cleared. Detailed timing specifications are shown in **Table 4-12** (Read) and **Table 4-13** (Write).

Table 4-12 I/O Read Timing

Item	Symbol	IEEE Symbol	Min no. of ipg_clk_que	Max no. of ipg_clk_que
Data Delay after IORD	td(IORD)	tIGLQV	6	6
Data Hold following IORD	th(IORD)	tIGHQX	0	0
IORD Width Time	tw(IORD)	tIGLIGH	10	10
Address Setup before IORD	tsuA(IORD)	tAVIGL	5	5
Address Hold following IORD	thA(IORD)	tIGHAX	2	2
CE Setup before IORD	tsuCE(IORD)	tELIGL	1	1
CE Hold following IORD	thCE(IORD)	tIGHEH	2	2
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	1	1
REG Hold following IORD	thREG(IORD)	tIGHRGH	2	2
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	3
INPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH	3	3
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL	4	4
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH	3	3
Wait Delay Falling from IORD	tdWT(IORD)	tIGLWTL	4	4
Data Delay from Wait Rising	td(WT)	tWTHQV	0	0
Wait Width Time	wt(WT)	tWTLWTH	0	21(180 for CF+ Card)

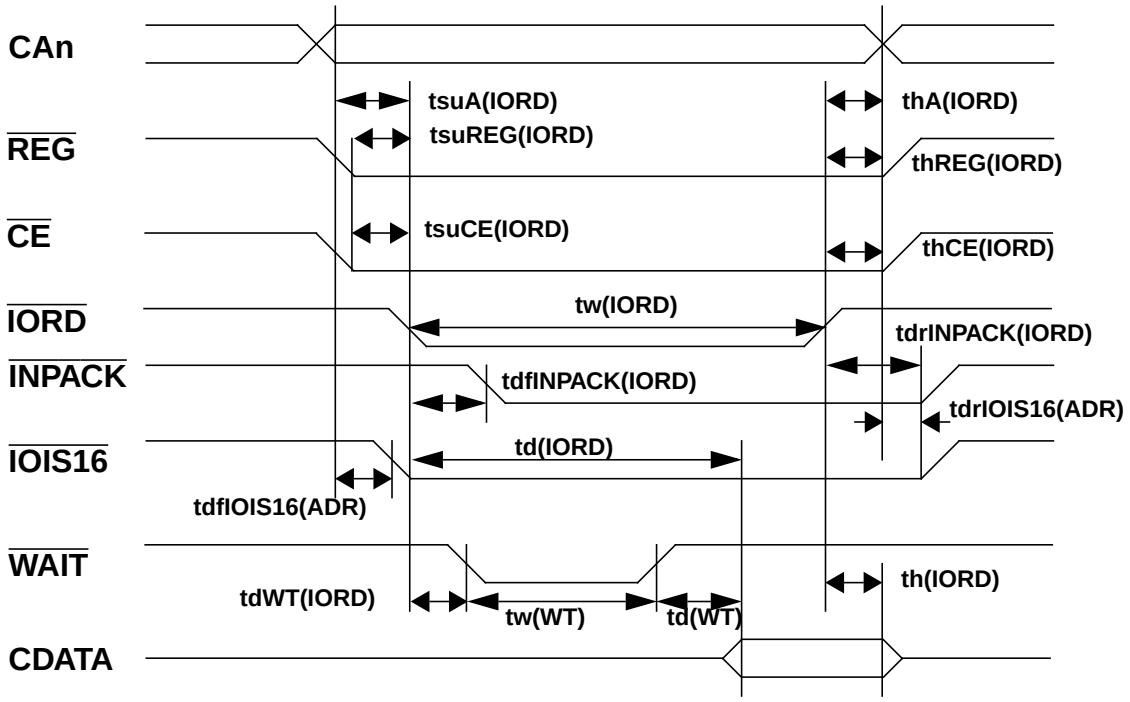

Figure 4-12 I/O Read Timing Diagram

Table 4-13 I/O Write Timing

Item	Symbol	IEEE Symbol	Min no. of ipg_clk_que	Max no. of ipg_clk_que
Data Setup before IOWR	tsu(IOWR)	tDVIWH	4	4
Data Hold following IOWR	th(IOWR)	tIWHDX	2	2
IOWR Width Time	tw(IOWR)	tIWLIWH	10	10
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	5	5
Address Hold following IOWR	thA(IOWR)	tIWHAX	2	2
CE setup before IOWR	tsuCE(IOWR)	tELIWL	1	1
CE Hold following IOWR	thCE(IOWR)	tIWHEH	2	2
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	1	1
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	2	2
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL	4	4
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH	3	3
Wait Delay Falling from IOWR	tdWT(IOWR)	tIWLWTL	4	4
IOWR high from Wait high	tdrIOWR(WT)	tWTJIWH	0	0
Wait Width Time	tw(WT)	tWTLWTH	0	21(180 for CF+ Card)

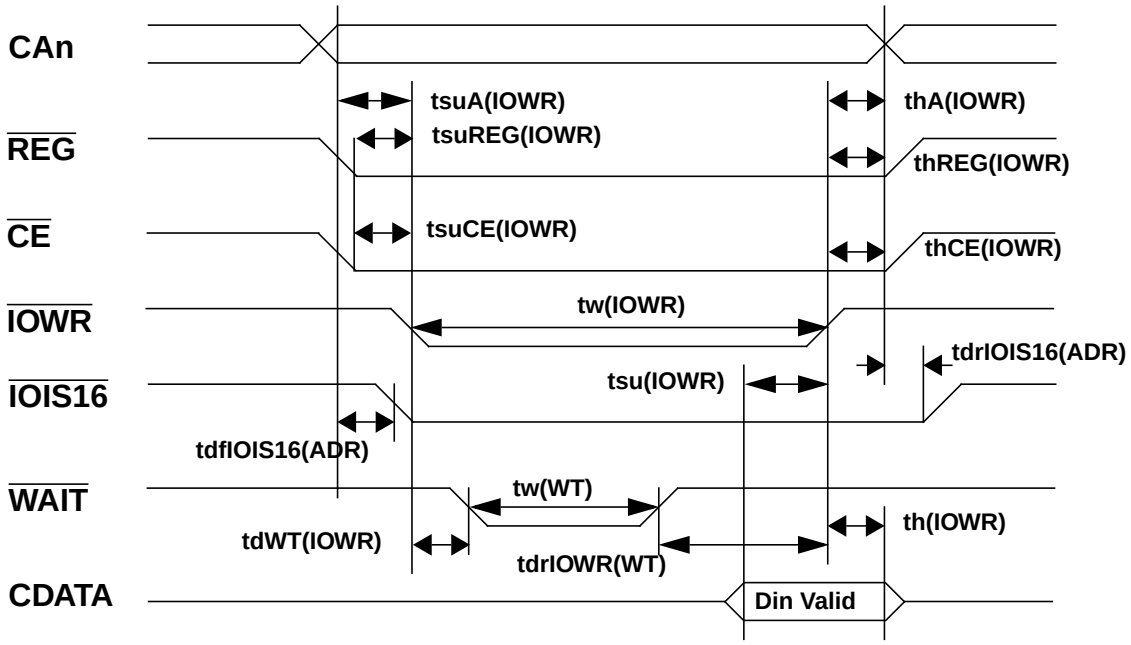

Figure 4-13 I/O Write Timing Diagram

4.6 Low Power Mode Options

4.6.1 CFHC In System Run Mode

In run mode with the CFHC system enable (CFE) bit in the CFHC control register cleared, the CFHC system is in a low-power, disabled state. CFHC registers can still be accessed (not all can be written, please see **3.3 Register Descriptions** for detail information of each register), but clocks to the core of this module are disabled.

4.6.2 CFHC In System Wait Mode

CFHC operation in wait mode depends upon the state of the CFSWAI bit of CFSCR1.

- If CFSWAI is cleared, the CFHC operates normally when the CPU is in wait mode.
- If CFSWAI is set, CFHC clock generation ceases and the CFHC module enters a power conservation state when the CPU is in wait mode. If CFSWAI is set, any card access in progress stops at wait mode entry. The transmission and reception resumes when the CFHC exits wait mode.

4.6.3 CFHC In System Stop Mode

The CFHC is inactive in stop mode for reduced power consumption. The STOP instruction does not affect CFHC register states.

4.7 Reset

After reset, the CFHC system is in a low-power, disabled state since the CFHC module enable (CFE) bit in the CFHC control register clear.

For signal status after reset, refer to **Table 2-1**.

Each register value after reset is shown in **Section 3**.

Section 5 Initialization/Application Information

5.1 Power Up/Down

When a CF/CF+ card is inserted into/removed from the socket, card detect interrupt will be generated if CFHC and card detect interrupt are enabled. So software can control the power up/down sequence. **Figure 5-1** shows one of the typical power up/down sequence.

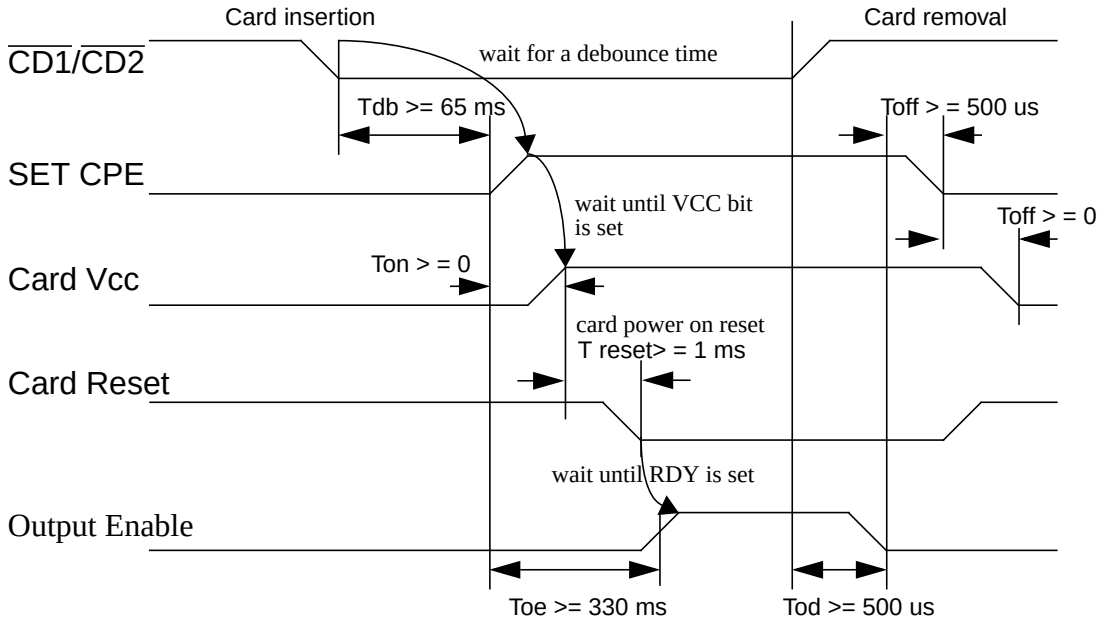

Figure 5-1 A Typical Timing Diagram of Power Sequence

Before the system entering into low power consumption mode (disabled, wait, stop), the software must make sure that the CF/CF+ card interface is ready by checking the CFISR and CFCR

5.2 Application Note

When MCU writes data to CF card through IP bus, it must get the first byte/word data ready into CFDR before invoke.

Software should configure the CFCCR, CFBBAR, CFBSR registers, and HIS/RWB bit of CFCR register to be ready before invoking. It’s forbidden to invoke read/write operation during CF card standby mode.

Software should not set the CRST bit of CF Status and Control Register 1 (CFSCR1) when any operation was active, until the operation is completed or stopped. When CRST bit of CF Status and Control Register

1 (CFSCR1) is high, a new operation invoking won’t cause any card read/write operation until CRST bit is cleared.

HCS12 Compact Flash Host Controller (CFHC) Block Guide End Sheet

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