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SMHC
Block Guide
V1.2

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Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
0.1	21 NOV 2001		Thomas Mui	Initial Release
0.2	30 NOV 2001		Thomas Mui	First Review
1.0	11 JAN 2002		Thomas Mui	- Format changes - Added section 2.2 of detailed signal descriptions - Update sections 3.1.3 & 3.1.4 for word access - Update sections 4.1.1, 4.1.3, 5.2 & 5.3 for continuous FIFO access
1.1	26 MAY 2003		Thomas Mui	- Update section 4.2.4 for table 4-2 and table 4-3 - Update sections 5.2, 5.3, 5.4, 5.5, 5.6 and 5.7 for swapping high/low bytes of command and address parameters
1.2	29 Nov 2004		Wai-On Law	Changed company logo.

Section 1 Introduction

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Section 1 Introduction

1.1 Overview

This block guide describes how the controller can be used as an interface for controlling smartmedia. The controller basically consists of a finite state machine, an ecc-generation circuit, Rx/Tx FIFOs, an QUE interface controller, a smartmedia control logic block and a clock logic block. **Figure 1-1** shows the block diagram of the smartmedia host controller.

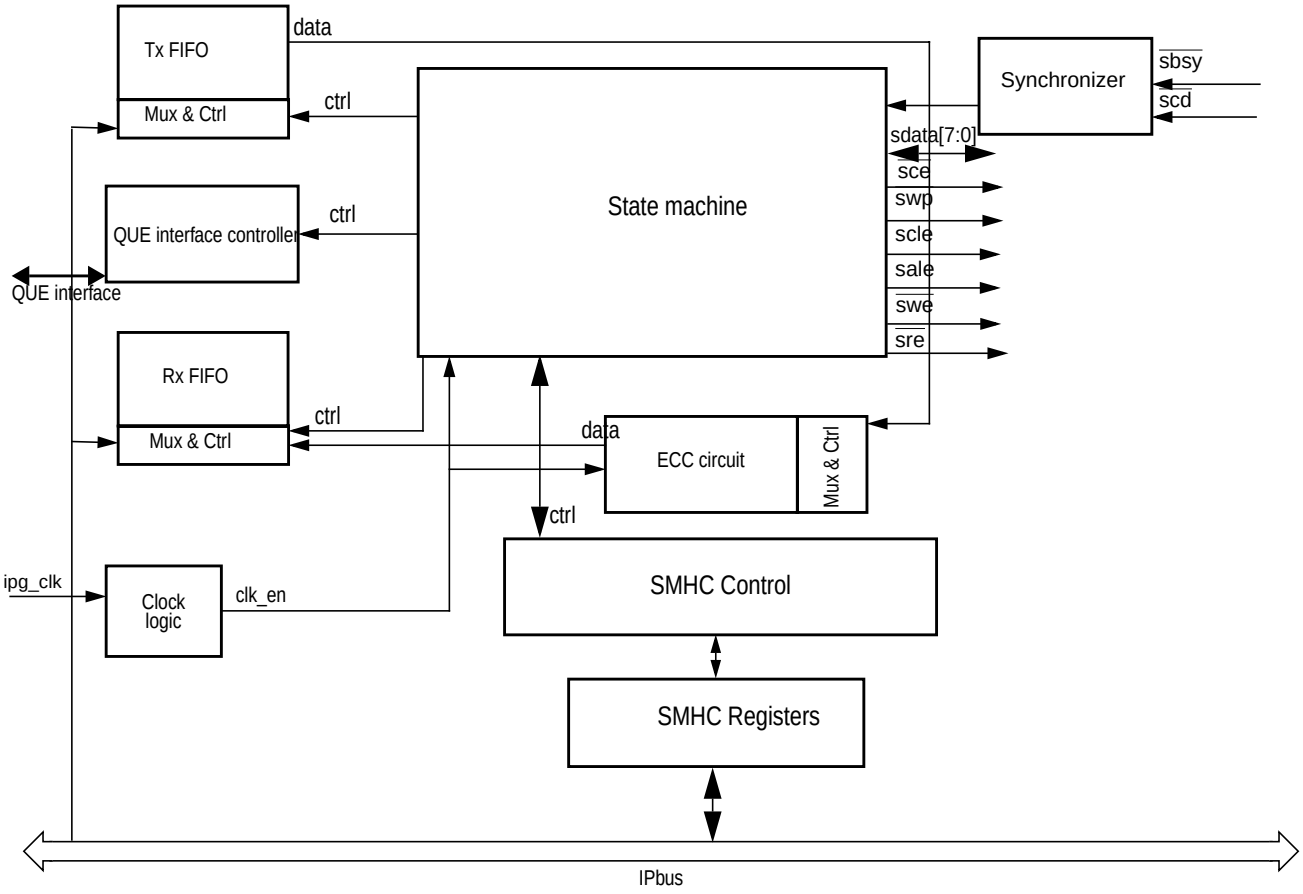

Figure 1-1 Block Diagram of smartmedia host controller

1.2 Features List

- Built-in 8 word FIFO buffers for both Tx and Rx

- Built-in ECC generation circuit
- QUE interface support for fast data movement
- Maskable hardware interrupts
- Support 16, 256 + 16, 512 + 16 block data transfer to/from smartmedia
- Built-in parity check of block address field
- Support smartmedia card from 4MB to 128MB
- Sequential read mode not supported

1.3 Modes of operation

- Normal mode

  All logic in all clock domains are active, unless SMHCEN in SMC($00) is cleared

- Power save mode

  The logic in core clock domain is inactive to save power when SMHCEN in SMC($00) is cleared.

Section 2 External Signal Description

2.1 Overview

The smartmedia host controller provides support for the standard smartmedia interface. Figure 2-1 and table 2-1 describe the smartmedia hardware interface required signals.

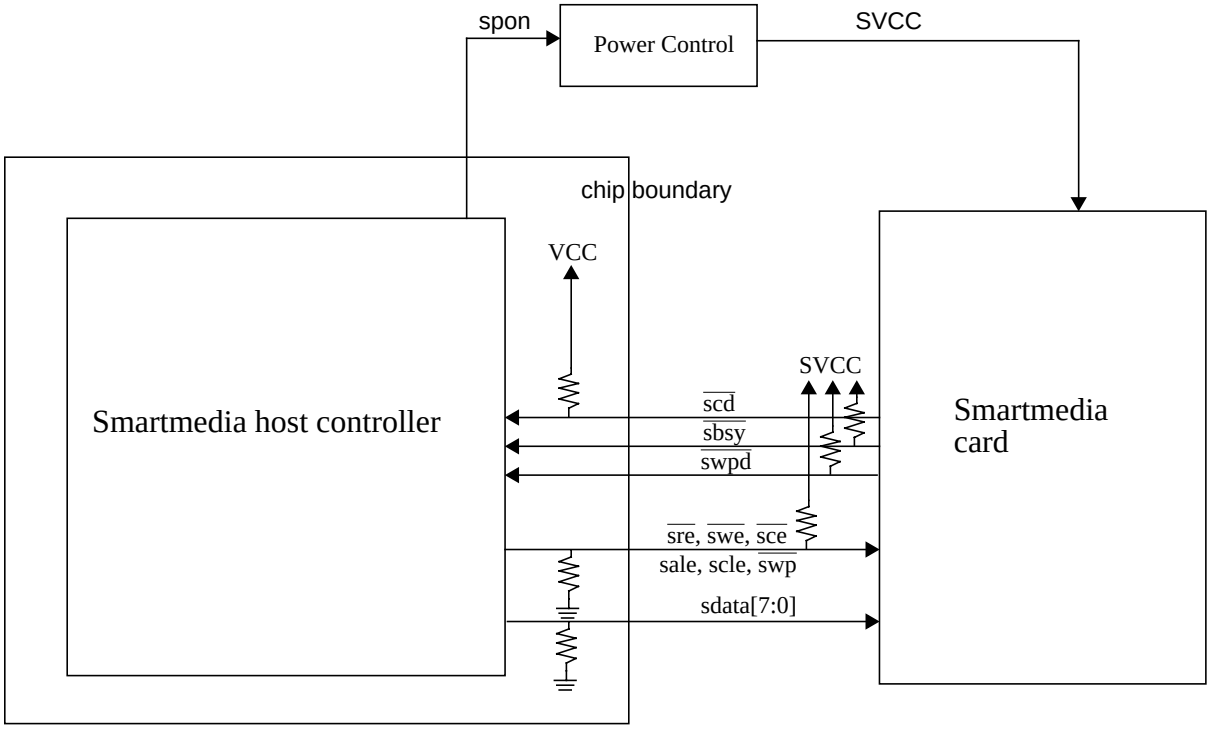

Figure 2-1 Smartmedia interface

Signal Name	Number of Pins	Signal	Type Description	Remarks
$\overline{\text{sbsy}}$	1	input	Smartmedia busy	10k SVCC pull up (schmitt trigger)
$\overline{\text{scd}}$	1	input	Smartmedia card detect	10k VCC pull up (schmitt trigger)
$\overline{\text{sce}}$	1	output	Smartmedia card enable	100k SVCC pull up
$\overline{\text{swp}}$	1	output	Smartmedia write protect	100k pull down
scle	1	output	Smartmedia command latch enable	100k pull down
sale	1	output	Smartmedia address latch enable	100k pull down
$\overline{\text{swe}}$	1	output	Smartmedia write enable	100k SVCC pull up
$\overline{\text{sre}}$	1	output	Smartmedia read enable	100k SVCC pull up
sdata[7:0]	8	inout	Smartmedia data[7:0]	100k pull down
spon	1	output	Smartmedia power on	
$\overline{\text{swpd}}$	1	input	Smartmedia write protect seal detect	10k SVCC pull up (schmitt trigger)
Total	18			

Table 2-1 Smartmedia interface

Interface signals spon and $\overline{\text{swpd}}$ are to be implemented by general I/O and will not be included in the smartmedia host controller. Its features will be handled by software.

2.2 Detailed Signal Descriptions

The following subsections describe each external signals separately.

2.2.1 $\overline{\text{SBSY}}$ - Smartmedia busy

This signal is to detect whether the smartmedia card is busy.

2.2.2 $\overline{\text{SCD}}$ - Smartmedia card detect

This signal is to detect whether the smartmedia card is present.

2.2.3 $\overline{\text{SCE}}$ - Smartmedia card enable

This signal is to enable the smartmedia card when asserted.

2.2.4 $\overline{\text{SWP}}$ - Smartmedia write protect

This signal is to write protect the smartmedia card when asserted.

2.2.5 SCLE - Smartmedia command latch enable

This signal is to command enable the smartmedia card when asserted.

2.2.6 SALE - Smartmedia address latch enable

This signal is to address enable the smartmedia card when asserted.

2.2.7 $\overline{\text{SWE}}$ - Smartmedia write enable

This signal is to write enable the smartmedia card when asserted.

2.2.8 $\overline{\text{SRE}}$ - Smartmedia read enable

This signal is to read enable the smartmedia card when asserted.

2.2.9 SDATA[7:0] - Smartmedia data

This signal provides data transfer between the host and the smartmedia card.

Section 3 Memory Map/Register Definition.

Table 3-1 shows the registers associated with the smartmedia module.

Table 3-1 SMHC Memory Map

Address Offset	Use	Access
$00	Smartmedia Control Register(SMC)	Read/Write
$01	Smartmedia Handshake Register(SMHS)	Write only
$02	Smartmedia Transmit FIFO Data Register(SMTDATA)	Write only
$02	Smartmedia Receive FIFO Data Register(SMRDATA)	Read only
$04	Smartmedia Interrupt Status Register(SMISR)	Read/Write
$05	Smartmedia Interrupt Mask Register(SMIMR)	Read/Write
$06	Smartmedia Status Register(SMS)	Read only
$07	Smartmedia FIFO Control/Status Register(SMFCS)	Read/Write
$08	Smartmedia Clock Rate Register(SMCLKR)	Read/Write

3.1 Register Descriptions

This section consists of register descriptions in address order.

3.1.1 Smartmedia Control Register(SMC)

$00

Bit	7	6	5	4	3	2	1	0
R	0	SMHCEN	FRST	SMRST	QEN	ECCEN	CNT1	CNT0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-1 Smartmedia Control Register(SMC)

QEN and ECCEN of the SMC register define the configuration during read/page program operations while CNT1 and CNT0 define the configuration during page program operation.

CNT1:CNT0 - Specify the no. of bytes of data to be transferred to smartmedia for page program operation, as shown in the following table.

Table 3-2 CNT1:CNT0 settings of SMC Register

CNT1:CNT0	No. of bytes(page program)
0:0	Reserved
0:1	16
1:0	256 + 16
1:1	512 + 16

If configuration = 0:0 during page program operation, the SME flag of the SMS Register will be set by the internal state machine.

ECCEN - Enable/disable ECC generation during read/page program operations.

1 = enable ECC generation.

0 = disable ECC generation.

QEN - Enable/disable QUE during read/page program operations.

1 = enable QUE request.

0 = disable QUE request.

SMRST - State machine reset. State machine of the smartmedia host controller will be reset to IDLE state.

1 = state machine reset.

0 = no reset.

FRST - FIFO reset. Reset Rx and Tx FIFOs when SMRST is set to reset the state machine.

1 = Reset Rx and Tx FIFOs when SMRST is set to reset the state machine.

0 = no reset.

SMHCEN - Smartmedia host controller enable. This bit enables the smartmedia host controller.

1 = enable smartmedia host controller.

0 = disable smartmedia host controller.

3.1.2 Smartmedia Handshake Register(SMHS)

$01

Bit	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								SCE
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-2 Smartmedia Handshake Register(SMHS)

The handshake register serves the handshaking function between the internal state machine and the cpu.

SCE - Start command execution. If command is present in the transmit data FIFO, writing "1" to this bit will start the command execution. Write "0" has no effect.

If command is not present in the transmit data FIFO when writing "1" to this bit, the SME flag of the SMS Register will be set "1" by the internal state machine.

During command execution, user has no write access to SMHS Register and thus writing has no effect.

1 = start command execution.

0 = no command execution.

3.1.3 Smartmedia Transmit FIFO Data Register(SMTDATA)

The transmit FIFO Data register is a 16-bit register. The bit position assignments of the register and its settings are described below.

When TBF of SMFCS Register is "1", write data is ignored and it is not stored to the FIFO.

Write to this register must be in aligned word.

$02

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	Tx DATA BUFFER															
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-3 Smartmedia Transmit FIFO DATA Register(SMTDATA)

For page program operation with the QUE interface enabled, all write access to SMTDATA Register will be ignored when the QUE interface is transferring data to the internal state machine during command execution.

B15 to B0 - Transmit FIFO Data Buffer. When TBF = 0, transmit buffer is available for data writes. When TBF = 1, write data is ignored.

3.1.4 Smartmedia Receive FIFO DATA Register(SMRDATA)

The receive FIFO Data register is a 16-bit register. The bit position assignments of the register and its settings are described below.

When RBE of SMFCS Register is "1", the FIFO read operation is ignored and invalid data will be read.

Read to this register must be in aligned word.

$02

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Rx DATA BUFFER															
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-4 Smartmedia Receive FIFO DATA Register(SMRDATA)

For read operation with the QUE interface enabled, all read access to SMRDATA Register will return indeterminate value when the QUE interface is receiving data from the internal state machine during command execution.

B15 to B0 - Receive FIFO Data Buffer. When RBE = 0, valid receive data is available in the buffer. When RBE = 1, invalid data is read.

3.1.5 Smartmedia Interrupt Status Register(SMISR)

The smartmedia interrupt status register describes the interrupt information of the host controller.

$04

Bit	7	6	5	4	3	2	1	0
R	0	HCE	ECCR	RDR	RDP	CDIN	CDOUT	RDY
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-5 Smartmedia Interrupt Status Register(SMISR)

HCE - Host controller error interrupt. This bit is set when the SME flag of the SMS Register is set.

1 = host controller error.

0 = None.

When writing ’1’, this bit is changed to ’0’.

ECCR - ECC ready interrupt. This bit is set when the ECC generation result is ready to be read by user from the Rx data FIFO during read operation.

1 = ECC ready.

0 = None.

When writing ’1’, this bit is changed to ’0’.

RDR - Redundant data ready interrupt. This bit is set when the redundant area data is ready to be read by user from the Rx data FIFO during read operation.

1 = Redundant data ready.

0 = None.

When writing ’1’, this bit is changed to ’0’.

RDP - Redundant data pending interrupt. This bit is set when redundant area data needs to be written by user to the Tx data FIFO during page program operation.

1 = Redundant data pending.

0 = None.

When writing ’1’, this bit is changed to ’0’.

CDIN - Card Insert interrupt. This bit is set if smartmedia card is inserted.

1 = card insert request.

0 = None.

When writing ’1’, this bit is changed to ’0’.

CDOUT - Card Out interrupt. This bit is set if smartmedia card is ejected.

1 = card out request.

0 = None.

When writing ’1’, this bit is changed to ’0’.

RDY - Smartmedia ready interrupt. This bit is set when $\overline{\text{sbsy}}$ signal of smartmedia changes from "Low" to "High".

1 = "Busy" to "Ready" request.

0 = None.

When writing ’1’, this bit is changed to ’0’.

3.1.6 Smartmedia Interrupt Mask Register(SMIMR)

$05

Bit	7	6	5	4	3	2	1	0
R W	INTEN	HCEIEN	ECCRIEN	RDRIEN	RDPIEN	CDINIEN	CDOUTIEN	RDYIEN
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-6 Smartmedia Interrupt Mask Register(SMIMR)

INTEN - Interrupt Enable. Interrupt signal will be generated when an interrupt condition occurs if INTEN is set to "1".

1 = interrupt enable.

0 = interrupt disable.

HCEIEN - The host controller error interrupt enable.

1 = enable host controller error interrupt.

0 = disable host controller error interrupt.

ECCRIEN - The ECC ready interrupt enable.

1 = enable ECC ready interrupt.

0 = disable ECC ready interrupt.

RDRIEN - The redundant data ready interrupt enable.

1 = enable redundant data ready interrupt.

0 = disable redundant data ready interrupt.

RDPIEN - The redundant data pending interrupt enable.

1 = enable redundant data pending interrupt.

0 = disable redundant data pending interrupt.

CDINIEN - The card in interrupt enable.

1 = enable card in interrupt.

0 = disable card in interrupt.

CDOUTIEN - The card out interrupt enable.

1 = enable card out interrupt.

0 = disable card out interrupt.

RDYIEN - The ready interrupt enable.

1 = enable "Busy" to "Ready" interrupt.

0 = disable "Busy" to "Ready" interrupt.

3.1.7 Smartmedia Status Register(SMS)

$06

Bit	7	6	5	4	3	2	1	0
R	0	CEC	SME	BAF2P	BAF1P	DRQ	BUSY	CP
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-7 Smartmedia Status Register(SMS)

The status register indicates the present status of the smartmedia host controller.

CP - Card present. Shows inserting status of smartmedia.

1 = smartmedia present.

0 = No smartmedia present.

BUSY - Shows the smartmedia is busy or ready.

1 = smartmedia busy.

0 = smartmedia ready.

DRQ - QUE request. This bit is ’1’ when data is requested through the QUE interface. Otherwise, this bit is ’0’.

1 = QUE request generated.

0 = No QUE request generated.

BAF1P - Block Address Field-1 parity check. This bit is meaningful only when the 8-words of redundant area data in the Rx data FIFO is being read by the user. Refer to section 5.8 for details.

1 = The parity of Block Address Field-1 is invalid.

0 = The parity of Block Address Field-1 is valid.

BAF2P - Block Address Field-2 parity check. This bit is meaningful only when the 8-words of redundant area data in the Rx data FIFO is being read by the user. Refer to section 5.8 for details.

1 = The parity of Block Address Field-2 is invalid.

0 = The parity of Block Address Field-2 is valid.

SME - State machine error. This bit is set "1" when either one of the following conditions occurs:

1. SCE of SMHS Register is set when there is no command present in the Tx Data FIFO. SME will be set "1" by the internal state machine during command execution.

2. If CNT1:CNT0 of SMC Register = "0:0" during page program operation, SME will be set "1" by the internal state machine during command execution.

CEC - Command execution complete. This bit will be reset to "0" when the command execution is complete.

1 = command execution by internal state machine not yet finished.

0 = command execution by internal state machine is finished.

3.1.8 Smartmedia FIFO Control/Status Register(SMFCS)

The FIFO Control/Status Register shows the empty and full flags of the receive data FIFO and the transmit data FIFO. It also controls the Rx and Tx FIFO flush.

$07

Bit	7	6	5	4	3	2	1	0
R	0	0	RFL	TFL	RBE	RBF	TBE	TBF
W								
RESET:	0	0	0	0	1	0	1	0

= Unimplemented or Reserved

Figure 3-8 Smartmedia FIFO Status Register(SMFCS)

RFL - Receive FIFO flush.

1 = Flush Rx data FIFO.

0 = No operation.

TFL - Transmit FIFO flush.

1 = Flush Tx data FIFO.

0 = No operation.

RBE - The receive FIFO empty flag. This bit indicates whether the receive data FIFO is empty.

1 = Receive data FIFO empty.

0 = Receive data FIFO not empty.

RBF - The receive FIFO full flag. This bit indicates whether the receive data FIFO is full.

1 = Receive data FIFO full.

0 = Receive data FIFO not full.

TBE - The transmit FIFO empty flag. This bit indicates whether the transmit data FIFO is empty.

1 = Transmit data FIFO empty.

0 = Transmit data FIFO not empty.

TBF - The transmit FIFO full flag. This bit indicates whether the transmit data FIFO is full.

1 = Transmit data FIFO full.

0 = Transmit data FIFO not full.

3.1.9 Smartmedia Clock Rate Register(SMCLKR)

The Smartmedia Clock Rate Register specifies the pre-scalar settings.

$08

Bit	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PS2	PS1	PS0
W								
RESET:	0	0	0	0	0	0	1	1

= Unimplemented or Reserved

Figure 3-9 Smartmedia Clock Rate Register(SMCLKR)

PS2:PS0 - The pre-scalar settings are defined in the following tables:

Table 3-3 Pre-scalar settings of SMCLKD Register

PS2:PS1:PS0	Frequency after pre-scalar
0:0:0	ipg_clk
0:0:1	1/2 ipg_clk
0:1:0	1/3 ipg_clk
0:1:1	1/4 ipg_clk
1:0:0	1/5 ipg_clk
1:0:1	1/6 ipg_clk
1:1:0	1/7 ipg_clk
1:1:1	1/8 ipg_clk

Section 4 Functional description

The architecture of the smartmedia host controller basically consists of a FSM for generating the smartmedia control signals, a QUE interface controller and Rx/Tx data FIFO for QUE transfer, while the Tx data FIFO also acts as a command buffer for storing the command to be executed and its column address and page address parameters. Rx and Tx data FIFOs should be empty before starting a command. Only one command should be written to the Tx data FIFO each time. No command should be written to the Tx data FIFO unless the previous command execution is complete.

Program, erase, read and other operating modes are controlled by the following commands.

Table 4-1 Operating command table

functions	commands	address parameters
Serial Data Input (Note 2)	$80	$0000 PA1 PA2 [PA3]
Read1 (Note 1)	$00	$0000 PA1 PA2 [PA3]
Read2 (Note 1)	$01	$0000 PA1 PA2 [PA3]
Read3 (Note 1)	$50	$0000 PA1 PA2 [PA3]
Reset	$FF	N/A
Block Erase (Note 2)	$60	PA1 PA2 [PA3]
Status Read	$70	N/A
ID Read	$90	$0000

(Note 1) If Read1($00), Read2($01), Read3($50) are used for address pointer operation, no address parameters are required.

(Note 2) Page Program command($10) and Block Erase command 2nd cycle($D0) are not needed since the FSM will automatically write these two commands to the smartmedia during Page Program operation and Block Erase operation.

The timing spec. of different operating modes should be referred to section 7 of the smartmedia electrical specifications.

4.1 SMHC operation

To start an operation, SMC Register should be configured first. The command should then be written to the Tx data FIFO. The address parameters should also be written to the Tx data FIFO if required.

The FSM is polling the SCE bit of the SMHS Register. Once the SCE bit of the SMHS Register is set to "1", the FSM will start decode and execute the command.

The FSM will generate the corresponding internal control signals and the interface control signals to the smartmedia. It will also handle the timing requirements of the smartmedia protocols.

Interrupts will be generated when user's attention is required by the FSM(ECCR, RDR, RDP or RDY interrupts of SMISR Register). This is described in details in the following sections.

4.1.1 page program operation(512 + 16 byte, 256 + 16 byte transfer)

After the Read1/Read2 command($00/$01) is written to the Tx data FIFO, a "1" should be written to the SCE bit of the SMHS Register. The FSM will write the command to the smartmedia to set the address pointer. When the command execution is completed, the FSM will reset the CEC bit of the SMS Register to "0". The user can then start set up the page program operation.

After the Serial Data Input command($80) and its address parameters are written to the Tx data FIFO, the SCE bit of the SMHS Register should be set to "1". The FSM will write the command and its address to the smartmedia.

If QUE is enabled, the FSM will generate QUE request for data. The QUE request will be disabled until 512/256 bytes of data have been written into the Tx Data FIFO. The FSM will transfer the data from the Tx Data FIFO to the smartmedia continuously until 512/256 bytes of data have been transferred. If QUE is not enabled, the user should first check that the Tx Data FIFO to be empty. The user can then write 512/256 bytes of data into the Tx Data FIFO if it is not full. The FSM will transfer the data from the Tx Data FIFO to the smartmedia continuously until 512/256 bytes of data have been transferred.

If ECC is enabled, the FSM will then transfer the 6/3 bytes of ECC data from the ECC generation circuit to the Rx data FIFO. An RDP interrupt will be generated. The user should read the 4/2 words of ECC data from the Rx data FIFO. If ECC is not enabled, an RDP interrupt will be generated.

The user should then write the 16 bytes of redundant area data to the Tx data FIFO. When the Tx data FIFO is full, the FSM will write the 16 bytes of redundant area data to the smartmedia. Page Program command($10) will then be written to the smartmedia. RDY interrupt will be generated when the smartmedia goes from busy to ready. The FSM will then reset the CEC bit of the SMS Register to "0". User should poll the CEC bit of the SMS Register to be "0" before starting another command.

4.1.2 page program operation(16 byte transfer)

After the Read3 command($50) is written to the Tx data FIFO, a "1" should be written to the SCE bit of the SMHS Register. The FSM will write the command to the smartmedia to set the address pointer. When the command execution is completed, the FSM will reset the CEC bit of the SMS Register to "0". The user can then start set up the page program operation.

After the Serial Data Input command($80) and its address parameters are written to the Tx data FIFO, the SCE bit of the SMHS Register should be set to "1". The FSM will write the command and its address to the smartmedia. An RDP interrupt will be generated.

The user should then write the 16 bytes of redundant area data to the Tx data FIFO. When the Tx data FIFO is full, the FSM will write the 16 bytes of redundant area data to the smartmedia. Page Program command($10) will then be written to the smartmedia. RDY interrupt will be generated when the

smartmedia goes from busy to ready. The FSM will then reset the CEC bit of the SMS Register to "0". User should poll the CEC bit of the SMS Register to be "0" before starting another command.

4.1.3 read operation(512 + 16 byte, 256 + 16 byte transfer)

After the Read1/Read2($00/$01) and its address parameters are written to the Tx data FIFO, a "1" should be written to the SCE bit of the SMHS Register. The FSM will write the command and its address to the smartmedia.

If QUE is enabled, the FSM will transfer 512/256 bytes of data from the smartmedia to the Rx Data FIFO. QUE request will be generated if data is present in the Rx Data FIFO. QUE request will be disabled when 512/256 bytes of data have been transferred from the Rx Data FIFO. If QUE is not enabled, the FSM will transfer 512/256 bytes of data from the smartmedia to the Rx Data FIFO. The user should read 512/256 bytes of data from the Rx Data FIFO if the Rx Data FIFO is not empty.

If ECC is enabled, the FSM will then transfer the 6/3 bytes of ECC data from the ECC generation circuit to the Rx data FIFO. An ECCR interrupt will then be generated. The user should read the 4/2 words of ECC data from the Rx data FIFO. After the ECC data are read by the user, the FSM will read the 16 bytes of redundant area data from the smartmedia and put into the Rx data FIFO. An RDR interrupt will be generated. If ECC is not enabled, the FSM will read the 16 bytes of redundant area data from the smartmedia and put into the Rx data FIFO. An RDR interrupt will be generated.

The user should then read the 16 bytes of redundant area data from the Rx data FIFO. The FSM will reset the CEC bit of the SMS Register to "0". User should poll the CEC bit of the SMS Register to be "0" before starting another command.

4.1.4 read operation(16 byte transfer)

After the Read3($50) and its address parameters are written to the Tx data FIFO, a "1" should be written to the SCE bit of the SMHS Register. The FSM will write the command and its address to the smartmedia.

The FSM will read the 16 bytes of redundant area data from the smartmedia and put into the Rx data FIFO. An RDR interrupt will be generated.

The user should then read the 16 bytes of redundant area data from the Rx data FIFO. The FSM will reset the CEC bit of the SMS Register to "0". User should poll the CEC bit of the SMS Register to be "0" before starting another command.

4.1.5 read status operation

After the Status Read($70) command is written to the Tx data FIFO, a "1" should be written to the SCE bit of the SMHS Register. The FSM will write the command to the smartmedia.

The FSM will then read the status from the smartmedia and put it in the Rx Data FIFO.

The FSM will then reset the CEC bit of the SMS Register to "0". User should poll the CEC bit of the SMS Register to be "0". The user should then read 1 word of status data(Lower byte is the status; Upper byte can be ignored) from the Rx data FIFO.

4.1.6 block erase operation

After the Block Erase command($60) and its address parameters are written to the Tx data FIFO, a "1" should be written to the SCE bit of the SMHS Register. The FSM will write the command and its address to the smartmedia.

The FSM will then write the Block Erase command 2nd cycle($D0) to the smartmedia. RDY interrupt will be generated when the smartmedia goes from busy to ready. The FSM will then reset the CEC bit of the SMS Register to "0". User should poll the CEC bit of the SMS Register to be "0" before starting another command.

4.1.7 reset operation

After the Reset command($FF) is written to the Tx data FIFO, a "1" should be written to the SCE bit of the SMHS Register. The FSM will write the command to the smartmedia.

RDY interrupt will be generated when the smartmedia goes from busy to ready. The FSM will then reset the CEC bit of the SMS Register to "0". User should poll the CEC bit of the SMS Register to be "0" before starting another command.

4.1.8 read ID operation

After the ID Read($90) command and its address parameter are written to the Tx data FIFO,a "1" should be written to the SCE bit of the SMHS Register. The FSM will write the command and its address to the smartmedia.

The FSM will then read the maker code and device code from the smartmedia and put it in the Rx Data FIFO.

The FSM will then reset the CEC bit of the SMS Register to "0". User should poll the CEC bit of the SMS Register to be "0". The user should then read 1 word of ID data(Upper byte is the device code while lower byte is the maker code) from the Rx data FIFO.

4.2 Functional block description

In this section, a brief introduction will be described on each important blocks of the smartmedia host controller.

4.2.1 FIFO & QUE interface

The receive data FIFO and the transmit data FIFO are 8 words in size respectively. Both the Rx and Tx data FIFOs have their own empty and full status flags. Both data FIFOs can be flushed. The FIFO structure is implemented by multiplexing the two different access strobes from QUE and the cpu, and controlling the multiplexer by a FSM. Data portion of read/page program operations can be transferred through the QUE interface to reduce the cpu's load.

4.2.2 Clock Control

The clock rate is specified by the settings of the SMCLKR Register. The clock rate after prescalar can be 1, 1/2, 1/3, 1/4, 1/5, 1/6, 1/7, 1/8 of the ipg_clk. User should set the SMCLKR Register such that the clock rate after prescalar is 15MHz or lower. The following diagram shows the interface signals timing.

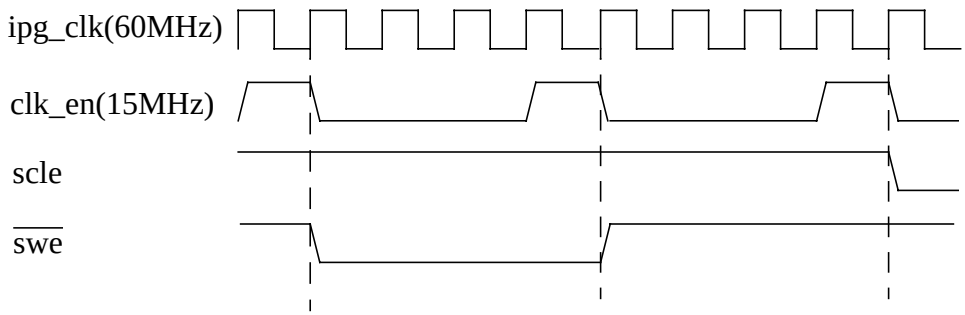

Figure 4-1 Interface signals timing for 15MHz clock rate

4.2.3 Finite State machine

The finite state machine is mainly used for command decoding and command execution. It also handles the QUE data transfer and the ECC data transfer. The control signals of the smartmedia($\overline{sce}$, $\overline{sre}$, $\overline{swe}$, sale, scle and $\overline{swp}$) are generated by the FSM. The FSM is complex and will not be described here in details.

4.2.4 ECC generation

The smartmedia host controller has a built-in ECC generation circuit for ECC calculation. If the ECCEN bit of the mode register is enabled during read/write operations, the ECC generation circuit will generate the ECC and the user can simply read the ECC results from the Rx data FIFO. The format for 256 byte and 512 byte data stream is as follows:

Table 4-2 ECC results format in Rx data FIFO for 256 byte data stream

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
LP7	LP6	LP5	LP4	LP3	LP2	LP1	LP0	LP15	LP14	LP13	LP12	LP11	LP10	LP9	LP8
CP5	CP4	CP3	CP2	CP1	CP0	"1"	"1"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"

For 256 bytes data stream, lower/upper byte of 1st word = line parity[15:0]. Upper byte of 2nd word = column parity[5:0] + "11".

Table 4-3 ECC results format in Rx data FIFO for 512 byte data stream

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
LP7	LP6	LP5	LP4	LP3	LP2	LP1	LP0	LP15	LP14	LP13	LP12	LP11	LP10	LP9	LP8
CP5	CP4	CP3	CP2	CP1	CP0	"1"	"1"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"
LP7	LP6	LP5	LP4	LP3	LP2	LP1	LP0	LP15	LP14	LP13	LP12	LP11	LP10	LP9	LP8
CP5	CP4	CP3	CP2	CP1	CP0	"1"	"1"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"

For 512 bytes data stream, lower/upper byte of 1st word = line parity[15:0] of 1st 256 bytes data. Upper byte of 2nd word = column parity[5:0] + "11" of 1st 256 bytes data. Lower/upper byte of 3rd word = line parity[15:0] of 2nd 256 bytes data. Upper byte of 4th word = column parity[5:0] + "11" of 2nd 256 bytes data.

4.2.5 ECC scheme

22 bits of ECC are generated for every 256 bytes of the storing area. ECC Field-1 and ECC Field-2 are used for data storing area-1 and data storing area-2, respectively.

The ECC scheme is capable of single-bit correction and 2-bit random-error detection. ECCs are generated only for data areas but not for page-data redundant areas containing ECCs. This is because the data in the page-data redundant area is duplicated for reliability and this duplication provides a means of checking the integrity of the data. For ECC calculations, 256 bytes are handled in the form of a 2048-bit serial data.

There are a total of 22 bits of parity data (6 bits for column parity and 16 bits for line parity) as follows: CP0, CP1, CP2, CP3, CP4, CP5, LP00, LP01, LP02, ..., LP14, and LP15. The parity data that have been generated are stored in the page-data redundant area in the order shown below:

Table 4-4 ECC data format of page-data redundant area

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	512+16 Bytes/Page
LP07	LP06	LP05	LP04	LP03	LP02	LP01	LP00	520,525 Bytes
LP15	LP14	LP13	LP12	LP11	LP10	LP09	LP08	521,526 Bytes
CP5	CP4	CP3	CP2	CP1	CP0	"1"	"1"	522, 527 Bytes

Section 5 Initialization/Application Information

In this section, the procedures of operations and precautions for page program, read, reset, read ID, read status and block erase are described. Pointer operation and block address field parity checking are also briefly described.

5.1 Pointer operation

The address pointer can be set by Read1($00), Read2($01) and Read3($50) commands. Read1($00) command sets the pointer to ’A area(0~255byte), Read2($01) command sets the pointer to ’B area(256~511byte), and Read3($50) command sets the pointer to C’ area(512~527byte). Read1($00) or Read3($50) is sustained until another address pointer command is inputted. Read2($01) command is effective only for one operation. After any operation of read, page program, erase and reset with Read2($01) command, the address pointer returns to A’ area by itself. To page program data starting from ’A, ’B, ’C area, commands of Read1($00), Read2($01), Read3($50) should be inputted respectively before the Serial Data Input($80) command is written.

5.2 Page program

For page program, the address pointer should first be set by commands Read1($00), Read2($01) or Read3($50). The procedures are as follows:

1. Write $0000/$0100/$5000 to SMTDATA Register
2. Set SCE bit of SMHS Register to "1"
3. Poll CEC bit of SMS Register. The CEC bit = ’0’ when command is finished

If the address pointer is set to area ’A, CNT1:CNT0 of SMC Register should be set to "1:1".

If the address pointer is set to area ’B, CNT1:CNT0 of SMC Register should be set to "1:0".

If the address pointer is set to area ’C, CNT1:CNT0 of SMC Register should be set to "0:1".

The QEN bit and ECCEN bit of SMC Register should also be configured.

The page program(512 + 16, 256 + 16 byte transfer) procedures are as follows:

1. Enable RDPIEN, RDYIEN and INTEN bits of SMIMR Register
2. Write SMC Register(To configure QEN, ECCEN, CNT1, CNT0)

3. Write $8000 to SMTDATA Register
4. Write column address $0000 to SMTDATA Register
5. Write page address PA7~PA0:$00 to SMTDATA Register
6. Write page address PA15~PA8:$00 to SMTDATA Register
7. Write page address 000000bPA17~PA16:$00 to SMTDATA Register if required
8. Set SCE bit of SMHS Register to "1"
9. If QUE not enabled:

    poll TBE bit of SMFCS Register to be "1"

Repeat the following 2 steps 128 times if 256 + 16 byte transfer, 256 times if 512 + 16 byte transfer:

    poll TBF bit of SMFCS Register to be "0"

    Write 1 word of data to SMTDATA Register

10. Wait for RDP interrupt:

clear RDP interrupt by writing "1" to the RDP bit of SMISR Register

If ECC enabled,

    read 2 words of ECC data from the SMRDATA Register if 256 + 16 byte transfer

    read 4 words of ECC data from the SMRDATA Register if 512 + 16 byte transfer

11. Write 8 words of redundant area data to SMTDATA Register
12. Wait for RDY interrupt:

clear RDY interrupt by writing "1" to the RDY bit of SMISR Register

13. Poll CEC bit of SMS Register. The CEC bit = ’0’ when command is finished
14. Disable RDPIEN and RDYIEN bits of SMIMR Register

The page program (16 byte transfer) procedures are as follows:

1. Enable RDPIEN, RDYIEN and INTEN bits of SMIMR Register
2. Write SMC Register(To configure CNT1, CNT0)
3. Write $8000 to SMTDATA Register
4. Write column address $0000 to SMTDATA Register
5. Write page address PA7~PA0:$00 to SMTDATA Register
6. Write page address PA15~PA8:$00 to SMTDATA Register

7. Write page address 000000bPA17~PA16:$00 to SMTDATA Register if required
8. Set SCE bit of SMHS Register to "1"
9. Wait for RDP interrupt:

clear RDP interrupt by writing "1" to the RDP bit of SMISR Register

11. Write 8 words of redundant area data to SMTDATA Register
12. Wait for RDY interrupt:

clear RDY interrupt by writing ’1’ to the RDY bit of SMISR Register

13. Poll CEC bit of SMS register. The CEC bit = "0" when command is finished
14. Disable RDPIEN and RDYIEN bits of SMIMR Register

5.3 Read

The number of bytes of data to be transferred from smartmedia is specified by the command. Read1($00) command will read 512 bytes of data + 16 bytes of redundant area data. Read2($01) command will read 256 bytes of data + 16 bytes of redundant area data. Read3($50) command will read 16 bytes of redundant area data.

The read procedures of Read1($00) and Read2($01) are as follows:

1. Enable the ECCRIEN bit(if ECC enabled), RDRIEN and INTEN bit of SMIMR Register
2. Write SMC Register (To configure ECCEN and QEN)
3. Write $0000/$0100 to SMTDATA Register
4. Write column address $0000 to SMTDATA Register
5. Write page address PA7~PA0:$00 to SMTDATA Register
6. Write page address PA15~PA8:$00 to SMTDATA Register
7. Write page address 000000bPA17~PA16:$00 to SMTDATA Register if required
8. Set SCE bit of SMHS Register to "1"
9. If QUE not enabled:

Repeat the following 2 steps 128 times if 256 + 16 byte transfer, 256 times if 512 + 16 byte transfer:

poll RBE bit of SMFCS Register to be "0"

read 1 words of data from SMRDATA Register

10. If ECC enabled:

Wait for ECCR interrupt

clear ECCR interrupt by writing "1" to ECCR bit of SMISR Register

read 2 words of data from SMRDATA Register if Read2($01) command

read 4 words of data from SMRDATA Register if Read1($00) command

11. Wait for RDR interrupt:

clear RDR interrupt by writing "1" to RDR bit of SMISR

12. Read 8 words of data(redundant area data) from SMRDATA Register until the SMRDATA Register is empty

13. Poll CEC bit of SMS Register. The CEC bit = "0" when command is finished

14. Disable ECCRIEN bit, RDRIEN bit of SMIMR Register

The read procedures of Read3($50) are as follows:

1. Enable the RDRIEN bit and INTEN bit of SMIMR Register

2. Write $5000 to SMTDATA Register

3. Write column address $0000 to SMTDATA Register

4. Write page address PA7~PA0:$00 to SMTDATA Register

5. Write page address PA15~PA8:$00 to SMTDATA Register

6. Write page address 000000bPA17~PA16:$00 to SMTDATA Register if required

7. Set SCE bit of SMHS Register to "1"

8. Wait for RDR interrupt:

clear RDR interrupt by writing "1" to RDR bit of SMISR Register

9. Read 8 words of data(redundant area data) from SMRDATA Register until the SMRDATA Register is empty

10. Poll CEC bit of SMS Register. The CEC bit = "0" when command is finished

11. Disable RDRIEN bit of SMIMR Register

5.4 Read status

When the Status Read command($70) is executed, the status can be read.

The procedures are as follows:

1. Write $7000 to SMTDATA Register
2. Set SCE bit of SMHS Register to "1"
3. Poll CEC bit of SMS Register. The CEC bit = "0" when command is finished
4. Read 1 word of data (Lower byte is the status; Upper byte can be ignored) from SMRDATA Register

5.5 Block Erase

The Block Erase command($60) procedures are as follows:

1. Enable RDYIEN bit and INTEN bit of SMIMR Register
2. Write $6000 to SMTDATA Register
3. Write page address PA7~PA0:$00 to SMTDATA Register
4. Write page address PA15~PA8:$00 to SMTDATA Register
5. Write page address 000000bPA17~PA16:$00 to SMTDATA Register if required
6. Set SCE bit of SMHS Register to "1"
7. Wait for RDY interrupt:

clear RDY interrupt by writing "1" to the RDY bit of SMISR Register

8. Poll CEC bit of SMS Register. The CEC bit = "0" when command is finished
9. Disable RDYIEN bit of SMIMR Register

5.6 Reset

The Reset command($FF) procedures are as follows:

1. Enable RDYIEN bit and INTEN bit of SMIMR Register
2. Write $FF00 to SMTDATA Register
3. Set SCE bit of SMHS Register to "1"
4. Wait for RDY interrupt:

clear RDY interrupt by writing "1" to the RDY bit of SMISR Register

5. Poll CEC bit of SMS Register. The CEC bit = "0" when command is finished
6. Disable RDYIEN bit of SMIMR Register

5.7 Read ID

The ID Read command($90) procedures are as follows:

1. Write $9000 to SMTDATA Register
2. Write $0000 to SMTDATA Register
3. Set SCE bit of SMHS Register to "1"
4. Poll CEC bit of SMS Register. The CEC bit = "0" when command is finished
5. Read 1 word of data from SMRDATA Register (Upper byte is the device code while lower byte is the maker code)

5.8 Block address field parity checking

The smartmedia host controller has an internal circuit to calculate the parity of the block address. The Block Address Field-1 and the Block Address Field-2 data formats of the redundant area are shown below as a reference:

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	512+16 Bytes/Page
0	0	0	1	0	BA9	BA8	BA7	518, 523 Bytes
BA6	BA5	BA4	BA3	BA2	BA1	BA0	P	519, 524 Bytes

Bytes 518 & 519 is the block address field-1 while bytes 523 & 524 is the block address field-2. When the 8 words of redundant area data in the Rx data FIFO are ready to be read by user, it has the following format:

Table 5-1 Rx data FIFO format(redundant area)

even address D[15:8]	odd address D[7:0]
512	513
514	515
516	517
518	519
520	521
522	523
524	525
526	527

When making the look-up table for transforming logical addresses to physical addresses, the BAF1P and BAF2P bits of the SMS Register can be used to determine the validity of the parity of the block address fields. The procedures are as follows:

1. Read the SMRDATA Register 4 times.

2. Read the SMS Register (BAF1P of SMS Register shows whether the parity of Block Address Field-1 is valid)

3. Read the SMRDATA Register 3 times.

4. Read the SMS Register (BAF2P of SMS Register shows whether the parity of Block Address Field-2 is valid)

5. Read the SMRDATA Register once.

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