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S12SMRAM3P5K2EV1/D

SMRAM3P5K2E
Block Guide
V01.01

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TSPG 8/16 Bit MCU
Freescale Semiconductor, Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
0.1	23 Jan 2002	23 Jan 2002	Patrick Kong	Initial release
0.2	04 Feb 2002	04 Feb 2002	Patrick Kong	Updated memory map and functional descriptions
0.3	27 Mar 2002	27 Mar 2002	Patrick Kong	Updated block name and document number
0.4	24 Jun 2002	24 Jun 2002	Patrick Kong	Updated SmartMedia RAM address space
0.5	14 May 2003	14 May 2003	Patrick Kong	Fixed psmba bit calculation using HCS12 bit10 - 1 Changed the starting address of SM table 2 to $0800
0.6	22 Sep 2003	22 Sep 2003	Patrick Kong	Removed POPI classification
01.00	01 Mar 2004	01 Mar 2004	Patrick Kong	Changed version to 01.00.
1.1	03 Dec 2004	03 Dec 2004	Wai-On Law	Changed company logo.

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Section 1 Introduction

Figure 1-1 is a block diagram of SMRAM.

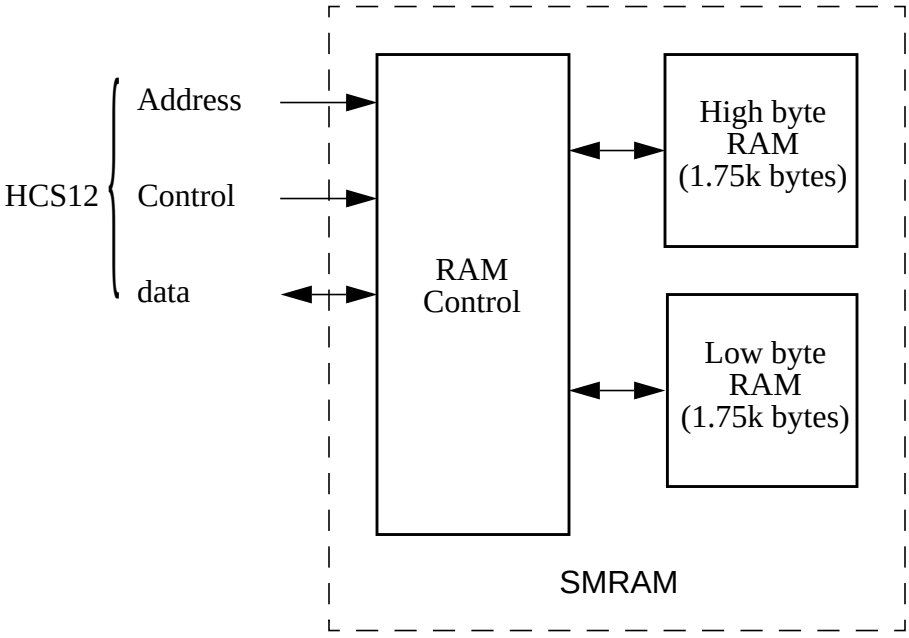

Figure 1-1 SMRAM Block Diagram

1.1 Overview

SMRAM is the system memory for HCS12 which consists of two synchronous SRAM and a memory controller. Part of the memory space can be programmed to function as the RAM (SmartMedia RAM) for the SmartMedia host controller.

1.2 Features

- 3.5k bytes system memory in normal mode
- 1084 bytes system memory and two 10-bit SmartMedia RAM (each of 1000 entries) in SM mode
- Parity generation in SM mode
- Single cycle access
- Support 8/16-bit access
- Support 16-bit misaligned access
- Support high address alignment

1.3 Modes of Operation

- Normal mode

  The whole memory address space from $0A00 to $17FF are used as system memory.
- SM mode

  Address $13C4 - $17FF is used as system memory.

  Address $0000 - $07CF is used as SmartMedia RAM.

  Address $0800 - $0FCF is used as SmartMedia RAM.

Section 2 External Signal Description

SMRAM does not have external signal.

Section 3 Memory Map/Register Definition

3.1 Memory Configuration

Figure 3-1 shows the memory maps of the SMRAM in normal mode and SM mode.

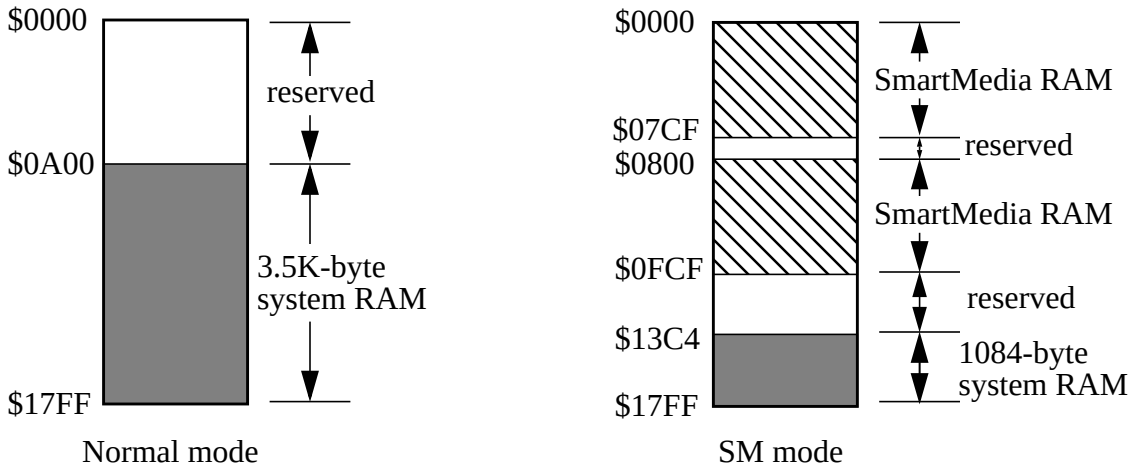

Figure 3-1 Memory Configuration

3.2 Module Memory Map

Table 3-1 is the module memory map for SMRAM registers.

Table 3-1 Module Memory Map

Address	Use	Access
$0	SMRAMCFG	R/W
$1	SMRAMSTAT	R
$2	Reserved[1]	R
$3	Reserved[1]	R

NOTES:
1. Reading the reserved address space will return zero data.

3.3 Register Descriptions

3.3.1 SMRAMCFG — SMRAM Configuration Register

Address offset: $0

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	SMMODE
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-2 SMRAMCFG

The SMRAMCFG register is used to configure the operating mode of SMRAM.

SMMODE — SmartMedia mode

The SMMODE bit enable the SmartMedia mode

1 = Configure to 1084 bytes system memory and two 10-bit SmartMedia RAM (each of 1000 entries).

0 = Configure to 3.5k bytes system memory.

3.3.2 SMRAMSTAT — SMRAM Status Register

Address offset: $1

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PSMBA
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-3 SMRAMSTAT

The SMRAMSTAT register is used to store the status of SMRAM.

PSMBA — Parity of the SmartMedia Block Address

The PSMBA bit store the even parity of the SmartMedia block address that has been accessed. Where SmartMedia block address equal to HCS12 address bit 10 - 1.

Section 4 Functional Description

The SMRAM addresses can be aligned on the upper or lower end of each 8k memory page by programming the RAMHAL bit of the Module Mapping Control register in HCS12. **Figure 4-1** illustrates the RAM address alignment. Read and write operations of the SMRAM can be performed in one cycle.

In normal mode, SMRAM is being configured to a 3.5k system memory with address space from $0A00 to $17FF. The system memory supports 8/16-bit accesses. And it supports misaligned access in 16-bit mode.

In SM mode, SMRAM is being configured to a 1084 bytes system memory with address space from $13C4 to $17FF and two 10-bit SmartMedia RAM with address space $0000 - $07CF and $0800 - $0FCF. The functions of the system memory is same as that in normal mode. But the SmartMedia RAM can only be accessed in 16-bit, aligned mode. For read operation, the 10-bit data from the SmartMedia RAM will be aligned on the lower bits of the read data bus, and the higher 6-bit value will always be zero. For write operation, the 10-bit data should align on the lower bits of the write data bus, and the high order 6-bit value will be ignored. A even parity of the SmartMedia block address will be generated and stored in SMRAMSTAT when the SmartMedia RAM is being read.

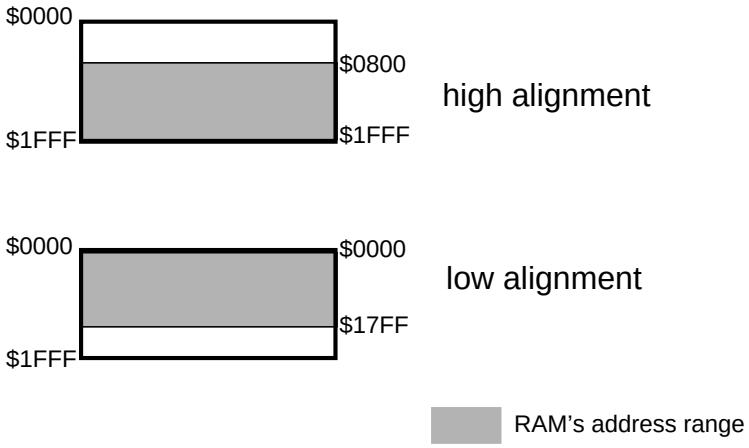

Figure 4-1 6K RAM address alignment in 8K memory space

Section 5 Initialization/Application Information

None

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