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USB20D6E2F
Block Guide
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TSPG 8/16 Bit MCU
Freescale Semiconductor, Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V00.01	21 Mar 2002	21 Mar 2002	Y.H. Cheng	First Draft version
V00.02	20 Mar 2002	20Mar 2002	Y.H. Cheng	Update Memory Map/Register Definition Update Initialization/Application Information
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V00.05	18 Nov 2002	18 Nov 2002	Y.H. Cheng	-Add Resume interrupt mask, for async wake up. -Remove dependency to MEN for bits RESUME and SPHY in IMCR register. - Add SNAK bit to UEPCSR4A, UEPCSR5A to increase flexibility in updating endpoint buffer data. - Clarify behaviour of Short packet and zero length operation for Physical endpoint 4 and 5. - update misc. typo mistakes.
V00.06	3 June 2003	3 June 2003	Y.H. Cheng	- Added PHYRST and EPRST bits for resetting PHY and UEPCSRxx respectively. - Clarify description of MRST to exclude reset of PHY submodule - Added DISCON bit to allow USB bus to be put into high impedance state. - Added ACTEP active endpoint field in UMSR1 - Modified definition for SPD field in UMSR1 - Removed PHYCP and SYSCS bit in UMSR1 since function was handled by CRG_U - Upated SPHY bit definition and disable update when PLLSEL bit is set to 1. - Modifed definition of Stall for physical endpoint 0 and 1 to protocol stall - Modifed definition of Stall for physical endpoint 2 to 6 to functional stall - update misc. typo mistakes. - Add HRSTIZ pin in PHY test mode pin out for UF32
V00.07	11 June 2003	11 June 2003	Y.H. Cheng	- Modified DISCON bit reset state to ’1’ disconnect - Modified description for EPRST to reset USSC and URSC bits when writen to 1 - Modifeid description of PHYRST so that this feature can be activated when PLLSEL = 0, MEN= 0 and MCE = 1.
V00.08	24 June 2003	24 June 2003	Y.H. Cheng	- Change ROMONE assignment in Table 7-1 per new SoCGuide - Update incorrect assignment in Table 7-1 (VREGEN, REF3V) - Add information on Test Interface pin assignment for 64pin option. - Add description on test limitation on 64 pin option. - Removed clock by-pass functional test mode - operation covered by other modes.

Version Number	Revision Date	Effective Date	Author	Description of Changes
V00.09	26 Nov 2003	26 Nov 2003	Y.H. Cheng	- Remove Test Related Information and MCP classification for custiomer specification.
V01.00	26 Nov 2003	26 Nov 2003	Y.H. Cheng	- Updated UCCSR register bit naming consistancy, all references to DONECSRS is updated to DONEECRU - Updated section 2.2.3 title D- should be D+ instead
V01.01	23 Mar 2004	23 Mar 2004	Y.H. Cheng	- Removed all references to Physical Endpoint 6. - Clarify available logical endpoints in Table 3-10
V01.02	29 Nov 2004	29 Nov 2004	Wai-On Law	Changed company logo.
V01.03	20 Feb 2006	20 Feb 2006	Wai-On Law	Removed the empty Section 5.

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Preface

The USB20 is a specialized block used in a complete SoC design for implemention Full-speed and High-speed communication as specified in the USB2.0 specifications. Content of the Block Guide is intended for re-use as reference material in customer documentation. The Block Guide must contain sufficient detail for an end customer to understand and use the block within a final System-on-a-Chip design.

Terminology

CRC: Cyclic Redundancy Checks

FS: Full Speed

HS: High Speed

IPBI: IP Bus Interface

IPFI: IP Fifo Bus Interface

IPSI: IP Slave Bus Interface

S12: HCS12 Core

SIE: Serial Interface Engine

PIE: Parallel Interface Engine

USB20: USB 2.0 Module

UDC: USB Device Controller

UPHY: USB Physical Layer Interface Block

VCI: Virtual Component Interface

Section 1 Introduction

This block guide provides an overview of the universal serial bus 2.0 (USB20) module that is compatible with the IP Bus used in the HCS12 MCU family. This USB module is designed to serve as a high-speed (HS) USB device which is compliant with the Universal Serial Bus Specification Rev 2.0. Control, Interrupt, Isochronous and Bulk endpoints are supported. Endpoint 0 IN/OUT is the default control endpoint, other endpoints are configurable for the other three transfer types.

The USB physical layer interface (UPHY) is integrated in the USB20 module. Both the USB High Speed (480Mbps) and Full Speed (12Mbps) transceivers are connected to the USB bus and could be activated or deactivated according to the USB2.0 protocol.

Figure 1-1 is a high level block diagram of the USB20 module, showing the interaction of various functional blocks.

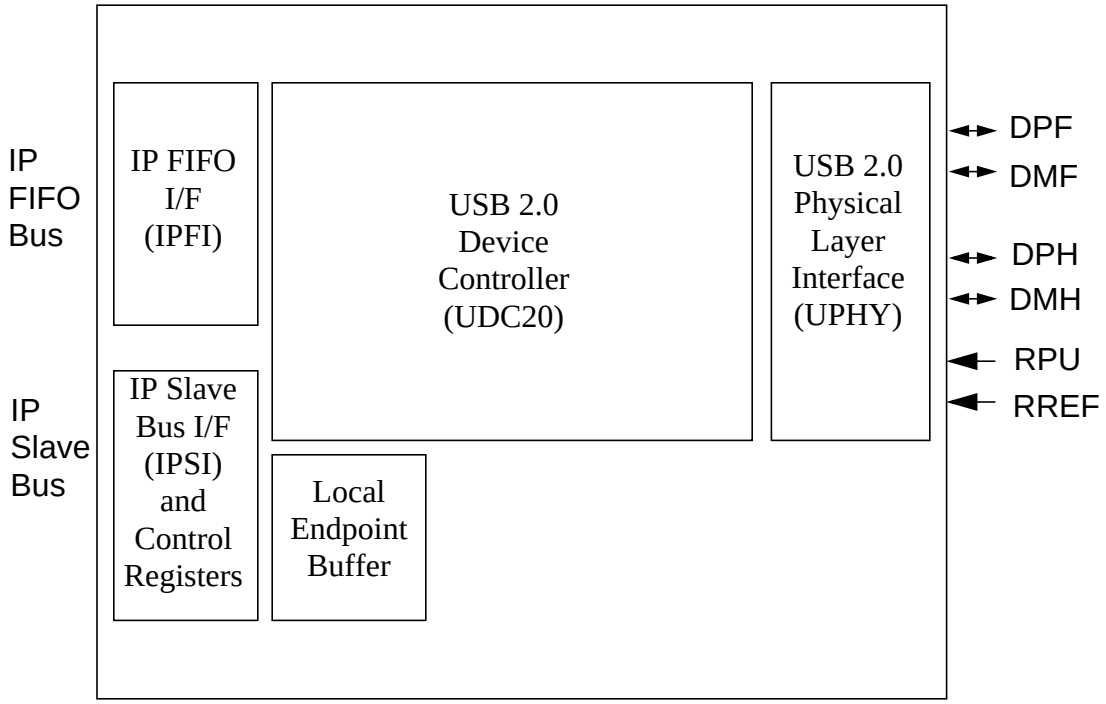

Figure 1-1 USB20 Block Diagram

1.1 Overview

The USB20 module complies with the Universal Serial Bus Specification Rev2.0. Users are strongly recommended to read this standard before proceeding with this block guide.

The USB20 module supports the USB Full-speed and High-speed protocols with the on chip USB device controller (UDC20) block and the USB Physical Interface (UPHY) block. The UDC20 block can support control, interrupt, isochronous and bulk endpoints. This is ideal for implementing the Bulk-only or Control Bulk Interrupt (CBI) Mass Storage Device Class devices. While the isochronous feature can be used in other devices classes.

The UDC20 block is under program control by the HCS12 core through the IP Slave Bus (IPSB). There are 6 independent endpoints which can be configured as Control, Interrupt, Bulk and Isochronous IN/OUT endpoints. Two 64-byte endpoint buffers are associated with physical endpoint 1 which is used as the default control endpoint (endpoint 0). Another two 64-byte endpoint buffers are associated with physical endpoint 2 and 3.

For physical endpoints 4 and 5, the endpoint buffers are located outside of the module. The endpoints data are transferred to and fro through the IP Fifo bus interface (IPFI) connecting to the IQUE module. This architecture facilitates an optimum sustained data transfer between other on-chip module and the USB20 module.

1.2 Features

Features of the USB20 module includes:

- Universal Serial Bus Specification 2.0 full-speed and high-speed device functions.
  - 480 Mbps data rate for high-speed operation
  - 12Mbps data rate for full-speed operation
  - Handles USB protocol
  - Handles USB device states
  - SYNC/EOP generation and checking
  - Supports chirp mechanism for high speed recognition
  - data and clock recovery from serial stream on the USB
  - Bit-stuffing/unstuffing and bit stuff error detection
  - Supports USB2.0 Test Mode
  - Supports PING protocol
  - Supports high speed isochronous data toggle scheme
  - Perform CRC with CRC5 checking and CRC16 generation and checking
  - Maintains data toggle bits
- Endpoint Configuration

  - one default control IN/OUT endpoint and 5 independent configurable physical endpoints.
  - Physical Endpoint 1 (default IN/OUT endpoint) with 64-byte transmit buffer, 64-byte receive buffer and 8-byte dedicated receive buffer for setup packet.
  - Physical Endpoint 2 and 3 each associate with 64-byte endpoint buffer.
  - Physical Endpoint 4 and 5 each associate with a buffer located in the IQUE module accessible through the IPF Interface. Single buffer and double buffer can be configured in the IQUE module.
- Suspend and resume operations with remote wakeup support
- USB generated interrupts:
  - Suspend interrupt
  - Resume interrupt
  - Transfer complete interrupt
  - Setup packet interrupt
  - Start-of-frame interrupt
  - Transfer error interrupt
  - USB reset interrupt
- STALL, NAK and ACK handshake generation
  - Support automatic double buffering for both transmit and receive packet for physical endpoints 4 and 5. When endpoint 4 is configured for Bulk OUT operation NYET, ACK and NAK handshake will be generated automatically per number of receive buffers available.

1.3 Modes of Operation

The USB20 module will support the following modes of operation

- Run Mode

  Normal USB device operation when the chip is in run mode and module is enabled

- Suspend Mode

  When suspend condition at the USB bus is detected by the USB20 module and the HCS12 enable suspend operation in the USB20 module. The USB20 module will enter a low power suspend mode. The USB20 will exit suspend mode when a resume or reset condition is detected on the USB bus, this will in turn generate an interrupt to the HCS12 and report the condition accordingly. The second possible means of exiting suspend is through remote wakeup operation, in this case the HCS12 will initiate the resume operation in the USB20 module.

Section 2 External Signal Description

2.1 Overview

The USB20 module has the external signals as listed in **Table 2-1**.

Table 2-1 Signal Properties

Name	Port	Function	Reset State	Pull up
DMF	—	USB D- data line (Full Speed)	—	—
DMH	—	USB D- data line (High Speed)	—	—
DPF	—	USB D+ data line (Full Speed)	—	—
DPH	—	USB D+ data line (High Speed)	—	—
RPU	—	USB D+ pull up resistor termination	—	—
RREF	—	External bias resistor input	—	—
VSSA	—	Analog ground	—	—
VSSA1	—	Analog ground 1	—	—
VDDA	—	analog 3.3V generated from internal regulator	—	—

2.2 Detailed Signal Descriptions

The following subsections describe each external signals separately

2.2.1 DMF - USB D- data line (Full speed)

DMF is the analog input output line associated with the on chip full-speed driver and differential data receiver. This is also used as the line termination for high-speed operation where the DMF driver drives to ground.

2.2.2 DMH - USB D- data line (High speed)

DMH is the analog input output line associated with the on chip high-speed current driver and differential data receiver for high-speed data communication. A current source derived from a positive supply is switched into DMH to signal a K state. The normal value of the current source is 17.78mA.

2.2.3 DPF - USB D+ data line (Full speed)

DPF is the analog input output line associated with the on chip full-speed driver and differential data receiver. This is also used as the line termination for high-speed operation where the DPF driver drives to ground.

2.2.4 DPH - USB D+ data line (High speed)

DPH is the analog input output line associated with the on chip high-speed current driver and differential data receiver for high-speed data communication. A current source derived from a positive supply is switched into DPH to signal a J state. The normal value of the current source is 17.78mA.

2.2.5 PRU - USB D+ pull up resistor termination

PRU is an analog input for USB20 module DPF line termination. A 1.5k Ohm pull-up resistor to 3.3V should be connected to this pin for full speed device recognition by the hub or host port upstream.

2.2.6 RREF External bias resistor

RREF is an analog input for the USB physical layer interface, a 510 Ohm reference resistor should be connected to this pin for proper operation of the on chip digital lock loop DLL for frequency synthesis.

2.2.7 VSSA, VSSA1

Analog ground for USB PHY analog module

2.2.8 VDDA

Analog 3.3V supply generated from internal voltage regulator for supplying external 1.5k pull up resistor.

Section 3 Memory Map/Register Definition

Table 3-1shows the registers associated with the USB20 module

Table 3-1 Module Memory Map

Address	Use	Access
$0000-$0001	USB20 Module Control Register (UMCR)	R/W
$0002-$0003	USB20 Module Status Register 1 (UMSR1)	R/W
$0004-$0005	USB20 Interrupt Mask Register (UIMR)	R/W
$0006-$0007	Reserved[1]	—
$0008-$0009	USB20 Test Register (UTR)[2]	R/W
$000A-$000B	USB20 Timestamp Register (UTSR)	R/W
$000C-$000D	USB20 Configuration Control Status Register (UCCSR)	R/W
$000E-$000F	USB20 Endpoint and Configuration Select Register (UEPCSELR)	R/W
$0010-$0013	USB20 UDC Configuration Register (UUCFGR)	R/W
$0014-$0015	USB20 Endpoint Control Status Register 0 (UEPCSR0)	R/W
$0016-$0017	USB20 Endpoint Control Status Register 1 (UEPCSR1)	R/W
$0018-$0019	USB20 Endpoint Control Status Register 2 (UEPCSR2)	R/W
$001A-$001B	USB20 Endpoint Control Status Register 3 (UEPCSR3)	R/W

Table 3-1 Module Memory Map

$001C-$001D	USB20 Endpoint Control Status Register 4 A (UEPCSR4A)	R/W
$001E-$001F	USB20 Endpoint Control Status Register 4 B (UEPCSR4B)	R/W
$0020-$0021	USB20 Endpoint Control Status Register 5 A(UEPCSR5A)	R/W
$0022-$0023	USB20 Endpoint Control Status Register 5 B (UEPCSR5B)	R/W
$0024-$0025	Reserved	R/W
$0026-$0037	Reserved	—
$0038-$003F	USB20 Setup Data Buffer (USTB)	R/W
$0040-$007F	Reserved	—
$0080-$00BF	USB20 Endpoint Local Buffer (UEPLB0)	R/W
$00C0-$00FF	USB20 Endpoint Local Buffer (UEPLB1)	R/W

NOTES:
1. Read to Reserved location will return 0, all write will be ignored.
2. Register UTR is intended for factory test purposes only.

3.1 Register Descriptions

This section consists of register descriptions in address order.

3.1.1 USB20 Module Control Register (UMCR)

Address Offset: $0000 (UMCR)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	MEN	MCE	0	RESUME	SPHY	0	0	0	0	0	DISCON	SDSUP	EXSPD	RWUC	SPWR	SCSUP
W			MRST			PHYRST	EPRST									
RESET:	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-1 USB20 Module Control Register (UMCR)

MEN — Module Enable

This bit is used to enable or disable the USB20 module operation.
1 = USB20 module is enabled.
0 = USB20 module is disabled.

MCE — Module Clock Enable

This bit is used to enable or disable the clock to the USB20 module. It can only be set or clear when MEN = 0.
1 = clock to USB20 module is enabled.
0 = clock to USB20 module is disabled.

MRST — Module Reset

This write only bit is used to reset the USB20 module except the PHY submodule. Writing a 1 to this bit will reset the USB20 module except MCE bit, while a 0 has no effect. This bit can only be written when MEN = 0 and MCE = 1. This bit will always read back as 0.

RESUME — Remote Wakeup Indication

This bit is used to request the PHY to generate the RESUME request to the host. When this bit is set to 1, remote wakeup feature enabled by host and SPHY = 0, the USB20 module will initiate remote wakeup. This bit can only be written to 1 when MEN = 0 and MCE = 1.

1 = request remote wakeup.
0 = No remote wakeup requested.

SPHY — Suspend PHY

This bit is used to request the PHY to enter suspend mode and it will not generate a 60MHz clock for use by the CRG_U. This is usually used to enter a power reduced mode when Suspend state is detected. When this bit is 1 the PHY will be put into suspend mode. This bit can only be written when MCE = 1 and PLLSEL (in CRG_U) = 0.

1 = Suspend the PHY module.
0 = Normal PHY operation.

PHYRST — Physical Layer Reset

This write only bit is used to reset the Physical Layer of the USB20 module. Writing a 1 to this bit will reset the Physical Layer, while a 0 has no effect. This bit can only be written when MEN = 0 and MCE = 1 and PLLSEL (in CRG_U) = 0. This bit will always read back as 0.

EPRST — Endpoint Reset

This write only bit is used to reset all the endpoint control status registers, USSC, URSC, SETOVR and SETUP bits in UMSR1 in the USB20 module. Writing a 1 to this bit will perform the reset, while a 0 has no effect. This bit can only be written when MEN = 0 and MCE = 1. This bit will always read back as 0.

DISCON — Device Disconnect

This bit is used to disable the drivers and terminations on D+ and D- lines and put the USB bus into high impedance state. When this bit is set to 1, the USB20 module will put the USB bus into high impedance state. This bit can only be written when MEN = 0 and MCE = 1.

1 = Device Disconnect.
0 = Normal operation on USB Bus.

SDSUP — Set Descriptor Command Support

This bit when set to 1, the USB20 will accept a Set Descriptor command and the 8-byte of setup data will be available to the application in the setup data buffer for further decoding and respond by the system firmware. When the bit is set to 0, the USB20 will not support the Set Descriptor command and will issue a STALL handshake during the Data and Status phases of the command. The setup data will not be available to the application in this case. This bit can only be written when and MCE = 1.

1 = Set Descriptor command is supported.
0 = Set Descriptor command is not supported.

EXSPD — Expected Speed

This bit is used to configure the expected speed. When this bit is set to 1, the USB20 module will not output the chirp handshake during reset. If the bit is set to 0, the USB20 module will attempt the high speed detection protocol during reset. This bit can only be written when MEN = 0 and MCE = 1.

1 = Expected Speed is full-speed.

0 = Expected Speed is high-speed.

RWUC - Remote Wakeup Capable

This bit is used to select if the device support remote wakeup. This information is required to be passed to the host in response to the Get Status command. This bit can only be written when MEN = 0 and MCE = 1.

1 = The device is remote wakeup capable.

0 = The device does not support remote wakeup.

SPWR - Self Powered

This bit is used to select if the device is self power or bus power. This information is required to be passed to the host in response to the Get Status command. This bit can only be written when MEN = 0 and MCE = 1.

1 = Indicates self-powered device.

0 = Indicates bus-powered device.

SCSUP - Synch Frame command Support

This bit when set to 1, the USB20 will accept a Synch Frame command and the 8-byte of setup data will be available to the application in the setup data buffer for further decoding and respond by the system firmware. When the bit is set to 0, the USB20 will not support the Synch Frame command and will issue a STALL handshake during the Data and Status phases of the command. The setup data will not be available to the application in this case. This bit can only be written when MEN = 0 and MCE = 1.

1 = Synch Frame command is supported.

0 = Synch Frame command is not supported.

3.1.2 USB20 Module Status Register 1 (UMSR1)

Address Offset: $0002 (UMSR1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	ACTEP			USSC	URSC	ENUMD	0	0	0	SPD	0	USD	URD	SOF	SETOVR	SETUP
W																
RESET:	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-2 USB20 Module Status Register 1 (UMSR1)

ACTEP — Active Endpoint

Indicate the current active endpoint having transaction in progress. This field is intended for system firmware debug and testing only.

Table 3-2 ACTEP Field Value

Value	Active Endpoint
000	Physical Endpoint 0
001	Physical Endpoint 1
010	Physical Endpoint 2
011	Physical Endpoint 3
100	Physical Endpoint 4
101	Physical Endpoint 5
110	Physical Endpoint 6
111	No transaction in Progress

USSC — USB20 Suspend Status Change

Indicates that the USB20 module has detected a suspend status change since last clearing of this bit. Writing a 1 to this bit will clear this status bit to 0.

1 = suspend status change detected.

0 = no suspend status change since last clearing of this bit.

URSC — USB20 Reset Status Change

Indicates that the USB20 module has detected a reset status change since last clearing of this bit. Writing a 1 to this bit will clear this status bit to 0.

1 = reset status change detected.

0 = no reset status change since last clearing of this bit.

ENUMD — Enumeration Done

This bit will be asserted high when the chirp handshake has completed.

1 = Enumeration is completed.

0 = Enumeration in Progress or reset has not been detected.

SPD — Set Endpoint Configuration Request

This signal indicates the result of chirp handshake. If the device connects to 1.1 host controller or hub, then after enumeration, the SPD field will indicate that the USB20 module is operating in full speed mode. If the device connects to 2.0 host controller or hub, then after enumeration, the SPD field will indicate that the USB20 is operating in high speed mode. The field data is only valid when ENUMD is 1.

Table 3-3 SPEED Field Value

Value	Meaning
0	High Speed
1	Full Speed

USD — USB Suspend Detected

This bit will be asserted high when suspend state on the bus is detected by the USB20 module.

1 = Suspend state detected on the bus.
0 = The bus is not in suspend state.

URD - USB Reset Detected

This bit will be asserted high when reset state on the bus is detected by the USB20 module.
1 = Reset state detected on the bus.
0 = USB not in reset state.

SOF — Start of Frame

Indicates that the USB20 module has received a valid Start of Frame token. This bit means a SOF and a micro SOF is detected in full-speed opertion and high-speed operation respectively. Note that the USB20 module will not synthesize missing SOF, hence user firmware should keep track of the number of missing SOF token using a local timer and update the frame number accordingly if required. Writing a 1 to this bit will clear this status bit to 0.
1 = SOF token detected.
0 = no SOF token detected since last clearing of this bit.

SETOVR - USB Setup Command Overrun

This bit will be asserted high when SETUP is 1 and a new setup command of type class or vendor, and standard request GET_DESCRIPTOR is received. The old setup token will be overwritten by the new setup token. Writing a 1 to this bit will clear this status bit to 0.
1 = setup token overrun condition has occur
0 = no setup token overrun since last clearing of this bit.

SETUP - USB Setup Command Detected

This bit will be asserted high when setup command is a GET_DESCRIPTOR, class specific or vendor specific command. All other standard setup command is processed by the USB20 module automatically and will not set this bit. Writing a 1 to this bit will clear this status bit to 0.
1 = setup token was received
0 = no setup token received since last clearing of this bit.

3.1.3 USB20 Interrupt Mask Register (UIMR)

Address Offset: $0004 (UIMR)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	RESUMEIE	SETECRIE	USSCIE	URSCIE	0	0	0	0	0	0	0	0	SOFIE	SETOVRIE	SETUPIE
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-3 USB20 Interrupt Mask Register (UIMR)

RESUMEIE — Resume Interrupt Enable

When this bit is set, the interrupt associated with USD = 0, resume detected, will generate an interrupt.
1 = Enable interrupt associated with USD = 0.
0 = Disable interrupt associated with USD = 0 .

SETECRIE — Set Endpoint Configuration Request Interrupt Enable

When this bit is set, the interrupt associated with SETECR bit in UCCSR register will generate an interrupt.
1 = Enable interrupt associated with SETECR.
0 = Disable interrupt associated with SETECR.

USSCIE — USB20 Suspend Status Change Interrupt Enable

When this bit is set, the interrupt associated with USSC bit in UMSR1 register will generate an interrupt.
1 = Enable interrupt associated with USSC.
0 = Disable interrupt associated with USSC.

URSCIE — USB20 Reset Status Change Interrupt Enable

When this bit is set, the interrupt associated with URSC bit in UMSR1 register will generate an interrupt.
1 = Enable interrupt associated with URSC.
0 = Disable interrupt associated with URSC.

SOFIE — Start of Frame Inter rupt Enable

When this bit is set, the interrupt associated with SOF bit in UMSR1 register will generate an interrupt.
1 = Enable interrupt associated with SOF.
0 = Disable interrupt associated with SOF.

SETOVFIE — Setup Command Overrun Interrupt Enable

When this bit is set, the interrupt associated with SETOVF bit in UMSR1 register will generate an interrupt.
1 = Enable interrupt associated with SETOVF.
0 = Disable interrupt associated with SETOVF.

SETUPIE — Setup Command Interrupt Enable

When this bit is set, the interrupt associated with SETUP bit in UMSR1 register will generate an interrupt.
1 = Enable interrupt associated with SETUP.
0 = Disable interrupt associated with SETUP.

3.1.4 USB20 Test Register (UTR)

Address Offset: $0008 (UTR)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	TME	USD	0	TMS	
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-4 USB20 Test Register (UTR)

TME — Test mode enable

Enable one of the USB20 test modes, this bit can only be set when TMS field is not 00. It canan be written to 0 anytime.

1 = Enable USB20 test mode

0 = Disable USB20 test mode

USD — UDC Scale Down

The bit is used to enable a shorter timer for enumeration and suspend/resume operation. This bit can only be written to 1 when in special modes.

1 = Enable USB20 scale down test feature.

0 = Normal operation.

TMS — Test mode select

The field selects one of the test modes and normal operating mode of the USB20 module. This field can be set to 0 at any time but can only be written to value other than 0 when in special mode. The test mode will be entered when TME is set.

Table 3-4 Test mode select field value

Value	Meaning
00	Normal Operation
01	UTMI observe test mode
10	UDC test mode
11	PHY test mode

3.1.5 USB20 Timestamp Register (UTSR)

Address Offset: $000A (UTSR)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	TIMEST										
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-5 USB20 Timestamp Register (UTSR)

TIMEST[10:0] — Start of Frame SOF frame number.

This field is read only and indicate the frame number associated with the last SOF token received. Since the USB20 module will not synthesize missing start of frame. This field will not be updated when the SOF token is corrupted or missing.

3.1.6 USB20 Configuration Control Status Register (UCCSR)

Address Offset: $000C (UCCSR)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CFGVALID	INTFVALID	SETECR	DONEECRU	CFG				INTF				ALTINTF			
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-6 USB20 Configuration Control Status Register (UCCSR)

This register reflect the configuration state of the USB20 module per Set Configuration/Set Interface command from the USB Host . It is also used to acknowledge that the system firmware has successfully updated the Endpoint Configuration Register per the Set Configureation/Set Interface request.

CFGVALID — Configuration Valid

Indicates that the USB20 module has received a valid Set Configuration Command from the host and the value in the CFG field is valid.

1 = CFG field is valid.

0 = CFG field is not valid

INTFVALID — Interface/Alternate Setting Valid

Indicates that the USB20 module has received a valid Set Interface Command from the host and the value in the INTF and ALTINTF fields are valid.

1 = INTF and ALTINTF fields are valid.
0 = INTF and ALTINTF fields are not valid.

SETECR — Set Endpoint Configuration Request

Indicates that USB20 module currently sending NAK handshake to the status IN command from the host. The status IN command is related to Set Configuration/Set Interface command. The firmware should update the Endpoint Control Registers (UEPCR) per the requested Configuration, Interface and Alternate Setting. Then the DONEECRU bit should be set to acknowledge this request.
1 = Set Configuration/Set Interface command is in progress and require service.
0 = No Set Configuration/Set Interface command is in progress or has been serviced.

DONEECRU — Done Endpoint Configuration Update

This bit is can be read and written to 0 any time; it can only be written to 1 when SETECR bit is set to 1. This bit is an acknowledge to SETECR request that the firmware has completed the update to the Endpoint Control Registers (UECR). SETECR will be negated upon setting the DONEECRU bit. This bit will be reset to 0 upon the negation of SETECR bit by the USB20 module.
1 = Indicates that updates to Endpoint Configuration Register is completed per SETECR request.
0 = No action.

CFG[3:0] — Current Configuration

This field indicate the current configuration of the USB20 module selected by the host using Set Configuration command. The value of the field is only valid when CFGVALID is 1.

INTF[3:0] — Current Interface

This field indicate the current interface of the USB20 module selected by the host using Set Interface command. The value of the field is only valid when INTFVALID is 1.

ALTINTF[3:0] — Current Alternate Setting

This field indicate the current interface of the USB20 module selected by the host using Set Interface command. The value of the field is only valid when INTFVALID is 1.

3.1.7 USB20 Endpoint and Configuration Select Register (UEPCSELR)

Address Offset: $000E (UEPCSELR)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	UCRSEL				0	EPBSEL1			0	EPBSEL0		
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-7 USB20 Endpoint and Configuration Select Register (UEPCSELR)

UCRSEL— USB20 Configuration Register Select

This field selects one of the configuration register accessible through UUCFGR.

Table 3-5 UCRSEL Field Values

Value	Meaning
0000	Reserved
0001	Physical Endpoint 1 configuration (UPECFGR1) accessible through UUCFGR
0010	Physical Endpoint 2 configuration (UPECFGR2) accessible through UUCFGR
0011	Physical Endpoint 3 configuration (UPECFGR3) accessible through UUCFGR
0100	Physical Endpoint 4 configuration (UPECFGR4) accessible through UUCFGR
0101	Physical Endpoint 5 configuration (UPECFGR5) accessible through UUCFGR
0110	Reserved
0111	Reserved
1000	Number of configurations and interfaces register (UNCIR) accessible through UUCFGR
1001	Number alternate settings register (UNASR) accessible through UUCFGR
1010	Reserved
1011	Reserved
1100	Reserved
1101	Reserved
1110	Reserved
1111	Reserved

EPBSEL1— Endpoint Buffer Select 1

This field selects one of the 64-bytes local endpoint buffer accessible through UEPLB1. Note that there is no local endpoint buffer associated with physical endpoints 4 and 5.

Table 3-6 EPBSEL1 Field Values

Value	Meaning
0000	Local Endpoint Buffer Associated with Physical Endpoint 1 (IN) accessible through UEPLB1
0001	Local Endpoint Buffer Associated with Physical Endpoint 1 (OUT) accessible through UEPLB1
0010	Local Endpoint Buffer Associated with Physical Endpoint 2 accessible through UEPLB1
0011	Local Endpoint Buffer Associated with Physical Endpoint 3 accessible through UEPLB1
0100	Reserved
0101	Reserved
0110	Reserved
0111	Reserved

EPBSEL0— Endpoint Buffer Select 0

This field selects one of the 64-bytes local endpoint buffer accessible through UEPLB0. Note that there is no local endpoint buffer associated with physical endpoints 4 and 5.

Table 3-7 EPBSEL0 Field Values

Value	Meaning
0000	Local Endpoint Buffer Associated with Physical Endpoint 1 (IN) accessible through UEPLB0
0001	Local Endpoint Buffer Associated with Physical Endpoint 1 (OUT) accessible through UEPLB0

Table 3-7 EPBSEL0 Field Values

Value	Meaning
0010	Local Endpoint Buffer Associated with Physical Endpoint 2 accessible through UEPLB0
0011	Local Endpoint Buffer Associated with Physical Endpoint 3 accessible through UEPLB0
0100	Reserved
0101	Reserved
0110	Reserved
0111	Reserved

3.1.8 USB20 UDC Configuration Register (UUCFGR)

The definition of this UDC Configuration Register (UUCFGR) located at $0010 is dependent on the value of the UCRSEL field of the UEPCSELR register. Below sections shows the bit field definition with different UCRSEL setting.

3.1.8.1 USB20 Physical Endpoint Configuration Register (UPECFGRn)

When UCRSEL field of UEPCSELR is selecting one of the physical endpoint configuration register (UPECFGRn) the register bit field is as follows:

Address Offset: $0010 (UPECFGRn)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	NISOF		MAXPSZ											EPASET		
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	EPASET		EPINTF			EPCFG				EPTYPE		EP-DIR	EPNUM			
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-8 USB20 Physical Endpoint Configuration Register (UPECFGRn)

This 32-bit read/write register is used for physical endpoint configuration. This register only support 32-bit write which is archieved by writing the high order 16-bit word (at lower address) and then the low order 16-bit word (at higher address). The actual write operation will be performed when the low order word is written.

NISOF — Number of Isochronous IN commands per Microframe

Reserved field if non high speed isochronous IN endponts. If the endpoint is high speed isochronous IN endpoint, this field indicates the number of isochronous IN commands the application will send in a given microframe.

Table 3-8 NISOF Field Values

Value	Meaning
00	Use only DATA0 pid for all transfer from this endpoint.
01	Use only DATA0 pid for all transfer from this endpoint.
10	Use DATA1 pid for first transfer and DATA0 pid for the second transfer in a given microframe from this endpoint.
11	Use DATA2 pid for the first transfer and DATA1 pid for the second transfer and DATA0 for the third transfer in a given microframe from this endpoint.

MAXPSZ — Maximum Packet Size

Indicates the maximum packet size that the endpoint can support.

EPASET — Endpoint Alternate Setting

Indicates the alternate setting that the endpoint belongs to.

EPINTF — Endpoint Interface

Indicates the interface that the endpoint belongs to.

EPCFG — Endpoint Configuration

Indicates the configuration that the endpoint belongs to.

EPTYPE — Endpoint Type

The transfer type that the endpoint is supporting

Table 3-9 Endpoint Type

Value	Meaning
00	Control
01	Isochronous
10	Bulk
11	Interrupt

EPDIR — Endpoint Direction

Indicates the endpoint direction that the endpoint belongs to.

1 = In

0 = Out

EPNUM — Endpoint Number

Indicates the endpoint number that the endpoint belongs to.

Below is a summary of valid settings for the UUCFGR for the different physical endpoint.

Table 3-10 Summary of Valid settings for UUCFGR

Physical Endpoint	NISOF	MAXPSZ[1]	EPASET	EPINTF	EPCFG	EPTYPE[2]	EPDIR[3]	EPNUM
1[4]	0	*[5]	0	0	0	00	0[6]	0
2	0	*	*	*	*	10/11	1/0	*[7]
3	0	*	*	*	*	10/11	1/0	*
4	*	*	*	*	*	01/10/11	0	*
5	*	*	*	*	*	01/10/11	1	*

NOTES:
1. MaxPktSize must be selected according to USB 2.0 specification, and not exceed the endpoint buffer size allocated to the physical endpoint.
2. Endpoint type must be selected from those listed for each endpoint, operation with other value is not specified.
3. Endpoint Direction must be selected from those listed for each endpoint, operation with other value is not specified.
4. Physical endpoint 1 is assoicated with the default endpoint 0 IN/OUT, all fields of the UPECFGR must be set as shown.
5. All entries with * should be set in accordance to application requirements.
6. This is actually a bidirectional endpoint.
7. EPNUM field marked with * should only have values from 1 to 3. EPNUM = 3 should only be assigned to one and only one Physical endpoint.

3.1.8.2 USB20 Number of Configurations/Interfaces Register (UNCIR)

When UCRSEL field of UEPCSELR is selecting the number of configuration/interface register (UNCIR) the register bit field is as follows:

Address Offset: $0010 (UNCIR)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	NINTC2			0	NINTC1			0	0	NCFG	
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-9 USB20 Number of Configurations/Interfaces Register (UNCIR)

This 32-bit read/write register is used for endpoint configuration. This register only support 32-bit write which is archieved by writing the high order 16-bit word (at lower address) and then the low order 16-bit word (at higher address). The actual write operation will be performed when the low order word is written. This register can be read anytime but can only be written when the USB20 module is not enabled.

NINTC2 — Number of Interfaces in Configuration 2

This field sets the maximum number of interfaces for Configuration 2, valid values are from 0 to 4. Values from 5 to 7 are reserved. Set Interface setup command from host when device is in configuration 2 will be accepted when the targeted interface number is less than or equal to this field, otherwise a STALL response will be issued.

NINTC1 — Number of Interfaces in Configuration 1

This field sets the maximum number of interfaces for Configuration 1, valid values are from 0 to 4. Values from 5 to 7 are reserved. Set Interface setup command from host when device is in configuration 1 will be accepted when the targeted interface number is less than or equal to this field, otherwise a STALL response will be issued.

NCFG — Number of Configurations supported

This field sets the maximum number of configurations supported, valid values are from 0 to 2. Value of 3 is reserved. A value of 0 means that the device can only accept deconfiguration setup command, i.e. Set Configuration command with configuration 0. Set Configuration setup command from host will be accepted when the targeted configuration number is less than or equal to this field, otherwise a STALL response will be issued.

3.1.8.3 USB20 Number of Alternate Settings Register (UNASR)

When UCRSEL field of UEPCSELR is selecting the number of alternate settings register (UNASR) the register bit field is as follows:

Address Offset: $0010 (UNASR)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R W	NAI3C2				NAI2C2				NAI1C2				NAI0C2			
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	NAI3C1				NAI2C1				NAI1C1				NAI0C1			
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-10 USB20 Number of Alternate Settings Register (UNASR)

This 32-bit read/write register is used for endpoint configuration. This register only support 32-bit write which is archieved by writing the high order 16-bit word (at lower address) and then the low order 16-bit word (at higher address). The actual write operation will be performed when the low order word is written. This register can be read anytime but can only be written when the USB20 module is not enabled.

NAI3C2 — Number of Alternate Setting in Interface 3 of Configuration 2

This field sets the maximum number of alternate settings in interface 3 for Configuration 2, valid values are from 0 to F. Set Interface setup command addressed to interface 3 from host when device is in configuration 2 will be accepted when the targeted alternate setting number is less than this field, otherwise a STALL response will be issued.

NAI2C2 — Number of Alternate Setting in Interface 2 of Configuration 2

This field sets the maximum number of alternate settings in interface 2 for Configuration 2, valid values are from 0 to F. Set Interface setup command addressed to interface 2 from host when device is in configuration 2 will be accepted when the targeted alternate setting number is less than this field, otherwise a STALL response will be issued.

NAI2C2 — Number of Alternate Setting in Interface 1 of Configuration 2

This field sets the maximum number of alternate settings in interface 1 for Configuration 2, valid values are from 0 to F. Set Interface setup command addressed to interface 1 from host when device is in configuration 2 will be accepted when the targeted alternate setting number is less than this field, otherwise a STALL response will be issued.

NAI2C2 — Number of Alternate Setting in Interface 0 of Configuration 2

This field sets the maximum number of alternate settings in interface 0 for Configuration 2, valid values are from 0 to F. Set Interface setup command addressed to interface 0 from host when device is in configuration 2 will be accepted when the targeted alternate setting number is less than this field, otherwise a STALL response will be issued.

NAI3C1 — Number of Alternate Setting in Interface 3 of Configuration 1

This field sets the maximum number of alternate settings in interface 3 for Configuration 1, valid values are from 0 to F. Set Interface setup command addressed to interface 3 from host when device is in configuration 1 will be accepted when the targeted alternate setting number is less than this field, otherwise a STALL response will be issued.

NAI2C1 — Number of Alternate Setting in Interface 2 of Configuration 1

This field sets the maximum number of alternate settings in interface 2 for Configuration 1, valid values are from 0 to F. Set Interface setup command addressed to interface 2 from host when device is in configuration 1 will be accepted when the targeted alternate setting number is less than this field, otherwise a STALL response will be issued.

NAI2C1 — Number of Alternate Setting in Interface 1 of Configuration 1

This field sets the maximum number of alternate settings in interface 1 for Configuration 1, valid values are from 0 to F. Set Interface setup command addressed to interface 1 from host when device is in configuration 1 will be accepted when the targeted alternate setting number is less than this field, otherwise a STALL response will be issued.

NAI2C1 — Number of Alternate Setting in Interface 0 of Configuration 1

This field sets the maximum number of alternate settings in interface 0 for Configuration 1, valid values are from 0 to F. Set Interface setup command addressed to interface 0 from host when device is in configuration 1 will be accepted when the targeted alternate setting number is less than this field, otherwise a STALL response will be issued.

3.1.9 USB20 Endpoint Control Status Register 0 (UEPCSR0)

Register address $0014 (UEPCSR0)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	STALL	DVALID	TFRC	TCIE	0	0	0	0	0	TXSIZ						
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-11 USB20 Endpoint Control Status Register 0 (UEPCSR0)

This register is associated with the default IN endpoint 0.

STALL - Stall

When this bit is set, protocol STALL handshake will be generated for all transaction associated with this endpoint. This bit will be cleared automatically when a SETUP token is received.

1 = STALL handshake
0 = Normal handshake

DVALID — Data Valid

Indicates the data in the local endpoint buffer is valid. User should set this bit when the endpoint buffer is initialized with data and the correct packet size is set in the RXTXSIZE field. On completion of the IN transaction, this bit will be cleared automatically by the USB20 module. When the bit is 0 all IN data request associated with the endpoint will be NAK.

This bit is set to 0 upon reset.

1 = Data is valid
0 = Data is not valid

TFRC — Transfer Completed

Indicates that a transaction assoicated with this endpoint has just been completed. Writing a 1 to this bit will clear this bit to 0.

1 = Transfer Completed and require firmware attention.
0 = No action

TCIE — Transfer complete interrupt enable

When this bit is set, an interrupt will be generated when the TFRC bit is set to 1.

1 = enable transfer complete interrupt.
0 = disable transfer complete interrupt.

TXSIZ — transmit data size

This field inidcates the size of valid data in the endpoint buffer when the DVALID bit is 1.

3.1.10 USB20 Endpoint Control Status Register 1 (UEPCSR1)

Register address $0016 (UEPCSR1)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	STALL	DVALID	TFRC	TCIE	0	0	0	0	0	RXSIZ						
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-12 USB20 Endpoint Control Status Register 1 (UEPCSR1)

This register is associated with the default OUT endpoint 0.

STALL - Stall

When this bit is set, protocol STALL handshake will be generated for all transactions assocated with this endpoint. This bit will be cleared automatically when a SETUP token is received.

1 = STALL handshake
0 = Normal handshake

DVALID — Data Valid

Indicates the data in the local endpoint buffer is valid. User should wait until the bit is set to 1 by the USB20 module before processing the data in the endpoint buffer which size is qualified by the RXTXSIZE field. On completion of processing of all data associated with the OUT transaction, user should clear the bit to 0 to allow upcoming OUT packet reception. When the bit is 1, all OUT data and PING token associated with the endpoint will be NAK.

This bit is set to 0 upon reset.

1 = Data is valid
0 = Data is not valid

TFRC — Transfer Completed

Indicates that a transaction assoicated with this endpoint has just been completed. Writing a 1 to this bit will clear this bit to 0.

1 = Transfer Completed and require firmware attention.
0 = No action

TCIE — Transfer complete interrupt enable

When this bit is set, an interrupt will be generated when the TFRC bit is set to 1.

1 = enable transfer complete interrupt.
0 = disable transfer complete interrupt.

RXSIZ — received data size

This field inidcates the size of valid data in the endpoint buffer when the DVALID bit is 1.

3.1.11 USB20 Endpoint Control Status Register 2 (UEPCSR2)

Register address $0018 (UEPCSR2)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	STALL	DVALID	TFRC	TCIE	0	0	0	0	0	RXTXSIZ						
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-13 USB20 Endpoint Control Status Register 2 (UEPCSR2)

This register is associated with the physical endpoint 2.

STALL - Stall

When this bit is set, functional STALL handshake will be generated for all transactions assocated with this endpoint. This bit will be cleared automically when a transaction associated with the endpoint is received.

1 = STALL handshake
0 = Normal handshake

DVALID — Data Valid

Indicates the data in the local endpoint buffer is valid. When the associated endpoint is an IN endpoint, user should set this bit when the endpoint buffer is initialized with data and the correct packet size is set in the RXTXSIZE field. On completion of the IN transaction, this bit will be cleared automatically by the USB20 module. When the bit is 0 all IN data request associated with the endpoint will be NAK.

When the associated endpoint is an OUT endpoint, user should wait until the bit is set to 1 by the USB20 module before processing the data in the endpoint buffer which is qualified by the RXTXSIZE field. On completion of processing of all data associated with the OUT transaction, user should clear the bit to 0 to allow upcoming OUT packet reception. When the bit is 1, all OUT data and PING token associated with the endpoint will be NAK.

This bit is set to 0 upon reset

1 = Data is valid
0 = Data is not valid

TFRC — Transfer Completed

Indicates that a transaction assoicated with this endpoint has just been completed. Writing a 1 to this bit will clear this bit to 0.

1 = Transfer Completed and require firmware attention.
0 = No action

TCIE — Transfer complete interrupt enable

When this bit is set, an interrupt will be generated when the TFRC bit is set to 1.
1 = enable transfer complete interrupt.
0 = disable transfer complete interrupt.

RXTXSIZ — receive and transmit data size

This field inidcates the size of valid data in the endpoint buffer qualified by the DVALID bit.

3.1.12 USB20 Endpoint Control Status Register 3 (UEPCSR3)

Register address $001A (UEPCSR3)

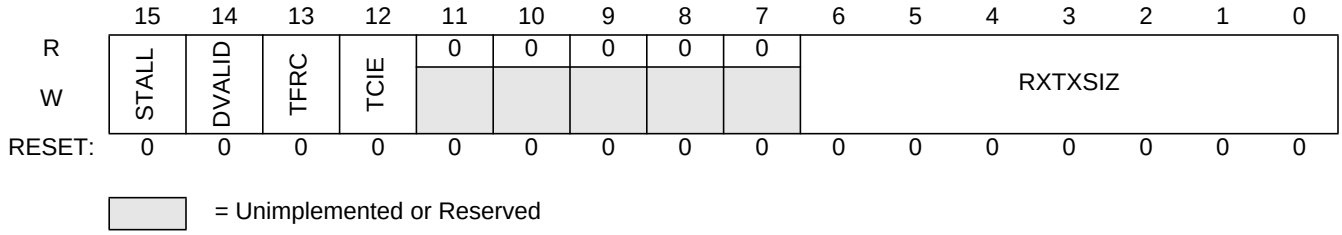

Figure 3-14 USB20 Endpoint Control Status Register 3 (UEPCSR3)

This register is associated with the physical endpoint 3.

STALL - Stall

When this bit is set, functional STALL handshake will be generated for all transactions assocated with this endpoint. This bit will be cleared automically when a transaction associated with the endpoint is received.
1 = STALL handshake
0 = Normal handshake

DVALID — Data Valid

Indicates the data in the local endpoint buffer is valid. When the associated endpoint is an IN endpoint, user should set this bit when the endpoint buffer is initialized with data and the correct packet size is set in the RXTXSIZE field. On completion of the IN transaction, this bit will be cleared automatically by the USB20 module. When the bit is 0 all IN data request associated with the endpoint will be NAK.

When the associated endpoint is an OUT endpoint, user should wait until the bit is set to 1 by the USB20 module before processing the data in the endpoint buffer which is qualified by the RXTXSIZE field. On completion of processing of all data associated with the OUT transaction, user should clear the bit to 0 to allow upcoming OUT packet reception. When the bit is 1, all OUT data and PING token associated with the endpoint will be NAK.

This bit is set to 0 upon reset
1 = Data is valid
0 = Data is not valid

TFRC — Transfer Completed

Indicates that a transaction assoicated with this endpoint has just been completed. Writing a 1 to this bit will clear this bit to 0.

1 = Transfer Completed and require firmware attention.

0 = No action

TCIE — Transfer complete interrupt enable

When this bit is set, an interrupt will be generated when the TFRC bit is set to 1.

1 = enable transfer complete interrupt.

0 = disable transfer complete interrupt.

RXTXSIZ — receive and transmit data size

This field inidcates the size of valid data in the endpoint buffer qualified by the DVALID bit.

3.1.13 USB20 Endpoint Control Status Register 4 A (UEPCSR4A)

Register address $001C (UEPCSR4A)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	STALL	SNAK	TFRC	TCIE	CTERR	RXSIZ										
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-15 USB20 Endpoint Control Status Register 4 A (UEPCSR4A)

This register is associated with the physical endpoint 4. This endpoint must be configured as OUT only. If this physical endpoint is configured as IN, then all transaction will be STALL.

STALL - Stall

When this bit is set, functional STALL handshake will be generated for all transactions assocated with this endpoint. This bit will be cleared automically when a transaction associated with the endpoint is received.

1 = STALL handshake

0 = Normal handshake

SNAK - Send NAK

When this bit is set, NAK handshake will be generated for all transactions assocated with this endpoint. It is also recommended to set this bit and NAK all incoming USB traffic addressed to this endpoint when the RXSIZ or the associated IQUE channel need to be manipulated by software. When STALL is also set, STALL handshake will be sent instead

1 = NAK handshake

0 = Normal handshake

TFRC — Transfer Completed

Indicates that a transaction assoicated with this endpoint has just been completed. Writing a 1 to this bit will clear this bit to 0.

1 = Transfer Completed and require firmware attention.

0 = No action.

TCIE — Transfer complete interrupt enable

When this bit is set, an interrupt will be generated when the TFRC bit is set to 1.

1 = enable transfer complete interrupt.

0 = disable transfer complete interrupt.

CTERR — Continue on Transfer Error

The bit is for controlling the endpoint to continue to transfer even on tranfer error.

1 = Continue to Transfer even on Transfer Error.

0 = NAK all transfer request on Transfer Error.

RXSIZ — receive data size

This field inidcates the size of data received in the last transaction. When zero length packet is received, no data will be stored to the IQUE thru the associated Queue Channel.

3.1.14 USB20 Endpoint Control Status Register 4 B (UEPCSR4B)

Register address $001E (UEPCSR4B)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SPKT	SPKTIE	TFRERR	TERRIE	EBAVA		0	0	CURMP				MPPB			
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-16 USB20 Endpoint Control Status Register 4 B (UEPCSR4B)

This register is associated with the physical endpoint 4.

SPKT — Short Packet Received

This bit is set by the UDC20 to indicates that a packet with size less than MAXPSZ for this endpoint is received. NAK handshake will be generated when this bit is set. Writing a 1 to this bit will clear this bit to 0.

1 = Last packet is a short packet or zero length packet.

0 = Size of last packet is of size MAXPSZ or no packet has received since activation of the endpoint.

SPKTIE — Short Packet Received interrupt enable

When this bit is set, an interrupt will be generated when the SPKT bit is set to 1.

1 = enable short packet receive interrupt.

0 = disable short packet receive interrupt.

TFRERR — Transfer Error

This bit is set by the USB20 to inidcates that the last transaction has error and the firmware is required to adjust the pointers in the IQUE module to resend (for IN endpoint) or flush (for OUT endpoint) the packet data in the endpoint buffer. In cases where maxpktsize is equals to the IQUE block size this pointer adjustment is done automatically, and this condition will not need any firmware intervention. Hence, user should set CTERR to 0 to allow transfer to continue. All request to this endpoint will be NAK when TFRERR = 1 and CTERR = 0. Writing a 1 to this bit will clear this bit to 0.

1 = Transfer Error has occur.

0 = No Error occur since last reset or clearing of this bit.

TERRIE — Transfer error interrupt enable

When this bit is set, an interrupt will be generated when the TFRERR bit is set to 1.

1 = enable transfer error interrupt.

0 = disable transfer error interrupt.

0 = disable transfer error interrupt.

EBAVA - Number of empty buffer available

This is a read only field valid only when the endpoint is configured for OUT operation. For Bulk OUT operation at high speed, when a packet is receive and this field is 0, then the packet will be NAK; if this field is 01 then the packet will be NYET; if this field is 10 then the packet will be ACK. For other out operations, 00 will NAK the packet while 01 and 10 will ACK the packet.

Table 3-11 EBAVA

Value	Meaning
00	none empty buffer available
01	one empty buffer available
10	two or more empty buffer available
11	Reserved

CURMP — Current maxpkt index

This field indicate the current maxpkt within a buffer that the endpoint is using for next transaction. For OUT endpoint, this field will point to the next empty buffer. For IN endpoint, this field will point to the next maxpkt of valid data to be transfer. This index starts at 0 for beginning of buffer.

MPPB— Maxpkt per Block

This field value plus 1 is the number of maxpkt per buffer. For example in High speed bulk operation, maxpktsize is 512, if the buffer in the IQUE is set also to 512 then this field should be 0. Another example is in full speed bulk operation where maxpktsize is 64, if buffer in the IQUE is also 512 then this field should be set to 7.

3.1.15 USB20 Endpoint Control Status Register 5 A(UEPCSR5A)

Register address $0020 (UEPCSR5A)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	STALL	SNAK	TFRC	TCIE	CTERR	TXSIZ										
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-17 USB20 Endpoint Control Status Register 5 A (UEPCSR5A)

This register is associated with the physical endpoint 5. This endpoint must be configured as IN only. If this physical endpoint is configured as OUT, then all transaction will be STALL.

STALL - Stall

When this bit is set, functional STALL handshake will be generated for all transactions assocated with this endpoint. This bit will be cleared automically when a transaction associated with the endpoint is received.

1 = STALL handshake
0 = Normal handshake

SNAK - Send NAK

When this bit is set, NAK handshake will be generated for all transactions assocated with this endpoint. It is also recommended to set this bit and NAK all incoming USB traffic addressed to this endpoint when the RXSIZ or the associated IQUE channel need to be manipulated by software. When STALL is also set, STALL handshake will be sent instead

1 = NAK handshake
0 = Normal handshake

TFRC — Transfer Completed

Indicates that a transaction assoicated with this endpoint has just been completed. Writing a 1 to this bit will clear this bit to 0.

1 = Transfer Completed and require firmware attention.
0 = No action.

TCIE — Transfer complete interrupt enable

When this bit is set, an interrupt will be generated when the TFRC bit is set to 1.

1 = enable transfer complete interrupt.
0 = disable transfer complete interrupt.

CTERR — Continue on Transfer Error

The bit is for controlling the endpoint to continue to transfer even on tranfer error.

1 = Continue to Transfer even on Transfer Error
0 = NAK all transfer request on Transfer Error

TXSIZ — transmit data size

This field inidcates the size of the next transfer. When sending zero length packet, no data will be fetch from the IQUE module and the packet will be sent indenpendent of the value of BVLD.

3.1.16 USB20 Endpoint Control Status Register 5 B (UEPCSR5B)

Register address $0022 (UEPCSR5B)

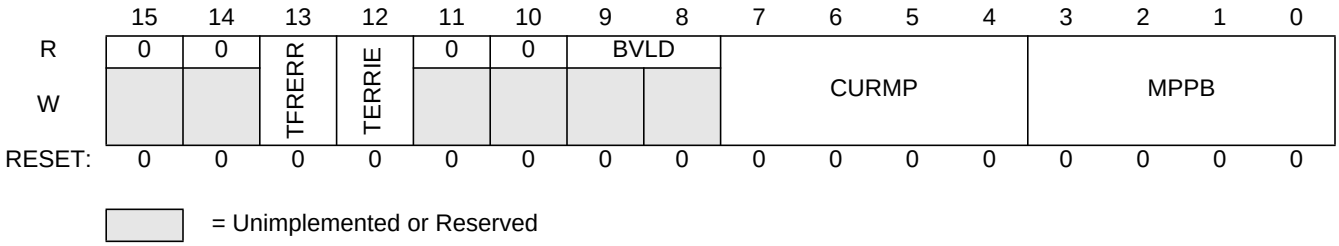

Figure 3-18 USB20 Endpoint Control Status Register 5 B (UEPSR5B)

This register is associated with the physical endpoint 5.

TFRERR — Transfer Error

This bit is set by the USB20 to inidcates that the last transaction has error and the firmware is required to adjust the pointers in the IQUE module to resend (for IN endpoint) or flush (for OUT endpoint) the packet data in the endpoint buffer. In cases where maxpktsize is equals to the IQUE block size this pointer adjustment is done automatically, and this condition will not need any firmware intervention. Hence, user should set CTERR to 0 to allow transfer to continue. All request to this endpoint will be NAK when TFRERR = 1 and CTERR = 0. Writing a 1 to this bit will clear this bit to 0.
1 = Transfer Error has occur.
0 = No Error occur since last reset or clearing of this bit.

TERRIE — Transfer error interrupt enable

When this bit is set, an interrupt will be generated when the TFRERR bit is set to 1.
1 = enable transfer error interrupt.
0 = disable transfer error interrupt.

BVLD - Number of valid buffer

This is a read only field valid only when the endpoint is configured for IN operation. For IN operation, data will be sent when BVLD value is 01 or 10. However, in the case of zero length packet, it will be sent independent of this field as long as STALL and SNAK are both 0.

Table 3-12 BVLD

Value	Meaning
00	no valid data available
01	one buffer of valid data available
10	two or more buffers of valid data available
11	Reserved

CURMP — Current maxpkt index

This field indicate the current maxpkt within a buffer that the endpoint is using for next transaction. For OUT endpoint, this field will point to the next empty buffer. For IN endpoint, this field will point to the next maxpkt of valid data to be transfer. This index starts at 0 for beginning of buffer.

MPPB— Maxpkt per Block

This field value plus 1 is the number of maxpkt per buffer. For example in High speed bulk operation, maxpktsize is 512, if the buffer in the IQUE is set also to 512 then this field should be 0. Another example is in full speed bulk operation where maxpktsize is 64, if buffer in the IQUE is also 512 then this field should be set to 7.

3.1.17 USB20 Setup Data Buffer (USTB)

The Setup Data Buffer is located from $0038 - $003F. This buffer stores the last setup data received. The content is valid only when SETUP = 1.

3.1.18 USB20 Endpoint Local Buffer (UEPLB0)

The Endpoint Local Buffer is located from $0080 - $00BF. Refer to **3.1.7** on selecting the local endpoint buffer to be accessible through this window.

3.1.19 USB20 Endpoint Local Buffer (UEPLB1)

The Endpoint Local Buffer is located from $00C0 - $00FF. Refer to **3.1.7** on selecting the local endpoint buffer to be accessible through this window.

Section 4 Functional Description

In this section individual functional sub blocks of the USB20 module as shown in **Figure 1-1**will be described in details.

4.1 Interrupt Sources

The USB20 module will generate the following interrupts to the S12 core as listed in **Table 4-1**.

Table 4-1 Interrupt Sources

Source	Name	Interrupt Description	Associated Flag (Register)	Associated Enable (Register)	Comment
0	USCI	USB status change	USSC(UMSR1) URSC(UMSR1) USD(UMSR1)	USSCIE(UIMR) URSCIE(UIMR) RESUMEIE(UMIR)	USD = 0, Resume Interrupt is asynchronous and can generate interrupt during stop
1	SOFI	Start of Frame	SOF(UMSR1)	SOFIE(UIMR)	
2	SETUPI	SETUP command related	SETOVR(UMSR1) SETUP(UMSR1)	SETOVRIE(UIMR) SETUPIE(UIMR)	
3	SETECRI	Set Endpoint Configuration Request	SETECR(UCCSR)	SETECRIE(UIMR)	
4	EP0INI	Endpoint 0 IN interrupt	TFRC(UEPCSR0)	TCIE(UEPCSR0)	
5	EP0OUTI	Endpoint 0 OUT interrupt	TFRC(UEPCSR1)	TCIE(UEPCSR1)	
6	EP2I	Physical Endpoint 2 interrupt	TFRC(UEPCSR2)	TCIE(UEPCSR2)	
7	EP3I	Physical Endpoint 3 interrupt	TFRC(UEPCSR3)	TCIE(UEPCSR3)	
8	EP4I	Physical Endpoint 4 interrupt	TFRC(UEPCSR4A) SPKT (UEPCSR4B) TFRERR (UEPCSR4B)	TCIE(UEPCSR4A) SPKTIE (UEPCSR4B) TERRIE (UEPCSR4B)	
9	EP5I	Physical Endpoint 5 interrupt	TFRC(UEPCSR5A) TFRERR (UEPCSR5B)	TCIE(UEPCSR5A) TERRIE (UEPCSR5B)	
10	EP6I	Physical Endpoint 6 interrupt	TFRC(UEPCSR6)	TCIE(UEPCSR6)	

4.2 USB Device Controller (UDC20)

The UDC20 block handles all USB protocol and provides a simple read/write protocol for the HCS12 core. **Figure 4-1** shows a block diagram of the UDC20 block.

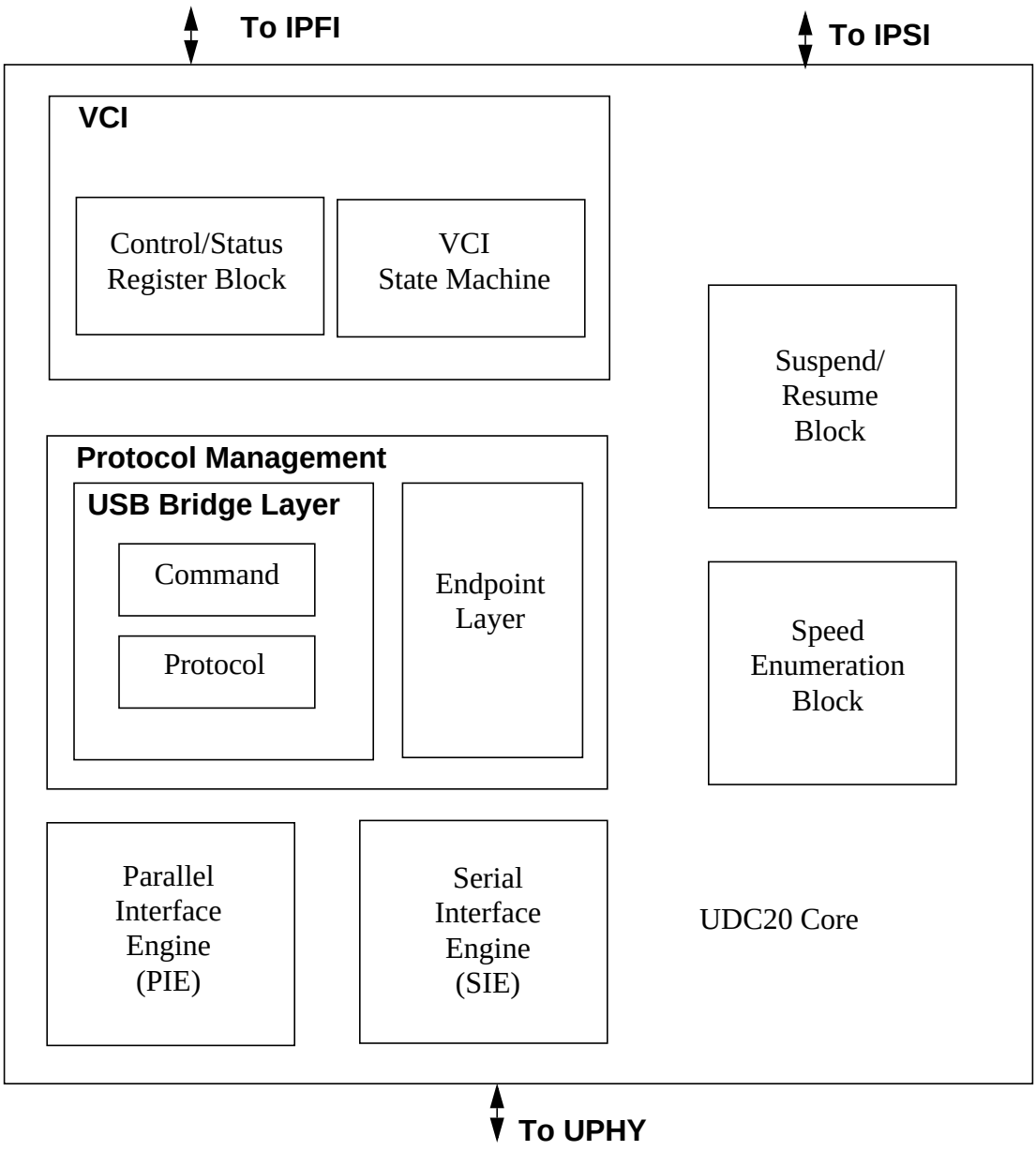

Figure 4-1 UDC20 Block Diagram

4.2.1 Speed Enumeration Block

This block performs all Reset functions, such as detecting Reset, generating chirps, and controlling the pull-up resistor.

4.2.2 Suspend/Resume Block

This block performs all Suspend and Resume functions, such as detecting Suspend and Resume operations and generating Remote Resume.

4.2.3 Parallel Interface Engine (PIE)

This block performs all front-end functions, such as token packet decoding, CRC5 checking, and CRC16 generation and checking. This block is active when the UDC20 core is in high-speed mode.

4.2.4 Serial Interface Engine (SIE)

This block performs all the front-end functions, such as token packet decoding, CRC5 checking, and CRC16 generation and checking. This block is active when the UDC20 core is in full-speed mode.

4.2.5 Protocol Management Block

The Protocol Management Block consists of the Bridge Layer and the Endpoint Layer.

4.2.5.1 Bridge Layer

This block contains a Protocol Layer and a Command Layer. The Protocol Layer controls the PIE by providing handshake signals and transfer data while handling the application bus protocol. The Command Layer stores the information received in the SETUP packet and decodes the SETUP data. The Bridge Layer also handles error recovery and decodes all standard control transfers addressed to endpoint zero. The module is programmed not to decode the Get Descriptor command and pass it to the fimwire for decoding. The Bridge Layer also passes all Vendor/Class commands to the system firmware, so that the application can decode the command and act accordingly. This feature provides the flexibility of using the UDC20 core in multiple applications.

4.2.5.2 Endpoint Layer

This block contains the configuration information of all the endpoints programmed through the IPSI. This info is in turn used by the Bridge layer for USB transaction processing.

4.2.6 Virtual Component Interface

This block has two sub-blocks: the Control/Status register (CSR) and VCI State Machine.

4.2.6.1 Control/Status register

This block contains all the Control and Status registers that are essential for core operation. This block stores each endpoints information regarding endpoint packet size, type, and direction. The CSR also registers the pointers to the descriptors to be read when the Get Descriptor command is received.

4.2.6.2 VCI State Machine

The VCI State Machine transfers data from/to the application with VCI read/write commands. This block runs on the application interface system clock provided by the user. This block generates read cycles to fetch endpoint data from the application when the UDC20 core receives an IN token. The VCI transfers the received data from the UDC20 core to the application by generating write cycles when the UDC20 core receives OUT or SETUP data. After each token (IN, OUT, or SETUP) data transfer, this block generates a Status write to the application.

4.3 USB Physical Layer Interface (UPHY)

The UPHY block handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic. **Figure 4-2** shows the functional sub-blocks in the UPHY block.

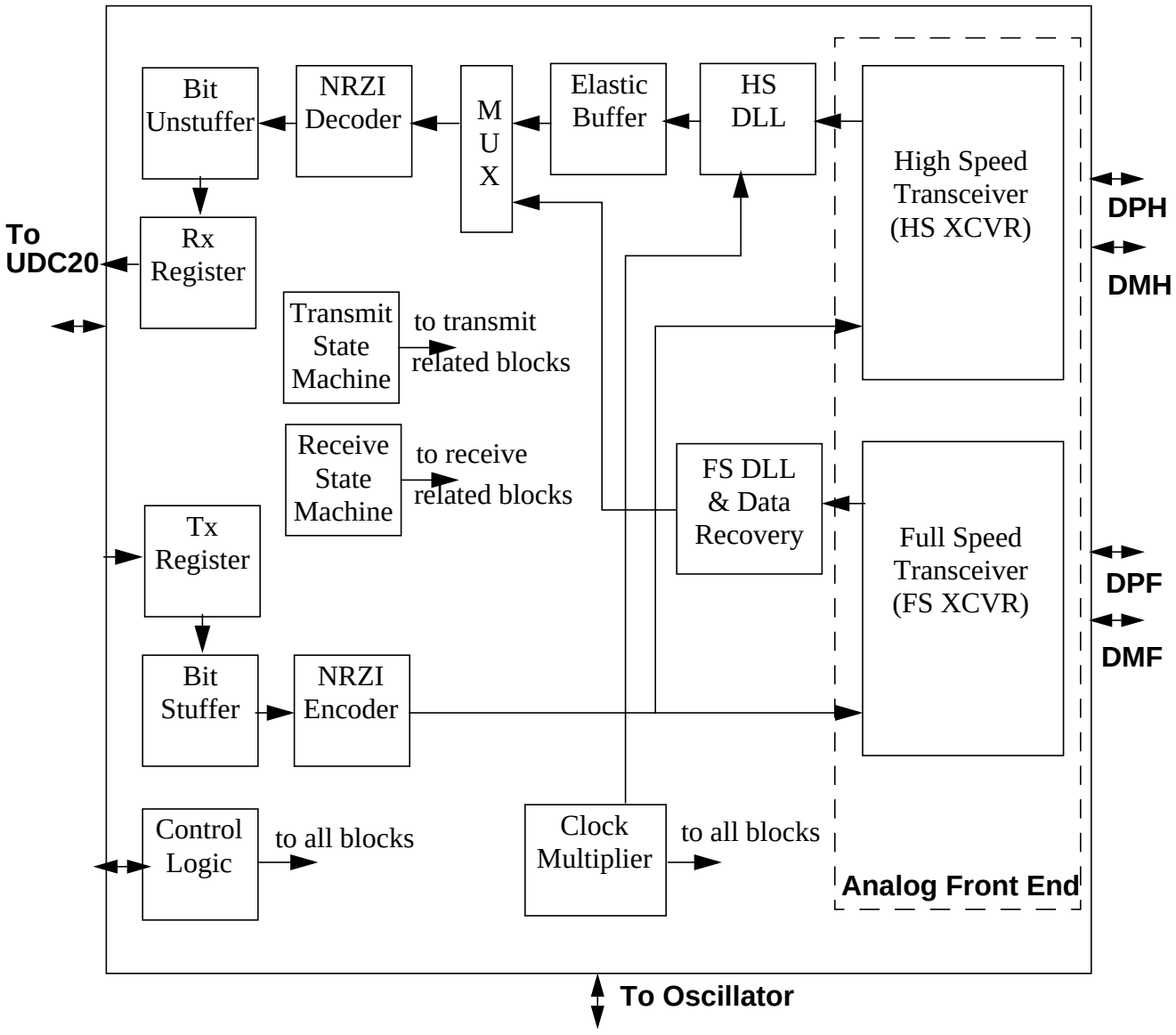

Figure 4-2 UPHY Block Diagram

4.3.1 High Speed Transceiver (HS XCVR)

HS XCVR contains the low-level analog circuitry required to physically interface USB 2.0 signaling to the USB DP/DM signal lines.

4.3.2 Full Speed Transceiver (FS XCVR)

FS XCVR includes the logic necessary to send and receive the FS data on USB. USB 2.0 signaling to the USB DP/DM signal lines.

4.3.3 Clock Multiplier

Clock Multiplier generates the internal clocks for the UPHY and the 60MHz clock for the CRG.

4.3.4 High Speed Delay Line PLL (HS DLL)

DLL extracts clock and data from the data received over the USB 2.0 interface for reception by the Receive Deserializer. The data output from the DLL is synchronous with the local clock.

4.3.5 Elasticity Buffer

Elasticity Buffer is used to compensate for difference between transmitting and receiving clocks. The USB specification defines a maximum clock error of +/- 500 ppm. When the error is calculated over the maximum packet size up to +/- 12 bits of drift can occur. The elasticity buffer is filled to a threshold prior to enabling the remainder of the down stream receive logic.

4.3.6 Multiplexer (MUX)

The MUX block allows the data from the HS or FS receivers to be routed to the shared receive logic.

4.3.7 NRZI Decoder

The NRZI Decoder is compliant to standard USB specification, and it can operate at FS and HS data rates.

4.3.8 Bit Unstuffer

The Bit Unstuffer is compliant to standard USB specification, and it can operate at FS and HS data rates. The bit unstuffer is a state machine, which strips a stuffed 0 bit from the data stream and detects bit stuff errors.

4.3.9 Receive (Rx) Register

Rx Register is in charge of converting serial data received from the USB to parallel data.

4.3.10 Receive State Machine

The block is responsible in decoding downstream USB traffic.

4.3.11 NRZI Encoder

The NRZI Encoder is compliant to standard USB specification, and it can operate at FS and HS data rates.

4.3.12 Bit Stuffer

Bit Stuffer is used by insert a zero after every six consecutive ones in the data stream before the data is NRZI encoded in order to ensure adequate signal transitions. Bit stuffing is enabled beginning with the SYNC Pattern and through the entire transmission. The data one that ends the SYNC Pattern is counted as the first one in a sequence.

4.3.13 Transmit (Tx) Register

Tx Register is responsible for buffering and serializing upstream USB data from the UDC20 before the data is transmitted out from the UPHY

4.3.14 Transmit State Machine

This block is responsible in encoding upstream USB traffic.

4.4 IP Slave Bus Interface (IPSI)

The IPSI will support all HCS12 access to the control and status registers within this block and those control and status register in the UDC20 block. The endpoint buffers for endpoints 0 and 1 in the USB20 module is also access through this interface.

4.5 IP Fifo Bus Interface (IPFI)

The IPFI will support IP FIFO bus for usb endpoint 2 IN/OUT data transfer.

4.6 Endpoint Buffer

This is a SRAM block for used as the Endpoint buffer for the endpoints 0 IN/OUT and 1 IN/OUT. Each endpoint is associated with a 64-byte endpoint buffer.

Block Guide End Sheet

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