PIM_9UF32
Block Guide
V02.05

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TSPG 8/16 Bit MCU
Freescale Semiconductor, Inc.

Revision History

Release Number	Date	Author	Summary of Changes
V00.01	19 Feb 2002	K.N. Chan	Initial version for 1st 912UF32 revision
V00.02	09 May 2002	K.N. Chan	1. Update table Pin Configuration Summary 2. modify the priority in port A, B and E Pin Functions and Priorities Table
V00.03	28 May 2002	K.N. Chan	1. Add 4.9 port U section 2.Modify 4.9 port S to high-impedance inputs during reset
V00.04	10 Jun 2002	K.N. Chan	1. Update Port R and T with 8 channels Timer
V00.05	24 Jun 2002	K.N. Chan	1. Update Port R with SCI
V01.00	08 Sep 2002	K.N. Chan	1. Update with UDC test mode and PHY test mode
V01.01	23 Sep 2002	K.N. Chan	1. Add ipp_ind_exsupen
V02.00	09 Apr 2003	K.N. Chan	Update for 912UF32 production revision 1. Match for the SOC guide - Port A PA[7:0] : CFD[15:8] :ATAD[15:8] - Port B PB[7:0] : CFD[7:0] : ATAD[7:0] 2. Add HRST1Z at PJ0
V02.01	07 Jul 2003	K.N. Chan	Update PPS description and pull state after reset for each port
V02.02	15 Aug 2003	Wai-On Law	1. Added MODRR description. 2. Added 64pin configuration.
V02.03	19 Sep 2003	Wai-On Law	Added pull mode details to pin function tables in sec 2.
V02.04	03 Mar 2004	Wai-On Law	Corrected the MODRR0 bit description.
V02.05	23 Sep 2004	Wai-On Law	1. Improved the MODRR bit description. 2. Removed XCLKS in block diagram. 3. Changed company logo.

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Section 1 Introduction

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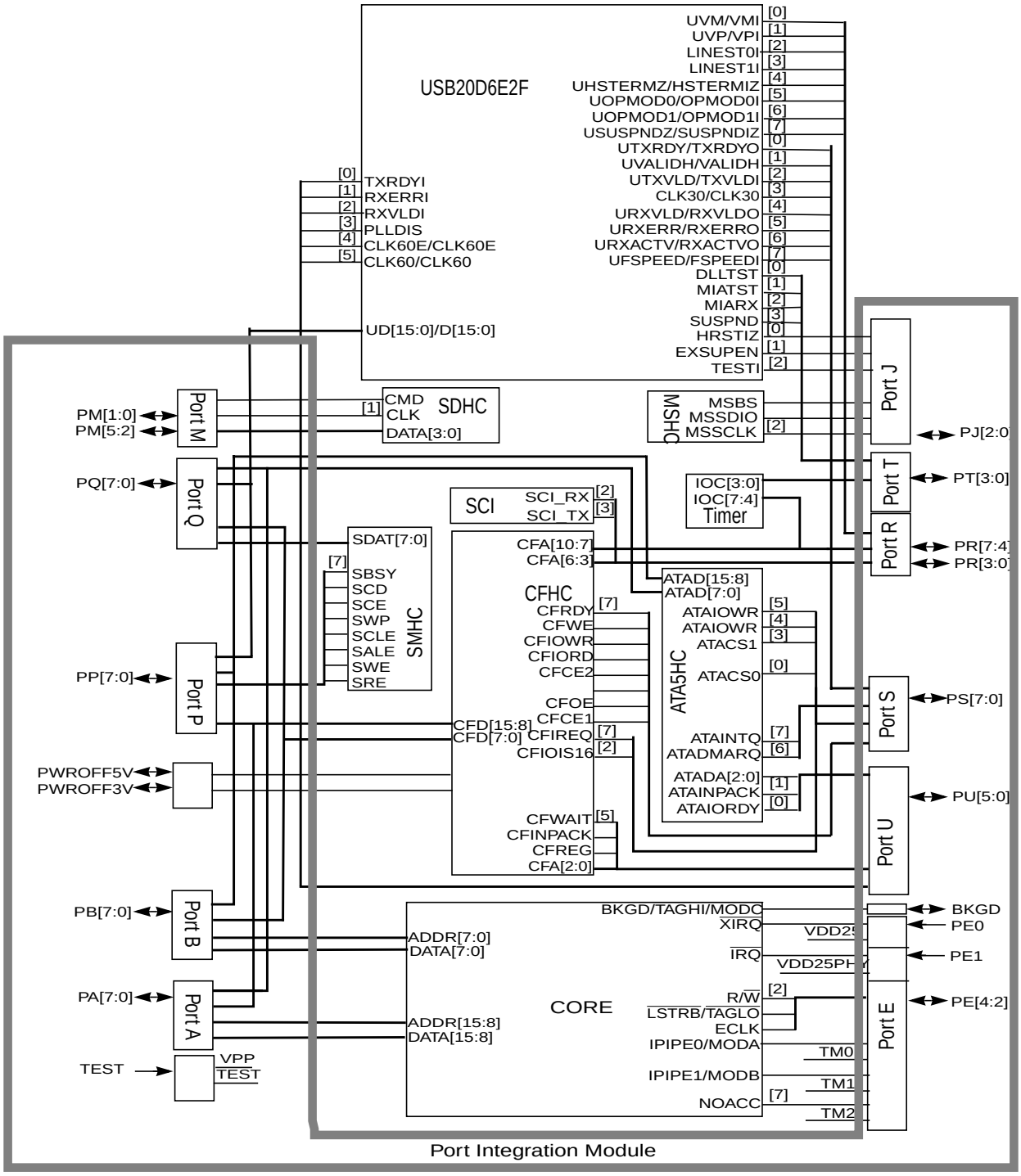

Figure 1-1 PIM_9UF32 Block Diagram

1.1 Overview

The Port Integration Module establishes the interface between the peripheral modules and the I/O pins for all ports except RUP, RREF, XO, XI, DP and DM.

This section covers:

- port A, B and E related to the core logic and multiplexed bus interface,
- port A, B, P, Q, S and U also associated with ATA5HC module
- port T and R associated with TIM module
- port M associated with SDHC module
- port J associated with MSHC module
- port P and Q associated with SMHC module
- port R, S, U, P and Q associated with CFHC module
- port R associated with SCI module
- port Q, P, T, J, T, U, S and R associated with UDC observe mode/PHY test mode

Each I/O pin can be configured by several registers: Input/output selection, drive strength reduction, enable and select of pull resistors and status flags.

The I/O’s of ATA5HC modules can be routed from their default location to determined pins.

The implementation of the Port Integration Module is device dependent.

1.2 Features

The PIM_9UF32 includes the following features:

- Input/output selection
- 3V/5V output drive with two selectable drive strength
- 3V/5V digital and analog input
- Input with selectable pull-up or pull-down device

1.3 Modes of Operation

1.3.1 Run Mode

No low power options exist for this module in run mode.

1.3.2 Wait Mode

No low power options exist for this module in wait mode.

1.3.3 Stop Mode

All clocks are stopped.

Section 2 External Signal Description

2.1 Overview

This section lists and describes the signals that do connect off-chip. All ports start up as general purpose inputs on reset.

2.2 Signal properties

Table 2-1 shows all the pins and their functions that are controlled by the PIM_9UF32. If there is more than one function associated with a pin, the priority is indicated by the position in the table from top (highest priority) to down (lowest priority).

Table 2-1 Pin Functions and Priorities in 100pin Configuration

Port	Pin Name	Pin Function	Description	Pull Mode	Pin Func. (Pull Mode) after Reset
Port E	PE0	$\overline{\text{XIRQ}}$	Non-Maskable interrupt	S12Core[1]	PE0 (Hi-Z)
		PE0	Port E channel 0 5V Input		
	PE1	$\overline{\text{IRQ}}$	Maskable Interrupt	S12Core[1]	PE1 (Hi-Z)
		PE1	Port E channel 1 5V Input		
	PE2	R/$\overline{\text{W}}$	R/W in expanded mode	S12Core[1]	PE2 (Hi-Z)
		PE2	Port E channel 2 5V I/O		
	PE3	$\overline{\text{LSTRB/TAGLO}}$	Low-Byte Strobe/Tag Low	S12Core[1]	PE3 (Hi-Z)
		PE3	Port E channel 3 5V I/O		
	PE4	ECLK	Bus Clock Output	S12Core[1]	PE4 (Hi-Z)
		PE4	Port E channel 4 5V I/O		
	PE5	IPIPE0/MODA	Instruction Queue Tracking Signal 0/Mode Input A	S12Core[1]	PE5 (Hi-Z)
		PE5	Port E channel 5 5V I/O		
	PE6	IPIPE1/MODB	Instruction Queue Tracking Signal 1/Mode Input B	S12Core[1]	PE6 (Hi-Z)
		PE6	Port E channel 6 5V I/O		
	PE7	NOACC	Access	S12Core[1]	PE7 (Hi-Z)
		PE7	Port E channel 7 5V I/O		

Port	Pin Name	Pin Function	Description	Pull Mode	Pin Func. (Pull Mode) after Reset
Port A	PA0	ADDR8/DATA8	Multiplexed Address Data 8	S12Core[1]	PA0 (Hi-Z)
		ATAD08	ATA Data 8	Hi-Z	
		CFD08	CF Data 8	Hi-Z	
		PA0	Port A channel 0 3V/5V I/O	S12Core[1]	
	PA1	ADDR9/DATA9	Multiplexed Address Data 9	S12Core[1]	PA1 (Hi-Z)
		ATAD09	ATA Data 9	Hi-Z	
		CFD09	CF Data 9	Hi-Z	
		PA1	Port A channel 1 3V/5V I/O	S12Core[1]	
	PA2	ADDR10/DATA10	Multiplexed Address Data 10	S12Core[1]	PA2 (Hi-Z)
		ATAD10	ATA Data 10	Hi-Z	
		CFD10	CF Data 10	Hi-Z	
		PA2	Port A channel 2 3V/5V I/O	S12Core[1]	
	PA3	ADDR11/DATA11	Multiplexed Address Data 11	S12Core[1]	PA3 (Hi-Z)
		ATAD11	ATA Data 11	Hi-Z	
		CFD11	CF Data 11	Hi-Z	
		PA3	Port A channel 3 3V/5V I/O	S12Core[1]	
	PA4	ADDR12/DATA12	Multiplexed Address Data 12	S12Core[1]	PA4 (Hi-Z)
		ATAD12	ATA Data 12	Hi-Z	
		CFD12	CF Data 12	Hi-Z	
		PA4	Port A channel 4 3V/5V I/O	S12Core[1]	
	PA5	ADDR13/DATA13	Multiplexed Address Data 13	S12Core[1]	PA5 (Hi-Z)
		ATAD13	ATA Data 13	Hi-Z	
		CFD13	CF Data 13	Hi-Z	
		PA5	Port A channel 5 3V/5V I/O	S12Core[1]	
	PA6	ADDR14/DATA14	Multiplexed Address Data 14	S12Core[1]	PA6 (Hi-Z)
		ATAD14	ATA Data 14	Hi-Z	
		CFD14	CF Data 14	Hi-Z	
		PA6	Port A channel 6 3V/5V I/O	S12Core[1]	
	PA7	ADDR15/DATA15	Multiplexed Address Data 15	S12Core[1]	PA7 (Hi-Z)
		ATAD15	ATA Data 15	Hi-Z	
		CFD15	CF Data 15	Hi-Z	
		PA7	Port A channel 7 3V/5V I/O	S12Core[1]	

Port	Pin Name	Pin Function	Description	Pull Mode	Pin Func. (Pull Mode) after Reset
Port B	PB0	ADDR0/DATA0	Multiplexed Address Data 0	S12Core[1]	PB0 (Hi-Z)
		ATAD00	ATA Data 0	Hi-Z	
		CFD00	CF Data 0	Hi-Z	
		PB0	Port B channel 0 3V/5V I/O	S12Core[1]	
	PB1	ADDR1/DATA1	Multiplexed Address Data 1	S12Core[1]	P (Hi-Z)B1
		ATAD01	ATA Data 1	Hi-Z	
		CFD01	CF Data 1	Hi-Z	
		PB1	Port B channel 1 3V/5V I/O	S12Core[1]	
	PB2	ADDR2/DATA2	Multiplexed Address Data 2	S12Core[1]	PB2 (Hi-Z)
		ATAD02	ATA Data 2	Hi-Z	
		CFD02	CF Data 2	Hi-Z	
		PB2	Port B channel 2 3V/5V I/O	S12Core[1]	
	PB3	ADDR3/DATA3	Multiplexed Address Data 3	S12Core[1]	PB3 (Hi-Z)
		ATAD03	ATA Data 3	Hi-Z	
		CFD03	CF Data 3	Hi-Z	
		PB3	Port B channel 3 3V/5V I/O	S12Core[1]	
	PB4	ADDR4/DATA4	Multiplexed Address Data 4	S12Core[1]	PB4 (Hi-Z)
		ATAD04	ATA Data 4	Hi-Z	
		CFD04	CF Data 4	Hi-Z	
		PB4	Port B channel 4 3V/5V I/O	S12Core[1]	
	PB5	ADDR5/DATA5	Multiplexed Address Data 5	S12Core[1]	PB5 (Hi-Z)
		ATAD05	ATA Data 5	Hi-Z	
		CFD05	CF Data 5	Hi-Z	
		PB5	Port B channel 5 3V/5V I/O	S12Core[1]	
	PB6	ADDR6/DATA6	Multiplexed Address Data 6	S12Core[1]	PB6 (Hi-Z)
		ATAD06	ATA Data 6	Hi-Z	
		CFD06	CF Data 6	Hi-Z	
		PB6	Port B channel 6 3V/5V I/O	S12Core[1]	
	PB7	ADDR7/DATA7	Multiplexed Address Data 7	S12Core[1]	PB7 (Hi-Z)
		ATAD07	ATA Data 7	Hi-Z	
		CFD07	CF Data 7	Hi-Z	
		PB7	Port B channel 7 3V/5V I/O	S12Core[1]	

Port	Pin Name	Pin Function	Description	Pull Mode	Pin Func. (Pull Mode) after Reset
Port T	PT0	DLLTST	UTMI test modes from PHY	Hi-Z	PT0 (Hi-Z)
		CFA00	CF Address 0	Hi-Z	
		IOC0	Timer Channel 0	PIM[2]	
		PT0	Port T channel 0 3V/5V I/O	PIM[2]	
	PT1	MIATST	UTMI test modes from PHY	Hi-Z	PT1 (Hi-Z)
		CFA01	CF Address 1	Hi-Z	
		IOC1	Timer Channel 1	PIM[2]	
		PT1	Port T channel 1 3V/5V I/O	PIM[2]	
	PT2	MIARX	UTMI test modes from PHY	Hi-Z	PT2 (Hi-Z)
		CFA02	CF Address 2	Hi-Z	
		IOC2	Timer Channel 2	PIM[2]	
		PT2	Port T channel 2 3V/5V I/O	PIM[2]	
	PT3	SUSPND	suspend indication from PHY	Hi-Z	PT3 (Hi-Z)
		CFWE	CF WE	Hi-Z	
		IOC3	Timer Channel 3	PIM[2]	
		PT3	Port T channel 3 3V I/O	PIM[2]	
Port M	PM0	SDCMD	SD/MMC CMD	Pullup	PM0 (Hi-Z)
		CFRDY/CFIREQ	CF RDY and CF IREQ	Pullup	
		PM0	Port M channel 0 3V I/O	PIM[2]	
	PM1	SDCLK	SD/MMC CLK	Hi-Z	PM1 (Hi-Z)
		CFREG	CF REG	Hi-Z	
		PM1	Port M channel 1 3V I/O	PIM[2]	
	PM2	SDDATA0	SD/MMC DATA0	Pullup	PM2 (Hi-Z)
		CFWAIT	CF WAIT	Pullup	
		PM2	Port M channel 2 3V I/O	PIM[2]	
	PM3	SDDATA1	SD/MMC DATA1	Pullup	PM3 (Hi-Z)
		CFINPACK	CF INPACK	Pullup	
		PM3	Port M channel 3 3V I/O	PIM[2]	
	PM4	SDDATA2	SD/MMC DATA2	Pullup	PM4 (Hi-Z)
		CFIOIS16	CF IOIS16	Pullup	
		PM4	Port M channel 4 3V I/O	PIM[2]	
	PM5	SDDATA3	SD/MMC DATA3	Pulldown	PM5 (Hi-Z)
		CFIORD	CF IORD	Hi-Z	
		PM5	Port M channel 5 3V I/O	PIM[2]	

Port	Pin Name	Pin Function	Description	Pull Mode	Pin Func. (Pull Mode) after Reset
Port J	PJ0	HRSTIZ	UTMI Hardware reset	Hi-Z	PJ0 (Hi-Z)
		MSBS	Memory Stick Bus state	Pulldown	
		CFIOWR	CF IOWR	Hi-Z	
		PJ0	Port J channel 0 3V I/O	PIM[2]	
	PJ1	EXSUPEN	UTMI external supply enable	Hi-Z	PJ1 (Hi-Z)
		MSSDIO	Memory Stick Serial Data I/O	Pulldown	
		CFCE1	CF CE1	Hi-Z	
		PJ1	Port J channel 1 3V I/O	PIM[2]	
	PJ2	TESTI	UTMI Observe Mode	Hi-Z	PJ2 (Hi-Z)
		MSSCLK	Memory Stick Serial Clock	Pulldown	
		CFCE2	CF CE2	Hi-Z	
		PJ2	Port J channel 2 3V I/O	PIM[2]	

Port	Pin Name	Pin Function	Description	Pull Mode	Pin Func. (Pull Mode) after Reset
Port P	PP0	UD[8]/D[8]	UTMI Observe Mode/PHY test mode	Hi-Z	PP0 (Hi-Z)
		SBSY	Smartmedia SBSY	Hi-Z	
		CFD08	Alternate CF DATA 8	Hi-Z	
		ATAD08	ATA Data 8	Hi-Z	
		PP0	Port P channel 0 3V I/O	PIM[2]	
	PP1	UD[9]/D[9]	UTMI Observe Mode/PHY test mode	Hi-Z	PP1 (Hi-Z)
		SCD	Smart media SCD	Pullup	
		CFD09	Alternate CF DATA 9	Hi-Z	
		ATAD09	ATA Data 9	Hi-Z	
		PP1	Port P channel 1 3V I/O	PIM[2]	
	PP2	UD[10]/D[10]	UTMI Observe Mode/PHY test mode	Hi-Z	PP2 (Hi-Z)
		SCE	Smartness SCE	Hi-Z	
		CFD10	Alternate CF DATA 10	Hi-Z	
		ATAD10	ATA Data 10	Hi-Z	
		PP2	Port P channel 2 3V I/O	PIM[2]	
	PP3	UD[11]/D[11]	UTMI Observe Mode/PHY test mode	Hi-Z	PP3 (Hi-Z)
		SWP	Smart media SWP	Pulldown	
		CFD11	Alternate CF DATA 11	Hi-Z	
		ATAD11	ATA Data 11	Hi-Z	
		PP3	Port P channel 3 3V I/O	PIM[2]	
	PP4	UD[12]/D[12]	UTMI Observe Mode/PHY test mode	Hi-Z	PP4 (Hi-Z)
		SCLE	Smart media SCLE	Pulldown	
		CFD12	Alternate CF DATA 12	Hi-Z	
		ATAD12	ATA Data 12	Hi-Z	
		PP4	Port P channel 4 3V I/O	PIM[2]	
	PP5	UD[13]/D[13]	UTMI Observe Mode/PHY test mode	Hi-Z	PP5 (Hi-Z)
		SALE	Smart media SALE	Pulldown	
		CFD13	Alternate CF DATA 13	Hi-Z	
		ATAD13	ATA Data 13	Hi-Z	
		PP5	Port P channel 5 3V I/O	PIM[2]	
	PP6	UD[14]/D[14]	UTMI Observe Mode/PHY test mode	Hi-Z	PP6 (Hi-Z)
		SWE	Smart media SWE	Hi-Z	
		CFD14	Alternate CF DATA 14	Hi-Z	
		ATAD14	ATA Data 14	Hi-Z	
		PP6	Port P channel 6 3V I/O	PIM[2]	
	PP7	UD[15]/D[15]	UTMI Observe Mode/PHY test mode	Hi-Z	PP7 (Hi-Z)
		SRE	Smart media SRE	Hi-Z	
		CFD15	Alternate CF DATA 15	Hi-Z	
		ATAD15	ATA Data 15	Hi-Z	
		PP7	Port P channel 7 3V I/O	PIM[2]	

Port	Pin Name	Pin Function	Description	Pull Mode	Pin Func. (Pull Mode) after Reset
Port Q	PQ0	UD[0]/D[0]	UTMI Observe Mode/PHY test mode	Hi-Z	PQ0 (Hi-Z)
		SDAT0	Smart media Data 0	Pulldown	
		CFD00	Alternate CF DATA 0	Hi-Z	
		ATAD00	ATA Data 0	Hi-Z	
		PQ0	Port Q channel 0 3V I/O	PIM[2]	
	PQ1	UD[1]/D[1]	UTMI Observe Mode/PHY test mode	Hi-Z	PQ1 (Hi-Z)
		SDAT1	Smart media Data 1	Pulldown	
		CFD01	Alternate CF DATA 1	Hi-Z	
		ATAD01	ATA Data 1	Hi-Z	
		PQ1	Port Q channel 1 3V I/O	PIM[2]	
	PQ2	UD[2]/D[2]	UTMI Observe Mode/PHY test mode	Hi-Z	PQ2 (Hi-Z)
		SDAT2	Smart media Data 2	Pulldown	
		CFD02	Alternate CF DATA 2	Hi-Z	
		ATAD02	ATA Data 2	Hi-Z	
		PQ2	Port Q channel 2 3V I/O	PIM[2]	
	PQ3	UD[3]/D[3]	UTMI Observe Mode/PHY test mode	Hi-Z	PQ3 (Hi-Z)
		SDAT3	Smartmedia Data 3	Pulldown	
		CFD03	Alternate CF DATA 3	Hi-Z	
		ATAD03	ATA Data 3	Hi-Z	
		PQ3	Port Q channel 3 3V I/O	PIM[2]	
	PQ4	UD[4]/D[4]	UTMI Observe Mode/PHY test mode	Hi-Z	PQ4 (Hi-Z)
		SDAT4	Smartmedia Data 4	Pulldown	
		CFD04	Alternate CF DATA 4	Hi-Z	
		ATAD04	ATA Data 4	Hi-Z	
		PQ4	Port Q channel 4 3V I/O	PIM[2]	
	PQ5	UD[5]/D[5]	UTMI Observe Mode/PHY test mode	Hi-Z	PQ5 (Hi-Z)
		SDAT5	Smartmedia Data 5	Pulldown	
		CFD05	Alternate CF DATA 5	Hi-Z	
		ATAD05	ATA Data 5	Hi-Z	
		PQ5	Port Q channel 5 3V I/O	PIM[2]	
	PQ6	UD[6]/D[6]	UTMI Observe Mode/PHY test mode	Hi-Z	PQ6 (Hi-Z)
		SDAT6	Smartmedia Data 6	Pulldown	
		CFD06	Alternate CF DATA 6	Hi-Z	
		ATAD06	ATA Data 6	Hi-Z	
		PQ6	Port Q channel 6 3V I/O	PIM[2]	
	PQ7	UD[7]/D[7]	UTMI Observe Mode/PHY test mode	Hi-Z	PQ7 (Hi-Z)
		SDAT7	Smartmedia Data 7	Pulldown	
		CFD07	Alternate CF DATA 7	Hi-Z	
		ATAD07	ATA Data 7	Hi-Z	
		PQ7	Port Q channel 7 3V I/O	PIM[2]	

Port	Pin Name	Pin Function	Description	Pull Mode	Pin Func. (Pull Mode) after Reset
Port R	PR0	UVM/VMI	UTMI Observe Mode/PHY test mode	Hi-Z	PR0 (Hi-Z)
		CFA03	CF Address 3	PIM[2]	
		PR0	Port R channel 0 3V/5V I/O	PIM[2]	
	PR1	UVP/VPI	UTMI Observe Mode/PHY test mode	Hi-Z	PR1 (Hi-Z)
		CFA04	CF Address 4	PIM[2]	
		PR1	Port R channel 1 3V/5V I/O	PIM[2]	
	PR2	LINEST0I	UTMI Observe Mode/PHY test mode	Hi-Z	PR2 (Hi-Z)
		CFA05	CF Address 5	PIM[2]	
		SCI_RX	SCI RX	PIM[2]	
		PR2	Port R channel 2 3V/5V I/O	PIM[2]	
	PR3	LINEST1I	UTMI Observe Mode/PHY test mode	Hi-Z	PR3 (Hi-Z)
		CFA06	CF Address 6	PIM[2]	
		SCI_TX	SCI TX	PIM[2]	
		PR3	Port R channel 3 3V/5V I/O	PIM[2]	
	PR4	UHSTERMZ/HSTERMIZ	UTMI Observe Mode/PHY test mode	Hi-Z	PR4 (Hi-Z)
		CFA07	CF Address 7	PIM[2]	
		IOC4	Timer Channel 4	PIM[2]	
		PR4	Port R channel 4 3V/5V I/O	PIM[2]	
	PR5	UOPMOD0/OPMOD0I	UTMI Observe Mode/PHY test mode	Hi-Z	PR5 (Hi-Z)
		CFA08	CF Address 8	PIM[2]	
		IOC5	Timer Channel 5	PIM[2]	
		PR5	Port R channel 5 3V/5V I/O	PIM[2]	
	PR6	UOPMOD1/OPMOD1I	UTMI Observe Mode/PHY test mode	Hi-Z	PR6 (Hi-Z)
		CFA09	CF Address 9	PIM[2]	
		IOC6	Timer Channel 6	PIM[2]	
		PR6	Port R channel 6 3V/5V I/O	PIM[2]	
	PR7	USUSPNDZ/SUSPNDIZ	UTMI Observe Mode/PHY test mode	Hi-Z	PR7 (Hi-Z)
		CFA10	CF Address 10	PIM[2]	
		IOC7	Timer Channel 7	PIM[2]	
		PR7	Port R channel 7 3V/5V I/O	PIM[2]	

Port	Pin Name	Pin Function	Description	Pull Mode	Pin Func. (Pull Mode) after Reset
Port S	PS0	UTXRDY/TXRDYO	UTMI Observe Mode/PHY test mode	Hi-Z	PS0 (Hi-Z)
		CFCE1	CF CE1	Hi-Z	
		ATACS0	ATA Chip Select 0	Hi-Z	
		PS0	Port S channel 0 3V/5V I/O	PIM[2]	
	PS1	UVALIDH/VALIDH	UTMI Observe Mode/PHY test mode	Hi-Z	PS1 (Hi-Z)
		CFOE	CF OE	Hi-Z	
		PS1	Port S channel 1 3V/5V I/O	PIM[2]	
	PS2	UTXVLD/TXVLDI	UTMI Observe Mode/PHY test mode	Hi-Z	PS2 (Hi-Z)
		CFIOIS16	CF IOIS16	Pullup	
		PS2	Port S channel 2 3V/5V I/O	PIM[2]	
	PS3	CLK30/CLK30	UTMI Observe Mode/PHY test mode	Hi-Z	PS3 (Hi-Z)
		CFCE2	CF CE2	Hi-Z	
		ATACS1	ATA Chip Select 1	Hi-Z	
		PS3	Port S channel 3 3V/5V I/O	PIM[2]	
	PS4	URXVLD/RXVLDO	UTMI Observe Mode/PHY test mode	Hi-Z	PS4 (Hi-Z)
		CFIORD	CF IORD	Hi-Z	
		ATAIORD	ATA I/O Read	Hi-Z	
		PS4	Port S channel 4 3V/5V I/O	PIM[2]	
	PS5	URXERR/RXERRO	UTMI Observe Mode/PHY test mode	Hi-Z	PS5 (Hi-Z)
		CFIOWR	CF IOWR	Hi-Z	
		ATAIOWR	ATA I/O Write	Hi-Z	
		PS5	Port S channel 5 3V/5V I/O	PIM[2]	
	PS6	URXACTV/RXACTVO	UTMI Observe Mode/PHY test mode	Hi-Z	PS6 (Hi-Z)
		CFWE	CF WE	Hi-Z	
		ATADMARQ	ATA DMA Request	Pulldown	
		PS6	Port S channel 6 3V/5V I/O	PIM[2]	
	PS7	UFSPEED/FSPEEDI	UTMI Observe Mode/PHY test mode	Hi-Z	PS7 (Hi-Z)
		CFRDY/CFIREQ	CF RDY and CF IREQ	Pullup	
		ATAINTQ	ATA Interrupt	Pulldown	
		PS7	Port S channel 7 3V/5V I/O	PIM[2]	

Port	Pin Name	Pin Function	Description	Pull Mode	Pin Func. (Pull Mode) after Reset
Port U	PU0	TXRDYI	UTMI Observe Mode/PHY test mode	Hi-Z	PU0 (Hi-Z)
		CFWAIT	CF Wait	Pullup	
		ATAIORDY	ATA IORDY	Pullup	
		PU0	Port U channel 0 3V/5V I/O	PIM[2]	
	PU1	RXERRI	UTMI Observe Mode/PHY test mode	Hi-Z	PU1 (Hi-Z)
		CFINPACK	CF INPACK	Pullup	
		ATAINPACK/ATADMACK	ATA INPACK or ATA DMACK	Hi-Z	
		PU1	Port U channel 1 3V/5V I/O	PIM[2]	
	PU2	RXVLDI	UTMI Observe Mode/PHY test mode	Hi-Z	PU2 (Hi-Z)
		CFREG	CF REG	Hi-Z	
		PU2	Port U channel 2 3V/5V I/O	PIM[2]	
	PU3	PLLDIS	UTMI Observe Mode/PHY test mode	Hi-Z	PU3 (Hi-Z)
		CFA00	CF Address 0	Hi-Z	
		ATADA0	ATA Device Address 0	Hi-Z	
		PU3	Port U channel 3 3V/5V I/O	PIM[2]	
	PU4	CLK60E/CLK60E	UTMI Observe Mode/PHY test mode	Hi-Z	PU4 (Hi-Z)
		CFA01	CF Address 1	Hi-Z	
		ATADA1	ATA Device Address 1	Hi-Z	
		PU4	Port U channel 4 3V/5V I/O	PIM[2]	
	PU5	CLK60/CLK60	UTMI Observe Mode/PHY test mode	Hi-Z	PU5 (Hi-Z)
		CFA02	CF Address 2	Hi-Z	
		ATADA2	ATA Device Address 2	Hi-Z	
		PU5	Port U channel 5 3V/5V I/O	PIM[2]	
-	BKGD	BKGD/ MODC/ $\overline{\text{TAGHI}}$	Refer to MEBI and BDM in S12 Core User Guide		

NOTES:
1. See S12 Core Guide for details of controlling pullup/down of Ports A, B, and E.
2. See Section 3 of PIM Block Guide for details of pullup/down controls.

Table 2-2 Pin Functions and Priorities in 64pin Configuration

Port	Pin Name	Pin Function	Description	Pull Mode after Reset	Pin Func. (Pull Mode) after Reset
Port E	PE0	$\overline{\text{XIRQ}}$	Non-Maskable Interrupt	S12Core[1]	PE0 (Hi-Z)
		PE0	Port E Channel 0 5V Input		
	PE2	R/$\overline{\text{W}}$	R/W in Expanded Mode	S12Core[1]	PE2 (Hi-Z)
		HRSTIZ	UTMI Hardware Reset	Hi-Z	
		PE2	Port E channel 2 5V I/O	S12Core[1]	
	PE3	$\overline{\text{LSTRB/TAGLO}}$	Low-Byte Strobe/Tag Low	S12Core[1]	PE3 (Hi-Z)
		TESTI	UTMI Observe Mode	Hi-Z	
		CFA3	CF Address 3	S12Core[1]	
		PE3	Port E Channel 3 5V I/O	S12Core[1]	
	PE4	ECLK	Bus Clock Output	S12Core[1]	PE4 (Hi-Z)
		SUSPND	Suspend Indication from PHY	Hi-Z	
		PE4	Port E Channel 4 5V I/O	S12Core[1]	
	PE5	IPIPE0/MODA	Instruction Queue Tracking Signal 0/Mode Input A	S12Core[1]	PE5 (Hi-Z)
		DLLTST	UTMI Test Modes from PHY	Hi-Z	
		CFA8	CF Address 8	S12Core[1]	
		PE5	Port E Channel 5 5V I/O	S12Core[1]	
	PE6	IPIPE1/MODB	Instruction Queue Tracking Signal 1/Mode Input B	S12Core[1]	PE6 (Hi-Z)
		MIATST	UTMI Test Modes from PHY	Hi-Z	
		CFA9	CF Address 9	S12Core[1]	
		PE6	Port E Channel 6 5V I/O	S12Core[1]	
	PE7	NOACC	Access	S12Core[1]	PE7 (Hi-Z)
		MIARX	UTMI Test Modes from PHY	Hi-Z	
		CFA10	CF Address 10	S12Core[1]	
		PE7	Port E Channel 7 5V I/O	S12Core[1]	
Port A	PA0	UD[8]/D[8]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PA0 (Hi-Z)
		ADDR8/DATA8	Multiplexed Address Data 8	S12Core[1]	
		ATAD08	ATA Data 8	Hi-Z	
		CFD08	CF Data 8	Hi-Z	
		SDCMD	SD/MMC CMD	S12Core[1]	
		PA0	Port A Channel 0 3V/5V I/O	S12Core[1]	
	PA1	UD[9]/D[9]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PA1 (Hi-Z)
		ADDR9/DATA9	Multiplexed Address Data 9	S12Core[1]	
		ATAD09	ATA Data 9	Hi-Z	
		CFD09	CF Data 9	Hi-Z	
		SDCLK	SD/MMC CLK	S12Core[1]	
		PA1	Port A Channel 1 3V/5V I/O	S12Core[1]	

Port	Pin Name	Pin Function	Description	Pull Mode after Reset	Pin Func. (Pull Mode) after Reset
Port A	PA2	UD[10]/D[10]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PA2 (Hi-Z)
		ADDR10/DATA10	Multiplexed Address Data 10	S12Core[1]	
		ATAD10	ATA Data 10	Hi-Z	
		CFD10	CF Data 10	Hi-Z	
		SDDATA0	SD/MMC Data0	S12Core[1]	
		PA2	Port A Channel 2 3V/5V I/O	S12Core[1]	
	PA3	UD[11]/D[11]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PA3 (Hi-Z)
		ADDR11/DATA11	Multiplexed Address Data 11	S12Core[1]	
		ATAD11	ATA Data 11	Hi-Z	
		CFD11	CF Data 11	Hi-Z	
		SDDATA1	SD/MMC Data1	S12Core[1]	
		PA3	Port A Channel 3 3V/5V I/O	S12Core[1]	
	PA4	UD[12]/D[12]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PA4 (Hi-Z)
		ADDR12/DATA12	Multiplexed Address Data 12	S12Core[1]	
		ATAD12	ATA Data 12	Hi-Z	
		CFD12	CF Data 12	Hi-Z	
		SDDATA2	SD/MMC Data2	S12Core[1]	
		PA4	Port A Channel 4 3V/5V I/O	S12Core[1]	
	PA5	UD[13]/D[13]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PA5 (Hi-Z)
		ADDR13/DATA13	Multiplexed Address Data 13	S12Core[1]	
		ATAD13	ATA Data 13	Hi-Z	
		CFD13	CF Data 13	Hi-Z	
		SDDATA3	SD/MMC Data3	S12Core[1]	
		PA5	Port A Channel 5 3V/5V I/O	S12Core[1]	
	PA6	UD[14]/D[14]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PA6 (Hi-Z)
		ADDR14/DATA14	Multiplexed Address Data 14	S12Core[1]	
		ATAD14	ATA Data 14	Hi-Z	
		CFD14	CF Data 14	Hi-Z	
		MSBS	Memory Stick Bus State	S12Core[1]	
		PA6	Port A Channel 6 3V/5V I/O	S12Core[1]	
	PA7	UD[15]/D[15]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PA7 (Hi-Z)
		ADDR15/DATA15	Multiplexed Address Data 15	S12Core[1]	
		ATAD15	ATA Data 15	Hi-Z	
		CFD15	CF Data 15	Hi-Z	
		PA7	Port A Channel 7 3V/5V I/O	S12Core[1]	

Port	Pin Name	Pin Function	Description	Pull Mode after Reset	Pin Func. (Pull Mode) after Reset
Port B	PB0	UD[0]/D[0]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PB0 (Hi-Z)
		ADDR0/DATA0	Multiplexed Address Data 0	S12Core[1]	
		ATAD00	ATA Data 0	Hi-Z	
		CFD00	CF Data 0	Hi-Z	
		IOC0	Timer Channel 0	S12Core[1]	
		PB0	Port B Channel 0 3V/5V I/O	S12Core[1]	
	PB1	UD[1]/D[1]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PB1 (Hi-Z)
		ADDR1/DATA1	Multiplexed Address Data 1	S12Core[1]	
		ATAD01	ATA Data 1	Hi-Z	
		CFD01	CF Data 1	Hi-Z	
		IOC1	Timer Channel 1	S12Core[1]	
		PB1	Port B Channel 1 3V/5V I/O	S12Core[1]	
	PB2	UD[2]/D[2]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PB2 (Hi-Z)
		ADDR2/DATA2	Multiplexed Address Data 2	S12Core[1]	
		ATAD02	ATA Data 2	Hi-Z	
		CFD02	CF Data 2	Hi-Z	
		IOC2	Timer Channel 2	S12Core[1]	
		PB2	Port B Channel 2 3V/5V I/O	S12Core[1]	
	PB3	UD[3]/D[3]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PB3 (Hi-Z)
		ADDR3/DATA3	Multiplexed Address Data 3	S12Core[1]	
		ATAD03	ATA Data 3	Hi-Z	
		CFD03	CF Data 3	Hi-Z	
		IOC3	Timer Channel 3	S12Core[1]	
		PB3	Port B Channel 3 3V/5V I/O	S12Core[1]	
	PB4	UD[4]/D[4]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PB4 (Hi-Z)
		ADDR4/DATA4	Multiplexed Address Data 4	S12Core[1]	
		ATAD04	ATA Data 4	Hi-Z	
		CFD04	CF Data 4	Hi-Z	
		IOC4	Timer Channel 4	S12Core[1]	
		PB4	Port B Channel 4 3V/5V I/O	S12Core[1]	
	PB5	UD[5]/D[5]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PB5 (Hi-Z)
		ADDR5/DATA5	Multiplexed Address Data 5	S12Core[1]	
		ATAD05	ATA Data 5	Hi-Z	
		CFD05	CF Data 5	Hi-Z	
		IOC5	Timer Channel 5	S12Core[1]	
		PB5	Port B Channel 5 3V/5V I/O	S12Core[1]	

Port	Pin Name	Pin Function	Description	Pull Mode after Reset	Pin Func. (Pull Mode) after Reset
Port B	PB6	UD[6]/D[6]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PB6 (Hi-Z)
		ADDR6/DATA6	Multiplexed Address Data 6	S12Core[1]	
		ATAD06	ATA Data 6	Hi-Z	
		CFD06	CF Data 6	Hi-Z	
		IOC6	Timer Channel 6	S12Core[1]	
		PB6	Port B Channel 6 3V/5V I/O	S12Core[1]	
	PB7	UD[7]/D[7]	UTMI Observe Mode/PHY Test Mode	Hi-Z	PB7 (Hi-Z)
		ADDR7/DATA7	Multiplexed Address Data 7	S12Core[1]	
		ATAD07	ATA Data 7	Hi-Z	
		CFD07	CF Data 7	Hi-Z	
		IOC7	Timer Channel 7	S12Core[1]	
		PB7	Port B Channel 7 3V/5V I/O	S12Core[1]	
Port T	PT0	PLLDIS	UTMI Observe Mode/PHY Test Mode	Hi-Z	PT0 (Hi-Z)
		CFREG	CF REG	Hi-Z	
		SRE	SmartMedia SRE	Hi-Z	
		SDDATA0	SD/MMC Data0	Hi-Z	
		IOC0	Timer Channel 0	PIM[2]	
		PT0	Port T channel 0 3V/5V I/O	PIM[2]	
	PT1	RXVLDI	UTMI Observe Mode/PHY Test Mode	Hi-Z	PT1 (Hi-Z)
		CFOE	CF OE	Hi-Z	
		SWE	SmartMedia SWE	Hi-Z	
		SDDATA3	SD/MMC Data3	Hi-Z	
		IOC1	Timer Channel 1	PIM[2]	
		PT1	Port T channel 1 3V/5V I/O	PIM[2]	
Port M	PM3	RXERRI	UTMI Observe Mode/PHY Test Mode	Hi-Z	PM3 (Hi-Z)
		CFINPACK	CF INPACK	Pullup	
		SCE	SmartMedia SCE	Hi-Z	
		SDDATA1	SD/MMC DATA1	Pullup	
		IOC2	Timer Channel 2	PIM[2]	
		PM3	Port M Channel 3 3V I/O	PIM[2]	
	PM4	TXRDYI	UTMI Observe Mode/PHY Test Mode	Hi-Z	PM4 (Hi-Z)
		CFIOIS16	CF IOIS16	Pullup	
		SBSY	SmartMedia SBSY	Hi-Z	
		SDDATA2	SD/MMC DATA2	Pullup	
		IOC3	Timer Channel 3	PIM[2]	
		PM4	Port M Channel 4 3V I/O	PIM[2]	

Port	Pin Name	Pin Function	Description	Pull Mode after Reset	Pin Func. (Pull Mode) after Reset
Port J	PJ0	UTXRDY/TXRDYO	UTMI Observe Mode/PHY Test Mode	Hi-Z	PJ0 (Hi-Z)
		SALE	SmartMedia SALE	Pulldown	
		CFIOWR	CF IOWR	Hi-Z	
		ATAIOWR	ATA I/O Write	Hi-Z	
		PJ0	Port J Channel 0 3V I/O	PIM[2]	
	PJ1	UVALIDH/VALIDH	UTMI Observe Mode/PHY Test Mode	Hi-Z	PJ1 (Hi-Z)
		SCLE	SmartMedia SCLE	Pulldown	
		CFCE1	CF CE1	Hi-Z	
		ATACS0	ATA Chip Select 0	Hi-Z	
		PJ1	Port J Channel 1 3V I/O	PIM[2]	
	PJ2	UTXVLD/TXVLDI	UTMI Observe Mode/PHY Test Mode	Hi-Z	PJ2 (Hi-Z)
		SWP	SmartMedia SWP	Pulldown	
		CFCE2	CF CE2	Hi-Z	
		ATACS1	ATA Chip Select 1	Hi-Z	
		PJ2	Port J Channel 2 3V I/O	PIM[2]	

Port	Pin Name	Pin Function	Description	Pull Mode after Reset	Pin Func. (Pull Mode) after Reset
Port Q	PQ0	UVM/VMI	UTMI Observe Mode/PHY Test Mode	Hi-Z	PQ0 (Hi-Z)
		SDAT0	Smartmedia Data 0	Pulldown	
		CFA0	CF Address 0	Hi-Z	
		ATADA0	ATA Address 0	Hi-Z	
		PQ0	Port Q channel 0 3V I/O	PIM[2]	
	PQ1	UVP/VPI	UTMI Observe Mode/PHY Test Mode	Hi-Z	PQ1 (Hi-Z)
		SDAT1	Smartmedia Data 1	Pulldown	
		CFA1	CF Address 1	Hi-Z	
		ATADA1	ATA Address 1	Hi-Z	
		PQ1	Port Q channel 1 3V I/O	PIM[2]	
	PQ2	LINEST0I	UTMI Observe Mode/PHY Test Mode	Hi-Z	PQ2 (Hi-Z)
		SDAT2	Smartmedia Data 2	Pulldown	
		CFA2	CF Address 2	Hi-Z	
		ATADA2	ATA Address 2	Hi-Z	
		PQ2	Port Q channel 2 3V I/O	PIM[2]	
	PQ3	LINEST1I	UTMI Observe Mode/PHY Test Mode	Hi-Z	PQ3 (Hi-Z)
		SDAT3	Smartmedia Data 3	Pulldown	
		CFIORD	CF IORD	Hi-Z	
		ATAIORD	ATA I/O Read	Hi-Z	
		PQ3	Port Q channel 3 3V I/O	PIM[2]	
	PQ4	UHSTERMZ/HSTERMIZ	UTMI Observe Mode/PHY Test Mode	Hi-Z	PQ4 (Hi-Z)
		SDAT4	Smartmedia Data 4	Pulldown	
		CFA4	CF Address 4	PIM[2]	
		ATADMACK	ATA DMACK	Hi-Z	
		PQ4	Port Q channel 4 3V I/O	PIM[2]	
	PQ5	UOPMOD0/OPMOD0I	UTMI Observe Mode/PHY Test Mode	Hi-Z	PQ5 (Hi-Z)
		SDAT5	Smartmedia Data 5	Pulldown	
		CFA5	CF Address 5	PIM[2]	
		SDCMD	SD/MMC CMD	Hi-Z	
		IOC5	Timer Channel 5	PIM[2]	
		PQ5	Port Q channel 5 3V I/O	PIM[2]	
	PQ6	UOPMOD1/OPMOD1I	UTMI Observe Mode/PHY Test Mode	Hi-Z	PQ6 (Hi-Z)
		SDAT6	Smartmedia Data 6	Pulldown	
		CFA6	CF Address 6	PIM[2]	
		SDCLK	SD/MMC CLK	Hi-Z	
		IOC6	Timer Channel 6	PIM[2]	
		PQ6	Port Q channel 6 3V I/O	PIM[2]	

Port	Pin Name	Pin Function	Description	Pull Mode after Reset	Pin Func. (Pull Mode) after Reset
Port Q	PQ7	USUSPNDZ/SUSPNDIZ	UTMI Observe Mode/PHY Test Mode	Hi-Z	PQ7 (Hi-Z)
		SDAT7	Smartmedia Data 7	Pulldown	
		CFA7	CF Address 7	PIM[2]	
		IOC7	Time Channel 7	PIM[2]	
		PQ7	Port Q channel 7 3V I/O	PIM[2]	
Port S	PS4	URXVLD/RXVLDO	UTMI Observe Mode/PHY test mode	Hi-Z	PS4 (Hi-Z)
		SCI_RXD	SCI RX	PIM[2]	
		PS4	Port S channel 4 3V/5V I/O	PIM[2]	
	PS5	URXERR/RXERRO	UTMI Observe Mode/PHY test mode	Hi-Z	PS5 (Hi-Z)
		SCI_TXD	SCI TX	PIM[2]	
		PS5	Port S channel 5 3V/5V I/O	PIM[2]	
	PS6	URXACTV/RXACTVO	UTMI Observe Mode/PHY test mode	Hi-Z	PS6 (Hi-Z)
		CFWE	CF WE	Hi-Z	
		ATADMARQ	ATA DMA Request	Pulldown	
		MSSCLK	Memory Stick Serial Clock	Pulldown	
		PS6	Port S channel 6 3V/5V I/O	PIM[2]	
	PS7	UFSPEED/FSPEEDI	UTMI Observe Mode/PHY test mode	Hi-Z	PS7 (Hi-Z)
		CFRDY/CFIREQ	CF RDY and CF IREQ	Pullup	
		ATAINTQ	ATA Interrupt	Pulldown	
		MSSDIO	Memory Stick Serial Data I/O	Pulldown	
		PS7	Port S channel 7 3V/5V I/O	PIM[2]	
Port U	PU0	CLK30	UTMI Observe Mode/PHY test mode	Hi-Z	PU0 (Hi-Z)
		CFWAIT	CF Wait	Pullup	
		ATAIORDY	ATA IORDY	Pullup	
		SCD	SmartMedia SCD	Pullup	
		PU0	Port U channel 0 3V/5V I/O	PIM[2]	
-	BKGD	BKGD/ MODC/ $\overline{\text{TAGHI}}$	Refer to MEBI and BDM in STAR12 Core User Guide.		

Section 3 Memory Map/Register Definition

This section provides memory maps and detailed descriptions of all registers which are accessible to the end user. **Table 3-1** shows the register map of PIM_9UF32.

Table 3-1 Module Memory Map

Address offset[1]	Use	Access
$00	Port T I/O Register (PTT)	RW
$01	Port T Input Register (PTIT)	R
$02	Port T Data Direction Register (DDRT)	RW
$03	Port T Reduced Drive Register (RDRT)	RW
$04	Port T Pull Device Enable Register (PERT)	RW
$05	Port T Polarity Select Register (PPST)	RW
$06	Reserved	-
$07	Reserved	-
$08	Port M I/O Register (PTM)	RW
$09	Port M Input Register (PTIM)	R
$0A	Port M Data Direction Register (DDRM)	RW
$0B	Port M Reduced Drive Register (RDRM)	RW
$0C	Port M Pull Device Enable Register (PERM)	RW
$0D	Port M Polarity Select Register (PPSM)	RW
$0E	Reserved	-
$0F	Reserved	-
$10	Port J I/O Register (PTJ)	RW
$11	Port J Input Register (PTIJ)	R
$12	Port J Data Direction Register (DDRJ)	RW
$13	Port J Reduced Drive Register (RDRJ)	RW
$14	Port J Pull Device Enable Register (PERJ)	RW
$15	Port J Polarity Select Register (PPSJ)	RW
$16	Reserved	-
$17	Module Routing Register (MODRR)	RW
$18	Port P I/O Register (PTP)	RW
$19	Port P Input Register (PTIP)	R
$1A	Port P Data Direction Register (DDRP)	RW
$1B	Port P Reduced Drive Register (RDRP)	RW
$1C	Port P Pull Device Enable Register (PERP)	RW
$1D	Port P Polarity Select Register (PPSP)	RW
$1E	Reserved	-
$1F	Reserved	-
$20	Port Q I/O Register (PTQ)	RW
$21	Port Q Input Register (PTIQ)	R
$22	Port Q Data Direction Register (DDRQ)	RW
$23	Port Q Reduced Drive Register (RDRQ)	RW

Table 3-1 Module Memory Map

$24	Port Q Pull Device Enable Register (PERQ)	RW
$25	Port Q Polarity Select Register (PPSQ)	RW
$26	Reserved	-
$27	Reserved	-
$28	Port R I/O Register (PTR)	RW
$29	Port R Input Register (PTIR)	R
$2A	Port R Data Direction Register (DDRR)	RW
$2B	Port R Reduced Drive Register (RDRR)	RW
$2C	Port R Pull Device Enable Register (PERR)	RW
$2D	Port R Polarity Select Register (PPSR)	RW
$2E	Reserved	-
$2F	Reserved	-
$30	Port S I/O Register (PTS)	RW
$31	Port S Input Register (PTIS)	R
$32	Port S Data Direction Register (DDRS)	RW
$33	Port S Reduced Drive Register (RDRS)	RW
$34	Port S Pull Device Enable Register (PERS)	RW
$35	Port S Polarity Select Register (PPSS)	RW
$36	Reserved	-
$37	Reserved	-
$38	Port U I/O Register (PTU)	RW
$39	Port U Input Register (PTIU)	R
$3A	Port U Data Direction Register (DDRU)	RW
$3B	Port U Reduced Drive Register (RDRU)	RW
$3C	Port U Pull Device Enable Register (PERU)	RW
$3D	Port U Polarity Select Register (PPSU)	RW
$3E	Reserved	-
$3F	Reserved	-

NOTES:
1. *Register Address = Base Address + Address Offset, where Base Address is defined at the MCU level and Address Offset is defined at the module level*

3.1 Register Descriptions

The following table summarizes the effect on the various configuration bits, data direction (DDR), output level (I/O), reduced drive (RDR), pull enable (PE) and pull select (PS) for the ports. The configuration bit PS is used for two purposes:

1. Configure the sensitive interrupt edge (rising or falling), if interrupt is enabled.
2. Select either a pull-up or pull-down device if PE is active.

Table 3-2 Pin Configuration Summary

DDR	IO	RDR	PE	PS	Function	Pull Device
0	X	X	0	X	Input	Disabled
0	X	X	1	0	Input	Pull Up
0	X	X	1	1	Input	Pull Down
1	0	0	X	X	Output, full drive to 0	Disabled
1	1	0	X	X	Output, full drive to 1	Disabled
1	0	1	X	X	Output, reduced drive to 0	Disabled
1	1	1	X	X	Output, reduced drive to 1	Disabled

NOTE: *All bits of all registers in this module are completely synchronous to internal clocks during a register read.*

3.1.1 Port T Registers

Address Offset: $__00

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PTT3	PTT2	PTT1	PTT0
Write								
Reset:	-	-	-	-	0	0	0	0

= Reserved or unimplemented

Figure 3-1 Port T I/O Register (PTT)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

Address Offset: $__01

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PTIT3	PTIT2	PTIT1	PTIT0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-2 Port T Input Register (PTIT)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

Address Offset: $__02

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	DDRT3	DDRT2	DDRT1	DDRT0
Write:								
Reset:	-	-	-	-	0	0	0	0

= Reserved or unimplemented

Figure 3-3 Port T Data Direction Register (DDRT)

Read:Anytime.

Write:Anytime.

This register configures each port T pin as either input or output.
The TIMER forces the I/O state to be an output for each timer port associated with an enabled output compare. In these cases the data direction bits will not change.
The DDRT bits revert to controlling the I/O direction of a pin when the associated timer output compare is disabled.
The timer input capture always monitors the state of the pin.

DDRT[3:0] — Data Direction Port T
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTT or PTIT registers, when changing the DDRT register.

Address Offset: $__03

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	RDRT3	RDRT2	RDRT1	RDRT0
Write:								
Reset:	-	-	-	-	0	0	0	0

= Reserved or unimplemented

Figure 3-4 Port T Reduced Drive Register (RDRT)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port T output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRT[3:0] — Reduced Drive Port T

1 = Associated pin drives at about 1/6 of the full drive strength.

0 = Full drive strength at output.

Address Offset: $__04

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PERT3	PERT2	PERT1	PERT0
Write:								
Reset:	-	-	-	-	0	0	0	0

= Reserved or unimplemented

Figure 3-5 Port T Pull Device Enable Register (PERT)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERT[3:0] — Pull Device Enable Port T

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__05

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PPST3	PPST2	PPST1	PPST0
Write:								
Reset:	-	-	-	-	0	0	0	0

= Reserved or unimplemented

Figure 3-6 Port T Polarity Select Register (PPST)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPST[3:0] — Pull Select Port T

1 = A pull-down device is connected to the associated port T pin, if enabled by the associated bit in register PERT and if the port is used as input.

0 = A pull-up device is connected to the associated port T pin, if enabled by the associated bit in register PERT and if the port is used as input.

3.1.2 Port M Registers

Address Offset: $__08

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
Write:								
Reset	-	-	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-7 Port M I/O Register (PTM)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
The SDHC function (CMD, CLK, DATA0, DATA1, DATA2, DATA3) takes precedence over the general purpose I/O function if the associated SDHC module is enabled. *Refer to SDHC Block User Guide for details.*

Address Offset: $__09

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-8 Port M Input Register (PTIM)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

Address Offset: $__0A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
Write:								
Reset:	-	-	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-9 Port M Data Direction Register (DDRM)

Read:Anytime.

Write:Anytime.

This register configures each port M pin as either input or output.
The SDHC forces the I/O state to be an output for each port line associated with an enabled output (CLK). It also control the I/O state to be an input/output for each port line associated with an enabled input (CMD, DATA0,DATA1,DATA2,DATA3). In those cases the data direction bits will not change.
The DDRM bits revert to controlling the I/O direction of a pin when the associated peripheral module is disabled.

DDRM[5:0] — Data Direction Port M
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTM or PTIM registers, when changing the DDRM register.

Address Offset: $__0B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
Write:								
Reset:	-	-	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-10 Port M Reduced Drive Register (RDRM)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port M output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRM[5:0] — Reduced Drive Port M
1 = Associated pin drives at about 1/6 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__0C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
Write:								
Reset:	-	-	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-11 Port M Pull Device Enable Register (PERM)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or wired-or output. This bit has no effect if the port is used as push-pull output. Out of reset no pull device is enabled.

If SDHC is active, a pull-up or pull-down device can be activated on the CMD, DATA0, DATA1, DATA2 and DATA3.

PERM[5:0] — Pull Device Enable Port M

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__0D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
Write:								
Reset:	-	-	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-12 Port M Polarity Select Register (PPSM)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin. If SDHC is active, a pull-up device can be activated on the CMD,DATA0,DATA1,DATA2 inputs, but not a pull-down. If SDHC is active, a pull-down device can be activated on the DATA3 inputs, but not a pull-up.

PPSM[5:0] — Pull Select Port M

1 = A pull-down device is connected to the associated port M pin, if enabled by the associated bit in register PERM and if the port is used as a general purpose but not as SDHC.

0 = A pull-up device is connected to the associated port M pin, if enabled by the associated bit in register PERM and if the port is used as general purpose but not as SDHC.

3.1.3 Port J Registers

Address Offset: $__10

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	PTJ2	PTJ1	PTJ0
Write:								
Reset:	-	-	-	-	-	0	0	0

= Reserved or unimplemented

Figure 3-13 Port J I/O Register (PTJ)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
The MSHC function (MSBS, MSSDIO and MSSCLK) takes precedence over the general purpose I/O function if the associated MSHC module is enabled. *Refer to MSHC Block User Guide for details.*

Address Offset: $__11

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	PTIJ2	PTIJ1	PTIJ0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-14 Port J Input Register (PTIJ)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can be used to detect overload or short circuit conditions on output pins.

Address Offset: $__12

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	DDRJ2	DDRJ1	DDRJ0
Write:								
Reset:	-	-	-	-	-	0	0	0

= Reserved or unimplemented

Figure 3-15 Port J Data Direction Register (DDRJ)

Read:Anytime.

Write:Anytime.

This register configures each port J pin as either input or output.
The MSHC forces the I/O state to be an output on PJ0 (MSBS) and PJ2 (MSSCLK). The MSHC takes control of the I/O if enabled. In these cases the data direction bits will not change. The DDRJ bits revert to controlling the I/O direction of a pin when the associated peripheral module is disabled.

DDRJ[2:0] — Data Direction Port J
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTJ or PTIJ registers, when changing the DDRJ register.

Address Offset: $__13

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	RDRJ2	RDRJ1	RDRJ0
Write:								
Reset:	-	-	-	-	-	0	0	0

= Reserved or unimplemented

Figure 3-16 Port J Reduced Drive Register (RDRJ)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port J output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRJ[2:0] — Reduced Drive Port J
1 = Associated pin drives at about 1/6 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__14

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	PERJ2	PERJ1	PERJ0
Write:								
Reset:	-	-	-	-	-	0	0	0

= Reserved or unimplemented

Figure 3-17 Port J Pull Device Enable Register (PERJ)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled.

PERJ[2:0] — Pull Device Enable Port J

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__15

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	PPSJ2	PPSJ1	PPSJ0
Write:								
Reset:	-	-	-	-	-	0	0	0

= Reserved or unimplemented

Figure 3-18 Port J Polarity Select Register (PPSJ)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin if the port is used as general purpose I/O input. This bit has no effect if the port is used as push-pull output. Out of reset no pull device is enable.

If MSHC is active, a pull-down device are activated on the MSBS, MSSDIO and MSSCLK

PPSJ[2:0] — Pull Select Port J

1 = A pull-down device is connected to the associated port J pin, if enabled by the associated bit in register PERJ and if the port is used as general purpose I/O input.

0 = A pull-up device is connected to the associated port J pin, if enabled by the associated bit in register PERJ and if the port is used as general purpose I/O input.

Address Offset: $__17

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	MODRR4	MODRR3	MODRR2	MODRR1	MODRR0
Write:								
Reset:	-	-	-	0	0	0	0	0

= Reserved or unimplemented

Figure 3-19 Module Routing Register (MODRR)

Read:Anytime.

Write:Anytime.

This register configures the re-routing of ATA5HC, CFHC, MSHC, SDHC, SMHC, SCI and TIM on defined port pins.

MODRR[0] — Enable the routing of 64pin configuration

1 = Enable 64pin routing.[1] (see **Table 2-2**)
0 = Enable 100pin routing. (see **Table 2-1**)

MODRR[1] — Tied the unused pins in 64pin configuration (when MODRR[0]=1)

1 = Tie the unused pins (PP[7:0], PM[5],PM[2:0],PT[3:2],PU[5:1],PS[3:0],PQ[7:0]) to output mode, driving 0, and without pull device.
0 = Let the port registers control the unused pins.

MODRR[2] — Optional TIM routing in 64pin configuration (when MODRR[0]=1). It is intended for using the TIM interface and the SM/ATA/CF interface at the same time in 64pin configuration. When using the ATA/CF interface, MODRR[2] should be set to 1 to route the TIM interface to PQ/PM/PT in order to avoid conflict with the ATA/CF interface at PortB, or MODRR[2] should be 0 to route the TIM interface to PortB in order to avoid conflict with the SM interface.

1 = Route TIM IOC[7:0] to Port B [7:0] only
0 = Route TIM IOC[7:0] to PQ[7:4], PM[4:3], PT[1:0][2]

Table 3-3 TIM routing in 64pin configuration

MODRR[]	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
b'xxxxx0x1	PQ7[1]	PQ6[1,2]	PQ5[1,2]	PQ4[1,3]	PM4	PM3	PT1	PT0
b'xxxxx1x1	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

NOTES:
1. In 64pin configuration, CFA[7:4] and IOC[7:4] share the same pins and CF inteface has higher priority than TIM interface if enabled.
2. In 64pin configuration, SDCLK & SDCMD (when MODRR[3]=0) and IOC[6:5] share the same pins, and SD interface has higher priority than TIM interface if enabled.
3. In 64pin configuration, ATADMACK and IOC[4] share the same pin and ATA interface has higher priority than TIM interface if enabled.

MODRR[3] — Optional SDHC routing in 64pin configuration (when MODRR[0]=1). It is intended for using the SD interface and the SM/ATA interface at the same time in 64pin configuration. When using the ATA interface, MODRR[3] should be set to 1 to route the SD interface to PQ/PM/PT in order to avoid conflict with the ATA interface at PortA, or MODRR[3] should be 0 to route the SD interface to PortA in order to avoid conflict with the SM interface.

1 = Route SD interface to Port A [5:0] only
0 = Route SD interface to PQ[6:5], PM[4:3], PT[1:0][3]

NOTES:
1. In 64pin configuration, DDRQ[7:4] should be set to 1 (i.e. output mode) if CFA[7:4] are enabled to route to port Q [7:4].
2. In 64pin configuration (MODRR[0]=1), when MODRR[2]=0 to route the TIM interface to PQ/PM/PT, the ATA interface is assumed to be enabled and occupying PortB. The TIM interface to PortB is blocked due to lower priority than the ATA interface. But if the ATA interface is not enabled when MODRR[2]=0, TIM IOC inputs will come from PQ/PM/PT while TIM IOC outputs will go to both PQ/PM/PT and PortB.
3. In 64pin configuration (MODRR[0]=1), when MODRR[3]=0 to route the SD interface to PQ/PM/PT, the ATA interface is assumed to be enabled and occupying PortA. The SD interface to PortA is blocked due to lower priority than the ATA interface. But if the ATA interface is not enabled when MODRR[3]=0, SD inputs will come from PQ/PM/PT while SD outputs will go to both PQ/PM/PT and PortB.

Table 3-4 SDHC routing in 64pin configuration

MODRR[]	SDDATA3	SDDATA2	SDDATA1	SDDATA0	SDCLK	SDCMD
b'xxxx0xx1	PT1[1]	PM4	PM3	PT0[1]	PQ6	PQ5[1]
b'xxxx1xx1	PA5[2]	PA4[2]	PA3[2]	PA2[2]	PA1[2]	PA0[2]

NOTES:
1. On-chip pullup/down for SD interface is not available at PT1/PT0/PQ5. Off-chip pullup/down should be used.
2. Default pullups at portA are available and controlled by PUCR register (See S12 Core Guide for details of controlling pullups of port A). When port A is used for the SD interface, pullups of PA5 and PA1 must be disabled. Off-chip pulldown should be used for PA5. Also, Off-chip pullups should be used on PA4/PA3/PA2/PA0.

MODRR[4] — Optional CFHC routing in 100pin configuration (when MODRR[0]=0). It is intended for using the CF interface and the ATA interface at the same time in 100pin configuration.

Table 3-5 CFHC routing in 100pin configuration

MODRR[]	CFD[15:8]	CFD[7:0]	CFRDY	CFREG	CFWAIT	CFINPACK	CFIOIS16
b'xxx0xxx0	PA[7:0]	PB[7:0]	PS7	PU2	PU0	PU1	PS2
b'xxx1xxx0	PP[7:0]	PQ[7:0]	PM0	PM1	PM2	PM3	PM4

MODRR[]	CFIORD	CFIOWR	CFCE1	CFCE2	CFA0	CFA1	CFA2	CFWE
b'xxx0xxx0	PS4	PS5	PS0	PS3	PU3	PU4	PU5	PS6
b'xxx1xxx0	PM5	PJ0	PJ1	PJ2	PT0	PT1	PT2	PT3

3.1.4 Port P Registers

Address Offset: $__18

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-20 Port P I/O Register (PTP)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
The SMHC function takes precedence over the general purpose I/O function if the associated SMHC channel is enabled. *Refer to SMHC Block User Guide for details.*

The CFHC function takes precedence over the general purpose I/O function associated with if enabled. *Refer to CFHC Block User Guide for details.*

The ATA5HC function takes precedence over the general purpose I/O function associated with if enabled. *Refer to ATA5HC Block User Guide for details.*
If both SMHC and CFHC are enabled the SMHC functionality takes precedence.

If both SMHC and ATA5HC are enabled the SMHC functionality takes precedence.

If both CFHC and ATA5HC are enabled the ATA5HC functionality takes precedence.

Address Offset: $__19

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-21 Port P Input Register (PTIP)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can be also used to detect overload or short circuit conditions on output pins.

Address Offset: $__1A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRP7	DDRP6	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-22 Port P Data Direction Register (DDRP)

Read:Anytime.

Write:Anytime.

This register configures each port P pin as either input or output.
If the associated SMHC channel or CFHC channel or ATA5HC channel is enabled this register has no effect on the pins.
If a SMHC module is enabled, the SMHC determines the pin direction. *Refer to SMHC Block User Guide for details.*

If a CFHC module is enabled, the CFHC determines the pin direction. *Refer to CFHC Block User Guide for details.*

If a ATA5HC module is enabled, the ATA5HC determines the pin direction. *Refer to ATA5HC Block User Guide for details.*

SMHC has the highest priority to determines the pin direction.

The DDRP bits revert to controlling the I/O direction of a pin when the associated SMHC, CFHC and ATA5HC channel is disabled.

DDRP[7:0] — Data Direction Port P
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTP or PTIP registers, when changing the DDRP register.

Address Offset: $__1B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-23 Port P Reduced Drive Register (RDRP)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port P output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRP[7:0] — Reduced Drive Port P
1 = Associated pin drives at about 1/6 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__1C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-24 Port P Pull Device Enable Register (PERP)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as general purpose I/O input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERP[7:0] — Pull Device Enable Port P

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__1D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-25 Port P Polarity Select Register (PPSP)

Read:Anytime.

Write:Anytime.

This register serves a purpose by selecting a pull-up or pull-down device if enabled.

PPSP[7:0] — Pull Select Port P

1 = A pull-down device is connected to the associated port P pin, if enabled by the associated bit in register PERP and if the port is used as general purpose I/O input.

0 = A pull-up device is connected to the associated port P pin, if enabled by the associated bit in register PERP and if the port is used as general purpose I/O input.

3.1.5 Port Q Registers

Address Offset: $__20

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTQ7	PTQ6	PTQ5	PTQ4	PTQ3	PTQ2	PTQ1	PTQ0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-26 Port P I/O Register (PTQ)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
The SMHC function takes precedence over the general purpose I/O function if the associated SMHC channel is enabled. *Refer to SMHC Block User Guide for details.*
The CFHC function takes precedence over the general purpose I/O function associated with if enabled. *Refer to CFHC Block User Guide for details.*

The ATA5HC function takes precedence over the general purpose I/O function associated with if enabled. *Refer to ATA5HC Block User Guide for details.*
If both SMHC and CFHC are enabled the SMHC functionality takes precedence.

If both SMHC and ATA5HC are enabled the SMHC functionality takes precedence.

If both CFHC and ATA5HC are enabled the ATA5HC functionality takes precedence.

Address Offset: $__21

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIQ7	PTIQ6	PTIQ5	PTIQ4	PTIQ3	PTIQ2	PTIQ1	PTIQ0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-27 Port Q Input Register (PTIQ)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can be also used to detect overload or short circuit conditions on output pins.

Address Offset: $__22

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRQ7	DDRQ6	DDRQ5	DDRQ4	DDRQ3	DDRQ2	DDRQ1	DDRQ0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-28 Port Q Data Direction Register (DDRQ)

Read:Anytime.

Write:Anytime.

This register configures each port Q pin as either input or output.
If the associated SMHC channel or CFHC channel or ATA5HC channel is enabled this register has no effect on the pins.

If a SMHC module is enabled, the SMHC determines the pin direction. *Refer to SMHC Block User Guide for details.*

If a CFHC module is enabled, the CFHC determines the pin direction. *Refer to CFHC Block User Guide for details.*

If a ATA5HC module is enabled, the ATA5HC determines the pin direction. *Refer to ATA5HC Block User Guide for details.*

SMHC has the highest priority to determines the pin direction. CFHC have higher priority than ATA5HC to determine the pin direction.
The DDRQ bits revert to controlling the I/O direction of a pin when the associated SMHC, CFHC and ATA5HC channel is disabled.

DDRQ[7:0] — Data Direction Port Q
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTQ or PTIQ registers, when changing the DDRQ register.

Address Offset: $__23

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRQ7	RDRQ6	RDRQ5	RDRQ4	RDRQ3	RDRQ2	RDRQ1	RDRQ0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-29 Port Q Reduced Drive Register (RDRQ)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port Q output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRQ[7:0] — Reduced Drive Port Q
1 = Associated pin drives at about 1/6 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__24

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERQ7	PERQ6	PERQ5	PERQ4	PERQ3	PERQ2	PERQ1	PERQ0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-30 Port Q Pull Device Enable Register (PERQ)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERQ[7:0] — Pull Device Enable Port Q

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__25

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSQ7	PPSQ6	PPSQ5	PPSQ4	PPSQ3	PPSQ2	PPSQ1	PPSQ0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-31 Port Q Polarity Select Register (PPSQ)

Read:Anytime.

Write:Anytime.

This register serves a purpose by selecting a pull-up or pull-down device if enabled.

PPSQ[7:0] — Pull Select Port Q

1 = A pull-down device is connected to the associated port Q pin, if enabled by the associated bit in register PERQ and if the port is used as general purpose I/O input.

0 = A pull-up device is connected to the associated port Q pin, if enabled by the associated bit in register PERQ and if the port is used as general purpose I/O input.

3.1.6 Port R Registers

Address Offset: $__28

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTR7	PTR6	PTR5	PTR4	PTR3	PTR2	PTR1	PTR0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-32 Port P I/O Register (PTR)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
The CFHC and Timer function takes precedence over the general purpose I/O function associated with if enabled. *Refer to CFHC Block User Guide for details.*

If both CFHC and Timer are enabled, the CFHC functionality takes precedence.

If both CFHC and SCI are enabled, the CFHC functionality takes precedence.

Address Offset: $__29

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIR7	PTIR6	PTIR5	PTIR4	PTIR3	PTIR2	PTIR1	PTIR0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-33 Port R Input Register (PTIR)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This can be also used to detect overload or short circuit conditions on output pins.

Address Offset: $__2A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRR7	DDRR6	DDRR5	DDRR4	DDRR3	DDRR2	DDRR1	DDRR0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-34 Port R Data Direction Register (DDRR)

Read:Anytime.

Write:Anytime.

This register configures each port R pin as either input or output.
If the associated SMHC channel or CFHC channel or ATA5HC channel is enabled this register has no effect on the pins.
If a SMHC module is enabled, the SMHC determines the pin direction. *Refer to SMHC Block User Guide for details.*

If a CFHC module is enabled, the CFHC determines the pin direction. *Refer to CFHC Block User Guide for details.*

If a ATA5HC module is enabled, the ATA5HC determines the pin direction. *Refer to ATA5HC Block User Guide for details.*

SMHC has the highest priority to determines the pin direction. CFHC have higher priority than ATA5HC to determine the pin direction.
The DDRR bits revert to controlling the I/O direction of a pin when the associated SMHC, CFHC and ATA5HC channel is disabled.

DDRR[7:0] — Data Direction Port R
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTR or PTIR registers, when changing the DDRR register.

Address Offset: $__2B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRR7	RDRR6	RDRR5	RDRR4	RDRR3	RDRR2	RDRR1	RDRR0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-35 Port R Reduced Drive Register (RDRR)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port R output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRR[7:0] — Reduced Drive Port R

1 = Associated pin drives at about 1/6 of the full drive strength.
0 = Full drive strength at output.

Address Offset: $__2C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERR7	PERR6	PERR5	PERR4	PERR3	PERR2	PERR1	PERR0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-36 Port R Pull Device Enable Register (PERR)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERR[7:0] — Pull Device Enable Port R

1 = Either a pull-up or pull-down device is enabled.
0 = Pull-up or pull-down device is disabled.

Address Offset: $__2D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSR7	PPSR6	PPSR5	PPSR4	PPSR3	PPSR2	PPSR1	PPSR0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-37 Port R Polarity Select Register (PPSR)

Read:Anytime.

Write:Anytime.

This register serves a purpose by selecting a pull-up or pull-down device if enabled.

PPSR[7:0] — Pull Select Port R

1 = A pull-down device is connected to the associated port R pin, if enabled by the associated bit in register PERR and if the port is used as general purpose I/O input.

0 = A pull-up device is connected to the associated port R pin, if enabled by the associated bit in register PERR and if the port is used as general purpose I/O input.

3.1.7 Port S Registers

Address Offset: $__30

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-38 Port S I/O Register (PTS)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
The CFHC function takes precedence over the general purpose I/O function associated with if enabled. *Refer to CFHC Block User Guide for details.*

The ATA5HC function takes precedence over the general purpose I/O function associated with if enabled. *Refer to ATA5HC Block User Guide for details.* CFHC have higher priority than ATA5HC to take precedence.

Address Offset: $__31

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-39 Port S Input Register (PTIS)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This also can be used to detect overload or short circuit conditions on output pins.

Address Offset:$__32

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRS7	DDRS6	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-40 Port S Data Direction Register (DDRS)

Read:Anytime.

Write:Anytime.

This register configures each port S pin as either input or output

If the associated SMHC channel or CFHC channel or ATA5HC channel is enabled this register has no effect on the pins.
If a CFHC module is enabled, the CFHC determines the pin direction. *Refer to CFHC Block User Guide for details.*

If a ATA5HC module is enabled, the ATA5HC determines the pin direction. *Refer to ATA5HC Block User Guide for details.*

CFHC have higher priority than ATA5HC to determine the pin direction.
The DDRR bits revert to controlling the I/O direction of a pin when the associated CFHC and ATA5HC channel is disabled.

The DDRS bits revert to controlling the I/O direction of a pin when the associated channel is disabled.

DDRS[7:0] — Data Direction Port S
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTS or PTIS registers, when changing the DDRS register.

Address Offset: $__33

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-41 Port S Reduced Drive Register (RDRS)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port S output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRS[7:0] — Reduced Drive Port S

1 = Associated pin drives at about 1/6 of the full drive strength.

0 = Full drive strength at output.

Address Offset: $__34

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-42 Port S Pull Device Enable Register (PERS)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as output in wired-or (open drain) mode. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled.

PERS[7:0] — Pull Device Enable Port S

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__35

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-43 Port S Polarity Select Register (PPSS)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPSS[7:0] — Pull Select Port S

1 = A pull-down device is connected to the associated port S pin, if enabled by the associated bit in register PERS and if the port is used as general purpose I/O input.

0 = A pull-up device is connected to the associated port S pin, if enabled by the associated bit in register PERS and if the port is used as general purpose I/O input.

3.1.8 Port U Registers

Address Offset: $__38

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PTU5	PTU4	PTU3	PTU2	PTU1	PTU0
Write:								
Reset:	-	-	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-44 Port U I/O Register (PTU)

Read:Anytime.

Write:Anytime.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.
The CFHC function takes precedence over the general purpose I/O function associated with if enabled. *Refer to CFHC Block User Guide for details.*

The ATA5HC function takes precedence over the general purpose I/O function associated with if enabled. *Refer to ATA5HC Block User Guide for details.* CFHC have higher priority than ATA5HC to take precedence.

Address Offset: $__39

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PTIU5	PTIU4	PTIU3	PTIU2	PTIU1	PTIU0
Write:								
Reset:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

Figure 3-45 Port U Input Register (PTIU)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the status of the associated pins. This also can be used to detect overload or short circuit conditions on output pins.

Address Offset:$__3A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	DDRU5	DDRU4	DDRU3	DDRU2	DDRU1	DDRU0
Write:								
Reset:	-	-	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-46 Port U Data Direction Register (DDRU)

Read:Anytime.

Write:Anytime.

This register configures each port U pin as either input or output

If the associated SMHC channel or CFHC channel or ATA5HC channel is enabled this register has no effect on the pins.
If a CFHC module is enabled, the CFHC determines the pin direction. *Refer to CFHC Block User Guide for details.*

If a ATA5HC module is enabled, the ATA5HC determines the pin direction. *Refer to ATA5HC Block User Guide for details.*

CFHC have higher priority than ATA5HC to determine the pin direction.
The DDRR bits revert to controlling the I/O direction of a pin when the associated CFHC and ATA5HC channel is disabled.

The DDRU bits revert to controlling the I/O direction of a pin when the associated channel is disabled.

DDRU[7:0] — Data Direction Port U
1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on PTU or PTIU registers, when changing the DDRU register.

Address Offset: $__3B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	RDRU5	RDRU4	RDRU3	RDRU2	RDRU1	RDRU0
Write:								
Reset:	-	-	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-47 Port U Reduced Drive Register (RDRU)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each port U output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRU[7:0] — Reduced Drive Port U

1 = Associated pin drives at about 1/6 of the full drive strength.

0 = Full drive strength at output.

Address Offset: $__3C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PERU5	PERU4	PERU3	PERU2	PERU1	PERU0
Write:								
Reset:	-	-	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-48 Port U Pull Device Enable Register (PERU)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as output in wired-or (open drain) mode. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled.

PERU[7:0] — Pull Device Enable Port U

1 = Either a pull-up or pull-down device is enabled.

0 = Pull-up or pull-down device is disabled.

Address Offset: $__3D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PPSU5	PPSU4	PPSU3	PPSU2	PPSU1	PPSU0
Write:								
Reset:	-	-	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-49 Port U Polarity Select Register (PPSU)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPSU[7:0] — Pull Select Port U

1 = A pull-down device is connected to the associated port U pin, if enabled by the associated bit in register PERU and if the port is used as general purpose I/O input.

0 = A pull-up device is connected to the associated port U pin, if enabled by the associated bit in register PERU and if the port is used as general purpose I/O input.

Section 4 Functional Description

4.1 General

Each pin can act as general purpose I/O. In addition the pin can act as an output from a peripheral module or an input to a peripheral module.

A set of configuration registers is common to all ports. All registers can be written at any time, however a specific configuration might not become active.

Example:

Selecting a pull-up resistor. This resistor does not become active while the port is used as a push-pull output.

4.1.1 I/O register

This register holds the value driven out to the pin if the port is used as a general purpose I/O.

Writing to this register has only an effect on the pin if the port is used as general purpose output. When reading this address, the value of the pins is returned if the data direction register bits are set to 0.

If the data direction register bits are set to 1, the contents of the I/O register is returned. This is independent of any other configuration (**Figure 4-1**).

4.1.2 Input register

This is a read-only register and always returns the value of the pin (**Figure 4-1**).

4.1.3 Data direction register

This register defines whether the pin is used as an input or an output.

If a peripheral module controls the pin the contents of the data direction register is ignored (**Figure 4-1**).

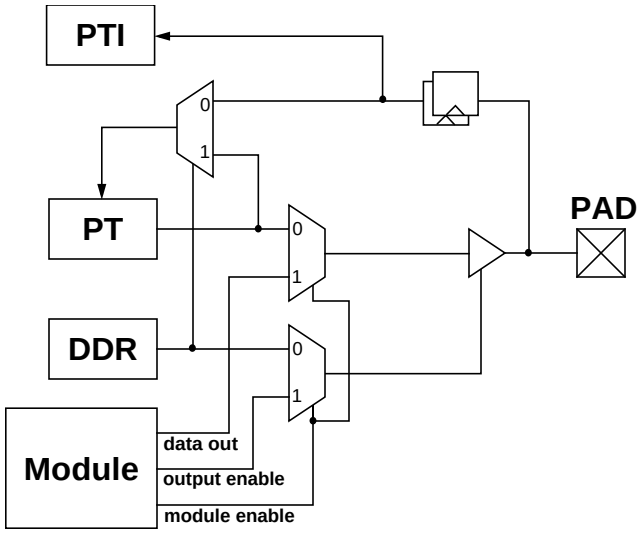

Figure 4-1 Illustration of I/O pin functionality

4.1.4 Reduced drive register

If the port is used as an output the register allows the configuration of the drive strength.

4.1.5 Pull device enable register

This register turns on a pull-up or pull-down device.

It becomes only active if the pin is used as an input or as a wired-or output.

4.1.6 Polarity select register

This register selects either a pull-up or pull-down device if enabled.

It becomes only active if the pin is used as an input. A pull-up device can be activated if the pin is used as a wired-or output.

4.2 Port T

This port is associated with the Timer, CFHC, SDHC, and SMHC modules.

In all modes, port T pins PT[3:0] can be used for either general-purpose I/O, with the channels of the Timer, or with the CFHC, SDHC or SMHC subsystems if enabled in MODRR.

Port T pins PT[3:2] are not available in the 64pin configuration.

During reset, port T pins are configured as high-impedance inputs.

4.3 Port M

This port is associated with the SDHC, CFHC, SMHC, and Timer modules.

In all modes, port M pins PM[5:0] can be used for either general purpose I/O, with the SDHC subsystems, or with the CFHC, SMHC or Timer subsystems if enabled in MODRR.

Port M pins PM[5] and PM[2:0] are not available in the 64pin configuration.

During reset, port M pins are configured as high-impedance inputs.

4.4 Port J

This port is associated with the MSHC, CFHC, ATA5HC and SMHC modules.

In all modes, port J pins PJ[2:0] can be used for either general purpose I/O, or with the MSHC subsystems, or with the CFHC, ATA5HC or SMHC subsystems if enabled in MODRR.

During reset, port M pins are configured as high-impedance inputs.

4.5 Port P

This port is associated with the SMHC, CFHC and ATA5HC modules.

In all modes, port P pins PP[7:0] can be used for either general purpose I/O, or with the SMHC, CFHC and ATA5HC subsystems.

Port P pins PP[7:0] are not available in the 64pin configuration.

During reset, port P pins are configured as high-impedance inputs.

4.6 Port Q

This port is associated with the SMHC, CFHC, ATA5HC, SDHC and Timer modules.

In all modes, port Q pins PQ[7:0] can be used for either general purpose I/O, with the SMHC, CFHC and ATA5HC subsystems, or with the SDHC and Timer subsystems if enabled in MODRR.

During reset, port Q pins are configured as high-impedance inputs.

4.7 Port R

This port is associated with the CFHC, SCI and Timer modules.

In all modes, port R pins PR[7:0] can be used for either general purpose I/O or with the CFHC subsystems. PR[7:4] can be used for Timer. PR[3:2] can be used for SCI.

Port R pins PR[7:0] are not available in the 64pin configuration.

During reset, port R pins are configured as high-impedance inputs.

4.8 Port S

This port is associated with the CFHC, ATA5HC, MSHC, and SCI modules.

In all modes, port S pins PS[7:0] can be used either for general-purpose I/O, with the CFHC and ATA5HC subsystems, or with the MSHC and SCI subsystems if enabled in MODRR.

Port S pins PS[3:0] are not available in the 64pin configuration.

During reset, port S pins are configured as high-impedance inputs.

4.9 Port U

This port is associated with the CFHC, ATA5HC, and SMHC modules.

In all modes, port U pins PU[5:0] can be used either for general-purpose I/O, with the CFHC and ATA5HC subsystems, or with the SMHC subsystem if enabled in MODRR.

Port U pins PU[5:1] are not available in the 64pin configuration.

During reset, port U pins are configured as high-impedance inputs.

4.10 Port A, B, E and BKGD pin

All port and pin logic is located in the core module. *Refer to S12_mebi Block User Guide for details.*

Section 5 Initialization/Application Information

5.1 General

The reset values of all registers are given in section **3.1 Register Descriptions**.

5.2 Reset Initialization

All registers including the data registers get set/reset asynchronously. **Table 5-1** summarizes the port properties after reset initialization.

Table 5-1 Port Reset State Summary

Port	Reset States		
	Data Direction	Pull Mode	Red. Drive
T	input	hiz	disabled
M	input	hiz	disabled
J	input	hiz	disabled
P	input	hiz	disabled
Q	input	hiz	disabled
R	input	hiz	disabled
S	input	hiz	disabled
U	input	hiz	disabled
A	Refer to HCS12 MEBI Block Guide for details.		
B			
E			
BKGD pin	Refer to HCS12 BDM Block Guide for details.		

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