HCS12 Memory Stick Host Controller Block Guide V1.7

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TSPG 8/16 Bit MCU
Freescale Semiconductor, Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
00.01	3 Dec 2001	3 Dec 2001	Willian Tang (R51754)	Draft for Review.
00.02	7 Dec 2001	7 Dec 2001	Willian Tang (R51754)	Revised after first reviewed.
00.02	12 Dec 2001	12 Dec 2001	Willian Tang (R51754)	Revised according to the review from Vincent Ko. Removed DTRQ and DTRQIE bits of MSCS2 Register
00.03	13 Dec 2001	13 Dec 2001	Willian Tang (R51754) Vincent Ko (R20206)	Linked the application models from Vincent Ko. Divided the 16-bit MSCS, MSCS2 and MSICS Registers into 6 8-bit Registers according to Vincent Ko' review: MSC0, MSC1, MSS0, MSS1, MSIC and MSIS. Added DTCMP bit.
1.0	17 Dec 2001	17 Dec 2001	Willian Tang (R51754)	First Release. Added DTCMPIE bit.
1.1	11 Jan 2002	11 Jan 2002	Michael Zheng (R58893)	Initial Tagged for review
1.2	14 Jan 2002	14 Jan 2002	Willian Tang (R51754)	Revised Figure 2-4 for internal signal names; Revised Figure 4-1 and 4-2 for signal names; Revised the description for PWS and SIEN bits of MSC0 Register; Added the description for the difference between power save and module disable modes in Section 4.5; Revised Section 4.5.1 for power save mode description (all control registers can be written under this mode); Revised Section 4.5.2 for register initialize after module disable mode accessed; Revised Section 4.4 for software reset description.
1.3	30 Jan 2002	30 Jan 2002	Michael Zheng (R58893)	Revised tagging for the changes that have been done to the BG.
1.4	18 May 2002	19 May 2002	Michael Zheng (R58893)	Revised tagging for the changes that have been done to the BG, delete pattern "mshc_div0.m", "mshc_div1.m", "mshc_auto_datasize.m". Updated the document number to S12MSHCVx/D. Revised the description for 2-bit DIV = 00 in Section 3.2.8. Revised the table 4-4 and removed the case DIV = 01. Removed the RED bit of MSC1 Register in Section 3.2.8. Added the description for MSCMD Register and changed the datasize range to 0 ~ 512 in Section 3.2.1, also for the adatasize range of MSACMD Register. Added the description for PWS in Section 4.5.0. Added the description for the RST bit and re-defined the NOCRC bit (only transmit) in Section 3.3.2. Revised the description for software reset (RST) in Section 4.4 Revised the description for ACD bit clear in Section 4.6 (P32). Removed the pattern (mshc_dte.m) tag to "not test" in Section 2.2.4.3. Added Note for Table 4-2 and Removed mask bit NOCRC for CRCE interrupt and mask bit SIEN for SIF/INT interrupt. Revised the figure of "read package command timing" for RDY set position in Section 5.1.2. Removed the QTAKE bit of MSC1 Register, and merged it to the DTRQE bit of MSC1 Register.

Version Number	Revision Date	Effective Date	Author	Description of Changes
1.5	9 June 2003	10 June 2003	Michael Zheng (R58893)	Revised some spelling mistake
1.6	27 Nov 2003		Wai-On Law	Removed POPI classification and NDA message.
1.7	29 Nov 2004		Wai-On Law	Changed company logo.

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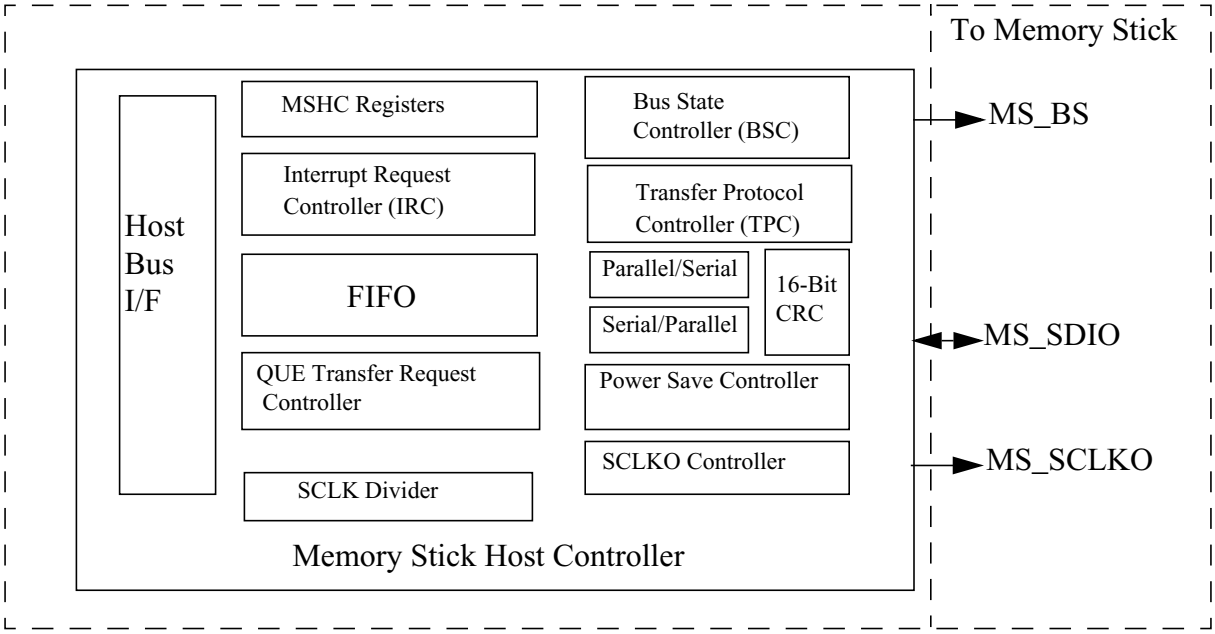

Figure 1-1 Memory Stick Host Controller Block Diagram

1.1 Overview

The Memory Stick Host Controller (MSHC) describes how data are transferred between Memory Stick Device and Host Buses.

1.2 Features

Memory Stick Host Controller includes these distinctive features:

- Built-in 8-byte (4-word) FIFO buffers for transmit and receive respectively.
- Built-in CRC circuit, CRC can be turned off.
- QUE transfer supported through Queue module. QUE transfer request condition is selectable based upon FIFO status.
- Automatic command execution (can be turned on/off) when an INT from the Memory Stick is detected.
- Built-in Serial Clock Divider, maximum 30.0 MHz serial data transfer rate.
- Protocol is started by writing to the command register from the CPU.
- Data transfer may be requested by QUE or CPU.
- RDY timeout period can be set in the number of serial clock.

- 16-bit host bus access (byte access not supported).
- Module core clock is targeted to run at 60MHz, and the bus clock will run at submultiple of module core clock.
- Module core is IP bus compatible, to connect Motorola’s MCU series.

1.3 Modes of Operation

- Run mode.

  It’s basic functional operating mode.Under run mode, MSHC may enter Module Disable mode. When MSCE bit of MSC0 Register is cleared, MSHC will be disabled, and enter a low power state. User can wake up MSHC via re-accessing this bit.

- Power Save mode.

  It is MSHC block-specific. User can set PWS bit of MSC0 Register to enter this mode. MSHC will enter partial low power state. See section 4 for details.

Section 2 External Signal Description

2.1 Overview

The MSHC module has 3 interface signal line connections to Memory Stick Device for data transfer: MS_BS, MS_SCLKO and MS_SDIO. Communication is always started from the MSHC and will operate the bus in either four state or two state access mode.

Table 2-1 External Signal Properties

Name	Port	Type	Function	Reset State	Pull up
MS_BS	PJ0	Output	Memory Stick Bus State	0	----
MS_SDIO	PJ1	I/O	Memory Stick Serial Data line	----	Pull Down
MS_SCLKO	PJ2	Output	Memory Stick Serial Out Clock	0	----

2.2 MSHC interface with Memory Stick Device Diagram

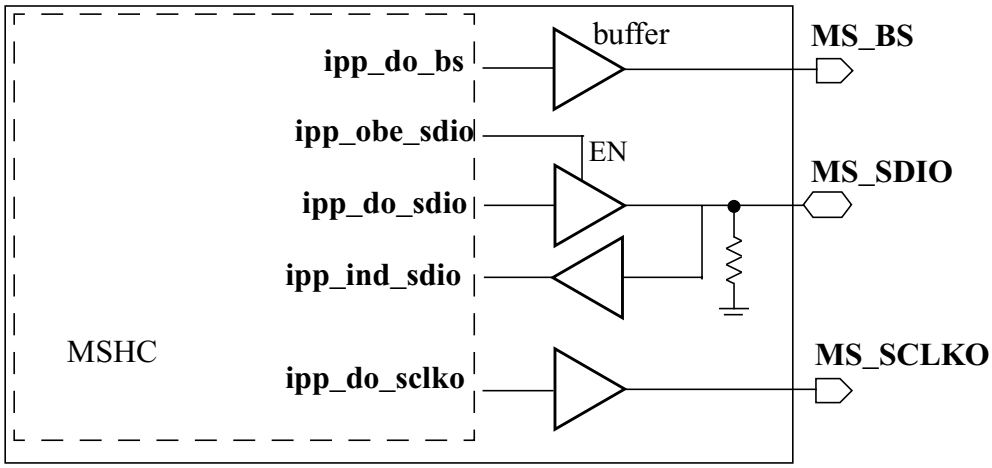

Figure 2-1 Memory Stick Interface Diagram

Section 3 Memory Map/Register Definition

3.1 Overview

This section provides a detailed description of all memory and registers accessible to the end user.

3.2 Module Memory Elements

Table 3-1 is the list of registers used in the Memory Stick Host Controller module.

Table 3-1 MSHC Memory Map

Address	USE	Width	Access
Base + $0	Memory Stick Command Register (MSCMD)	16	Read/Write
Base + $2	Memory Stick Control 0 Register (MSC0)	8	Read/Write
Base + $3	Memory Stick Status 0 Register (MSS0)	8	Read Only
Base + $4	Memory Stick Transmit FIFO DATA Register (MSTDATA)	16	Write Only
Base + $6	Memory Stick Receive FIFO DATA Register (MSRDATA)	16	Read Only
Base + $8	Memory Stick Interrupt Control Register (MSIC)	8	Read/Write
Base + $9	Memory Stick Interrupt Status Register (MSIS)	8	Read Only
Base + $A	Memory Stick Control 1 Register (MSC1)	8	Read/Write
Base + $B	Memory Stick Status 1 Register (MSS1)	8	Read Only
Base + $C	Memory Stick Auto Command Register (MSACMD)	16	Read/Write

Note : The base address is defined at chiptop.

Detailed usage of these MSHC registers is discussed in the following section.

3.2.1 Memory Stick Command (MSCMD)

Address Offset: $0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PID				0	0	DATASIZE									
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Reserved, Should be set to 0, other registers is same as this.

Figure 3-1 Memory Stick Command Register (MSCMD)

Protocol is started via writing to this register. Bit 10 and 11 are reserved, "0" will be read out, other bits can be written and read. Data cannot be written to the Command Register when the RDY bit of the MSIS Register is "0" while the protocol is executing. Data also should be written to this register while the SIE bit of MSC0 Register is set.

PID --- Packet ID:

DATASIZE --- Data Size:

3.2.2 Memory Stick Control 0 Register (MSC0)

Address Offset: $2

Bit	7	6	5	4	3	2	1	0
R	RST	PWS	SIEN	MSCE	NOCRC	BSYCNT		
W								
Reset	0	0	0	0	0	1	0	1

Figure 3-2 Memory Stick Control 0 Register (MSC0)

This register is initialized on power up or when RST bit of MSC0 is "1".

RST --- Reset:

The bit is not synchronous reset by itself.

1 = Reset Memory Stick Host Controller Module.

0 = No Reset (default).

PWS --- Power Save:

Data can only be written to 3 control registers (MSC0, MSC1 and MSIC) when PWS is "1". It is impossible to write PWS bit while the protocol is executing.

1 = MSHC Power Save Enabled.

0 = MSHC Power Save Disabled (default).

SIEN --- Serial Interface Enable:

Normally set to "1" during operation. When this bit is set to "0", the new protocol can not be started, the protocol which is being executed will not be affected. This bit should not be set to "0" immediately after write MSCMD to start a protocol, a serial clock at least is needed after write MSCMD.

1 = Serial Interface Enabled.

0 = Serial Interface Disabled (default).

MSCE --- Memory Stick Host Controller Enable:

1 = Memory Stick Host Controller is enabled.

0 = Memory Stick Host Controller is disabled (default).

With this bit accessed, MSHC will enter module disable mode.

NOCRC --- No CRC:

1 = Transmit CRC off.

0 = Transmit CRC on (default).

BSYCNT --- Busy Count, RDY timeout time setting (Serial Clock Count)

These three bits set the maximum BSY timeout time (set value x 4 +2) to wait until the RDY signal is outputted from the card. RDY timeout error detection is not performed when BSYCNT is 0. The initial value is 05h. Exceeding 5 x 4 + 2 = 22 serial clocks causes a RDY timeout error.

3.2.3 Memory Stick Status 0 Register (MSS0)

Address Offset: $3

Bit	7	6	5	4	3	2	1	0
R	0	0	0	0	RBE	RBF	TBE	TBF
W								
Reset	0	0	0	0	1	0	1	0

Figure 3-3 Memory Stick Status 0 Register (MSS0)

This register is initialized on power up or when RST bit of MSC0 is "1".

RBE --- Receive Buffer Empty Flag (Read Only).

1 = Receiver data buffer empty (default).

0 = Data available in receive data buffer.

RBF --- Receive Buffer Full Flag (Read Only).

1 = Receive data buffer full.

0 = Receive data buffer NOT full (default).

TBE --- Transmit Buffer Empty Flag (Read Only).

1 = Transmit data buffer empty (default).

0 = Data available in transmit data buffer.

TBF --- Transmit Buffer Full Flag (Read Only).

1 = Transmit data buffer full.

0 = Transmit data buffer NOT full.

3.2.4 Memory Stick Transmit FIFO DATA Register (MSTDATA)

Address Offset: $4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	TX DATA BUFFER															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 3-4 Memory Stick Transmit FIFO DATA Register (MSTDATA)

This register value is initialized on power up or when RST bit of MSC0 register is "1".

This register only can be written while DTRQE bit of MSC1 Register is "0" and should not be written before setting a write command to MSCMD Register, and it should not be written before DTRQ interrupt is set when DTRQIE bit of register MSIC is "1".

To send only one byte of data, the data byte must be written in Bits 15 through 8.

3.2.5 Memory Stick Receive FIFO DATA Register (MSRDATA)

Address Offset: $6

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	RX DATA BUFFER															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 3-5 Memory Stick Receive FIFO DATA Register (MSRDATA)

This Register value is initialized on power up or when RST bit of MSC0 Register is "1".

This register only can be read while DTRQE bit of MSC1 Register is "0".

To send only one byte of data, the byte data must be written in Bits 15 through 8.

3.2.6 Memory Stick Interrupt Control Register (MSIC)

Address Offset: $8

Bit	7	6	5	4	3	2	1	0
R	INTE	DTRQIE	DTCMPIE	FAEEN	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 3-6 Memory Stick Interrupt Control Register (MSIC)

This register is initialized on power up or when RST bit of MSC0 Register is "1".

INTE --- Interrupt Enable

An interrupt output signal is generated when an interrupt condition occurs after INTE has been set to "1".

1 = Interrupt output enabled.

0 = Interrupt output disabled (default).

DTRQIE --- Data Transfer Request Interrupt Enable :

This bit enables the data transfer request interrupt.

1 = Interrupt output is enabled during data transfer request.

0 = Interrupt output is disabled during data transfer request (default).

DTCMPIE --- Data Transfer Complete Interrupt Enable :

This bit enables the data transfer complete interrupt.

1 = Interrupt output is enabled during data transfer complete.

0 = Interrupt output is disabled during data transfer complete (default).

FAEEN --- FIFO Access Error Detection Enable.

1 = Invalid FIFO access detect enable.

0 = Invalid FIFO access detect disable (default).

This bit also enables to notify to FAE interrupt status bit of MSIS Register.

3.2.7 Memory Stick Interrupt Status Register (MSIS)

Address Offset: $9

Bit	7	6	5	4	3	2	1	0
R	RDY	SIF	DTRQ	DTCMP	0	FAE	CRCE	TOE
W								
Reset	1	0	0	0	0	0	0	0

Figure 3-7 Memory Stick Interrupt Status Register (MSIS)

This register is initialized on power up or when RST bit of MSC0 Register is "1". When the MSIS Register is read by host, the internal interrupt signal is set to high level (Negated).

RDY --- Ready flag (Read Only).

This bit is cleared to "0" when writing to the Command Register.

1 = Protocol ended (default).

0 = Protocol in progress, communications with Memory Stick.

SIF --- Serial I/F Interrupt flag (Read Only).

This bit is cleared to "0" when a new protocol starts by writing MSHC command register.

1 = Serial I/F receives INT from Memory Stick and no interrupt pended in MSHC.

0 = No Serial I/F Interrupt from Memory Stick (default).

DTRQ --- Data Transfer Request flag (Read Only).

This bit is set according to FIFO states and the setting of RFF and TFE bits of MSC1 Register. This bit is cleared to "0" when data is written to the Command Register.

1 = Data transfer request condition occurs.

0 = No Data transfer request condition occurs.

DTCMP --- Data Transfer Complete flag (Read Only).

This bit is set only when data transfer completed. This bit is cleared to "0" when data is written to the Command Register.

1 = Data transfer is completed.

0 = Data transfer is not completed.

FAE --- FIFO Access Error flag (Read Only).

This bit is cleared to "0" when MSS1 Register is read. This status bit is enabled by setting FAEEN bit of MSIC Register to "1", and can be disabled by setting FAEEN bit to "0".

1 = FIFO access error occurred.

0 = No FIFO access error occurred (default).

CRCE --- CRC Error flag (Read Only).

This bit is cleared to "0" when data is written to the Command Register. MS_BS output is set to LOW level when a CRC error occurs. Also, RDY becomes "1" and an interrupt signal is outputted.

1 = CRC error occurred.

0 = No CRC error occurred (default).

TOE --- Time Out Error flag (Read Only)

This bit is cleared to "0" when data is written to the Command Register. If the number of clock cycles exceeds the clock number setting by the BSYCNT bits of MSC0 Register and BSY from Memory Stick continues, then it is taken as a card malfunction and an RDY timeout error (TOE) is sent out. Also, RDY becomes "1" and an interrupt signal is outputted.

1 = BSY Timeout Error.

0 = No BSY Timeout Error (default).

3.2.8 Memory Stick Control 1 Register (MSC1)

Address Offset: $A

Bit	7	6	5	4	3	2	1	0
R	ACD	0	DIV		DTRQE	0	RFF	TFE
W								
Reset	0	0	1	0	0	0	0	0

Figure 3-8 Memory Stick Control 1 Register (MSC1)

This register is initialized on power up or when RST bit of MSC0 Register is "1". But its DIV bits are NOT reset by setting RST bit of MSC0 Register.

ACD --- Auto Command:

1 = A command is automatically executed after an INT is detected from Memory Stick.

0 = A command is not automatically executed after INT detected from Memory Stick (default).

DIV --- Divide Ratio:

These two bits only can be written in MSHC module disable mode.

The divider supports 2^N divide ratio. (N= 0,1,2,3) But N = 0 and 1 are reserved and can not be used. These two bits should not be written after setting MSCE bit of MSC0 Register to "1".This bit should be modified only when MSCE bit is “0”. The DIV setting is below:

00 = Reserved.

01 = Reserved.

10 = Divided by 4 (default).

11 = Divided by 8.

DTRQE --- Transfer through QUEUE module Enable:

1 = Enable QUE data transfer requests.

0 = Enable IP bus data transfer requests (default).

This bit must be set to "1" before initiating QUE data transfer.

RFF --- RxFIFO Full data transfer Request:

This bit controls the data transfer request signal in case of PID/APID is a read command.

1 = Generate data transfer request when RxFIFO is full.

0 = Generate data transfer request when RxFIFO has received at least one word.

TFE --- TxFIFO Empty data transfer Request:

This bit controls the data transfer request signal in case of PID/APID is a write command.

1 = Generate data transfer request if TxFIFO is empty.

0 = Generate data transfer request if at least 1 empty slot is available in TxFIFO.

3.2.9 Memory Stick Status 1 Register (MSS1)

Address Offset: $B

Bit	7	6	5	4	3	2	1	0
R	RUN	TOV	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 3-9 Memory Stick Status 1 Register (MSS1)

This register is initialized on power up or when RST bit of MSC0 Register is "1".

RUN --- RxFIFO Underrun Access:

When RxFIFO is empty, if Host or QUE reads the FIFO, the access means that the underrun operation is caused. This bit is cleared by writing "1" to this bit. When this bit is set, FAE bit of MSIS Register is set in case of FAEEN = 1, and FIFO access error occurs.

1 = Detect an invalid RxFIFO access (read) in case of RxFIFO is empty (RBE).

0 = No Error.

TOV --- TxFIFO Overrun Access:

When TxFIFO is full, if Host or QUE writes the FIFO, the access means that the overrun operation is caused. This bit is cleared by writing "1" to this bit. When this bit is set, FAE bit of MSIS Register is set in case of FAEEN =1, and FIFO access error occurs.

1 = Detect an invalid TxFIFO access (write) in case of TxFIFO is full (TBF).

0 = No Error.

However, since the FIFO’s pointer does not advance in spite of these invalid accesses (overrun and underrun), user does not need to clear the FIFO in such cases. This two bit (TOV and RUN) will be useful for debugging Host’s and QUE’s access operation.

3.2.10 Memory Stick Auto Command Register (MSACMD)

Address Offset: $C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	APID				0	0	ADATASIZE									
W																
Reset	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1

Figure 3-10 Memory Stick Auto Command Register (MSACMD)

This register is initialized on power up or when RST bit of MSC0 Register is "1".

APID --- Auto Command PID :

With Auto Command Function, the setting is same as PID setting of MSCMD Register.

ADATASIZE --- Auto Command Data Size :

Value determined for each APID code. The range is from 0 to 512. When NOCRC=1, adatasize should not be set to "0". The initial value is $001.

Section 4 Functional Description

The architecture of the MSHC basically consists of a Bus State controller (BSC) a QUE transfer request controller, and Rx/Tx data FIFO for QUE transfer.

To start an operation, some configuration bits in MSC0, MSIC and MSC1 should be set first such as MSCE etc. The QUE transfer and CRC option can be either enabled and disabled.

4.1 Data FIFO Operation & QUE transfer supported

MSHC features a built-in 8- byte (4-word) data FIFO for transmit and receive data between the FIFO memory and the MS card. The receive data FIFO and the transmit data FIFO are 4 words in size respectively. The FIFO structure is implemented by multiplexing the two different access strobes from external QUE and the CPU, and controlling the multiplexer by a FSM inside QUE Transfer Request Controller.

The DTRQE bit of MSC1 Register must be set to "1" if FIFO data transfer occurs on side of IQUE bus. Each data FIFO provides its own empty and full status flag. QUE transfer request controller will send out its requests to IQUE module according to FIFO status. After getting the acknowledges from IQUE, data transfer will occur.

The DTRQE bit of MSC1 Register must be set to "0" if FIFO data transfer occurs on side of IP bus. The FIFO access is provided through read/write from/to the MS Receive/Transmit FIFO Data Buffer Registers.

The following diagram shows the timing of IQUE interface.

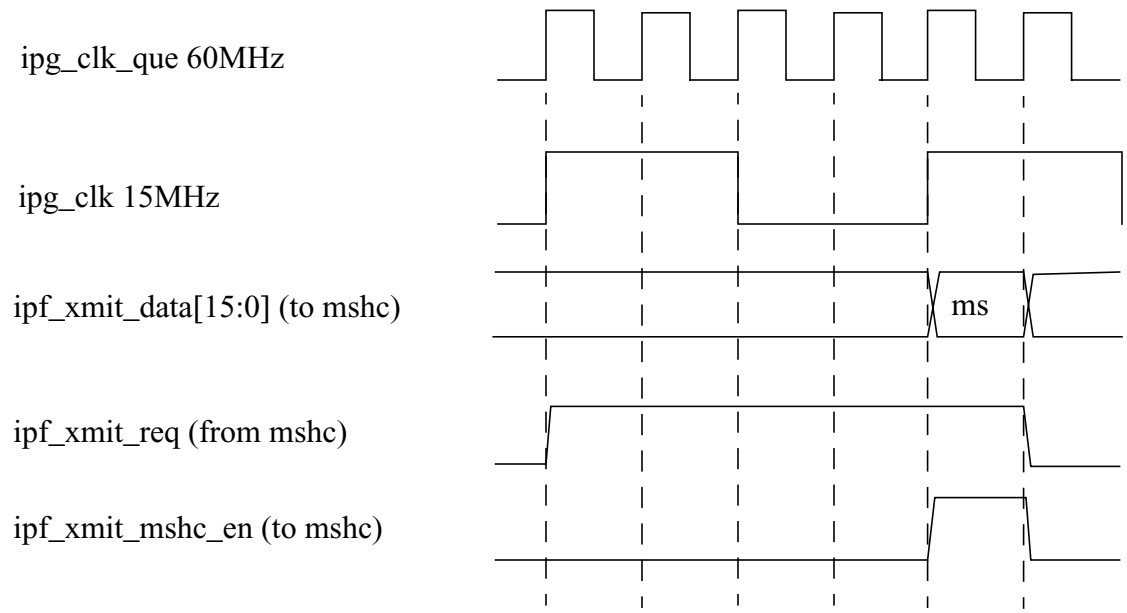

Figure 4-1 IQUE Interface single word read cycle timing

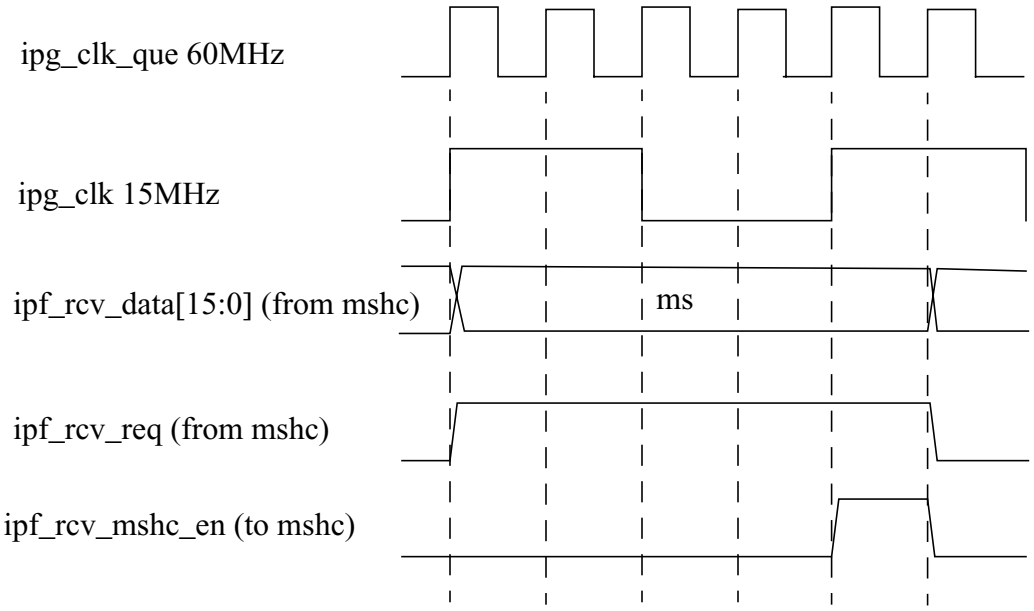

Figure 4-2 IQUE Interface single word write cycle timing

4.2 Interrupt Operation

The MSHC provides single interrupt to the Interrupt Controller.

4.2.1 Interrupt Sources

The MSHC module provides interrupt source/status flags to the programmer. Generally, after interrupt event occurs, there is distinction in the MSHC about how to clear the interrupt to the core and clear the interrupt condition in the MSHC (Interrupt Flag Clear). The following table depicts a summary of the interrupt sources that may cause interrupt to the interrupt controller of system.

Table 4-1 MSHC Interrupt Source Summary

Interrupt Flag Name	Interrupt Enable Setting(s)	Interrupt Disable Setting(s)	Interrupt Flag Clear	Interrupt (send out of MSHC) Negate
RDY(MSIS)	INTE(MSIC) = 1 SIEN(MSC0) = 1	INTE(MSIC) = 0	Write MSCMD	Read MSIS
SIF(MSIS)	INTE(MSIC) = 1	INTE(MSIC) = 0	Write MSCMD	Read MSIS
DTRQ(MSIS)	DTRQIE(MSIC) = 1 INTE(MSIC) = 1	INTE(MSIC) = 0 or DTRQIE(MSIC) = 0	- Write TXDATA for write TPC - Read RXDATA for Read TPC	Read MSIS or - Write TXDATA for write TPC - Read RXDATA for Read TPC
DTCMP(MSIS)	DTCMPIE(MSIC) = 1 INTE(MSIC) = 1	INTE(MSIC) = 0 or DTCMPIE(MSIC) = 0	Write MSCMD	Read MSIS
FAE(MSIS)	INTE(MSIC) = 1 FAEEN(MSIC) =1	INTE(MSIC) = 0	Read MSS1	Read MSIS
CRCE(MSIS)	INTE(MSIC) = 1 SIEN(MSC) = 1	INTE(MSIC) =0	Write MSCMD	Read MSIS
TOE(MSIS)	INTE(MSIC) = 1 SIEN(MSC0) = 1 BSYCNT(MSC0) > 0	INTE(MSIC) =0	Write MSCMD	Read MSIS

Note : The interrupt flag bits (RDY, SIF, DTCMP, CRCE, and TOE) are cleared in next protocol with write MSCMD register.

4.3 Reset Operation

The Memory Stick Control/Status Register’s RST bit provides a mechanism for software resets. When user writes "1" to RST bit, the MSHC Module will initiate a module and associated I/O reset.

A reset of the MSHC results in :

1, Register operation (Status after RST = 1 and immediately after RST = 0)

Table 4-2 Register Reset Values

Register	Reset Value
MS Command Register (MSCMD)	$0000
MS Control 0 Register (MSC0)	MSCE not changed, BSYCNT are $5, other bits are "0"
MS Status 0 Register (MSS0)	$0a
MS Transmit FIFO DATA Register (MSTDATA)	$0000
MS Receive FIFO DATA Register (MSRDATA)	$0000
MS Interrupt Control Register (MSIC)	$00
MS Interrupt Status Register (MSIS)	$80
MS Control 1 Register (MSC1)	DIV not changed, other bits are "0"
MS Status 1 Register (MSS1)	$00
MS Auto Command Register (MSACMD)	$7001

2, Output Signal Status

MS_BS, MS_SDIO, and MS_SCLKO (output) all go low level.

3, Interrupt and FIFO Operations.

Interrupt and QUE transfer request signals get invalid. The Transmit/Receive FIFO are cleared.

4, The executing protocol is terminated.

4.4 Power Save Mode and Module Disable Mode Operations

The "power save mode" of MSHC is a feature of the MSHC and should not be confused with the power save mode of system.

4.4.1 Register Access During Power Save Mode

Note that the following registers can not be written while the MSHC is in Power Save Mode (PWS bit = 1).

- MSCMD, MSTDATA and MSACMD Register.

4.4.2 Register Access while MSHC Module is Disabled

The following register only can be written in MSHC module disable mode (MSCE bit = 0).

- DIV[1:0] bits of MSC1 Register.

Setting the MSCE bit to "0" causes all of MSHC registers to initialize except the MSCE and RST bits of MSC0 Register and DIV bits of MSC1 Register.

4.5 Serial Clock Divider Operation

The Memory Stick Host Controller provides a configured serial clock frequency for flexible transfer rate control. Clock source is IQUE bus clock (60MHz),

Divider outputs serial clock for internal use and MS_SCLKO also is generated by it.

Table 4-3 Serial Clock Divider Settings

Serial Clock Source	DIV[1:0] Value (MSC1)	Divide Ratio	MS_SCLKO output
IQBUSCLK	10	Divide by 4	1/4 IQBUSCLK
IQBUSCLK	11	Divide by 8	1/8 IQBUSCLK

4.6 Built-in CRC

MSHC owns a built-in CRC circuit. For transmit data, CRC generation will be performed, for receive data, CRC check operation will be performed. CRC can be turned off by setting NOCRC bit of MSC0 Register to "1".

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