DOCUMENT NUMBER
S12ATA5HCV1/D

ATA5HC
Block Guide
V1.6

Original Release Date: 29 NOV 2001
Revised: 29 NOV 2004

TSPG 8/16 Bit MCU
Freescale Semiconductor, Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V0.1	29 NOV 2001		Daniel Yu	Initial Draft
V0.2	04 DEC 2001		Daniel Yu	Made changes on block diagram, syntax and format fixes, and re-organized application section
V1.0	18 DEC 2001		Daniel Yu	Minor syntax changes in signals ATA_CS0_B, ATA_CS1_B, tD, IPSI
V1.1	8 MAR 2002		Daniel Yu	Revise register map, and bit definitions.
V1.2	11 JUN 2002		Patrick Kong	Changed UREP bit to sticky bit Added pull down to INTRQ pin Changed the reset value of FE bit to 1 Spec. Tagging
V1.3	18 JUN 2002		Daniel Yu	Add a warning to remind users to set XNW bit to 1 during initialization
V1.4	06 JUN 2003		Daniel Yu	Clarify the ATA Drive Data Register (DDR) description
V1.5	22 SEP 2003		Daniel Yu	Clarify AF bit in HDMAM register. Specify the unused timing field in UDMA mode - t2cyctyp, tds, tdh, tfs, taz and tar
V1.6	29 NOV 2004		Wai-On Law	Changed company logo.

Table of Contents

Section 5 Initialization/Application Information

Appendix A PIO Timing Diagrams

Appendix B Multiword DMA Timing Diagrams

Appendix C Ultra DMA Timing Diagrams

List of Figures

List of Tables

Preface

Content of this Block Guide is intended for re-use as reference material in customer documentation. This Block Guide should contain sufficient detail for an end customer to understand and use the block within a final System-on-a-Chip design.

Terminology

IP bus: Semiconductor Reuse Standard Intellectual Proprietary standard bus (see SRS v3.0 IP interface)

ATA-5: AT attachment level 5 standard

byte count: The value placed in the Byte Count register by the device to indicate the number of bytes to be transferred under this DRQ assertion when executing a PACKET PIO data transfer command.

byte count limit: The value placed in the Byte Count register by the host as input to a PACKET PIO data transfer command to indicate the maximum byte count that may be transferred under a single DRQ assertion.

CFA: The CompactFlash Association that created the specification for compact flash memory that uses the ATA interface.

CHS (cylinder-head-sector): This term defines the addressing of the data on the device by cylinder number, head number, and sector number.

command aborted: Command completion with ABRT set to one in the Error register and ERR set to one in the Status register.

command acceptance: A command is considered accepted whenever the currently selected device has the BSY bit cleared to zero in the Status register and the host writes to the Command register. An exception exists for the EXECUTE DEVICE DIAGNOSTIC (see 8.9 in ATA-5 standard) and DEVICE RESET commands (see 8.7 in ATA-5 standard).

Command Block registers: Interface registers used for delivering commands to the device or posting status from the device.

command completion: Command completion is the completion by the device of the action requested by the command or the termination of the command with an error, the placing of the appropriate error bits in the Error register, the placing of the appropriate status bits in the Status register, the clearing of both BSY and DRQ to zero, and the asserting of ATA_INTRQ if nIEN is cleared to zero and the command protocol specifies that ATA_INTRQ be asserted.

command packet: A command packet is a data structure transmitted to the device during the execution of a PACKET command that includes the command and command parameters.

command released: When a device supports overlap or queuing, a command is considered released when a bus release occurs before the command is completed.

Control Block registers: Interface registers used for device control and to post alternate status.

CRC: Cyclical Redundancy Check used to check the validity of certain data transfers.

device: Device is a storage peripheral. Traditionally, a device on the interface has been a hard disk drive, but any form of storage device may be placed on the interface provided the device adheres to this standard.

DMA (direct memory access) data transfer: A means of data transfer between device and host memory without host processor intervention.

don t care: A term to indicate that a value is irrelevant for the particular function described.

DRQ data block: This term describes a unit of data words transferred during a single assertion of DRQ when using PIO data transfer. A data block is transferred between the host and the device as a complete unit. A data block is a sector, except for data blocks of READ MULTIPLE and WRITE MULTIPLE commands. In the cases of READ MULTIPLE and WRITE MULTIPLE commands, the size of the data block may be changed in multiples of sectors by the SET MULTIPLE MODE command.

interrupt pending: Interrupt pending is an internal state of a device that exists when the device shall notify the host of an event by asserting ATA_INTRQ if nIEN is cleared to zero (see 6.3 in ATA-5 standard).

LBA (logical block address): This term defines the addressing of data on the device by the linear mapping of sectors.

native max address: The highest address a device accepts in the factory default condition, that is, the highest address that is accepted by the SET MAX ADDRESS command. The capacity defined by native max address may be different in CHS and LBA translations.

packet delivered command: A command that is delivered to the device using the PACKET command via a command packet that contains the command and the command parameters.

PIO (programmed input/output) data transfer: PIO data transfers are performed by the host processor utilizing PIO register accesses to the Data register.

read command: A command that causes the device to read data from the media (e.g., READ SECTOR(S), READ DMA, etc.).

register delivered command: A command that is delivered to the device by placing the command and all of the parameters for the command in the device Command Block registers.

register transfers: Register transfers refer to the host reading and writing any device register except the Data register. Register transfers are 8 bits wide.

released: Indicates that a signal is not being driven. For tri-state drivers, this means that the driver is in the high impedance state. For open-collector drivers, the driver is not asserted.

sector: A uniquely addressable set of 256 words (512 bytes).

Ultra DMA burst: An Ultra DMA burst is defined as the period from an assertion of ATA_DMACK_B to the subsequent negation of ATA_DMACK_B when Ultra DMA has been enabled by the host.

unrecoverable error: An unrecoverable error is defined as having occurred at any point when the device sets either the ERR bit or the DF bit to one in the Status register at command completion.

write command: A command that causes the device to write data to the media (e.g., WRITE SECTOR(S), WRITE DMA, etc.).

Conditional Text

No conditional text.

Section 1 Introduction

ATA5HC is a ATA-5 standard host controller for single device configuration, and it consists of four functional blocks:

- Asynchronous FIFO (AFIFO)
- ATA5HC state machine (ASM)
- IP FIFO bus I/F (IPFI)
- IP Slave bus I/F (IPSI)

Figure 1-1 is a block diagram of ATA5HC. Each channel represents interface protocol and doesn't associate with any hardware logic.

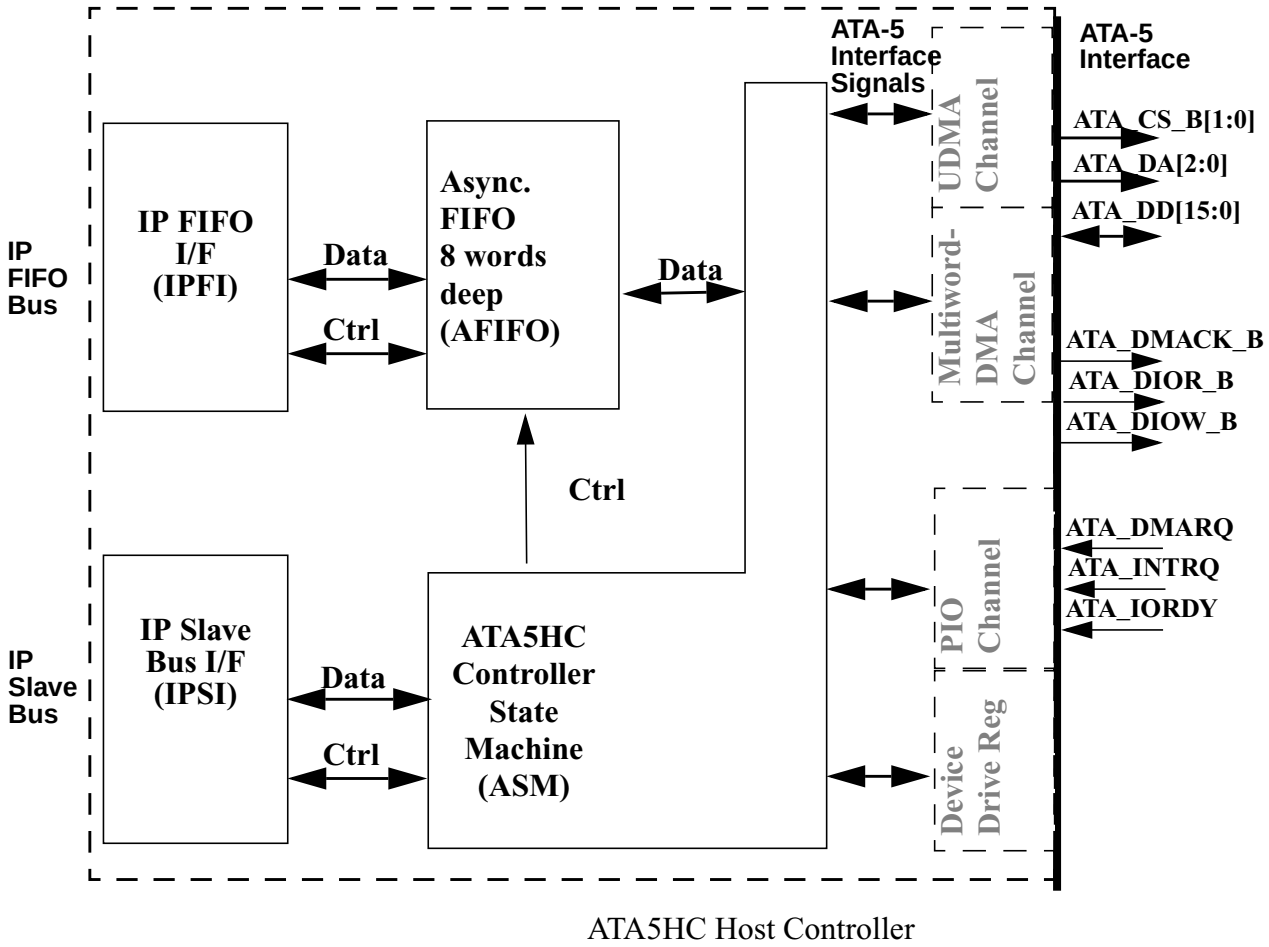


Figure 1-1 ATA5HC Block Diagram

1.1 Overview

The ATA5HC complies with the ATA-5 Specification except feature sets related to dual device configuration. Users are strongly recommended to read ATA-5 standard and IP interface in SRS V3.0 standard before reading this Block Guide.

This host controller supports interface protocols as specified in ATA-5 standard: PIO, Multiword DMA and Ultra DMA mode. To provide proper timing for these interface protocols, users need to set the timing registers by writing to them over IP Slave bus in IPSI. All of the ATA device internal registers are visible to users, and they are defined as mirror registers in ATA5HC. As specified in ATA-5 standard, all the features/functions are implemented by reading/writing to the device internal registers. Therefore, it is users' responsibility to provide software driver for this ATA5HC, and this ATA5HC will only support interface protocols.

In DMA transfer protocol, bulk data are passing in/out through IP FIFO Bus. From system perspective, co-ordination is required to ensure data can be transmitted/received over this IP FIFO Bus once DMA transfer is initiated by issuing DMA command to ATA device.

The operating frequency, which is module core clock frequency, should be in the range between 60 and 135 MHz. Too low a frequency couldn't guarantee proper sampling control signals, while too high a frequency would need to increase the bit size of timing registers.

1.2 Features

The ATA5HC has the following major features:

- Support ATA-5 standard transfer mode
  - PIO data transfer
  - Multiword DMA data transfer
  - UDMA data transfer
- Implement ATA-5 interface signal timing parameters with module core clock period resolution. These timing parameters are stored in ATA5HC timing registers such as HPIO1, HPIO2, etc.
- IP Slave bus and IP FIFO bus interface.
- 2 clock domains: module core clock (targeted at 60MHz), and DSTROBE at ATA-5 interface in Ultra DMA mode.
- Clock gating is available for module core clock domain for power saving feature.
- Asynchronous FIFO for robust clock boundary at ATA-5 interface in Ultra DMA mode.
- Independent software reset for AFIFO and ASM block.

1.3 Modes of Operation

ATA5HC supports the following modes of operation.

- Normal mode

  All logic in all clock domains are active.

- Power Saving mode

  The logic in module core clock domain will be inactive to save power. Users should clear the CLK_EN bit of HCFG register to enable this power saving mode.

ATA5HC will preserve its own mode of operation even though the overall system is in different modes: "stop", "wait" or "debug" mode. In other words, ATA5HC will not make use of the system "stop", "wait", or "debug" control signals.

Section 2 External Signal Description

2.1 Overview

ATA5HC has all the external interface for ATA-5 host controller except for the RESET- pin. Users should provide the RESET- pin to ATA cable externally. For electrical properties of ATA-5 interface, refer to section 4.2 electrical characteristics in ATA-5 standard specification.

Table 2-1 ATA External Signal Properties

Name	Port	ATA-5 interface pin names	Function	Reset State	Pull up/down	I/O
ATA_CS_B[1:0]	ATA_CS0_B ATA_CS1_B	CS0- CS1-	ATA: Chip-select for Command Block Regis-ters	1	--	O
ATA_DA[2:0]	ATA_DA2 ATA_DA1 ATA_DA0	DA2 DA1 DA0	ATA: Address 0-2	0	--	O
ATA_DD[15:0]	ATA_DD15 ATA_DD14 : ATA_DD0	DD15 DD14 : DD0	ATA: 16-bit data	Hi-Z	--	I/O
ATA_DIOR_B	ATA_DIOR_B	DIOR- HDMARDY- HSTROBE	ATA: READ=0, No READ=1	1	--	O
ATA_DIOW_B	ATA_DIOW_B	DIOW- STOP	ATA: WRITE=0, No WRITE=1	1	--	O
ATA_DMACK_B	ATA_DMACK_B	DMACK-	ATA: Active low DMA acknowledge	1	--	O
ATA_DMARQ	ATA_DMARQ	DMARQ	ATA: DMA Request	--	Passive pull down	I

Table 2-1 ATA External Signal Properties

Name	Port	ATA-5 interface pin names	Function	Reset State	Pull up/down	I/O
ATA_INTRQ	ATA_INTRQ	INTRQ	ATA: Interrupt Request	--	Passive pull down	I
ATA_IORDY	ATA_IORDY	IORDY DDMARDY-DSTROBE	ATA: Negated (0) to extend host transfer	--	Passive pull up	I

2.2 Detailed Signal Descriptions

The following subsections describe each external signals separately.

2.2.1 ATA_CS_B[1:0] — ATA chip select

These are the chip select signals from the host used to select the Command Block or Control Block registers. When ATA_DMACK_B is asserted, ATA_CS0_B and ATA_CS1_B shall be negated and transfers shall be 16 bits wide.

2.2.2 ATA_DA[2:0] — ATA device address

This is the 3-bit binary coded address asserted by the host to access a register or data port in the device.

2.2.3 ATA_DD[15:0] — ATA device data

This is an 8- or 16-bit bi-directional data interface between the host and the device. The lower 8 bits are used for 8-bit register transfers. Data transfers are 16-bits wide except for CFA device that implement 8-bit data transfers.

2.2.4 ATA_DIOR_B — Device I/O read:Ultra DMA ready:Ultra DMA data strobe

ATA_DIOR_B (known as ATA_DIOR_B at ATA-5 interface) is the strobe signal asserted by the host to read device registers or the Data port.

For Ultra DMA data-in bursts, ATA_DIOR_B (known as HDMARDY- at ATA-5 interface) acts as a flow control signal. This signal is asserted by the host to indicate to the device that the host is ready to receive Ultra DMA data-in bursts. The host may negate ATA_DIOR_B to pause an Ultra DMA data-in burst.

For an Ultra DMA data-out burst, ATA_DIOR_B (known as HSTROBE at ATA-5 interface) acts as a strobe signal from the host. Both the rising and falling edge of ATA_DIOR_B latch the data from ATA_DD[15:0] into the device. The host may stop generating ATA_DIOR_B edges to pause an Ultra DMA data-out burst.

2.2.5 ATA_DIOW_B — Device I/O write:Stop Ultra DMA burst

ATA_DIOW_B (known as ATA_DIOW_B at ATA-5 interface) is the strobe signal asserted by the host to write device registers or the Data port.

ATA_DIOW_B (known as STOP at ATA-5 interface) shall be negated by the host before data is transferred in an Ultra DMA burst. Assertion of ATA_DIOW_B by the host during an Ultra DMA burst signals the termination of the Ultra DMA burst.

2.2.6 ATA_DMACK_B — DMA acknowledge

This signal shall be used by the host in response to ATA_DMARQ to initiate DMA transfers.

2.2.7 ATA_DMARQ — DMA request

This signal, used for DMA data transfers between host and device, shall be asserted by the device when the device is ready to transfer data to or from the host. For Mulitword DMA transfers, the direction of data transfer is controlled by ATA_DIOR_B and ATA_DIOW_B. This signal is used in a handshake manner with ATA_DMACK_B, i.e., the device shall wait until the host asserts ATA_DMACK_B before negating ATA_DMARQ, and re-asserting ATA_DMARQ if there is more data to transfer. When a DMA operation is enabled, ATA_CS0_B and ATA_CS1_B shall not be asserted and transfers shall be 16 bits wide. This signal shall be released when the device is not selected.

2.2.8 ATA_INTRQ — Device interrupt

This signal is used by the selected device to interrupt the host system when interrupt pending is set. When the nIEN bit in DCTR is cleared to zero and the device is selected, ATA_INTRQ shall be enabled through a tri-state buffer. When the nIEN bit in DCTR is set to one or the device is not selected, the ATA_INTRQ signal shall be released. When asserted, this signal shall be negated by the device within 400 ns of the negation of ATA_DIOR_B that reads the Status register to clear interrupt pending. When asserted, this signal shall be negated by the device within 400 ns of the negation of ATA_DIOW_B that writes the Command register to clear interrupt pending. When the device is selected by writing to the Device/Head register while interrupt pending is set, ATA_INTRQ shall be asserted within 400 ns of the negation of ATA_DIOW_B that writes the Device/Head register. When the device is deselected by writing to the Device/Head register while interrupt pending is set, ATA_INTRQ shall be released within 400 ns of the negation of ATA_DIOW_B that writes the Device/Head register. For devices implementing the Overlapped feature set, if ATA_INTRQ assertion is being disabled using nIEN in DCTR at the same instant that the device asserts ATA_INTRQ, the minimum pulse width shall be at least 40 ns. This signal shall be released when the device is not selected.

2.2.9 ATA_IORDY — I/O channel ready:Ultra DMA ready:Ultra DMA data strobe

This signal is negated to extend the host transfer cycle of any host register access (read or write) when the device is not ready to respond to a data transfer request. If the device requires that the host transfer cycle

time be extended for PIO modes 3 and above, the device shall utilize ATA_IORDY. Hosts that use PIO modes 3 and above shall support ATA_IORDY.

For Ultra DMA data-out bursts, ATA_IORDY (known as DDMARDY- at ATA-5 interface) is a flow control signal. This signal is asserted by the device to indicate to the host that the device is ready to receive Ultra DMA data-out bursts. The device may negate ATA_IORDY to pause an Ultra DMA data-out burst.

For an Ultra DMA data-in burst, ATA_IORDY (known as DSTROBE at ATA-5 interface) is the data-in strobe signal from the device Both the rising and falling edge of DSTROBE latch the data from ATA_DD[15:0] into the host. The device may stop generating ATA_IORDY edges to pause an Ultra DMA data-in burst. This signal shall be released when the device is not selected.

Section 3 Memory Map/Register Definition

There is no memory space in this module, but a list of registers are defined. All of these registers are accessible in both supervisor and user mode through IP slave bus interface.

Table 3-1 is ATA5HC register map.

Table 3-1 ATA5HC Register Map

Address Offset	Use	Type
$00	Host Configuration (HCFG)	Read/Write
$02	Host Status (HSR)	Read/Write
$04	PIO Timing Register (HPIO1)	Read/Write
$06	PIO Timing Register (HPIO2)	Read/Write
$08	PIO Timing Register (HPIO3)	Read/Write
$0a	PIO Timing Register (HPIO4)	Read/Write
$0c	Multi-word DMA Timing Register (HDMA1)	Read/Write
$0e	Multi-word DMA Timing Register (HDMA2)	Read/Write
$10	Multi-word DMA Timing Register (HDMA3)	Read/Write
$12	Multi-word DMA Timing Register (HDMA4)	Read/Write
$14	Ultra DMA Timing Register (HUDMA1)	Read/Write
$16	Ultra DMA Timing Register (HUDMA2)	Read/Write
$18	Ultra DMA Timing Register (HUDMA3)	Read/Write
$1a	Ultra DMA Timing Register (HUDMA4)	Read/Write
$1c	Ultra DMA Timing Register (HUDMA5)	Read/Write
$1e	Ultra DMA Timing Register (HUDMA6)	Read/Write
$20	Ultra DMA Timing Register (HUDMA7)	Read/Write
$22	Ultra DMA Timing Register (HUDMA8)	Read/Write

Table 3-1 ATA5HC Register Map

$24	Ultra DMA Timing Register (HUDMA9)		Read/Write
$26 - $2c	Reserved		--
$2e	ATA Drive Control Register (DCTR) (For Write)		Write
	ATA Drive Alternate Status Register (DASR) (For Read)		Read
$30	ATA Drive Data Register (DDR)		Read/Write
$32	ATA Drive Feature Register (DFR) (For Write)		Write
	ATA Drive Error Register (DER) (For Read)		Read
$34	ATA Drive Sector Count Register (DSCR)		Read/Write
$36	ATA Drive Sector Number Register (DSNR)		Read/Write
$38	ATA Drive Cylinder Low Register (DCLR)		Read/Write
$3a	ATA Drive Cylinder High Register (DCHR)		Read/Write
$3c	ATA Drive Device/Head Register (DDHR)		Read/Write
$3e	ATA Drive Command Register (DCR) (For Write)	DMA Mode Register (HDMAM)	Write
	ATA Drive Status Register (DSR) (For Read)		Read

3.1 Register Descriptions

The registers are basically divided into two groups, host controller registers and device drive registers. The host controller registers will have prefix "H", such as HCFG, HSR, etc., while the device driver registers will have prefix "D", such as DCTR, DSR, etc.

All registers will have base address, which will be decoded in system level to have a module select signal asserted for ATA5HC module. This base address will not be visible to the ATA5HC module directly. The reserved address locations ($26-$2c) are restricted for use. Reading/writing from/to these registers will set RERR/WERR bit in Host Status Register (HSR).

Register read/write for 8-bit access is allowed. Bit 15-8 will represent even address, and bit 7-0 will represent odd address. For 16-bit access, the content in IP slave bus will read/write directly from/to the register content without byte re-arrangement.

For register read/write, this module has the option of supporting microcontroller core without peripheral I/O wait capability, and users should set XNW bit of register HCFG for this option. Accessing host controller registers in this option doesn’t require special procedure because read/write will be complete in a single cycle. While accessing device drive registers in this option, users should take the following procedures:

- For read operation, users should issue a "read" operation to the destination register at first, and then keep polling Host Status Register (HSR) to check on the drive register access busy (DRAB) bit. If this bit is set, users should wait until this bit is clear. When clear, users should issue a "read" operation to the same register location again. The data content will then be valid for reading.
- For write operation, users have the option of polling DRAB bit of HSR register continuously until this bit is clear to ensure the current write operation completed. Alternately, users can perform some other functions before polling HSR register.

Since the device register read/write shares the ATA-5 interface with other types of data transfers: Multiword DMA and Ultra DMA, users should poll bit TIP of HSR register until it is clear before reading/writing from/to device registers.

3.1.1 Host Controller Registers

Host Controller Registers include configuration, status, and timing registers. The timing registers will provide all the ATA-5 interface protocol timing. Users should set these registers for the corresponding mode of transfer.

Address Offset: $00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SMR	FR	0	0	CLK_EN	XNW	IE	IORDY_EN	0	0	0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-1 Host Configuration Register (HCFG)

Host Configuration is used to configure ATA5HC host controller configuration, and it also includes reset function to internal FIFO and state machine.

SMR — State Machine Reset

1 = Reset the ATA state machine to IDLE state for PIO, DMA and UDMA read/write.

1 = No operation.

FR — FIFO Reset

1 = Reset the FIFO when SMR bit of this register is set to reset the ATA state machine. During normal ATA transfer, the FIFO may also be reset by setting FR bit of DCR: ATA drive Command Register.

0 = No operation.

CLK_EN — module core clock Enable function

This is module core clock enable function. If asserted, module output signal module core clock_en will be asserted, and system should use this output signal to gate module core clock.

1 = Enable module core clock.

0 = Disable module core clock.

XNW — IPS_XFR_WAIT support

1 = Not supporting IPS_XFR_WAIT protocol. This option is designed for microcontroller core without peripheral I/O wait capability. The bus master has to poll DRAB bit in Host Status Register (HSR) to ensure the device drive register access completion.

0 = Support IPS_XFR_WAIT protocol. If register access is not complete yet, the "ips_xfr_wait" signal will be asserted. For read operation, the bus master has to wait for "ips_xfr_wait" signal deserted before completing device drive register read transfer.

Warning: Users MUST set this bit to 1 during initialization.

IE — Interrupt Enable

1 = Enable interrupt from ATA drive to CPU through IP bus.

0 = Disable interrupt from ATA drive to CPU through IP bus.

IORDY_EN — Enable ATA_IORDY function

1 = Set for ATA_IORDY support. Required for PIO mode 3 and above.

0 = No support for ATA_IORDY function.

Address Offset: $02

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	TIP	UREP	DRAB	0	FF	FE	RERR	WERR	0	0	0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-2 Host Status Register (HSR)

This register reports the operation status of ATA5HC host controller. UREP, RERR and WERR bits are sticky bit, and they have to be clear by writing one

TIP — transfer in progress

1 = Transaction in Progress indicator bit. This bit MUST be polled by the software before any PIO access. System bus will lock up if any PIO accesses are attempted while this bit is set. This bit is Read Only.

0 = No transaction in progress.

UREP — UDMA Read extended pause

1 = UDMA Read Extended Pause. This bit is set when drive stops strobing for an extended period of 256 module core clock cycles without initiating burst termination by negating ATA_DMARQ, during an UDMA read burst. The software may initiate an UDMA read burst termination in this case by setting HUT bit of HDMAM.

0 = No operation.

DRAB — Device Register Access Busy (Read only, write has no effect)

1 = Set if last register access is busy.

0 = Not busy.

FF — FIFO Full Flag (Read only, write has no effect)
1 = Set if FIFO full.
0 = Not full.

FE — FIFO Empty Flag (Read only, write has no effect)
1 = FIFO empty.
0 = Not empty.

RERR — Read on unimplemented register (Read only, clear by writing one)
1 = Set if reading from an unimplemented register.
0 = No error so far.

WERR — Write on unimplemented register (Read only, clear by writing one)
1 = Set if writing on an unimplemented register.
0 = No error so far.

Address Offset: $04.

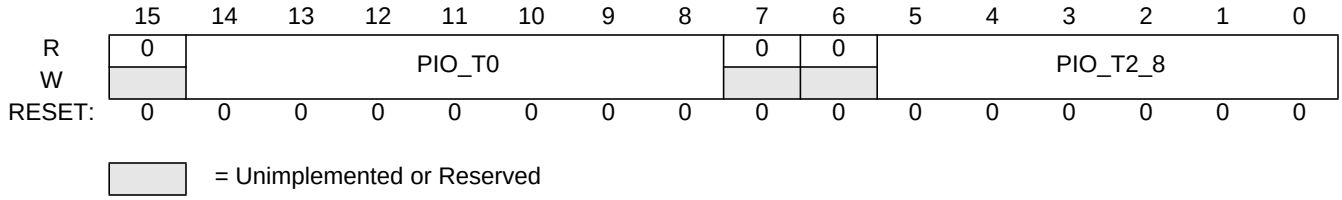


Figure 3-3 PIO Timing Register 1 (HPIO1)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

PIO_T0 — ATA-5 standard PIO timing t0

t0 is cycle time for PIO data transfer, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

PIO_T2_8 — ATA-5 standard PIO timing t2 for 8-bit transfer

t2 is pulse width for read/write control signal ATA_DIOR_B/ATA_DIOW_B, and this timing register should be set according to the supported mode, such mode 2, mode 3, etc.

Address Offset: $06

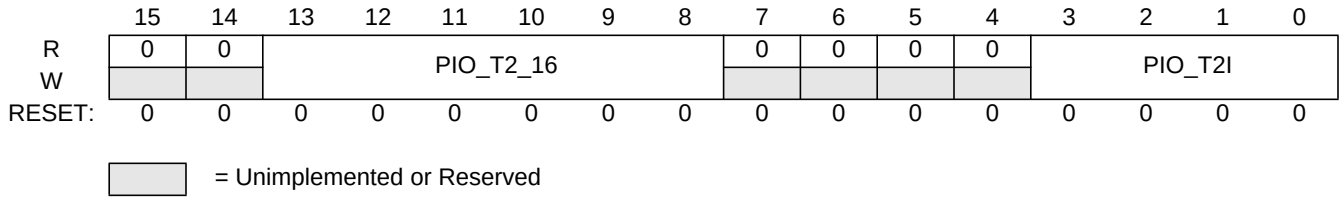


Figure 3-4 PIO Timing Register 2 (HPIO2)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

PIO_T2_16 — ATA-5 standard PIO timing t2 for 16-bit transfer

t2 is pulse width for read/write control signal ATA_DIOR_B/ATA_DIOW_B, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

PIO_T2I — ATA-5 standard PIO timing t2i

t2i is ATA_DIOR_B/ATA_DIOW_B recovery time, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

Address Offset: $08

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PIO_T4			0	0	0	0	PIO_T1			
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-5 PIO Timing Register 3 (HPIO3)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

PIO_T4 — ATA-5 standard PIO timing t4

t4 is PIO write (ATA_DIOW_B) data hold time, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

PIO_T1 — ATA-5 standard PIO timing t1

t0 is the timing from address valid to ATA_DIOR_B/ATA_DIOW_B setup, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

Address Offset: $0A

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PIO_TA			0	0	0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-6 PIO Timing Register 4 (HPIO4)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

PIO_TA — ATA-5 standard PIO timing ta

ta is ATA_IORDY setup time, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

Address Offset: $0C

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	DMA_T0							0	0	DMA_TD					
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-7 DMA Timing Register 1 (HDMA1)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

DMA_T0 — ATA-5 standard DMA timing t0

t0 is the cycle time for Multiword DMA transfer, and this timing register should be set according to the supported mode, mode 0, 1, 2

DMA_TD — ATA-5 standard DMA timing t_D

t_D is read/write control line (ATA_DIOR_B/ATA_DIOW_B) asserted pulse width timing, and this timing register should be set according to the supported mode, mode 0, 1, 2

Address Offset: $0E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	DMA_TK						0	0	0	0	DMA_TM			
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-8 DMA Timing Register 2 (HDMA2)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

DMA_TK — ATA-5 standard DMA timing t_K

t_K is timing for Multiword DMA read/write (ATA_DIOR_B/ATA_DIOW_B) negated pulse width, and this timing register should be set according to the supported mode, mode 0, 1, 2

DMA_TM — ATA-5 standard DMA timing t_m

t_m is timing from ATA_CS0_B, ATA_CS1_B valid to ATA_DIOR_B/ATA_DIOW_B, and this timing register should be set according to the supported mode, mode 0, 1, 2

Address Offset: $10

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	DMA_TH			0	0	0	0	0	DMA_TJ		
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-9 DMA Timing Register 3 (HDMA3)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

DMA_TH — ATA-5 standard DMA timing t_H

t_H is Multiword DMA write (ATA_DIOW_B) data hold time, and this timing register should be set according to the supported mode, mode 0, 1, 2

DMA_TJ — ATA-5 standard DMA timing t_J

t_J is Multiword DMA read/write (ATA_DIOR_B/ATA_DIOW_B) to DMA acknowledge (ATA_DMACK_B) hold, and this timing register should be set according to the supported mode, mode 0, 1, 2

Address Offset: $12

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	DMA_TN			0	0	0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-10 DMA Timing Register 4 (HDMA4)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

DMA_TN — ATA-5 standard DMA timing t_N

t_N is ATA_CS0_B, ATA_CS1_B hold time, and this timing register should be set according to the supported mode, mode 0, 1, 2

Address Offset: $14

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	UDMA_T2CYCTYP						0	0	0	UDMA_TCYC				
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-11 UDMA Timing Register 1 (HUDMA1)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

UDMA_T2CYCTYP — ATA-5 standard UDMA timing $t_{2CYCTYP}$

$t_{2CYCTYP}$ is Ultra DMA sustained average two cycle time, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.For current implementation, this register is not used.

UDMA_TCYC — ATA-5 standard UDMA timing t_{CYC}

t_{CYC} is Ultra DMA strobe edge to strobe edge cycle time, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

Address Offset: $16

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	UDMA_TDS			0	0	0	0	0	UDMA_TDH		
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-12 UDMA Timing Register 2 (HUDMA2)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

UDMA_TDS — ATA-5 standard UDMA timing t_{DS}

t_{DS} is Ultra DMA read data setup time, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.For current implementation, this register is not used.

UDMA_TDH — ATA-5 standard UDMA timing t_{DH}

t_{DH} is Ultra DMA read data hold time, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.For current implementation, this register is not used.

Address Offset: $18

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	UDMA_TDVS					0	0	0	0	0	UDMA_TDVH		
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-13 UDMA Timing Register 3 (HUDMA3)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

UDMA_TDVS — ATA-5 standard UDMA timing t_{DVS}

t_{DVS} is Ultra DMA write data setup time, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

UDMA_TDVH — ATA-5 standard UDMA timing t_{DVH}

t_{DVH} is Ultra DMA write data hold time, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

Address Offset: $1A

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	UDMA_TFS						0	0	UDMA_TLI					
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-14 UDMA Timing Register 4 (HUDMA4)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

UDMA_TFS — ATA-5 standard UDMA timing t_{FS}

t_{FS} is first strobe time during the initiation of Ultra DMA data transfer, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.For current implementation, this register is not used.

UDMA_TLI — ATA-5 standard UDMA timing t_{LI}

t_{LI} is limited interlock time with a defined maximum, when the drive or host are waiting for a response from each other, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.For current implementation, this register is not used.

Address Offset: $1C

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	UDMA_TMLI			0	0	0	0	0	UDMA_TAZ		
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-15 UDMA Timing Register 5 (HUDMA5)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

UDMA_TMLI — ATA-5 standard UDMA timing t_{MLI}

t_{MLI} is limited interlock time with a defined minimum, when the drive or host are waiting for a response from each other, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

UDMA_TAZ — ATA-5 standard UDMA timing t_{AZ}

t_{AZ} is maximum time allowed for output drivers to release from being driven, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.For current implementation, this register is not used.

Address Offset: $1E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	UDMA_TENV					0	0	0	0	UDMA_TSR			
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-16 UDMA Timing Register 6 (HUDMA6)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

UDMA_TENV — ATA-5 standard UDMA timing t_{ENV}

t_{ENV} is envelope time from ATA_DMACK_B to STOP and HDMARDY- during data-out burst initiation, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

UDMA_TSR — ATA-5 standard UDMA timing t_{SR}

t_{SR} is strobe to DMARDY time. If DMARDY is negated before this long after strobe edge then the recipient shall receive no more than one additional data word, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

Address Offset: $20

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	UDMA_TSS				0	0	0	UDMA_TRFS				
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-17 UDMA Timing Register 7 (HUDMA7)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

UDMA_TSS — ATA-5 standard UDMA timing t_{SS}

t_{SS} is the time from strobe edge to negation of ATA_DMARQ (when drive terminates the burst) or assertion of STOP (when host terminates the burst), and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

UDMA_TRFS — ATA-5 standard UDMA timing t_{RFS}

t_{RFS} is ready-to-final-strobe time. No strobe edges shall be sent this long after negation of DMARDY, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

Address Offset: $22

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	UDMA_TRP						0	0	0	0	0	UDMA_TACK		
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-18 UDMA Timing Register 8 (HUDMA8)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

UDMA_TRP — ATA-5 standard UDMA timing t_{RP}

t_{RP} is ready-to-pause time. The time that recipient shall wait to initiate pause after negating DMARDY, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

UDMA_TACK — ATA-5 standard UDMA timing t_{ACK}

t_{ACK} is setup and hold times for ATA_DMACK_B before negation or assertion, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

Address Offset: $24

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	UDMA_TZAH			0	0	0	0	0	0	0	0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-19 UDMA Timing Register 9 (HUDMA9)

This register provides timing on toggling control signals and strobing/detecting data bus. The resolution is a single cycle module core clock time duration, and users should set this register to satisfy timing requirement as specified in ATA-5 standard.

UDMA_TZAH — ATA-5 standard UDMA timing t_{ZAH}

t_{ZAH} is minimum delay time required for output drivers to assert or negate from release state, and this timing register should be set according to the supported mode, mode 0, 1, 2, 3, 4.

3.1.2 Device Drive Registers

These registers are actually located at the device. By reading/writing these mirror registers in ATA5HC, a PIO transfer will be issued to access the corresponding internal register in the device. The following table shows the address lines ATA_CS1_B, ATA_CS0_B, ATA_DA0, ATA_DA1 and ATA_DA2 w.r.t each mirror registers

Table 3-2 Address Map for internal ATA device drive registers

ATA_CS0_B	ATA_CS1_B	ATA_DA2	ATA_DA1	ATA_DA0	Use
1	0	1	1	0	ATA Drive Control Register (DCTR) (For Write)
					ATA Drive Alternate Status Register (DASR) (For Read)
0	1	0	0	0	ATA Drive Data Register (DDR)
0	1	0	0	1	ATA Drive Feature Register (DFR) (For Write)
					ATA Drive Error Register (DER) (For Read)
0	1	0	1	0	ATA Drive Sector Count Register (DSCR)
0	1	0	1	1	ATA Drive Sector Number Register (DSNR)

0	1	1	0	0	ATA Drive Cylinder Low Register (DCLR)
0	1	1	0	1	ATA Drive Cylinder High Register (DCHR)
0	1	1	1	0	ATA Drive Device/Head Register (DDHR)
0	1	1	1	1	ATA Drive Command Register (DCR) (For Write)
					ATA Drive Status Register (DSR) (For Read)

Note: 0 - voltage low; 1 - voltage high

The reset value of these registers are device dependent, and they shall not be specified in this block guide.

Address Offset: $2E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	BSY	DRDY	#		DRQ	obs		ERR	0	0	0	0	0	0	0	0
W						SRST	nIEN	ZERO								
RESET:	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

= Unimplemented or Reserved

Figure 3-20 ATA drive device control/alternate status register (DCTR/DASR)

This register is an ATA drive register. When written, it is device control register (DCTR). When read, it is alternate status register (DASR).

SRST — Host controlled software reset bit
1 = Drive executes software reset protocol.
0 = No operation.

nIEN — Host controlled interrupt enable
1 = ATA_INTRQ is disabled.
0 = ATA_INTRQ is enabled. For ATA host controller, enabling ATA_INTRQ is mandatory for DMA/UDMA data transfer modes.

ZERO — Mandatory clear bit when written
1 = Not allowed.
0 = When writing to this register, this bit must be always cleared to 0.

BSY — Drive busy
1 = transfers internal to drive are in progress. Host shall wait.
0 = No transfer in progress.

DRDY — Drive ready
1 = Ready.

0 = Not ready.

— ATA command dependent field

DRQ — Drive ready
1 = Indicates drive is ready to transfer a word of data.
0 = Not ready for transfer.

obs — obsolete fields

ERR — Drive error indicator
1 = Indicates an error during the execution of the previous command. For example, user should check this bit to see whether last UDMA data transfer is successful or not. That is, it is to check whether there is a CRC error in this case
0 = No error present.

Address Offset: $30

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	BYTE_E								BYTE_O							
RESET:	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

= Unimplemented or Reserved

Figure 3-21 ATA Drive Data Register (DDR)

This register is ATA drive data port register for read/write transfer.

BYTE_E — Even address byte of drive data. This should correspond to DD[7:0] in ATA-5 specification.

BYTE_O — Odd address byte of drive data. This should correspond to DD[15:8] in ATA-5 specification.

Address Offset: $32

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	#r1					ABRT	#r2		0	0	0	0	0	0	0	0
W	#w															
RESET:	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

= Unimplemented or Reserved

Figure 3-22 ATA Drive Feature/Error Register (DFR/DER)

When written, it is drive feature register (DFR).

#w — The content of this register is command dependent. The content of this register become command parameters when the ATA drive Command register is written.

Note:

- This register is written only when BSY and DRQ bits in register DSR equal zero and ATA_DMACK_B is not asserted.
- If this register is written when BSY and DRQ bits are set to one, the result is indeterminate.

When read, it is drive error register (DER). The content is valid when BSY and DRQ bits are set to zero and the ERR bit is set to one in register DSR. The content of this register is not valid when the drive is in the sleep mode.

#r1 — ATA command dependent field

ABRT — Drive command aborted

1 = Indicates that the requested command has been aborted because the command code or a command parameter is invalid or some other error has occurred.

0 = No abortion yet.

#r2 — ATA command dependent field

Address Offset: $34

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	#								0	0	0	0	0	0	0	0
W																
RESET:	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

= Unimplemented or Reserved

Figure 3-23 ATA Drive Sector Count Register (DSCR)

This ATA Drive register stores the sector count information.

— The content of these bits is command dependent. See chapter 8 of ATA-5 spec. for details. For most of the read/write commands, this register indicates the total number of sectors requested for transfer.

Note:

- This register is written only when BSY and DRQ bits in register DSR equal zero and ATA_DMACK_B is not asserted.
- If this register is written when BSY and DRQ bits are set to one, the result is indeterminate.
- The content of this register is not valid when the drive is in the sleep mode.

Address Offset: $36

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	#								0	0	0	0	0	0	0	0
W																
RESET:	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

= Unimplemented or Reserved

Figure 3-24 ATA Drive Sector Number Register (DSNR)

This ATA Drive register stores the sector number information.

— The content of these bits is command dependent. See chapter 8 of ATA-5 spec. for details. For most commands, this register indicates the starting sector number for the data transfer when CHS addressing is enabled. This register indicates part of the LBA address when the LBA addressing is enabled.

Note:

- This register is written only when BSY and DRQ bits in register DSR equal zero and ATA_DMACK_B is not asserted.
- If this register is written when BSY and DRQ bits are set to one, the result is indeterminate.
- The content of this register is not valid when the drive is in the sleep mode.

Address Offset: $38

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	#								0	0	0	0	0	0	0	0
W																
RESET:	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

= Unimplemented or Reserved

Figure 3-25 ATA Drive Cylinder Low Register (DCLR)

This ATA Drive register stores the lower 8-bit of cylinder address information.

— The content of these bits is command dependent. See chapter 8 of ATA-5 spec. for details. For most commands, this register indicates the lower eight bits of the CHS address when CHS addressing is enabled for the data transfer.This register indicates part of the LBA address when the LBA addressing is enabled.

Note:

- This register is written only when BSY and DRQ bits in register DSR equal zero and ATA_DMACK_B is not asserted.
- If this register is written when BSY and DRQ bits are set to one, the result is indeterminate.
- The content of this register is not valid when the drive is in the sleep mode.

Address Offset: $3A

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	#								0	0	0	0	0	0	0	0
W																
RESET:	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

= Unimplemented or Reserved

Figure 3-26 ATA Drive Cylinder High Register (DCHR)

This ATA Drive register stores the upper 8-bit of cylinder address information.

— The content of these bits is command dependent. See chapter 8 of ATA-5 spec. for details. For most commands, this register indicates the upper eight bits of the CHS address when CHS addressing is enabled for the data transfer.This register indicates part of the LBA address when the LBA addressing is enabled.

Note:

- This register is written only when BSY and DRQ bits in register DSR equal zero and ATA_DMACK_B is not asserted. If this register is written when BSY and DRQ bits are set to one, the result is indeterminate.
- The content of this register is not valid when the drive is in the sleep mode.

Address Offset: $3C

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	obs	#1	obs	DEV	#2				0	0	0	0	0	0	0	0
W																
RESET:	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

= Unimplemented or Reserved

Figure 3-27 ATA Drive Device/Head Register (DDHR)

This ATA Drive register stores device and header information.

obs — Obsolete, not used.

#1 — This bit is command dependent. In LBA addressing mode, this bit is set to one to indicate LBA addressing is chosen for the data transfer.

obs — Obsolete, not used.

DEV — This bit becomes effective when this register is written by the host or the signature is set by the drive. This bit distinguishes between the drive 0 and drive 1 connected to the ATA host controller.

1 = Device 1.
0 = Device 0.

#2 — The content of these bits is command dependent. See chapter 8 of ATA-5 spec. for details. For most commands, these bits indicate the head number when CHS addressing is enabled for the data transfer.These bits indicate part of the LBA address when the LBA addressing is enabled.

Note:

- This register is written only when BSY and DRQ bits in register DSR equal zero and ATA_DMACK_B is not asserted.
- The content of this register are valid only when BSY bit in register DSR is cleared to zero.
- If this register is written when BSY or DRQ bits are set to one, the result is indeterminate.
- The content of this register is not valid when the drive is in sleep mode.

- The DEV bit should always be written with 0 since this host controller module will only support single device configuration.

Address Offset: $3E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	BSY	DRDY	#r		DRQ	obs		ERR	PIE	HUT	AF	0	IE	UDMA	RD	WR
W	#w															
RESET:	--	--	--	--	--	--	--	--	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-28 ATA Drive Command Register (DCR/DSR) and ATA DMA mode register (HDMAM)

This register location actually represents two 8-bit device driver registers and one 8-bit host controller register. Bit 15-8 represent ATA device internal register DCR/DSR, while Bit 7-0 represent ATA Host Controller DMA mode register (HDMAM). They are putting together for the ease of programming.

When written, bit 15-8 represent ATA Drive Command Register (DCR):

#w — This field contains the command code being sent to the drive. Command execution begins immediately when this register is written. Writing this register clears any pending interrupt condition. See annex F of ATA-5 spec. for command codes and more details.

Note:

- For all commands except DEVICE RESET, this register is written only when BSY and DRQ bits in register DSR equal zero and ATA_DMACK_B is not asserted.
- If this register is written when BSY or DRQ bits are set to one, the result is indeterminate except for the DEVICE RESET command.
- The content of this register is not valid when the drive is in sleep mode.

When read, bit 15-8 represent ATA Drive Status Register (DSR):

BSY — Indicates that the drive is busy processing a command
1 = Busy.
0 = Not busy.

DRDY — Indicates that the drive is ready to accept executable commands
1 = Ready.
0 = Not ready.

#R — Command dependent. See chapter 8 of ATA-5 spec.

DRQ — Indicates that the drive is ready to transfer a word of data.
1 = Ready.
0 = Not ready.

obs — Obsolete, ignore it.

ERR — Indicates that the bits in the ATA drive Error register (DER) are valid or not.
1 = Valid.
0 = Not valid.
Note:
- The content of this register, except BSY, are invalid when BSY is set to one. BSY is valid at all times.
- Reading this register clears any pending interrupt condition. Host should read Alternate Status register instead when an interrupt is expected.
- The content of this register is not valid when the drive is in sleep mode.

Bit 7-0 represent ATA DMA mode register (HDMAM).

PIE — Pause Interrupt Enable. Enable ATA host to interrupt when ATA UDMA transfer pause is extended for 256 module core clock cycles. The software may set HUT bit of this register to terminate the hung/extended paused UDMA burst. The UREP bit of HSR is set to indicate that the extended pause has happened. This bit must not be written if wait count is larger than 256 module core clock cycles. The software may use other ATA5HC general purpose timers to monitor drive inactivity.
1 = Enable.
0 = Disable.

HUT — Host UDMA burst Terminate. Software can terminate UDMA burst prematurely, by setting this bit. Bits 5 through 0 are un-affected and will retain their previous values.
1 = Terminate Host UDMA burst.
0 = No effect.

AF — Automatic FIFO reset for AFIFO sub-block when UDMA or Multiword DMA transfer starts.However, in UDMA transfer, device could intermittenly turn on/off the DMARQ line, and this behavior will cause unexpected result. Therefore, UDMA transfer with AF = 1 is not recommended for a fool proof configuration.
1 = Reset FIFO.
0 = No operation.

IE — Enable drive interrupt to pass to CPU in DMA/UDMA modes. (see note)

Mandatory: Drive interrupt must be enabled by clearing nIEN bit of ATA drive device control register for DMA/UDMA mode transfers.
1 = Enable.
0 = Disable.

UDMA — This bit is set when UDMA protocol is selected, cleared when multiword DMA protocol is selected.
1 = UDMA protocol is selected.
0 = Multiword DMA protocol is selected.

RD — This bit is set when READ DMA command is issued.
1 = READ DMA is issued.

0 = Not issued.

WR — This bit is set when WRITE DMA command is issued.
1 = WRITE DMA is issued.
0 = Not issued.

Section 4 Functional Description

This ATA5HC module supports ATA-5 data transactions with single device configuration. All of the ATA device internal registers are visible to users as mirror registers in ATA5HC. In ATA-5 standard, all the features/functions are implemented by reading/writing to the device internal registers. Therefore, it is users' responsibility to provide software driver for this ATA5HC, and this ATA5HC will only support interface protocols.

There is an asynchronous hardware reset signal that will reset all hardware logics inside this module. Beside hardware reset, AFIFO and ASM block can also be reset independently by writing to FR bit and SMR bit of Host Configuration register (HCFG).

Interrupt signal to CPU (ipi_int) is asserted under the following conditions:

- During DMA transfer, IE bit of HDMAM register is set and ATA_INTRQ signal is asserted
- During PIO transfer, IE bit of HCFG register is set and ATA_INTRQ signal is asserted
- In UDMA transfer, pause is enforced for an extended period of 256 module core clock or above

4.1 ATA data transfers

There are three types ATA data transfers: PIO Mode, Multiword DMA Mode and Ultra DMA Mode.

4.1.1 PIO data transfer

When reading/writing from/to a device drive internal registers, a PIO data transfer is initiated. The ASM block in ATA5HC will take care of PIO protocol timing and control signals hand-shaking. However, the timing attributes are still coming from the timing registers HPIO1, HPIO2, HPIO3, and HPIO4. Users should set up these timing registers before reading/writing from/to a device drive internal registers. The timing diagram of PIO data transfer is shown in Appendix A.

4.1.2 Multiword DMA data transfer

Both Multiword DMA and Ultra DMA data transfer are invoked when users write a DMA commands such as READ DMA and WRITE DMA to the device command register (DCR). The device will look at the transfer mode field that has been previously set with the SET FEATURE command to determine whether it is a Multiword or Ultra DMA data transfer. If it is Multiword DMA and device is ready, the device will initiate the data transfer by asserting the ATA_DMARQ line. The ASM will take care of timing and control signals hand-shaking. Similar to PIO data transfer, the timing registers for Multiword DMA protocol are needed to be set before transfer.

Since the ATA5HC doesn't keep track of the commands that have been sent to the device, the ASM block will have no knowledge of whether it should be a read or write DMA command. Also, the type of DMA transfer is not known either. Therefore, the ATA DMA mode register is put together with DCR so that all of the missing information are simultaneously provided to the ASM block when DMA commands are sent. However, it is users' responsibility to do book keeping in software.

The timing diagrams are shown in Appendix B. The Multiword DMA data transfer consists of the following steps:

- Initiating the Multiword DMA data transfer by Device by asserting ATA_DMARQ.
- Sustaining the Multiword DMA data transfer.
- Both of host and device can terminate the data transfer.

After initiating the data transfer, ATA5HC may not be able to sustain the data transfer when IP FIFO Bus may not be ready to receive/transmit data for an extended period. Under such conditions, ATA_DIOR_B (when receiving data from device) and ATA_DIOW_B (when transmitting data to device) will not toggle, which will temporarily pause the data transfer.

4.1.3 Ultra DMA data transfer

The procedure in invoking Ultra DMA transfer is the same as Multiword DMA data transfer except that the transfer field in SET FEATURE command is set to Ultra DMA mode. The ASM block will also take care of protocol timing and control signals hand-shaking.

The timing diagrams for Ultra DMA mode are shown in Appendix C. The Ultra DMA data-in (reading data from device) transfer consists of the following steps:

- Initiating the Ultra DMA data transfer by 1) asserting ATA_DMARQ by Device and 2) Host responds with asserting ATA_DMACK_B
- Sustaining the Ultra DMA data transfer
- Host can pause the data transfer (optional)
- Both Host and Device can terminate the transfer, but only host will return CRC to device

The Ultra DMA data-out (writing data to device) transfer consists of the following steps:

- Initiating the Ultra DMA data transfer by 1) asserting ATA_DMARQ by Device and 2) Host responds with asserting ATA_DMACK_B
- Sustaining the Ultra DMA data transfer
- Device can pause the data transfer (optional)
- Both Host and Device can terminate the transfer, but only host will return CRC to device

4.2 Timing Attributes and Effective Data Rate

The timing attributes for PIO, Multiword DMA and Ultra DMA are implemented with module core clock period resolution. One can choose an arbitrary frequency for module core clock to illustrate the timing attributes calculation. Without loss of generality, let module core clock frequency be 60 MHz, that is, clock period is 16.7 ns. The cases on "max" and "min" requirement will be considered.

- For "max" requirement, e.g. t_{FS} in Ultra DMA mode 4 data-in burst (120 ns), users should set the field UDMA_TFS in register HUDMA4 to be less than or equal to 7. Therefore, the effective t_{FS} is 117 ns or less, and the "max" requirement is met.

- For "min" requirement, e.g. t_{CYC} in Ultra DMA mode 4 data-out burst (25 ns), users should set the field UDMA_TCYC in register HUDMA1 to be 2. Therefore, the effective t_{CYC} is 2 * 16.7 ns, which is greater than the minimum requirement 25 ns on t_{CYC}, and the requirement is met. Consequently, the effective data rate is actually 60 MByte/s.

Moreover, the effective data rate depends not only on these "min" and "max" timing attributes, but also on the throughput in IP FIFO Bus. Consider the following situation with:

- Ultra DMA mode 4 data-in data transfer
- Module core clock frequency at 60 MHz (same as clock frequency at IP FIFO Bus)
- IP FIFO Bus is 16-bit wide
- Percentage of cycles with actual data transfer at less than 0.5, e.g. one out of three cycles in IP FIFO Bus is being used in data transfer, and ATA5HC is waiting for IP FIFO Bus acknowledgement in other two cycles

The effective data rate is actually 2 * 60 * 0.33 MByte/s, and it is approximately equal to 40 MByte/s. Even though Ultra DMA mode 4 could provide 66 MByte/s data transfer bandwidth, the effective data rate is limited by IP FIFO Bus.

4.3 Sub-block AFIFO

This asynchronous FIFO (AFIFO) serves as a bi-directional data buffer for reading/writing data over ATA-5 interface. For receiving data in Ultra DMA data-in mode, it behaves as an asynchronous FIFO. While in all other cases of data transfer, it behaves as a synchronous FIFO.

4.4 Sub-block ASM

The ATA5HC state machine (ASM) will govern control logic generation and data movement, and it will support PIO, Multi-word DMA, Ultra DMA data transfer. Upon writing the device command registers, this sub-block will do the followings:

- toggling control lines properly such as ATA_DMACK_B, ATA_DIOR_B, etc.
- checking on device handshake signals such as ATA_DMARQ, ATA_INTRQ, etc.
- move data by reading/writing AFIFO sub-block in DMA modes, or a data buffer in PIO mode.

4.5 Sub-block IPSI

The IP Slave bus interface (IPSI) will support IP Slave bus interfaces for host controller. It is fully complaint with SRS V3.0.

4.6 Sub-block IPFI

The IPFI will support IP FIFO Bus for bulk data transfer during Ultra DMA and Multiword DMA mode. It implements the minimum set of signal, but fully comply with SRS V3.0 standard.

Whenever AFIFO sub-block is almost full when receiving data from IP FIFO Bus, IPFI will stop requesting data from IP FIFO Bus. In case of IP FIFO Bus not able to stop sending data to ATA5HC in time, IPFI sub-block is designed to receive one more piece of data from IP FIFO Bus even though IPFI has already stopped requesting data.

Section 5 Initialization/Application Information

5.1 ATA Device Reset

Hardware Reset:

The system should assert RESET- over ATA interface for a minimum of 25us after the power has stabilized within the system's specified tolerance.

Software Reset:

The host shall set the SRST bit to 1 in the Device Control register. Any subsequent setting and clearing of SRST bit must be at least 5us apart. However, the host should not set the SRST bit to a 1 in the Device Control register to enable the drive for software reset or issue a DEVICE RESET command while the BSY bit is set to 1 in register DSR.

DEVICE RESET Protocol: (prohibited for drives not implementing PACKET command feature set - non-ATAPI)
The host shall write the DEVICE RESET command in the Command register. (code: 08h).
The host should not issue a DEVICE RESET command while a DEVICE RESET command is in progress or the results are indeterminate.

5.2 Device Connection Configuration

Users are recommended to adopt 80-pin connector for Ultra DMA mode 3 or above data transfer. ATA5HC will support single device configuration, and all ATA-5 standard interface signals should be connected except the following pins:

Table 5-1 ATA-5 interface pin connection exceptions

Interface Pin	Tied at / Unconnected	Destination
CBLID-	Unconnected	
CSEL	Ground	Device

5.3 Usage in different transfer modes

5.3.1 PIO Mode transfer

PIO Mode transactions are the simplest transaction available on the ATA interface, and essentially consist of single word accesses across the ATA interface. Five PIO modes are available, and the timing parameters is only the difference among different modes. Moreover, a group of ATA commands will utilize PIO transfer (see section 8 command description in ATA-5 standard), and this group will sub-divided into 3 classes.

Class 1: PIO Read
PIO Single Sector Read [Identify Drive, Read Buffer, Read Sector(s)]
Interrupt is generated after each sector is read into the sector buffer
1) HOST: Write to ATA Control/Command Block registers to setup for the data read
2) HOST: Write to ATA command register to execute the read command
3) HOST: Software polls drive to see if it is ready.
4) DRIVE: Read sector from the physical medium to the sector buffer
5) DRIVE: Interrupt the HOST when done
6) HOST: Read the ATA Control/Command Block registers to get the status
7) DRIVE: Clear interrupt upon reading of Status Register
8) HOST: Read the ATA Data Register 256 times to get all 512 bytes from the sector buffer
9) Repeat steps 4-8 for multiple sectors.

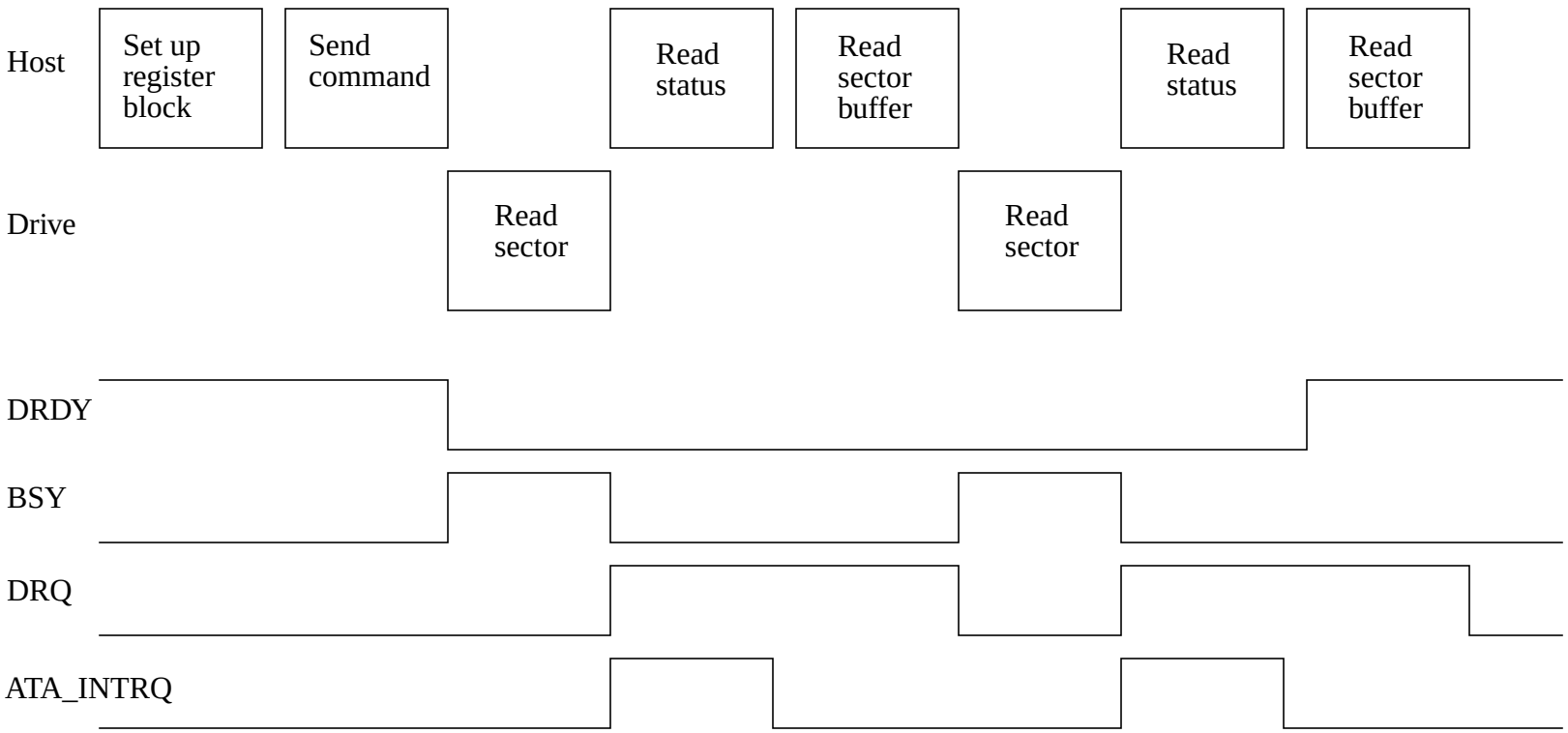


Figure 5-1 PIO Read Command (Class 1)

Class 2: PIO Write
Single Sector Write (Format, Write Buffer, Write Sector(s))
1) HOST: Write to ATA Control/Command Block registers to setup for the data write
2) HOST: Write to ATA command register to execute the write command
3) HOST: Software polls drive to see if it is ready.
4) HOST: Write the ATA Data Register 256 times to put all 512 bytes into the sector buffer
5) DRIVE: When the sector buffer is filled, write sector to the physical medium
6) DRIVE: Interrupt the HOST when done
7) HOST: Read the ATA Control/Command Block registers to get the status
8) DRIVE: Clear interrupt upon reading of Status Register
9) Repeat steps 4-8 for multiple sector writes

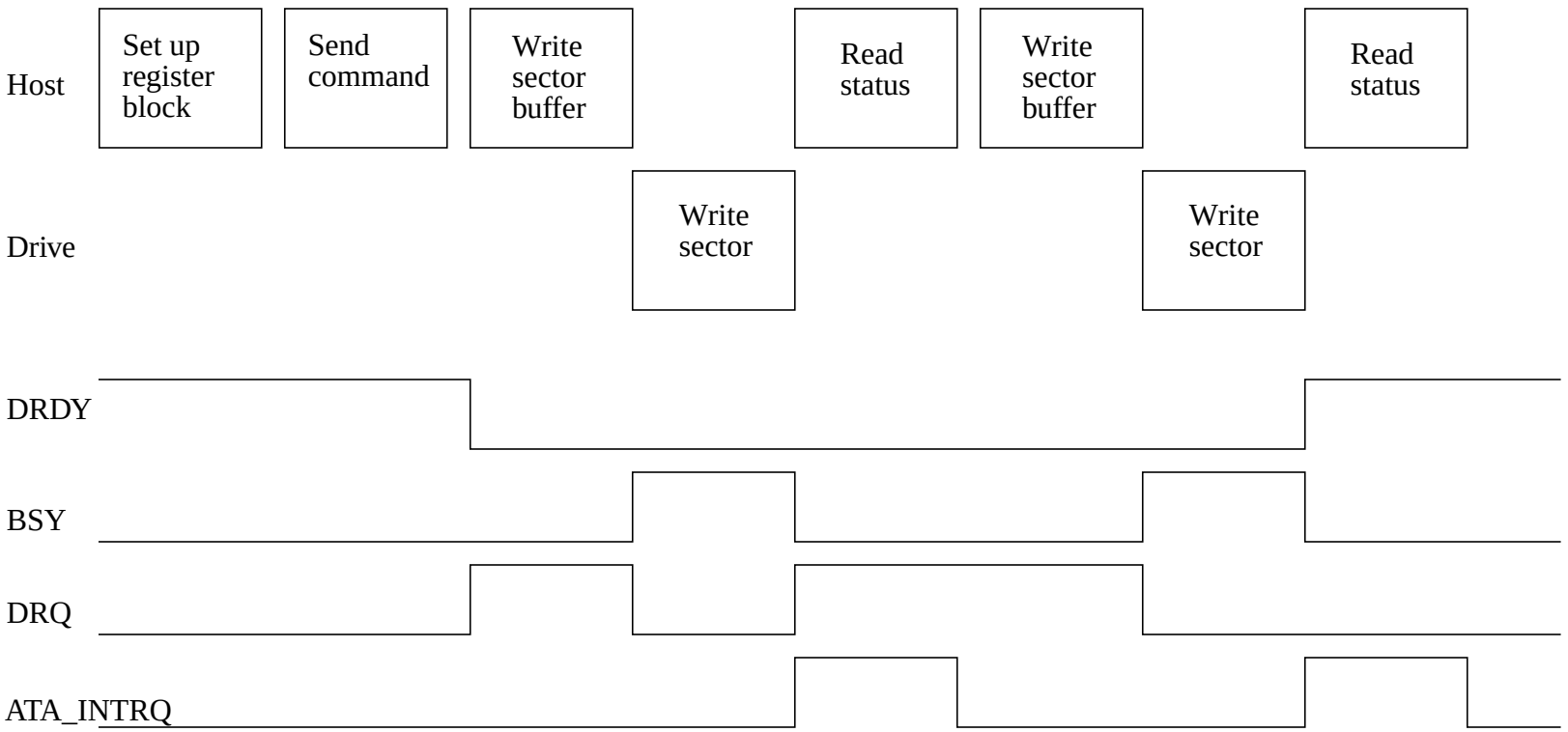


Figure 5-2 PIO Write Command (Class 2)

Class 3: Non-Data Command
1) HOST: Write to ATA Control/Command Block registers to setup for the data read
2) HOST: Write to ATA command register to execute the read command
3) DRIVE: Execute the command

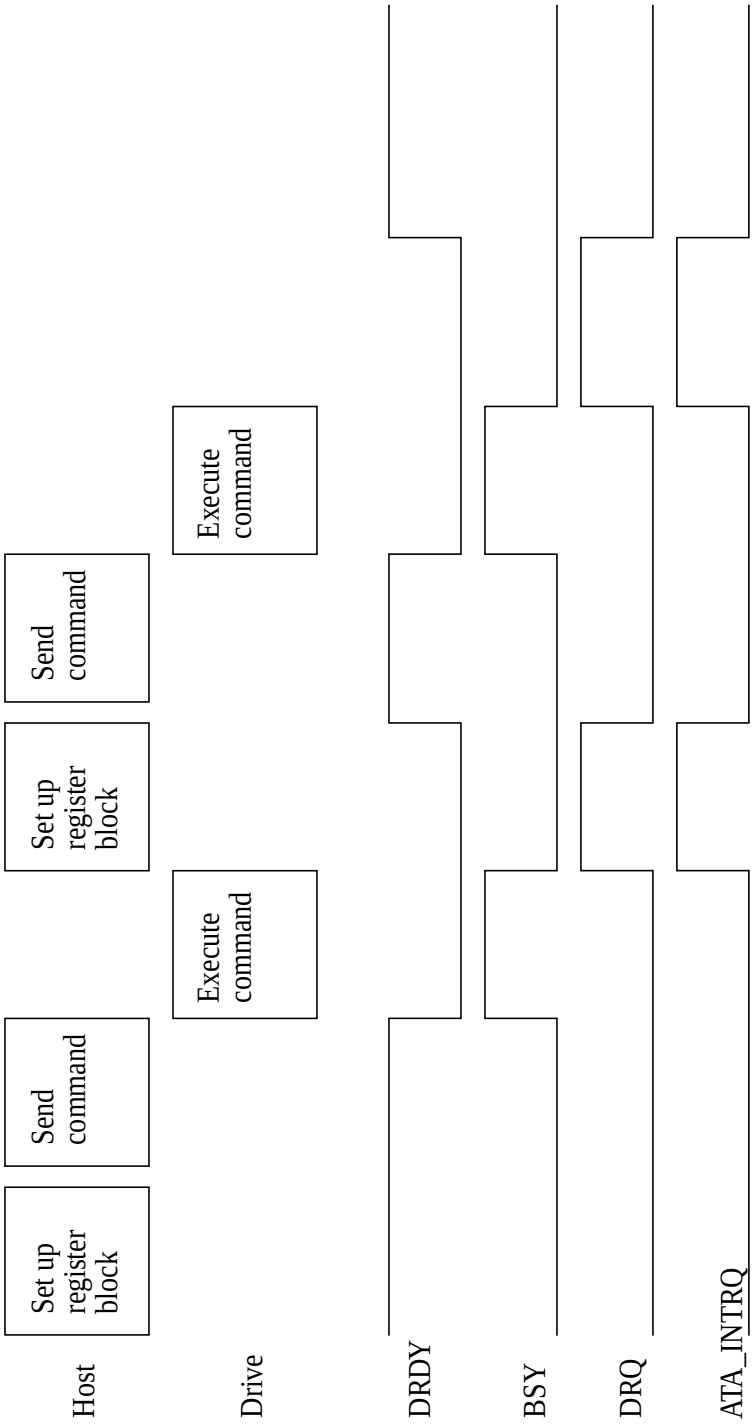


Figure 5-3 Non-Data Command (Class 3)

5.3.2 DMA data transfer

The DMA command comprises:

- READ DMA
- WRITE DMA

Both Multi-word DMA and Ultra DMA are DMA data transfer, they are invoked according to how the transfer field was set in SET FEATURE command previously. The following flow chart shows the software aspects and hardware aspects (those items involved with ATA_xxx signals) in DMA data transfer in a broad sense.

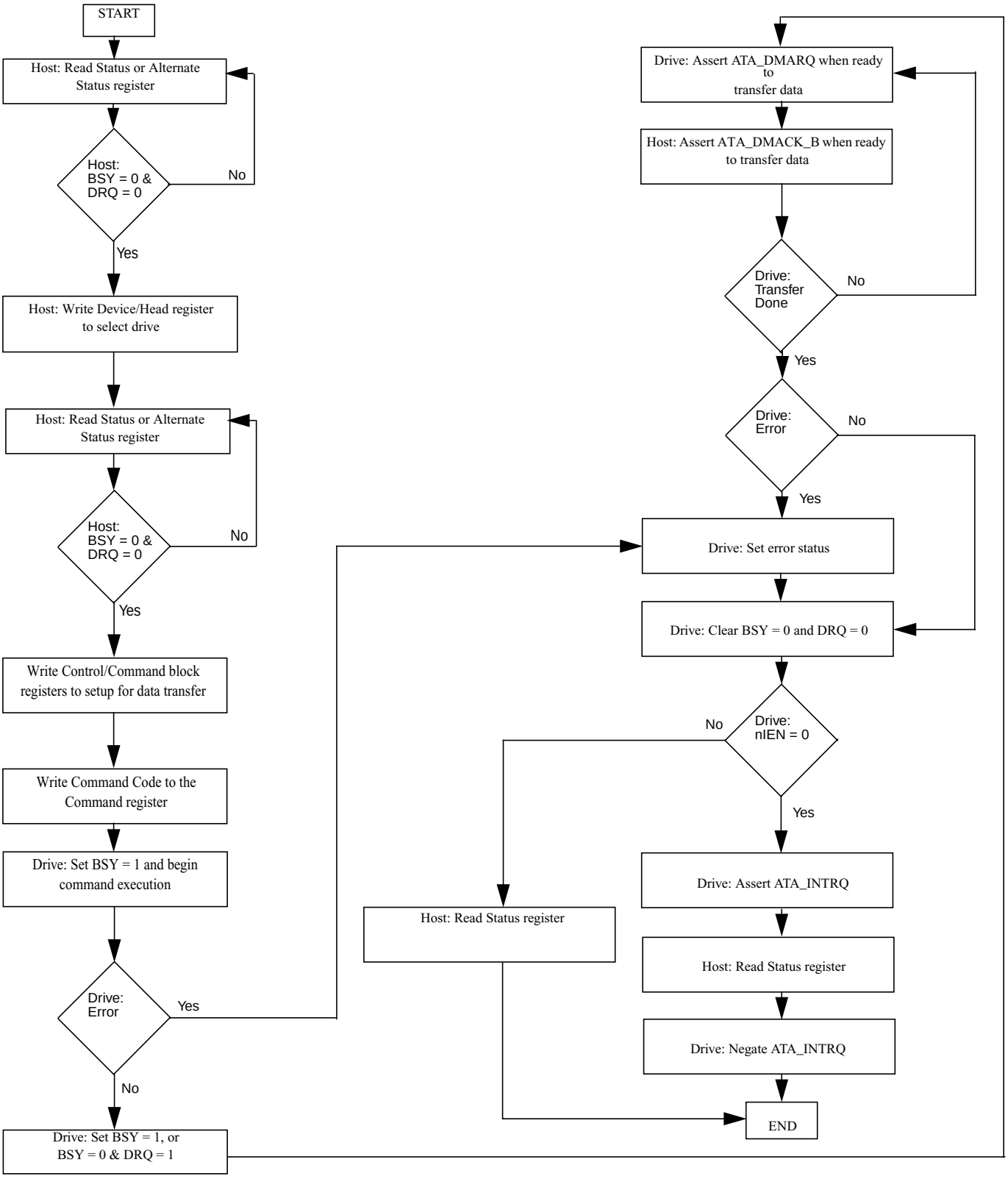


Figure 5-4 DMA Data Transfer Flow Chart

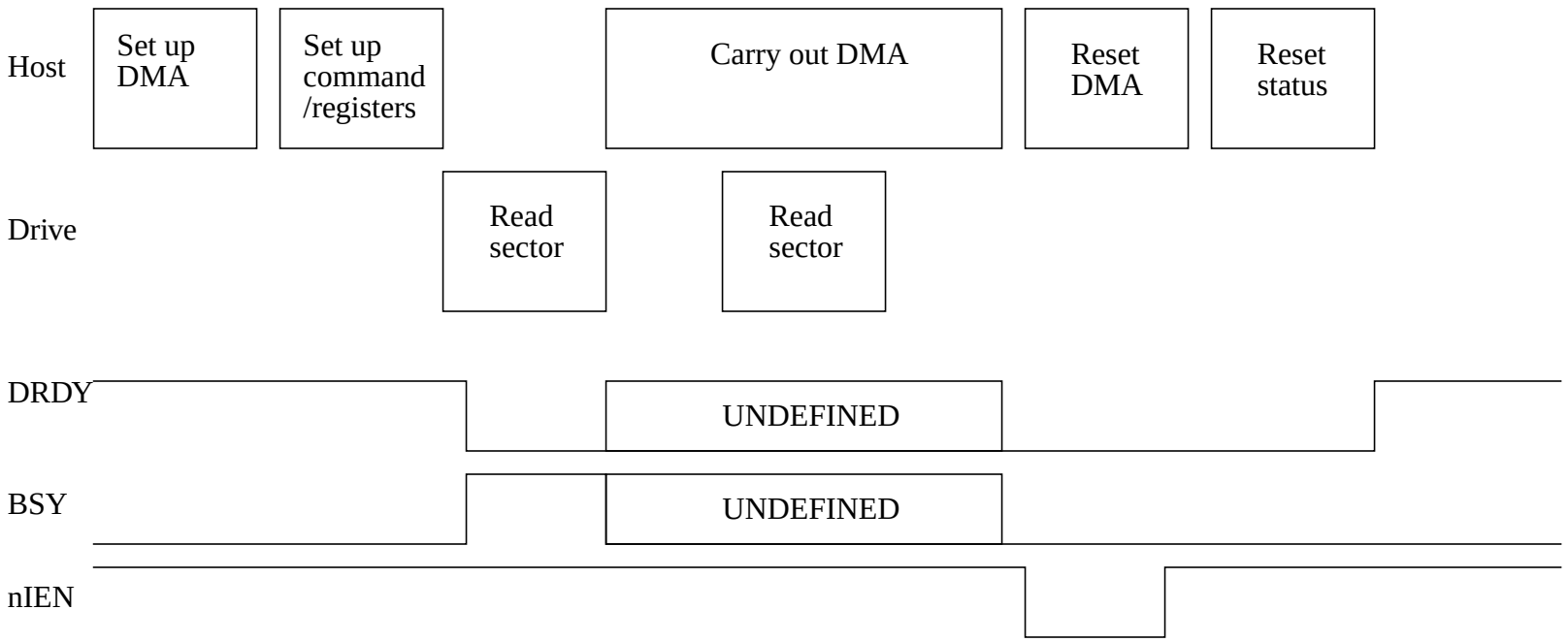
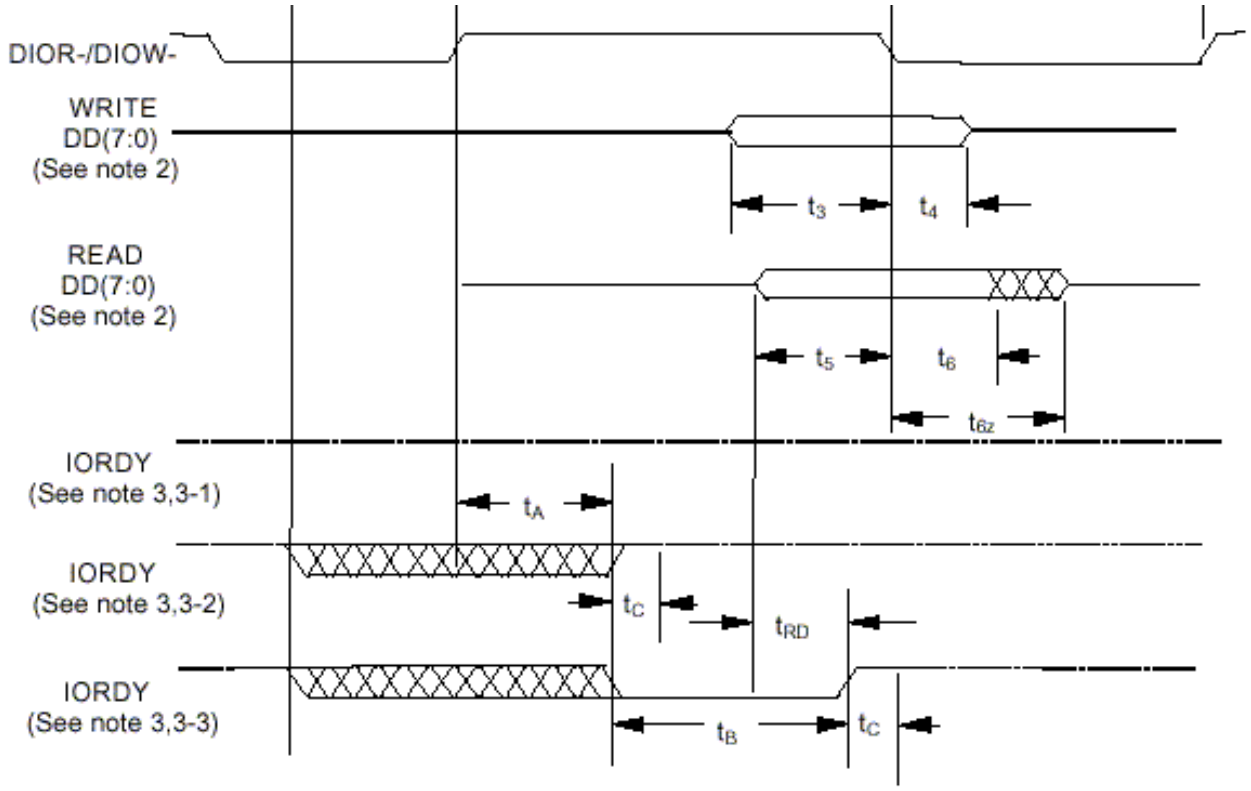


Figure 5-5 DMA Data Transfer Timing

Appendix A PIO Timing Diagrams

For active low signals such as DIOR-, asserted state means voltage low, while in active high signal such as IORDY, asserted state means voltage high.



NOTES –
1 Device address consists of signals CS0-, CS1- and DA(2:0)
2 Data consists of DD(7:0).
3 The negation of IORDY by the device is used to extend the register transfer cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:
3-1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.

Figure A-1 PIO data/register transfer to/from device

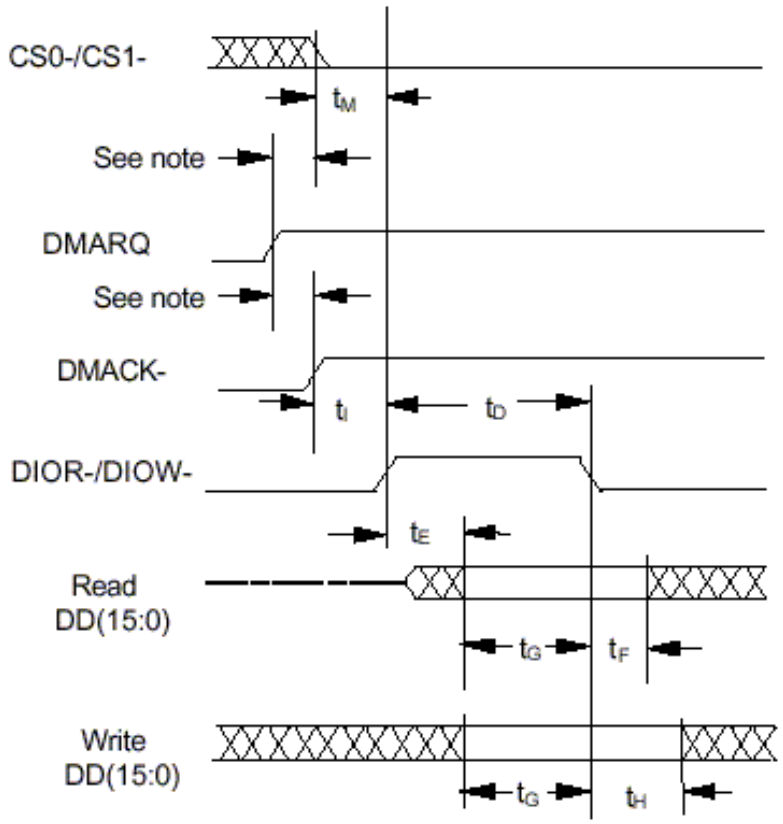
Table A-1 PIO data/register transfer timing

	PIO Timing Parameter	Min/ Max	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)
t0	Cycle Time	min	600	383	240	180	120
t1	Address valid to ATA_DIOR_B/ATA_DIOW_B setup	min	70	50	30	30	25
t2	ATA_DIOR_B/ATA_DIOW_B pulse width 16-bit 8-bit	min min	165 290	125 290	100 290	80 80	70 70
t2i	ATA_DIOR_B/ATA_DIOW_B recovery time	min	-	-	-	70	25
t3	ATA_DIOW_B data setup	min	60	45	30	30	20
t4	ATA_DIOW_B data hold	min	30	20	15	10	10
t5	ATA_DIOR_B data setup	min	50	35	20	20	20
t6	ATA_DIOR_B data hold	min	5	5	5	5	5
t9	ATA_DIOR_B/ATA_DIOW_B to address valid hold	min	20	15	10	10	10
tA	ATA_IORDY setup	max	35	35	35	35	35
tB	ATA_IORDY pulse width	max	1250	1250	1250	1250	1250

Note: All timing should be measured at the connector of the selected device.

Appendix B Multiword DMA Timing Diagrams

For active low signals such as DMACK-, asserted state means voltage low, while in active high signal such as DMARQ, asserted state means voltage high.



NOTE – The host shall not assert DMACK- or negate both CS0 and CS1 until the assertion of DMARQ is detected. The maximum time from the assertion of DMARQ to the assertion of DMACK- or the negation of both CS0 and CS1 is not defined.

Figure B-1 Initiating a Multiword DMA data transfer

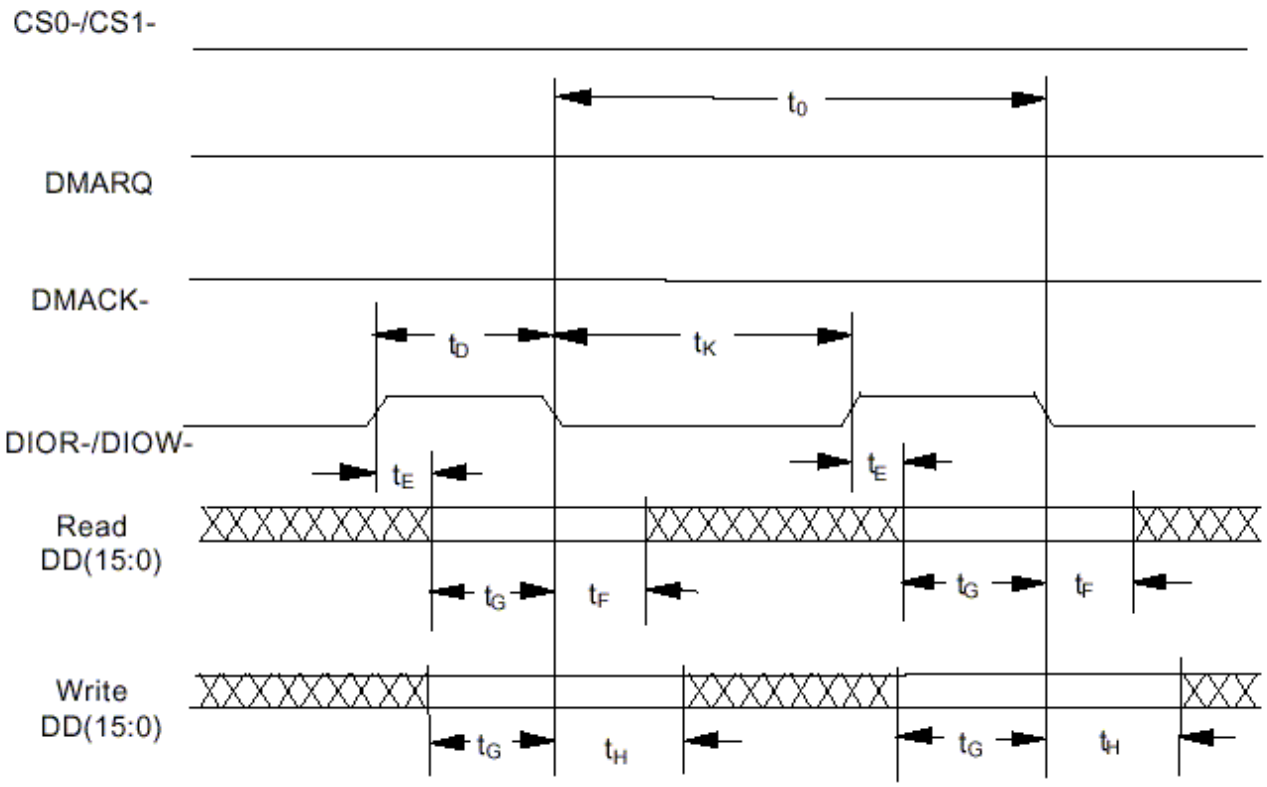
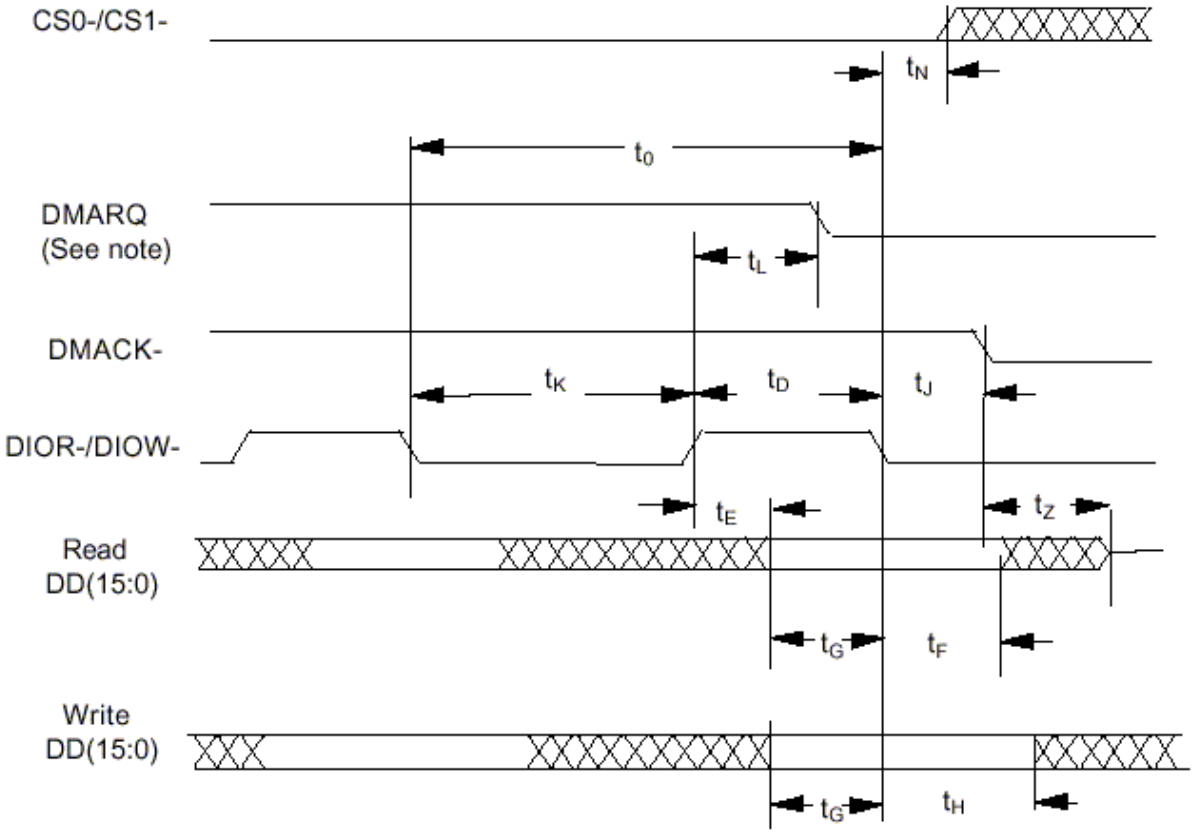
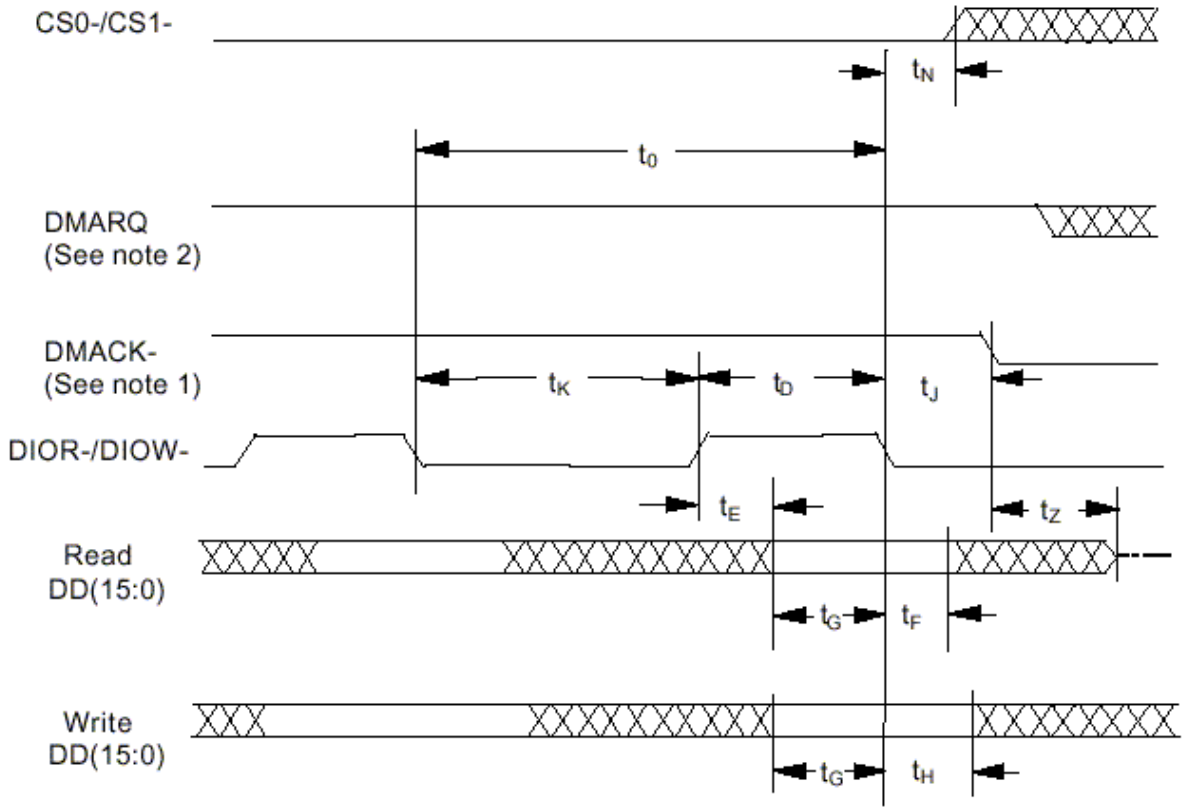


Figure B-2 Sustaining a Multiword DMA data transfer



NOTE – To terminate the data burst, the Device shall negate DMARQ within the t_L of the assertion of the current DIOR- or DIOW- pulse. The last data word for the burst shall then be transferred by the negation of the current DIOR- or DIOW- pulse. If all data for the command has not been transferred, the device shall reassert DMARQ again at any later time to resume the DMA operation

Figure B-3 Device terminating a Multiword DMA data burst



NOTE –
1 To terminate the transmission of a data burst, the host shall negate DMACK- within the specified time after a DIOR- or DIOW- pulse. No further DIOR- or DIOW- pulses shall be asserted for this burst.
2 If the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK- or may negate DMARQ at any time after detecting that DMACK- has been negated.

Figure B-4 Host terminating a Multiword DMA data burst

Table B-1 Multiword DMA data transfer timing

	Multiword DMA Timing Parameters	Min/Max	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)
t0	Cycle Time	min	480	150	120
tC	ATA_DMACK_B to ATA_DMARQ delay	max	---	--	--
tD	ATA_DIOR_B/ATA_DIOW_B pulse width (16-bit)	min	215	80	70
tE	ATA_DIOR_B data access	max	150	60	50
tG	ATA_DIOR_B/ATA_DIOW_B data setup	min	100	30	20
tF	ATA_DIOR_B data hold	min	5	5	5
tH	ATA_DIOW_B data hold	min	20	15	10
tI	ATA_DMACK_B to ATA_DIOR_B/ATA_DIOW_B setup	min	0	0	0
tJ	ATA_DIOR_B/ATA_DIOW_B to ATA_DMACK_B hold	min	20	5	5
tKr	ATA_DIOR_B negated pulse width	min	50	50	25
tKw	ATA_DIOW_B negated pulse width	min	215	50	25
tLr	ATA_DIOR_B to ATA_DMARQ delay	max	120	40	35
tLw	ATA_DIOW_B to ATA_DMARQ delay	max	40	40	35

Note: All timing should be measured at the connector of the selected device.

Appendix C Ultra DMA Timing Diagrams

For active low signals such as DMACK-, asserted state means voltage low, while in active high signal such as DMARQ, asserted state means voltage high.

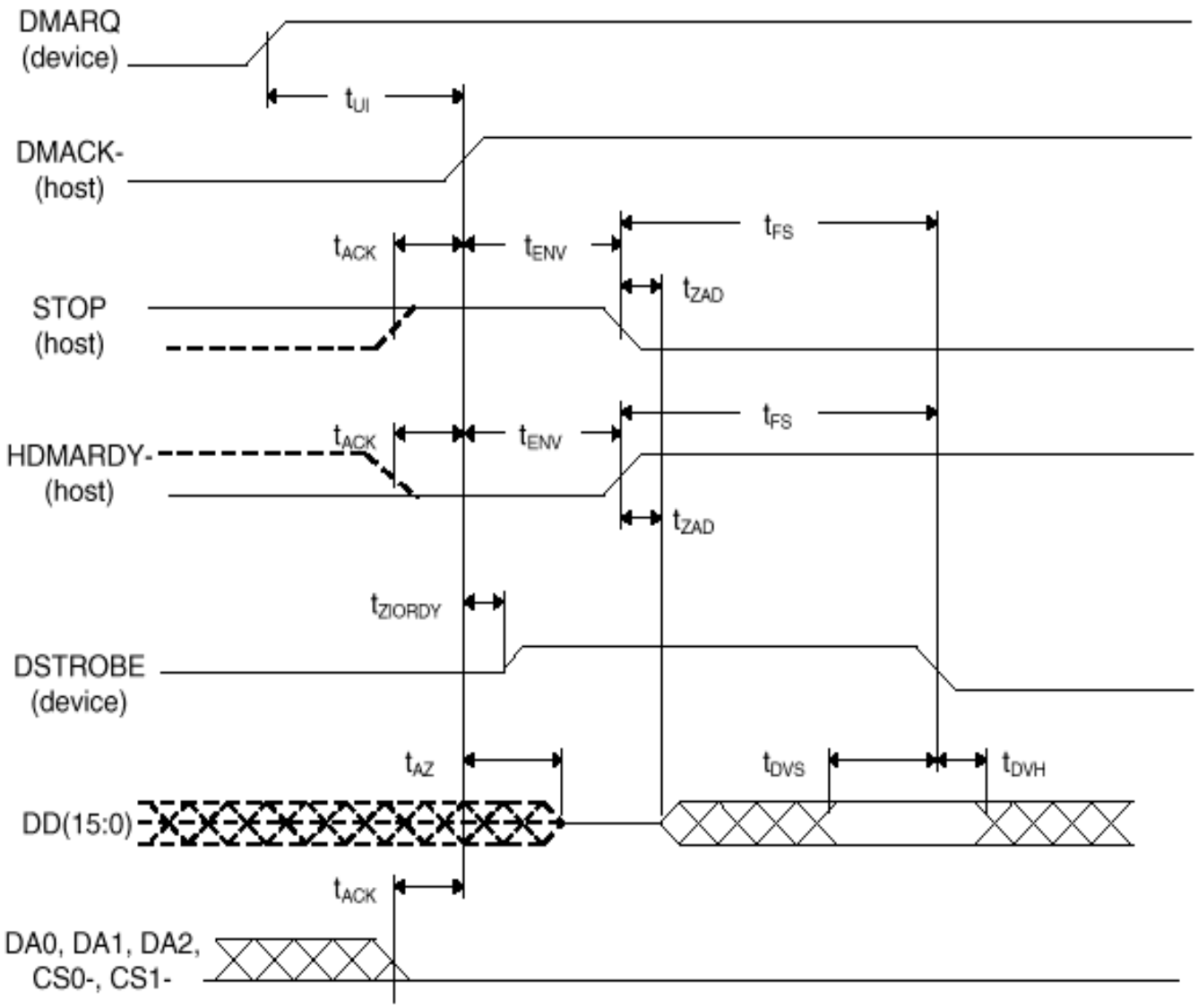


Figure C-1 Initiating an Ultra DMA data-in burst

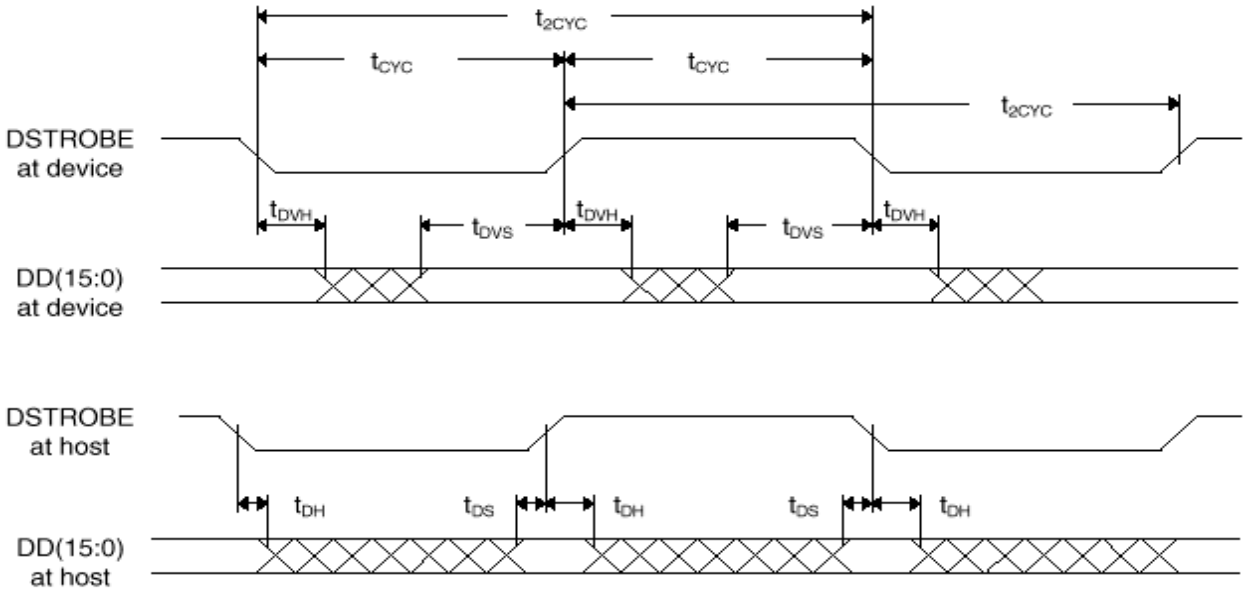


Figure C-2 Sustained Ultra DMA data-in burst

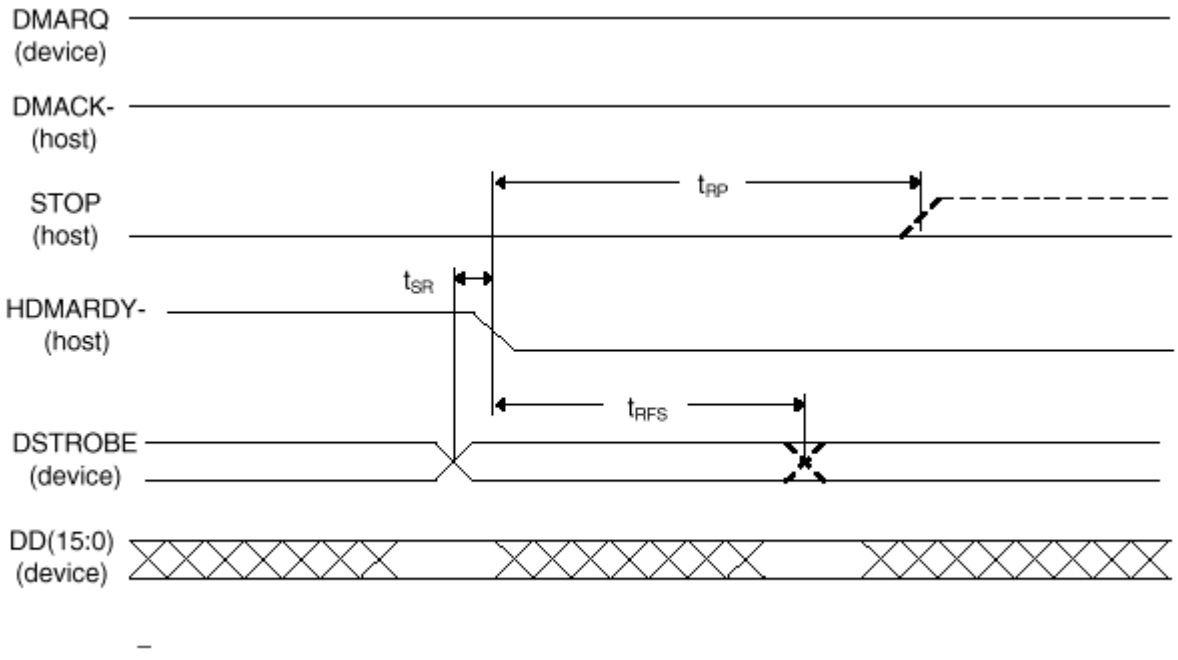


Figure C-3 Host pausing an Ultra data-in burst

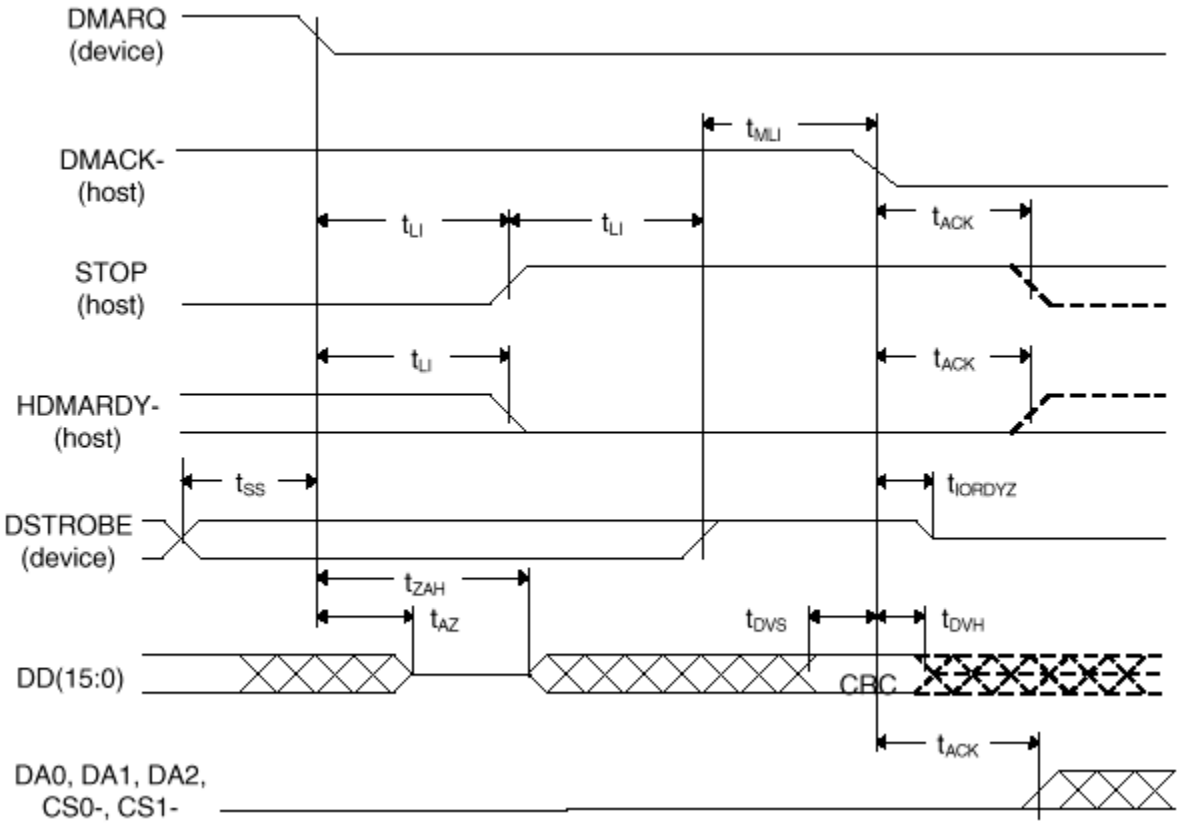


Figure C-4 Device terminating an Ultra DMA data-in burst

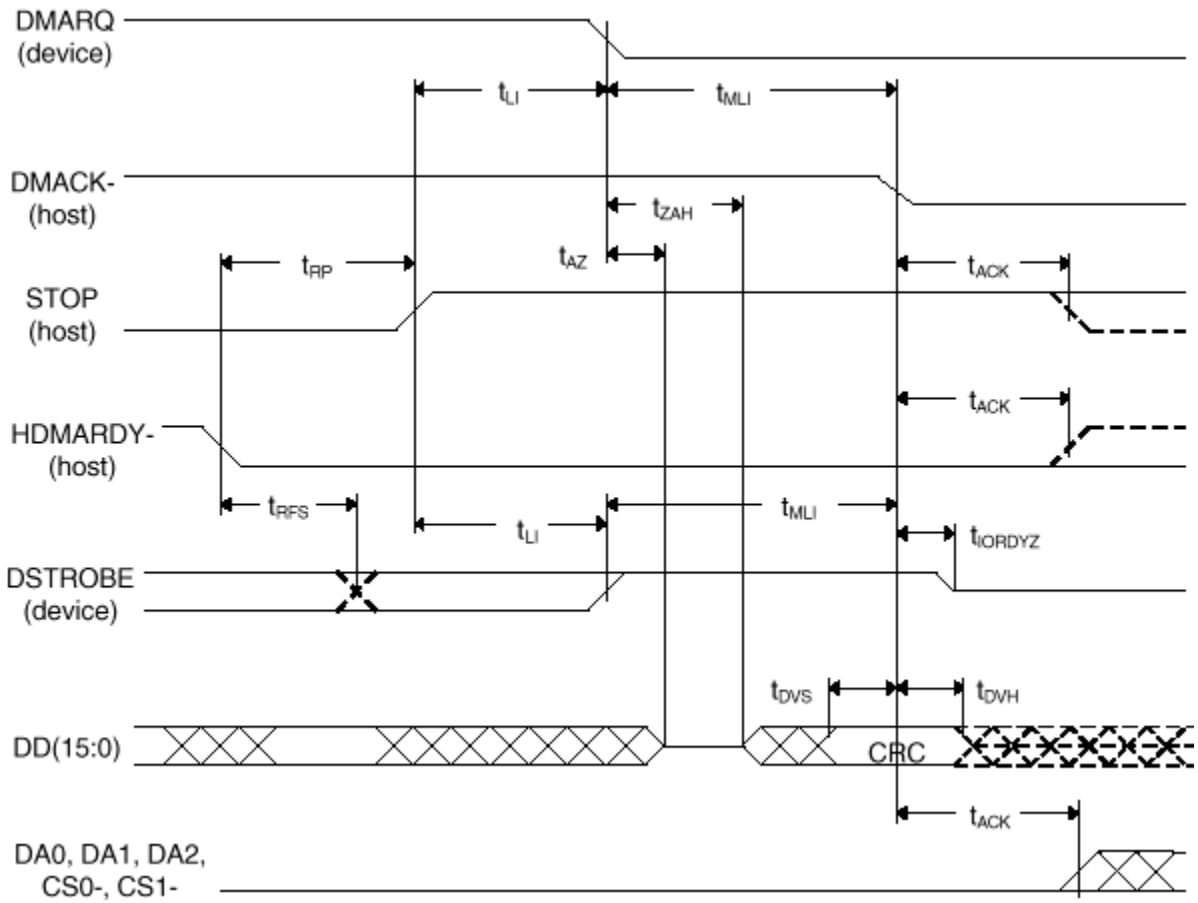


Figure C-5 Host terminating an Ultra data-in burst

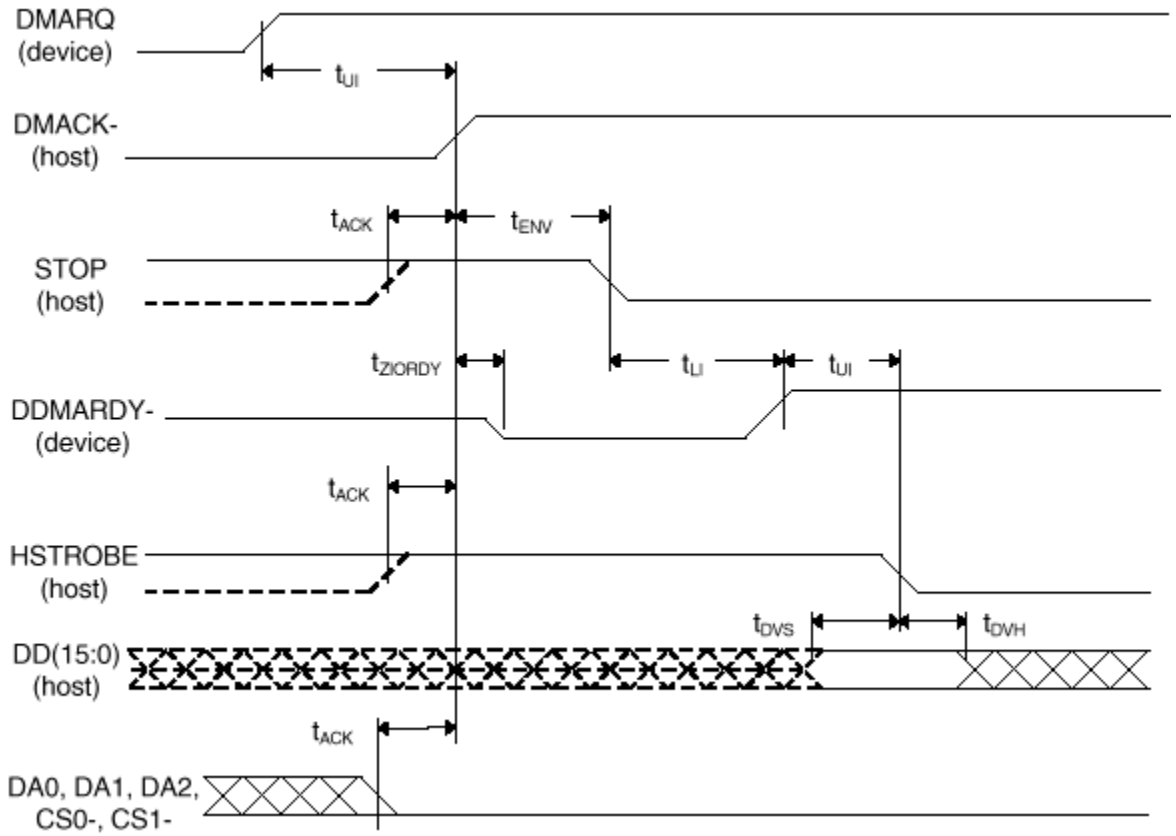


Figure C-6 Initiating an Ultra DMA data-out burst

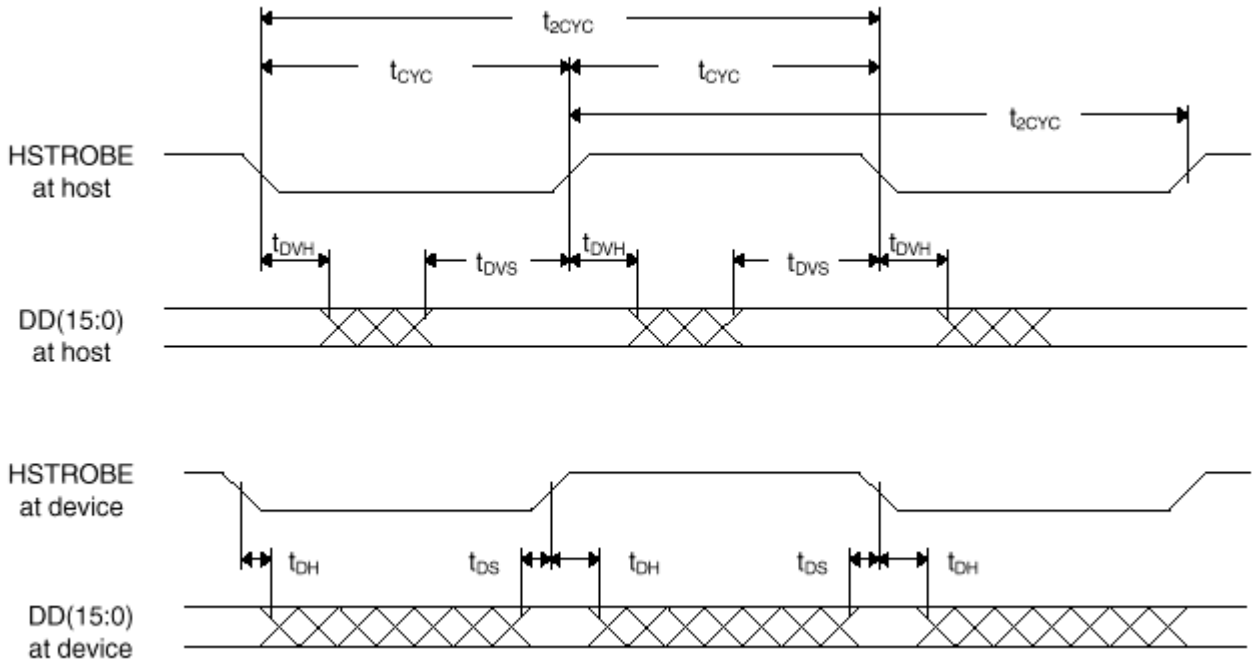


Figure C-7 Sustained Ultra DMA data-out burst

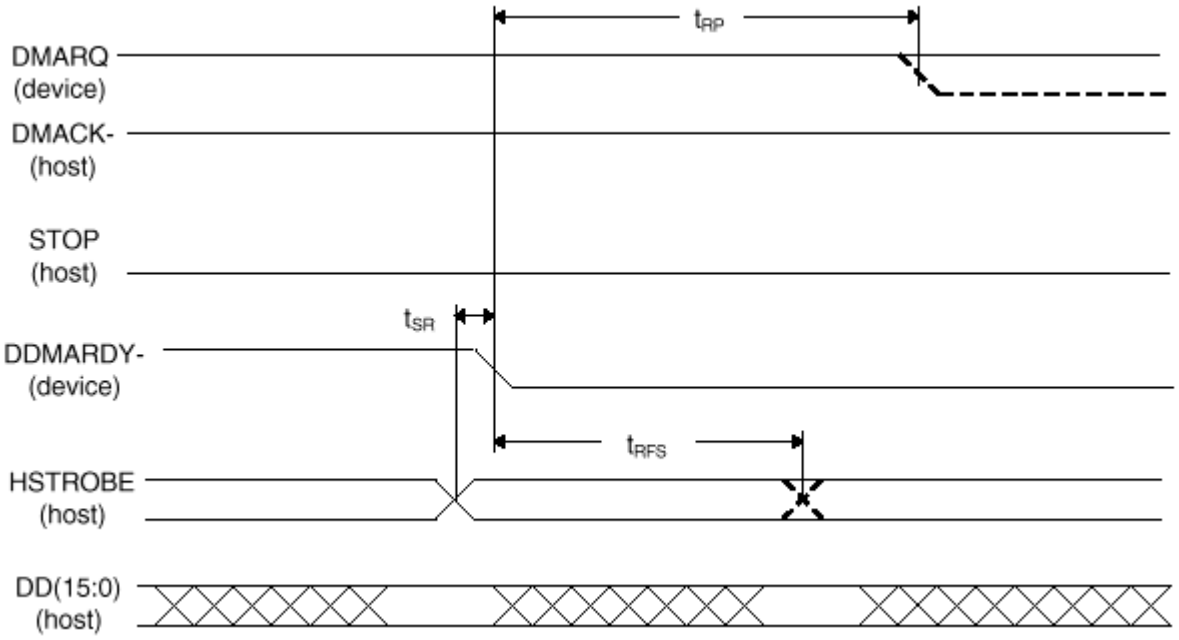


Figure C-8 Device pausing an Ultra DMA data-out burst

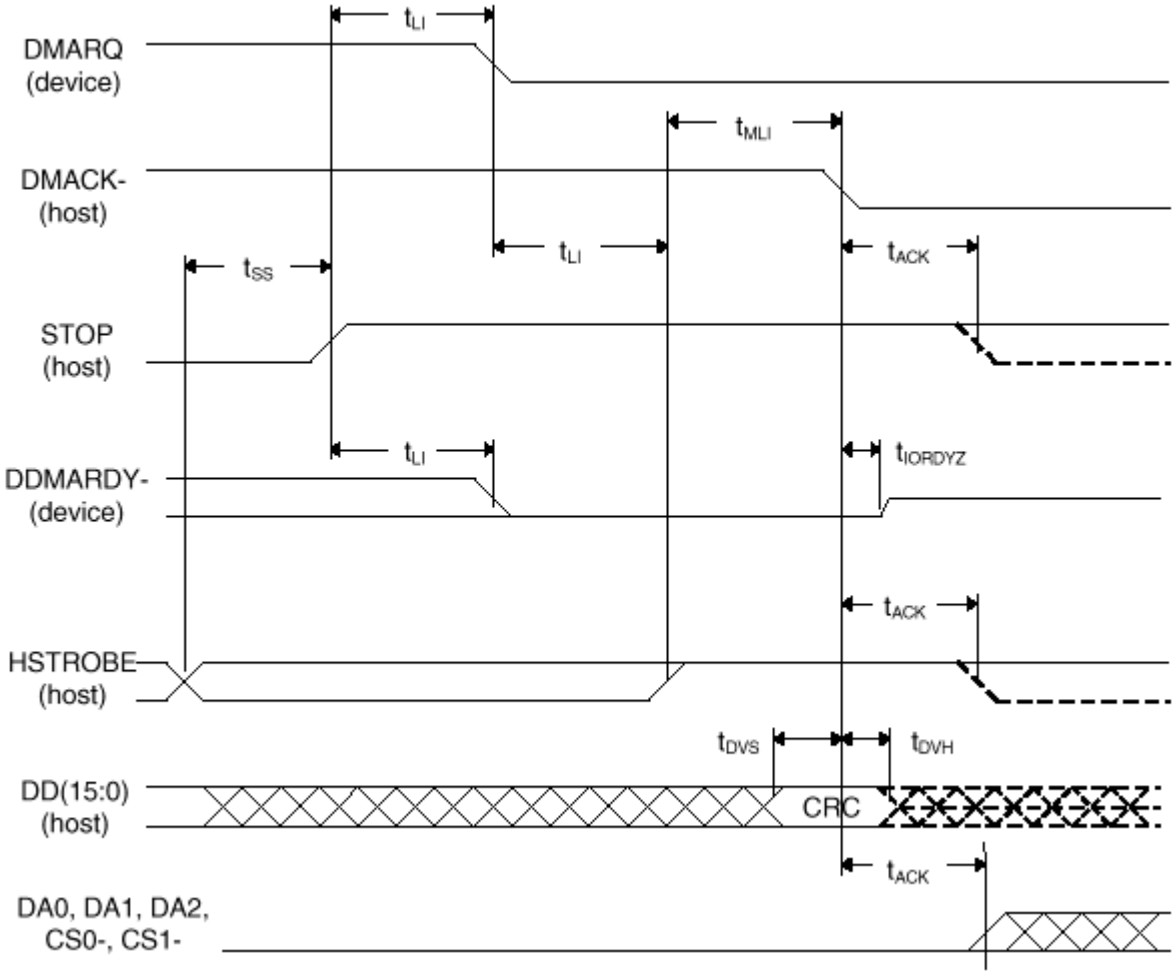


Figure C-9 Host terminating an Ultra DMA data-out burst

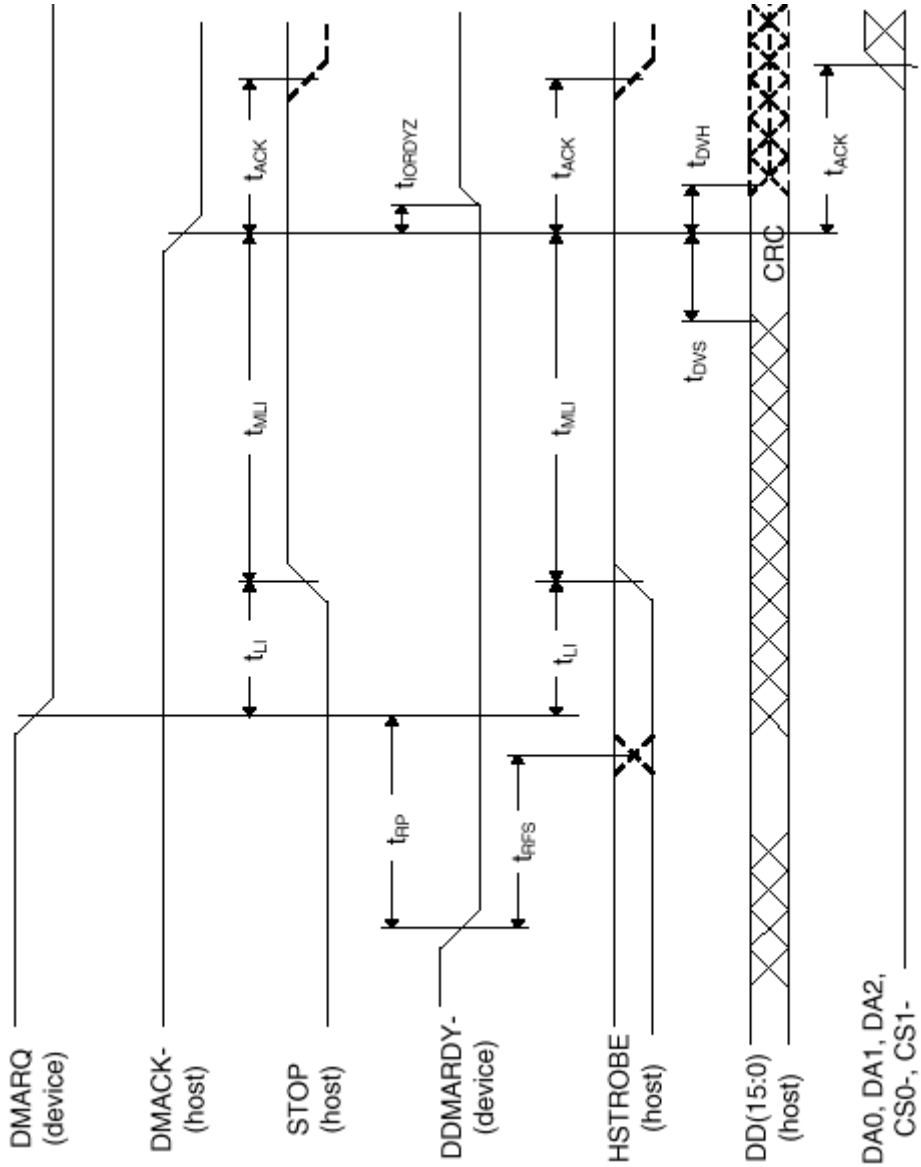


Figure C-10 Device terminating an Ultra data-out burst

Table C-1 Ultra DMA data transfer timing

NAME	MODE 0 (in ns)		MODE 1 (in ns)		MODE 2 (in ns)		MODE 3 (in ns)		MODE 4 (in ns)		COMMENT
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		Typical sustained average two cycle time
t_{CYC}	114		75		55		39		25		Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t_{2CYC}	235		156		117		86		57		Two cycle time allowing from clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	15		10		7		7		5		Data setup time at recipient
t_{DH}	5		5		5		5		5		Data hold time at recipient
t_{DVS}	70		48		34		20		6		Data valid setup time at sender (to STROBE edge)
t_{DVH}	6		6		6		6		6		Data valid hold time at sender (from STROBE edge)
t_{FS}	0	230	0	200	0	170	0	130	0	120	First STROBE time for drive to first negate DSTROBE from STOP during a data in burst
t_{LI}	0	150	0	150	0	150	0	100	0	100	Limited Interlock time (see note 1)
t_{MLI}	20		20		20		20		20		Interlock time with minimum (see note 1)
t_{UI}	0		0		0		0		0		Unlimited interlock time (see note 1)
t_{AZ}		10		10		10		10		10	Maximum time allowed for output drivers to release (from being asserted or negated)

NAME	MODE 0 (in ns)		MODE 1 (in ns)		MODE 2 (in ns)		MODE 3 (in ns)		MODE 4 (in ns)		COMMENT
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZAH}	20		20		20		20		20		Minimum delay time required for output drivers to assert or negate (from released state)
t_{ZAD}	0		0		0		0		0		
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Envelope time (from ATA_DMACK_B to STOP and HDMARDY- during data out burst initiation)
t_{SR}		50		30		20		NA		NA	STROBE to DMARDY time (if DMARDY is negated before this long after STROBE edge, the recipient shall receive no more than one additional data word)
t_{RFS}		75		70		60		60		60	Ready-to-Final STROBE time (no STROBE edges shall be sent this long after negation of DMARDY)
t_{RP}	160		125		100		100		100		Ready-to-Pause time (time that recipient shall wait to initiate pause after negating DMARDY)
t_{ATA_IORDYZ}		20		20		20		20		20	Pull-up time before allowing ATA_IORDY to be released
t_{ZATA_IORDY}	0		0		0		0		0		Minimum time drive shall wait before driving ATA_IORDY
t_{ACK}	20		20		20		20		20		Setup and hold times for ATA_DMACK_B (before assertion or negation)
t_{SS}	50		50		50		50		50		Time from STROBE edge to negation of ATA_DMARQ or assertion of STOP (when sender terminates a burst)

NAME	MODE 0 (in ns)		MODE 1 (in ns)		MODE 2 (in ns)		MODE 3 (in ns)		MODE 4 (in ns)		COMMENT
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	

Notes:

1 $t_{UI,}$ $t_{MLI,}$ t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, that is one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

2 All timing parameters are measured at the connector of the drive to which the parameter applies. For example, the sender shall stop generating STROBE edges t_{RFS} after the negation of DMARDY. Both STROBE and DMARDY timing measurement are taken at the connector of the sender. Even though the sender stops generating STROBE edges, additional STROBE edges may be received by the receiver due to propagation delay.

3 All timing measurement switching points (low to high and high to low) are to be taken at 1.5V.

Note: All timing should be measured at the connector of host or device whichever applies.

Index

Block Guide End Sheet

FINAL PAGE OF
76
PAGES