VREG_U
Block Guide
V01.04

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TSPG 8/16 Bit MCU
Freescale Semiconductor, Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
v0.1	10 DEC 2001		Terence Li	Initial Draft
v0.2	27 DEC 2001		Terence Li	Revised Version
v1.0	15 APR 2002		Terence Li	Changed all power channels to independent Revised max. current specification at all the channels
v1.1	30 OCT 2002		Terence Li	Added two more 3.3V independent power channels Added burn-in mode with register control Added register control to select external or internal regulator Revised max. current specification at all the channels
v1.2	21 NOV 2002		Terence Li	Added 5% or 10% voltage increase register option for burn-in mode
v1.3	5 MAR 2004		Terence Li	Updated voltage spreading and TC electrical specification
v1.4	23 NOV 2004		Wai-On Law	Removed electrical specification. Added description of register bits. Changed company logo.

Table of Contents

List of Figures

List of Tables

Preface

The content of this Block Guide is intended for re-use as reference material in customer documentation. The Block Guide must contain sufficient detail for an end customer to understand and use the block within a final System-on-a-Chip design.

Terminology

PHY: Universal Serial Bus 2.0 Physical Layer

LDO: Low drop-out. A type of linear voltage regulator in which the heading voltage can be very small but extra attention have to pay in external loading compensation.

OTA: Operational Transconductance Amplifier

PSRR: Power Supply Rejection Ratio

TC: Temperature Coefficient

VBE: Base-Emitter Voltage of Bipolar Junction Transistor

BJT: Bipolar Junction Transistor

Conditional Text

No conditional text.

Section 1 Introduction

The VREG_U is a linear voltage regulator module to provide 2.5V(+/-8%) and 3.3V(+/-8%) power from a (4.2V to 5.5V) power supply. It consists of two 2.5V power channels and four 3.3V power channels. All the six power channels are independent with each other.

Figure 1-1 is a block diagram of the VREG_U. It shows the functional organization of the block. It consists of six unit-gain buffers, a bandgap control reference generator, a power control logic and a power on reset pulse generator.

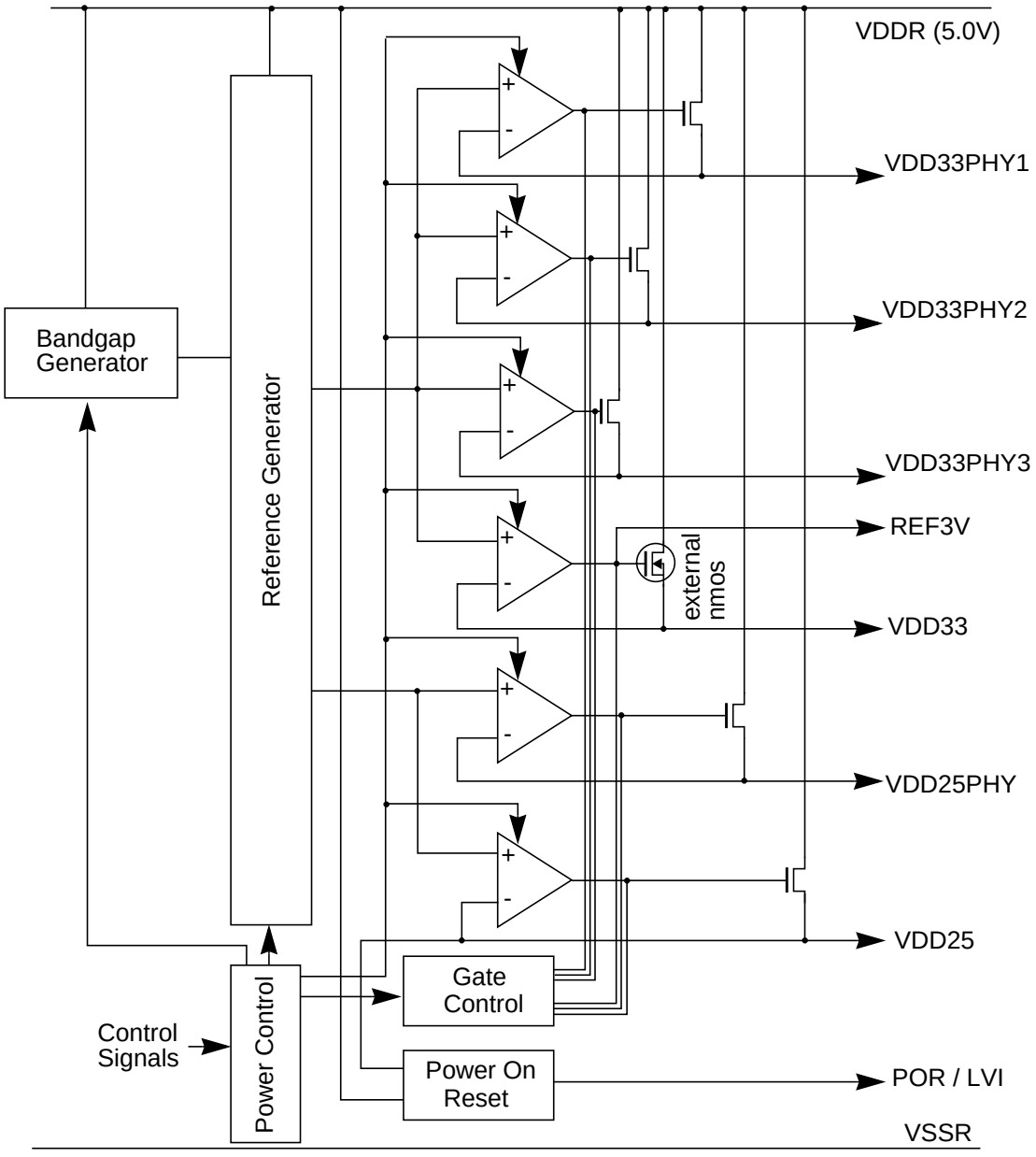

Figure 1-1 VREG_U Block Diagram

1.1 Overview

The VREG_U block is a non low-drop-out linear voltage regulator module to generate the supply voltage 2.5V(+/-8%) for the core logic, PHY(USB 2.0 Physical Layout) and memory blocks as well as 3.3V(+/-8%) for the I/O buffers and PHY out of the chip supply voltage (4.2V to 5.5V). **Figure 1-1** shows the block diagram of voltage regulator.

1.2 Features

- Non-LDO linear voltage regulator with six power channels and each channel has independent feedback
- One 3.3V external power channel works with external NMOS to provide high power drive ability
- Power channels can be disabled independently
- High PSRR (> 18dB up to 1GHz) with the use of low power bandgap reference
- Power on reset signal generation
- Register controlled voltage boost up for burn-in purpose
- Three different modes of operation

1.3 Modes of Operation

- RUN

  In run mode, regulating loop of the voltage regulator is active. This mode is selected whenever the device is neither in stop nor in pseudo stop mode and regulator is enabled.

- STANDBY

  Standby mode is selected when the device is in stop or pseudo stop mode and regulator is enabled. In standby mode the gates of the power transistors are directly connected to the reference voltage. In this case the voltage regulator acts as a voltage clamp. While in standby mode, the effective inner resistance of the regulator is increased, the quiescent current consumption of the regulator itself is heavily decreased.

- SHUTDOWN

  Shutdown mode is selected by tieing VREGEN (signal to disable all the regulator circuitries) to ground. In this case, the whole chip power must be supplied externally by applying 2.5V(+/-10%) and 3.3V(+/-10%) to operate. The power on reset pulse generation circuit is not affected by selecting shutdown mode.

Section 2 External Signal Description

2.1 Overview

VREG_U has six pad interfaces that connected off chip. Below is a table of signal properties (See **Table 2-1**).

Table 2-1 Signal Properties

Name	Port	Function	Reset State	Pull up / down
REF3V	REF3V	gate reference voltage for an external NMOS / data output for an external voltage regulator	0V	—
VDD25	VDD	2.5V regulated power rail for core	2.5V	—
VDD33	VDD3X	3.3V power rail for I/O buffers/external media	—	—
VDD33PHY3	VDDA	3.3V supply for USB D+ pull up resistor	3.3V	—
VDDR	VDDR	voltage regulator 5.0V power rail	5.0V	—
VSSR	VSSA1	voltage regulator / PHY transceiver ground rail	0V	—

2.2 Detailed Signal Descriptions

2.2.1 REF3V — Reference Gate Voltage

REF3V is either the gate reference voltage for an external NMOS of the internal 3.3V voltage regulator (**Figure 2-1**)or a 5V digital data output to control an external voltage regulator (**Figure 2-2**).

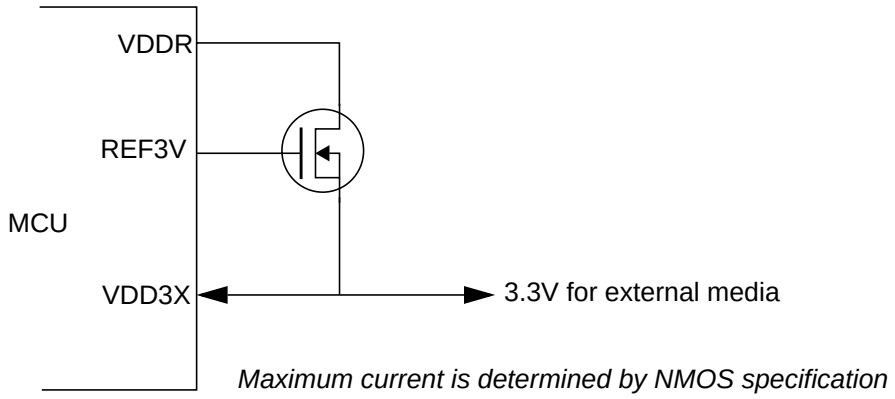

Figure 2-1 Internal Voltage Regulator with External NMOS Connections

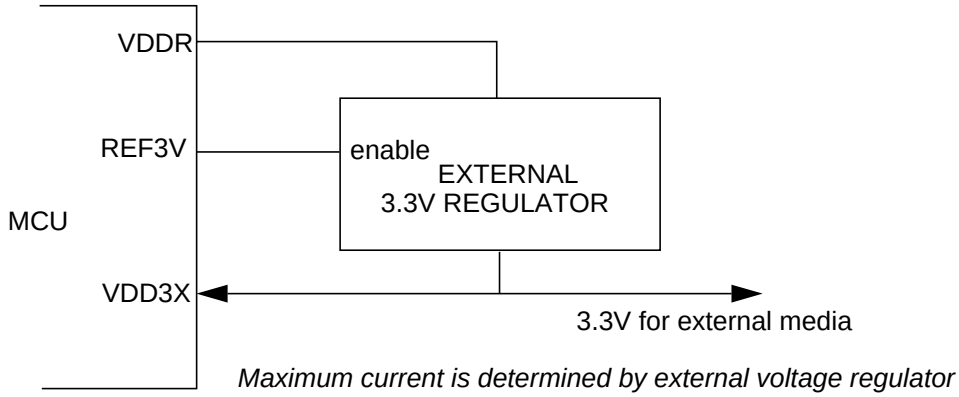

Figure 2-2 External Voltage Regulator Connections

2.2.2 VDD25 — 2.5V Power Rail

VDD25 is the power rail for the 2.5V core logic, memory blocks and UTMI logic of PHY. It is powered by a 2.5V internal voltage regulator.

2.2.3 VDD33 — 3.3V Power Rail

VDD33 is the power rail for the 3.3V I/O drivers. It is tied internally to the feedback path of REF3V of the 3.3V internal voltage regulator and can be powered by an external supply or an internal voltage regulator with an external NMOS.

2.2.4 VDD33PHY3 — 3.3V Power Rail for PHY

VDD33PHY3 is one of the power rail for the 3.3V PHY. It is powered by a 3.3V internal voltage regulator and is connected off chip at port VDDA for USB D+ pull up resistor.

2.2.5 VDDR — Voltage Regulator Power Rail

VDDR is the 5.0V power rail for the voltage regulator. The output current of the four regulating loops are drawn out from this pin.

2.2.6 VSSR — Voltage Regulator Ground Rail

VDDR is the ground rail for the voltage regulator and the ground reference of the bandgap reference.

Section 3 Memory Map/Register Definition

The VREG_U contains the register and associated bits for controlling the output of port REF3V as well as the status and voltage level of all power channels.

Table 3-1 shows the register associated with the VREG_U module.

Table 3-1 Module Memory Map

Address Offset	Use	Access
$00	VREG_U Module Control Register (VREGCTRL)	Read / Write

3.1 Register Descriptions

3.1.1 VREG_U Module Control Register (VREGCTRL)

Register address: Base Address + $00

	7	6	5	4	3	2	1	0
R	0	0	0	0	LEVEL	BURNEN[1]	EXTEN	DATA
W								
RESET:					0	0	0	0

= Unimplemented or Reserved

NOTES:
1. Register bit BURNEN is intended for factory test purposes only.

Figure 3-1 VREG_U Module Control Register (VREGCTRL)

The VREGCTRL register provides the selection of the use of internal 3.3V discrete NMOS voltage regulator or external 3.3V voltage regulator. In addition, it provides the selection of burn-in mode for factory testing purposes.

LEVEL — Voltage Level in Burn-in Mode (for test only)

This bit controls the increment voltage level of all power channels for burn-in factory test. This is valid only when the BURNEN bit is 1.

1 = 10% voltage increase for all power channels
0 = 5% voltage increase for all power channels

BURNEN — Burn-in Mode Enable (for test only)

This bit enables the voltage increase of all power channels for burn-in factory test. The increase level is determined by the LEVEL bit.

1 = Burn-in mode & voltage increase according to the LEVEL bit
0 = Normal mode

EXTEN — External NMOS Power Channel Enable

This bit controls the output mode of the REF3V pin, which can be an analog reference voltage output or a digital control output.
1 = Enable power channel for external NMOS & set REF3V as reference voltage
0 = Disable power channel for external NMOS & set REF3V as digital data output of the DATA bit

DATA — REF3V output data

When the REF3V pin is configured as digital output (i.e. when EXTEN=0), the value of this DATA bit is output to the REF3V pin.

Section 4 Functional Description

VREG_U is a quad channel non-LDO linear voltage regulator. It converts the VDDR from (4.2V - 5.5V) to (2.5V +/- 8%) for VDD25 and VDD25PHY as well as to (3.3V +/- 8%) for VDD33, VDD33PHY1, VDD33PHY2 and VDD33PHY3. All the power channels are independent and each channel consists of an OTA and a NMOS power transistor as shown in **Section 1 Introduction**. The OTA compares the output voltage with the reference voltage and commands the gate of the corresponding power transistor. The reference for regulation is derived by a bandgap reference. In standby operation, the OTAs are disabled and all the power transistors are connected directly to the reference voltage to minimize standby current.

Inside the VREG_U block, there is a power on reset pulse generator for the core logic by monitoring the core voltage and the VDDR voltage level.

The mode of operation is controlled by the state of the core and the control signals. In shutdown mode, VREG_U is completely disabled and all the power channels are in high impedance while in run mode, VREG_U always operates whenever the core is neither in stop mode nor in stop recovery mode. Otherwise, it will be in standby mode. The only exception is VDD33 channel in which can be disabled independently through register for external 3.3V powering.

During power up or reset, REF3V pin is pulled low so that large current drawn due to other media can be avoided and all the regulator loops are activated except VDD33 channel.

4.1 Reference Generator

The reference generator is comprised of a resistor ladder, an OTA and a bandgap reference.

4.1.1 Reference Generator

The reference generation is a resistor ladder in the OTA feedback path of bandgap reference multiplier. Different reference voltages are picked up from the corresponding points to the OTAs as regulation reference.

4.1.2 Bandgap Generator

The bandgap generator is a typical bandgap reference generator based on the addition of negative TC of VBE of BJT and positive TC voltage of delta VBE at different current densities. In regard to voltage regulation with +/- 8% accuracy, bandgap reference is a high-performance voltage reference.

4.2 Unit-gain Buffer

The unit-gain buffer is comprised of an OTA and a power transistor to form a unit-voltage gain and high current buffer.

4.2.1 OTA

The operational transconductance amplifier compares the reference voltage with the channel voltage to generate the gate voltage for the power transistor.

4.2.2 Power Transistor

The power transistors are NMOS with different current strengths so as to meet the corresponding current consumption of the power channels.

4.3 Power Control

The power control is used to define the logic for mode of operation, i.e. run mode, standby mode and shutdown mode.

4.3.1 Power Control

A combination logic to distribute the state of operation for reference generator and OTAs.

4.3.2 Gate Control

A circuitry to control the connection of power transistor gate among OTA’s output, VSSR and reference points of resistor ladder.

4.4 Power On Reset

The power on reset is a power on reset pulse generator for the core logic as well as a low voltage inhibit generator for the core logic by monitoring difference between the core voltage and the VDDR voltage.

Section 5 Initialization/Application Information

There is no initialization needed for this module. If VDD33 power channel is not needed, it should be disabled to save power by means of setting the corresponding register. The maximum output current of VDD33 power channel depends on the saturation current of the external nmos.

Index

Block Guide End Sheet

FINAL PAGE OF
22
PAGES