XSRAM20K
Block Guide
V01.00

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Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
01.00	13-Feb-03	13-Feb-03		Initial Release

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Preface

Terminology

Acronyms and Abbreviations	
SRAM	Static random access memory
SoC	System on Chip
CPU	Central processing unit, in this case the S12X_CPU
XGATE	16 bit RISC engine serving as versatile DMA controller

Section 1 Introduction

The XSRAM20K module forms a dual ported 20K bytes static random access memory as shown in **Figure 1-1**.

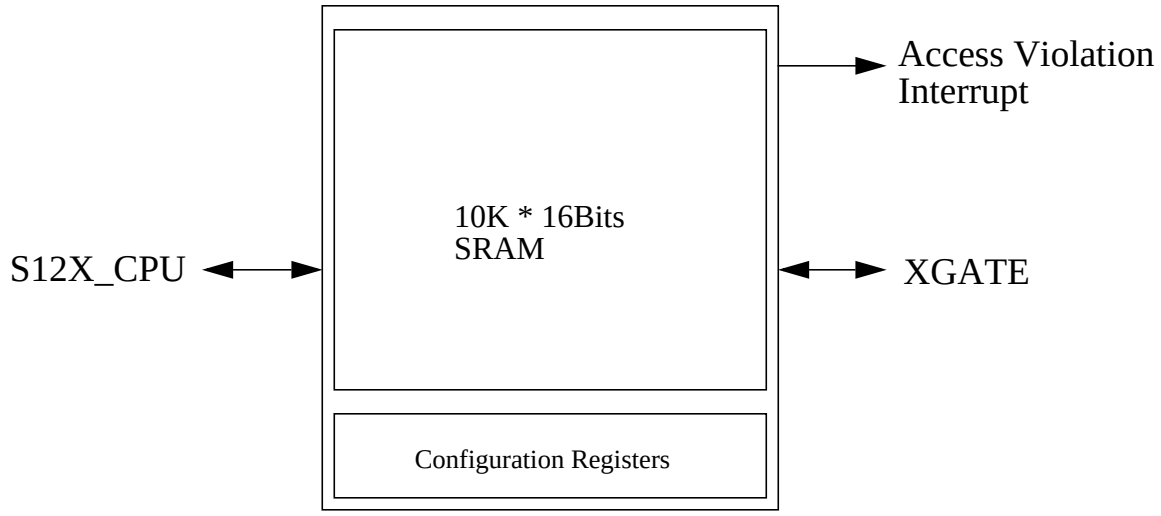

Figure 1-1 XSRAM20K Block Diagram

1.1 Overview

XSRAM20K is a dual ported 20K bytes static random access memory block. The memory can be configured into three regions:

- XGATE code region
- shared region
- CPU only region

1.2 Features

The XSRAM20K includes these features:

- 20 KBytes of static random access memory organised as 10K byte words of 16 bits each (byte accessible)

- Two accessports: 40Mwords/s CPU access port, 80Mwords/s XGATE access port
- supports single cycle misaligned word access on CPU port, on the XGATE port misaligned wordaccess is unsupported
- memory area is configurable into three regions with writeprotect feature
- interrupt capability on suppressed write operations

1.3 Modes of Operation

Refer to the SoC guide for a detailed explanation of the chip modes.

- Run Mode

  This is the basic mode of operation.
- Wait Mode

  XSRAM20K is behaving the same in Wait as in Run Mode.
- Stop Mode

  In full stop mode or pseudo stop mode the XSRAM20K module is stalled.

Section 2 External Signal Description

The XSRAM20K module has no external pins.

Section 3 Memory Map/Register Definition

This section provides a detailed description of address space and registers used by the XSRAM20K.

The memory map for the XSRAM20K is given below in **Table 3-1**. The address listed for each register is the sum of a base address and an address offset. The base address is defined at the SoC level and the address offset is defined at the module level.

Table 3-1 Register Memory Map

Address	Use	Access
$__00	XSRAM control register (XSCTRL)	Read / Write [1]
$__01	XSRAM XGATE code region upper boundary (XSXCUB)	Read / Write [2]
$__02	XSRAM shared region lower boundary (XSSRLB)	Read / Write [2]
$__03	XSRAM shared region upper boundary (XSSRUB)	Read / Write [2]

NOTES:
1. Certain bits are non-writable
2. Can only be written if XSRE=0

3.1 Register Descriptions

3.1.1 XSRAM Control Register

Register Address: $__00

	Bit 7	6	5	4	3	2	1	Bit 0
R	XSRE	0	0	0	0	XSAVIE	XSXAVIF	XSCAVIF
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-1 XSRAM Control Register (XSCTRL)

Read:anytime

Write:anytime; writes to the reserved bits have no effect

XSRE — XSRAM Region Check Enable Bit

This bit enables the XSRAM region checking and protection mechanism. If XSRE is cleared, there is no region checking performed, any memory location is writeable by both the CPU and the XGATE module. When XSRE is set, region checking is enabled, write access of the CPU to the XGATE code region as well as write access of the XGATE module to the outside the XGATE code region or the shared region is suppressed.

1 = XSRAM region check is enabled, region boundary registers cannot be written
0 = XSRAM region check is disabled, region boundary registers can be written

XSAVIE — XSRAM Access Violation Interrupt Enable

This bit enables the Access Violation Interrupt. If XSAVIE is set and either XSXAVF or XSCAVF is set, an interrupt is generated.

1 = Access Violation Interrupt Enabled
0 = Access Violation Interrupt Disabled

XSXAVIF — XSRAM XGATE Access Violation Interrupt Flag

When set, this bit indicates that the XGATE module has tried to write to memory location outside of the XGATE code region and outside of the shared region. This flag can be reset by writing ’1’ to the XSXAVIF bitlocation.

1 = XSRAM access violation generated by XGATE module detected
0 = XSRAM has not detected access violation generated by XGATE module

XSCAVIF — XSRAM CPU Access Violation Interrupt Flag

When set, this bit indicates that the CPU has tried to write to memory location inside the XGATE code region. This flag can be reset by writing ’1’ to the XSCAVIF bitlocation.

1 = XSRAM access violation generated by the CPU detected
0 = XSRAM has not detected access violation generated by the CPU

3.1.2 XSRAM XGATE Code Region Upper Boundary Register

Register Address: $__01

	Bit 7	6	5	4	3	2	1	Bit 0
R	1	XSXCU6	XSXCU5	XSXCU4	XSXCU3	XSXCU2	XSXCU1	XSXCU0
W								
Reset:	1	1	1	1	1	1	1	1

= Unimplemented or Reserved

Figure 3-2 XSRAM XGATE Code Region Upper Boundary Register (XSXCUB)

Read:anytime

Write:can be written anytime when XSRE=0; writes to the reserved bit have no effect

XSXCU[6:0] — XSRAM XGATE Code Region Upper Boundary Bits 6-0

These bits define the upper boundary of the code region allocated to the XGATE module in pages of 256 bytes. The selected page is included in the code region.

3.1.3 XSRAM Shared Region Lower Boundary Register

Register Address: $__02

	Bit 7	6	5	4	3	2	1	Bit 0
R	1	XSSL6	XSSL5	XSSL4	XSSL3	XSSL2	XSSL1	XSSL0
W								
Reset:	1	0	1	1	0	0	0	0

= Unimplemented or Reserved

Figure 3-3 XSRAM Shared Region Lower Boundary Register (XSSRLB)

Read:anytime

Write:can be written anytime when XSRE=0; writes to the reserved bit have no effect

XSSL[6:0] — XSRAM Shared Region Lower Boundary Bits 6-0

These bits define the lower boundary of the shared memory region in pages of 256 bytes. The selected page is included in the shared region.

3.1.4 XSRAM Shared Region Upper Boundary Register

Register Address: $__03

	Bit 7	6	5	4	3	2	1	Bit 0
R	1	XSSU6	XSSU5	XSSU4	XSSU3	XSSU2	XSSU1	XSSU0
W								
Reset:	1	1	1	1	1	1	1	1

= Unimplemented or Reserved

Figure 3-4 XSRAM Shared Region Upper Boundary Register (XSSRUB)

Read:anytime

Write:can be written anytime when XSRE=0; writes to the reserved bits have no effect

XSSU[6:0] — XSRAM Shared Region Upper Boundary Bits 6-0

These bits define the upper boundary of the shared memory region in pages of 256 bytes. The selected page is included in the shared region.

Section 4 Functional Description

4.1 General

The XSRAM20K module serves as random access memory for the CPU as well as code and data memory for the XGATE module. Via the configuration registers, the XSRAM20K can be configured into three regions:

- XGATE code region
- shared region
- region outside XGATE code region and shared region

If region checking is enabled, CPU write accesses into the XGATE code region is blocked. If the CPU tries to write the XGATE code region, the XSCAVIF is set, an interrupt is generated if enabled. Furthermore if the XGATE tries to write outside of the XGATE code region or shared region and the region checking is enabled, those write accesses are suppressed as well, XSXAVIF is set. The regions are defined by the values set in the boundary registers. The bottom address of the XGATE code region always starts at the lowest implemented memory address. The values of the boundary registers define the boundary address in 256 byte pages, the value set is included in the region. For example setting the shared region upper boundary register (XSSRUB) to $E0 and the shared region lower boundary register (XSSRLB) to $C1 defines the shared region to $F_C100 to $F_E0FF (global address).

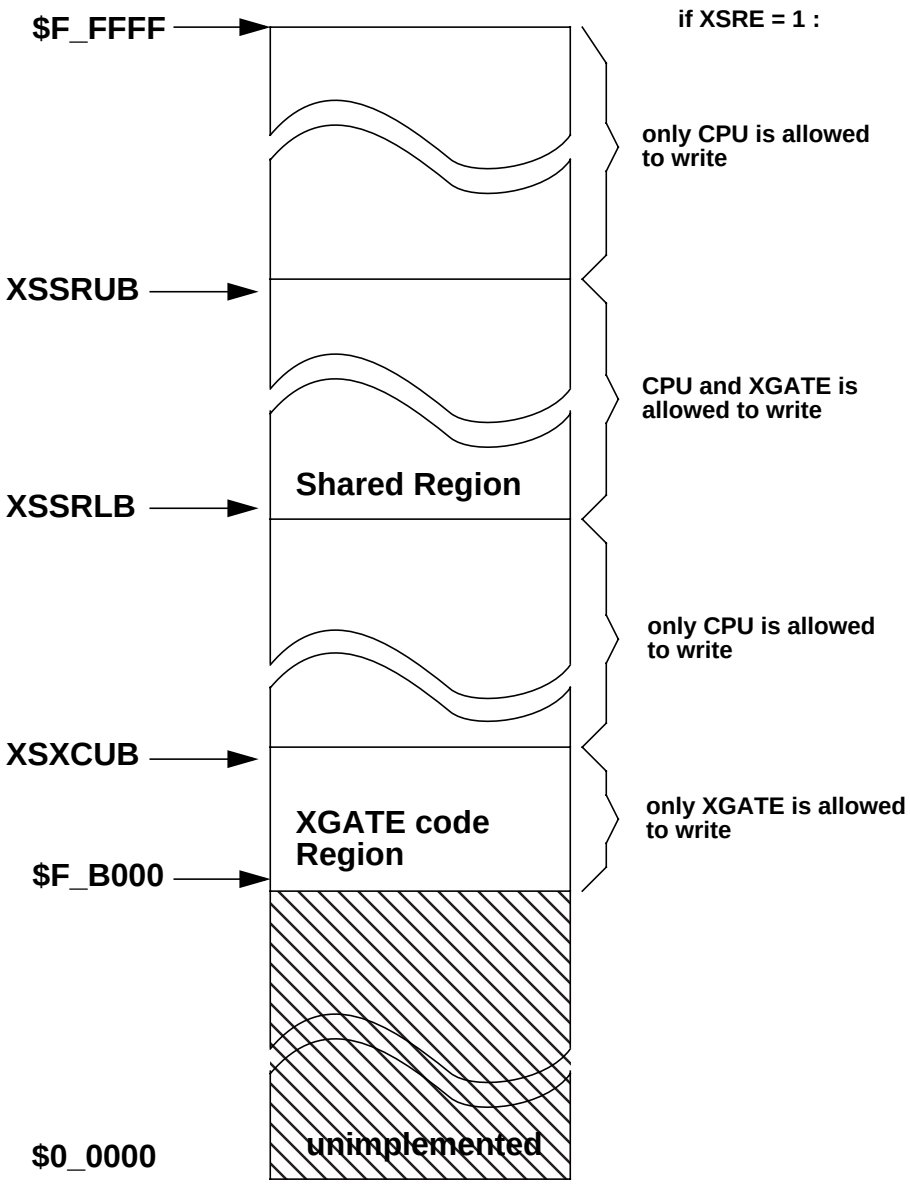

Figure 4-1 XSRAM20K region map

Section 5 Resets

5.1 General

At reset the XSRAM20K is not accessible. The reset state of each individual bit is listed within the Register Description section (see **Section 3 Memory Map/Register Definition**) which details the registers and their bit fields.

Section 6 Interrupts

6.1 General

The interrupt requested by the XSRAM20Kis listed in **Table 6-1**. Refer to the MCU Specification for related vector address and priority.

Table 6-1 XSRAM20K Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
CPU access violation, XGATE access violation	I Bit	XSAVIE in XSCTRL

See register description for further details.

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