

# VREG\_3V3

## Block User Guide

### V03.03

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**Semiconductor Products Sector**  
**Motorola, Inc**

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# Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V00.01	12 Apr 2001			Initial version
V00.02	7 June 2001			Added additional Register, slight changes to block diagram
V00.03	9 July 2001			Updated Figure A1; removing CTRL1, adding VSSR, LVDS/LVIF when not LVDE
V01.00	12 July 2001			Adding VREGEN to Table2-1; rewriting of Section 1.3 for better reading; Table A1 Num 3+4 Min value changed. Mode name changed.
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V01.02	04 Oct 2001			Reviewed LVI and LVD functionality
V1.03	19 Oct 2001			Updated Appendix A
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V 2.01	27 Jun 2002			New rev, minor updates, updated load capacitors
V 3.00	18 Apr 2003			Added API
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V 3.02	28 oct 2003			Corrected row 22 of <b>Table 3-2</b> ; Added comment to APIF; added note to Section <b>4.7</b> .
V 3.03	12 Jan 2004			Corrected: API RC-Oscillator is not available if VREG_3V3 in Shutdown Mode

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# Section 1 Introduction

## 1.1 Overview

Block VREG\_3V3 is a dual output voltage regulator providing two separate 2.5V (typ) supplies differing in the amount of current that can be sourced. The regulator input voltage range is from 3.3V up to 5V (typ).

## 1.2 Features

The block VREG\_3V3 includes these distinctive features:

- Two parallel, linear voltage regulators
  - Bandgap reference
- Low Voltage Detect (LVD) with Low Voltage Interrupt (LVI)
- Power On Reset (POR)
- Low Voltage Reset (LVR)
- Autonomous Periodical Interrupt (API)

## 1.3 Modes of Operation

There are three modes VREG\_3V3 can operate in:

- Full Performance Mode (FPM) (CPU is not in Stop Mode)

The regulator is active, providing the nominal supply voltage of 2.5V with full current sourcing capability at both outputs. Features LVD (Low Voltage Detect), LVR (Low Voltage Reset) and POR (Power-On Reset) are available. The API is available.
- Reduced Power Mode (RPM) (CPU is in Stop Mode)

The purpose is to reduce power consumption of the device. The output voltage may degrade to a lower value than in Full Performance Mode, additionally the current sourcing capability is substantially reduced. Only the POR is available in this mode, LVD and LVR are disabled. The API is available.
- Shutdown Mode

Controlled by VREGEN (see device level specification for connectivity of VREGEN).

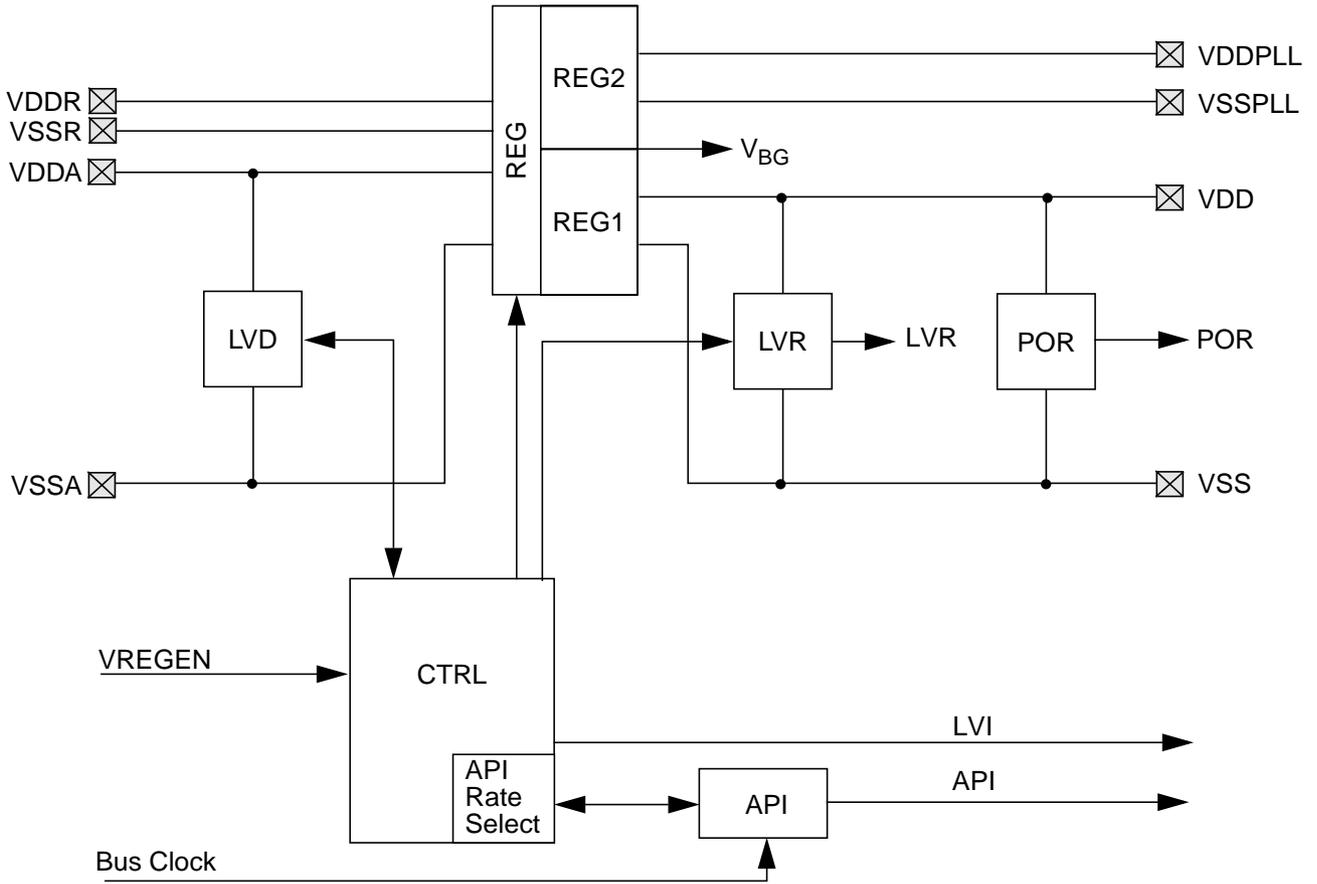
This mode is characterized by minimum power consumption. The regulator outputs are in a high impedance state, only the POR feature is available, LVD and LVR are disabled. The API internal RC-Oscillator clock is not available.

This mode must be used to disable the chip internal regulator VREG\_3V3, i.e. to bypass the VREG\_3V3 to use external supplies.

## 1.4 Block Diagram

**Figure 1-1** shows the function principle of VREG\_3V3 by means of a block diagram. The regulator core REG consists of two parallel subblocks, REG1 and REG2, providing two independent output voltages.

**Figure 1-1 VREG\_3V3 - Block Diagram**



LVD: Low Voltage Detect	REG: Regulator Core
LVR: Low Voltage Reset	CTRL: Regulator Control
POR: Power-on Reset	API: Auto. Periodical Interrupt
	⊠ PIN





## Section 2 Signal Description

### 2.1 Overview

Due to the nature of VREG\_3V3 being a voltage regulator providing the chip internal power supply voltages most signals are power supply signals connected to pads.

**Table 2-1** shows all signals of VREG\_3V3 associated with pins.

**Table 2-1 VREG\_3V3 - Signal Properties**

Name	Function	Reset State	Pull up
VDDR	VREG_3V3 power input (positive supply)	—	—
VSSR	VREG_3V3 power input (ground)	—	—
VDDA	VREG_3V3 quiet input (positive supply)	—	—
VSSA	VREG_3V3 quiet input (ground)	—	—
VDD	VREG_3V3 primary output (positive supply)	—	—
VSS	VREG_3V3 primary output (ground)	—	—
VDDPLL	VREG_3V3 secondary output (positive supply)	—	—
VSSPLL	VREG_3V3 secondary output (ground)	—	—
VREGEN (optional)	VREG_3V3 (Optional) Regulator Enable	—	—

### 2.2 Detailed Signal Descriptions

Check device level specification for connectivity of the signals.

#### 2.2.1 VDDR, VSSR - Regulator Power Input

Signal VDDR is the power input of VREG\_3V3. All currents sourced into the regulator loads flow through this pin. A chip external decoupling capacitor (100nF...220nF, X7R ceramic) between VDDR and VSSR can smoothen ripple on VDDR.

For entering Shutdown Mode pin VDDR should also be tied to ground on devices without VREGEN pin.

#### 2.2.2 VDDA, VSSA - Regulator Reference Supply

Signals VDDA/VSSA which are supposed to be relatively quiet are used to supply the analog parts of the regulator. Internal precision reference circuits are supplied from these signals. A chip external decoupling capacitor (100nF...220nF, X7R ceramic) between VDDA and VSSA can further improve the quality of this supply.

### 2.2.3 VDD, VSS - Regulator Output1 (Core Logic)

Signals VDD/VSS are the primary outputs of VREG\_3V3 that provide the power supply for the core logic. These signals are connected to device pins to allow external decoupling capacitors (100nF...220nF, X7R ceramic).

In Shutdown Mode an external supply driving VDD/VSS can replace the voltage regulator.

### 2.2.4 VDDPLL, VSSPLL - Regulator Output2 (PLL)

Signals VDDPLL/VSSPLL are the secondary outputs of VREG\_3V3 that provide the power supply for the PLL and Oscillator. These signals are connected to device pins to allow external decoupling capacitors (100nF...220nF, X7R ceramic).

In Shutdown Mode an external supply driving VDDPLL/VSSPLL can replace the voltage regulator.

### 2.2.5 VREGEN - Optional Regulator Enable

This optional signal is used to shutdown VREG\_3V3. In that case VDD/VSS and VDDPLL/VSSPLL must be provided externally. Shutdown Mode is entered with VREGEN being low. If VREGEN is high, the VREG\_3V3 is either in Full Performance Mode or in Reduced Power Mode.

For the connectivity of VREGEN see device specification.

**NOTE:** *Switching from FPM or RPM to shutdown of VREG\_3V3 and vice versa is not supported while MCU is powered.*

## Section 3 Memory Map and Registers

### 3.1 Overview

This section provides a detailed description of all registers accessible in VREG\_3V3.

### 3.2 Module Memory Map

Table 3-1 provides an overview of all used registers.

**Table 3-1 VREG\_3V3 - Memory Map**

Address Offset	Use	Access
\$_00	VREG_3V3 HT Control Register (VREGHTCL)	----
\$_01	VREG_3V3 Control Register (VREGCTRL)	R/W
\$_02	VREG_3V3 Autonomous Periodical Interrupt Control Register (VREGAPICL)	R/W
\$_03	VREG_3V3 Autonomous Periodical Interrupt Trimming Register (VREGAPITR)	R/W
\$_04	VREG_3V3 - Reserved 04	----
\$_05	VREG_3V3 - Reserved 05	----
\$_06	VREG_3V3 - Reserved 06	----
\$_07	VREG_3V3 - Reserved 07	----

### 3.3 Register Descriptions

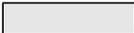
This section describes all the VREG\_3V3 registers and their individual bits.

#### 3.3.1 VREG\_3V3 - HT Control Register (VREGHTCL)

The VREGHTCL is reserved for test purposes.

Address Offset: \$\_00

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
RESET:	0	0	0	0	0	0	0	0

 = Unimplemented or Reserved

**Figure 3-1 VREG\_3V3 - HT Control Register (VREGHTCL)**

### 3.3.2 VREG\_3V3 - Control Register (VREGCTRL)

The VREGCTRL register allows the configuration of the VREG\_3V3 low voltage detect features.

Address Offset: \$\_01

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	LVDS	LVIE	LVIF
W								
RESET:	0	0	0	0	0	0	0	0

 = Unimplemented or Reserved

**Figure 3-2 VREG\_3V3 - Control Register (VREGCTRL)**

LVDS — Low Voltage Detect Status Bit

This read-only status bit reflects the input voltage. Writes have no effect.

1 = Input voltage  $V_{DDA}$  is below level  $V_{LVIA}$  and FPM.

0 = Input voltage  $V_{DDA}$  is above level  $V_{LVID}$  or RPM or Shutdown Mode.

LVIE — Low Voltage Interrupt Enable Bit

1 = Interrupt will be requested whenever LVIF is set.

0 = Interrupt request is disabled.

LVIF — Low Voltage Interrupt Flag

LVIF is set to 1 when LVDS status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (LVIE=1), LVIF causes an interrupt request.

1 = LVDS bit has changed.

0 = No change in LVDS bit.

**NOTE:** On entering the Reduced Power Mode the LVIF is not cleared by the VREG\_3V3.

### 3.3.3 VREG\_3V3 - Autonomous Periodical Interrupt Control Register (VREGAPICL)

The VREGAPICL register allows the configuration of the VREG\_3V3 autonomous periodical interrupt features.

Address Offset: \$\_02

	7	6	5	4	3	2	1	0
R	APICLK	APIR3	APIR2	APIR1	APIR0	APIFE	APIE	APIF
W								
RESET:	0	0	0	0	0	0	0	0

 = Unimplemented or Reserved

**Figure 3-3 VREG\_3V3 - Autonomous Periodical Interrupt Control Register (VREGAPICL)**

APICLK — Autonomous Periodical Interrupt Clock Select Bit

Selects the clock source for the API. Writable only if APIFE = 0.

1 = Bus clock used as source.

0 = Autonomous Periodical Interrupt clock used as source.

APIR[3:0] — Autonomous Periodical Interrupt Rate Bits

These bits define the timeout period of the API. See **Table 3-2** for details of the effect of the Autonomous Periodical Interrupt Rate Bits. Writable only if APIFE = 0.

**Table 3-2 VREG\_3V3 - Selectable Autonomous Periodical Interrupt Periods**

APICLK	APIR3	APIR2	APIR1	APIR0	Selected Period
0	0	0	0	0	0.5 ms <sup>1</sup>
0	0	0	0	1	1 ms <sup>1</sup>
0	0	0	1	0	2 ms <sup>1</sup>
0	0	0	1	1	2.5 ms <sup>1</sup>
0	0	1	0	0	5 ms <sup>1</sup>
0	0	1	0	1	7.5 ms <sup>1</sup>
0	0	1	1	0	10 ms <sup>1</sup>
0	0	1	1	1	20 ms <sup>1</sup>
0	1	0	0	0	25 ms <sup>1</sup>
0	1	0	0	1	50 ms <sup>1</sup>
0	1	0	1	0	75 ms <sup>1</sup>
0	1	0	1	1	100 ms <sup>1</sup>
0	1	1	0	0	200 ms <sup>1</sup>
0	1	1	0	1	250 ms <sup>1</sup>
0	1	1	1	0	500 ms <sup>1</sup>
0	1	1	1	1	750 ms <sup>1</sup>
1	0	0	0	0	5 * bus clock period
1	0	0	0	1	10 * bus clock period

**Table 3-2 VREG\_3V3 - Selectable Autonomous Periodical Interrupt Periods**

APICLK	APIR3	APIR2	APIR1	APIR0	Selected Period
1	0	0	1	0	20 * bus clock period
1	0	0	1	1	25 * bus clock period
1	0	1	0	0	50 * bus clock period
1	0	1	0	1	75 * bus clock period
1	0	1	1	0	100 * bus clock period
1	0	1	1	1	200 * bus clock period
1	1	0	0	0	250 * bus clock period
1	1	0	0	1	500 * bus clock period
1	1	0	1	0	750 * bus clock period
1	1	0	1	1	1000 * bus clock period
1	1	1	0	0	2000 * bus clock period
1	1	1	0	1	2500 * bus clock period
1	1	1	1	0	5000 * bus clock period
1	1	1	1	1	7500 * bus clock period

**NOTES:**

1. When trimmed within specified accuracy. See electrical specification for details.

**APIFE — Autonomous Periodical Interrupt Feature Enable Bit**

Enables the API Feature and starts the API Timer when set.

1 = Autonomous Periodical Interrupt is enabled and timer starts running.

0 = Autonomous Periodical Interrupt is disabled.

**APIE — Autonomous Periodical Interrupt Enable Bit**

1 = API Interrupt will be requested whenever APIF is set.

0 = API Interrupt request is disabled.

**APIF — Autonomous Periodical Interrupt Flag**

APIF is set to 1 when the in the API configured time has elapsed. This flag can only be cleared by writing a 1 to it. Clearing of the flag has precedence over setting.

Writing a 0 has no effect. If enabled (APIE=1), APIF causes an interrupt request.

1 = API timeout has occurred.

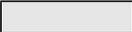
0 = API timeout has not yet occurred.

### 3.3.4 VREG\_3V3 - Autonomous Periodical Interrupt Trimming Register (VREGAPITR)

The VREGAPITR register allows to trim the API timeout period.

**Address Offset: \$\_03**

	7	6	5	4	3	2	6	0
R	APITR5	APITR4	APITR3	APITR2	APITR1	APITR0	0	0
W								
RESET:	0 <sup>1</sup>	0	0					

 = Unimplemented or Reserved

**NOTES:**

1. Reset value is either 0 or preset by factory. See Device User Guide for details.

**Figure 3-4 VREG\_3V3 - Autonomous Periodical Interrupt Trimming Register (VREGAPITR)**

APITR[5:0] — Autonomous Periodical Interrupt Period Trimming Bits

See **Table 3-3** for trimming effects.

**Table 3-3 VREG\_3V3 - Trimming Effect of APIT**

Bit	Trimming Effect
APITR[5]	increases period by ~25.0%
APITR[4]	decreases period by ~12.5%
APITR[3]	decreases period by ~ 6.2%
APITR[2]	decreases period by ~ 3.1%
APITR[1]	decreases period by ~ 1.6%
APITR[0]	decreases period by ~ 0.8%

### 3.3.5 VREG\_3V3 - Reserved\_04

The Reserved\_04 is reserved for test purposes.

**Address Offset: \$\_04**

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
RESET:	0	0	0	0	0	0	0	0

 = Unimplemented or Reserved

**Figure 3-5 VREG\_3V3 - Reserved\_04**

### 3.3.6 VREG\_3V3 - Reserved\_05

The Reserved\_05 is reserved for test purposes.

Address Offset: \$\_05

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
RESET:	0	0	0	0	0	0	0	0

 = Unimplemented or Reserved

Figure 3-6 VREG\_3V3 - Reserved\_05

### 3.3.7 VREG\_3V3 - Reserved\_06

The Reserved\_06 is reserved for test purposes.

Address Offset: \$\_06

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
RESET:	0	0	0	0	0	0	0	0

 = Unimplemented or Reserved

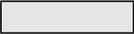
Figure 3-7 VREG\_3V3 - Reserved\_06

### 3.3.8 VREG\_3V3 - Reserved\_07

The Reserved\_07 is reserved for test purposes.

**Address Offset: \$\_07**

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
RESET:	0	0	0	0	0	0	0	0

 = Unimplemented or Reserved

**Figure 3-8 VREG\_3V3 - Reserved\_07**



## Section 4 Functional Description

### 4.1 General

Block VREG\_3V3 is a voltage regulator as depicted in **Figure 1-1**. The regulator functional elements are the regulator core (REG), a low voltage detect module (LVD), a control block (CTRL), a power-on reset module (POR) and a low voltage reset module (LVR).

### 4.2 REG - Regulator Core

VREG\_3V3, respectively its regulator core has two parallel, independent regulation loops (REG1 and REG2) that differ only in the amount of current that can be delivered.

The regulator is a linear regulator with a bandgap reference when operated in Full Performance Mode. It acts as a voltage clamp in Reduced Power Mode. All load currents flow from input VDDR to VSS or VSSPLL. The reference circuits are supplied by VDDA and VSSA.

#### 4.2.1 Full Performance Mode

In Full Performance Mode the output voltage is compared with a reference voltage by an operational amplifier. The amplified input voltage difference drives the gate of an output transistor.

#### 4.2.2 Reduced Power Mode

In Reduced Power Mode the gate of the output transistor is connected directly to a reference voltage to reduce power consumption.

### 4.3 LVD - Low Voltage Detect

Subblock LVD is responsible for generating the low voltage interrupt (LVI). LVD monitors the input voltage ( $V_{DDA}-V_{SSA}$ ) and continuously updates the status flag LVDS.

Interrupt flag LVIF is set whenever status flag LVDS changes its value.

The LVD is available in FPM and is inactive in Reduced Power Mode or Shutdown Mode.

### 4.4 POR - Power-On Reset

This functional block monitors VDD. If VDD is below  $V_{POR}$ , POR is asserted, if VDD exceeds  $V_{POR}$ , the POR is deasserted. POR asserted forces the MCU into Reset. POR Deasserted will trigger the power on sequence.

## 4.5 LVR - Low Voltage Reset

Block LVR monitors the primary output voltage VDD. If it drops below the assertion level ( $V_{LVRA}$ ) signal LVR asserts if VDD rises above the deassertion level ( $V_{LVRD}$ ) signal LVR deasserts. The LVR function is available only in Full Performance Mode.

## 4.6 CTRL - Regulator Control

This part contains the register block of VREG\_3V3 and further digital functionality needed to control the operating modes. CTRL also represents the interface to the digital core logic.

## 4.7 API - Autonomous Periodical Interrupt

Subblock API can generate periodical interrupts independent of the clock source of the MCU. To enable the timer the bit APIFE need to be set.

The API timer is either clocked by a trimmable internal RC-oscillator or the bus clock. Timer operation will freeze when MCU clock source is selected and bus clock is turned off. See CRG specification for details. The clock source can be selected with bit APICLK. APICLK can only be written when APIFE is not set.

Using bits APIR[3:0] the period can be selected after which amount of time an interrupt should be generated. The 1<sup>st</sup> period length might differ if APIR[3:0] is changed during APIFE = 1. As soon as APIFE is set the timer starts running. When the configured time has elapsed the Flag APIF is set. An interrupt, indicated by flag APIF=1, is triggered if interrupt enable bit APIE=1. The timer is started automatically again after it has sets APIF.

The API Trimming bits APITR[5:0] can be set by customer if accurate period or different period is wanted. See **Table 3-3** for the trimming effect of APITR.

**NOTE:** *The first period after enabling the counter by APIFE might be reduced.*

**NOTE:** *The API internal RC-Oscillator clock is not available if VREG\_3V3 is in Shutdown Mode.*

## Section 5 Resets

### 5.1 General

This section describes how VREG\_3V3 controls the reset of the MCU. The reset values of registers and signals are provided in **Section 3 Memory Map and Registers**. Possible reset sources are listed in **Table 5-1**.

**Table 5-1 VREG\_3V3 - Reset Sources**

Reset Source	Local Enable
Power-on Reset	always active
Low Voltage Reset	available only in Full Performance Mode

### 5.2 Description of Reset Operation

#### 5.2.1 Power-On Reset (POR)

During chip power-up the digital core may not work if its supply voltage VDD is below the POR deassertion level ( $V_{POR}$ ). Therefore signal POR which forces the other blocks of the device into reset is kept high until VDD exceeds  $V_{POR}$ . The MCU will run the start-up sequence after POR deassertion. The power-on reset is active in all operation modes of VREG\_3V3.

#### 5.2.2 Low Voltage Reset (LVR)

For details on low voltage reset see section **4.5 LVR - Low Voltage Reset**.



## Section 6 Interrupts

### 6.1 General

This section describes all interrupts originated by VREG\_3V3.

The interrupt vectors requested by VREG\_3V3 are listed in **Table 6-1**. Vector addresses and interrupt priorities are defined at MCU level.

**Table 6-1 VREG\_3V3 - Interrupt Vectors**

Interrupt Source	Local Enable
Low Voltage Interrupt (LVI)	LVIE=1; available only in Full Performance Mode
Autonomous Periodical Interrupt (API)	APIE=1;

## 6.2 Description of Interrupt Operation

### 6.2.1 LVI - Low Voltage Interrupt

In FPM VREG\_3V3 monitors the input voltage VDDA. Whenever VDDA drops below level  $V_{LVIA}$  the status bit LVDS is set to 1. Vice versa, LVDS is reset to 0 when VDDA rises above level  $V_{LVID}$ . An interrupt, indicated by flag LVIF=1, is triggered by any change of the status bit LVDS if interrupt enable bit LVIE=1.

**NOTE:** On entering the Reduced Power Mode the LVIF is not cleared by the VREG\_3V3.

### 6.2.2 API - Autonomous Periodical Interrupt

As soon as the configured timeout period of the API has elapsed the APIF bit is set. An interrupt, indicated by flag APIF=1, is triggered if interrupt enable bit APIE=1.







# Block Guide End Sheet

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