PIT_24B4C
Block Guide
V01.00

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Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
01.00	09-Feb-04	09-Feb-04		Initial Release

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Preface

Terminology

Acronyms and Abbreviations	
PIT	Periodic Interrupt Timer
ISR	Interrupt Service Routine
CCR	Condition Code Register
SoC	System on Chip
micro time bases	clock periods of the 16-bit timer modulus down-counters, which are generated by the 8-bit modulus down-counters.

Section 1 Introduction

The PIT_24B4C module contains four 24-bit timers, as shown in **Figure 1-1**.

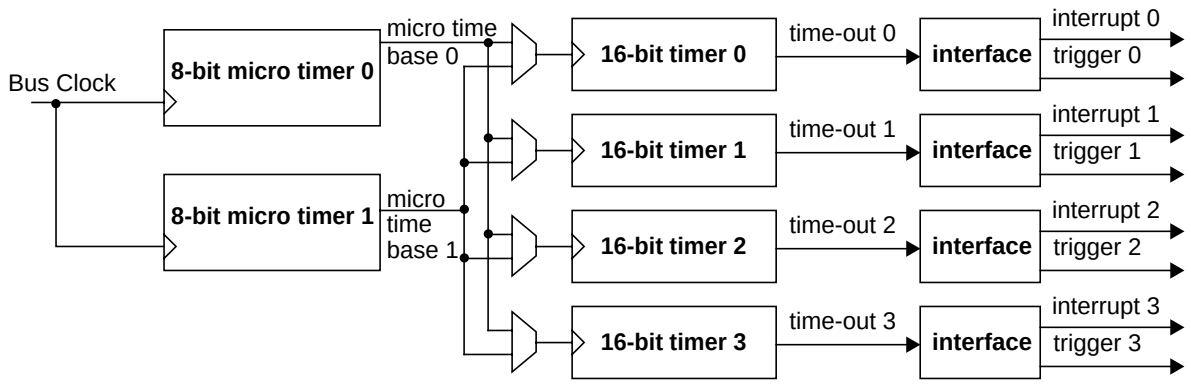


Figure 1-1 PIT_24B4C simplified Block Diagram

1.1 Overview

The PIT is an array of 24-bit timers which can be used to trigger peripheral modules or raise periodic interrupts.

1.2 Features

The PIT_24B4C includes these features:

- Four timers implemented as modulus down-counters with independent time-out periods
- Time-out periods selectable between 1 and 2^{24} bus clock cycles. Time-out equals m*n bus clock cycles with 1 <= m <= 256 and 1 <= n <= 65536
- The timers can be enabled individually
- Four time-out interrupts
- Four time-out trigger output signals available to trigger peripheral modules
- Start of timer channels can be aligned to each other

1.3 Modes of Operation

Refer to the SoC guide for a detailed explanation of the chip modes.

- Run Mode

This is the basic mode of operation.

- Wait Mode

  PIT operation in wait mode is controlled by the PITSWAI bit located in the PITCFLMT register. In wait mode, if the bus clock is globally enabled and if the PITSWAI bit is clear, the PIT operates like in run mode. In wait mode, if the PITSWAI bit is set, the PIT module is stalled.

- Stop Mode

  In full stop mode or pseudo stop mode the PIT module is stalled.

- Freeze Mode

  PIT operation in freeze mode is controlled by the PITFRZ bit located in the PITCFLMT register. In freeze mode, if the PITFRZ bit is clear, the PIT operates like in run mode. In freeze mode, if the PITFRZ bit is set, the PIT module is stalled.

Section 2 External Signal Description

The PIT module has no external pins.

Section 3 Memory Map/Register Definition

This section provides a detailed description of address space and registers used by the PIT.

The memory map for the PIT_24B4C is given below in **Table 3-1**. The address listed for each register is the sum of a base address and an address offset. The base address is defined at the SoC level and the address offset is defined at the module level. Reads from the reserved bits return zeros and writes to the reserved bits have no effect.

Table 3-1 Module Memory Map

Address	Use	Access
$__00	PIT Control and Force Load Micro Timer Register (PITCFLMT)	Read / Write [1]
$__01	PIT Force Load Timer Register (PITFLT)	Read / Write [1,2]
$__02	PIT Channel Enable Register (PITCE)	Read / Write [1]
$__03	PIT Multiplex Register (PITMUX)	Read / Write [1]
$__04	PIT Interrupt Enable Register (PITINTE)	Read / Write [1]
$__05	PIT Time-out Flag Register (PITTF)	Read / Write [1]
$__06	PIT Micro Timer Load Register 0 (PITMTLD0)	Read / Write
$__07	PIT Micro Timer Load Register 1 (PITMTLD1)	Read / Write
$__08, $__09	PIT Load Register 0 (PITLD0)	Read / Write
$__0A, $__0B	PIT Count Register 0 (PITCNT0)	Read / Write
$__0C, $__0D	PIT Load Register 1 (PITLD1)	Read / Write
$__0E, $__0F	PIT Count Register 1 (PITCNT1)	Read / Write

Table 3-1 Module Memory Map

$__10, $__11	PIT Load Register 2 (PITLD2)	Read / Write
$__12, $__13	PIT Count Register 2 (PITCNT2)	Read / Write
$__14, $__15	PIT Load Register 3 (PITLD3)	Read / Write
$__16, $__17	PIT Count Register 3 (PITCNT3)	Read / Write
$__18 - $__27	reserved registers[3]	Read / Write

NOTES:
1. Certain bits are non-writable.
2. Reading from this register returns all zeros.
3. Reading from these registers returns all zeros. Writing to these registers has no effect.

3.1 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

3.1.1 PIT Control and Force Load Micro Timer Register

Register Address: $__00

	Bit 7	6	5	4	3	2	1	Bit 0
R	PITE	PITSWAI	PITFRZ	0	0	0	0	0
W							PFLMT1	PFLMT0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-1 PIT Control and Force Load Micro Timer Register (PITCFLMT)

Read:anytime

Write:anytime; writes to the reserved bits have no effect

PITE — PIT Module Enable Bit

This bit enables the PIT module. If PITE is cleared, the PIT module is disabled and flag bits in the PITTF register are cleared. When PITE is set, individually enabled timers (PCE set) start down-counting with the corresponding load register values.

1 = PIT is enabled.
0 = PIT disabled (lower power consumption).

PITSWAI — PIT Stop in Wait Mode Bit

This bit is used for power conservation while in wait mode.

1 = PIT clock generation stops and freezes the PIT module when in wait mode
0 = PIT operates normally in wait mode

PITFRZ — PIT Counter Freeze while in Freeze Mode Bit

When during debugging a breakpoint (Freeze Mode) is encountered it is useful in many cases to freeze the PIT counters to avoid e.g. interrupt generation. The PITFRZ bit controls the PIT operation while in freeze mode.

1 = PIT counters are stalled when in freeze mode
0 = PIT operates normally in freeze mode

PFLMT[1:0] — PIT Force Load Bits for Micro Timer 1-0

These bits have only an effect if the corresponding micro timer is active and if the PIT module is enabled (PITE set). Writing a one into a PFLMT bit loads the corresponding 8-bit micro timer load register into the 8-bit micro timer down-counter. Writing a zero has no effect. Reading these bits will always return zero.

NOTE: *A micro timer force load affects all timer channels that use the corresponding micro time base!*

3.1.2 PIT Force Load Timer Register

Register Address: $__01

	Bit 7	6	5	4	3	2	1	Bit 0
R	0	0	0	0	0	0	0	0
W					PFLT3	PFLT2	PFLT1	PFLT0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-2 PIT Force Load Timer Register (PITFLT)

Read:anytime

Write:anytime; writes to the reserved bits have no effect

PFLT[3:0] — PIT Force Load Bits for Timer 3-0

These bits have only an effect if the corresponding timer channel (PCE set) is enabled and if the PIT module is enabled (PITE set). Writing a one into a PFLT bit loads the corresponding 16-bit timer load register into the 16-bit timer down-counter. Writing a zero has no effect. Reading these bits will always return zero.

3.1.3 PIT Channel Enable Register

Register Address: $__02

	Bit 7	6	5	4	3	2	1	Bit 0
R	0	0	0	0	PCE3	PCE2	PCE1	PCE0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-3 PIT Channel Enable Register (PITCE)

Read:anytime

Write:anytime; writes to the reserved bits have no effect

PCE[3:0] — PIT Enable Bits for Timer Channel 3-0

These bits enable the PIT channels 3-0. If PCE is cleared, the PIT channel is disabled and the corresponding flag bit in the PITTF register is cleared. When PCE is set, and if the PIT module is enabled (PITE =1) the 16-bit timer counter is loaded with the start count value and starts down-counting.

1 = the corresponding PIT channel is enabled.
0 = the corresponding PIT channel is disabled.

3.1.4 PIT Multiplex Register

Register Address: $__03

	Bit 7	6	5	4	3	2	1	Bit 0
R	0	0	0	0	PMUX3	PMUX2	PMUX1	PMUX0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-4 PIT Multiplex Register (PITMUX)

Read:anytime

Write:anytime; writes to the reserved bits have no effect

PMUX[3:0] — PIT Multiplex Bits for Timer Channel 3-0

These bits select if the corresponding 16-bit timer is connected to micro time base 1 or 0. If PMUX is modified, the corresponding 16-bit timer is immediately switched to the other micro time base.

1 = the corresponding 16-bit timer counts with micro time base 1.
0 = the corresponding 16-bit timer counts with micro time base 0.

3.1.5 PIT Interrupt Enable Register

Register Address: $__04

	Bit 7	6	5	4	3	2	1	Bit 0
R	0	0	0	0	PINTE3	PINTE2	PINTE1	PINTE0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-5 PIT Interrupt Enable Register (PITINTE)

Read:anytime

Write:anytime; writes to the reserved bits have no effect

PINTE[3:0] — PIT Time-out Interrupt Enable Bits for Timer Channel 3-0

These bits enable an interrupt service request whenever the time-out flag PTF of the corresponding PIT channel is set. When an interrupt is pending (PTF set) enabling the interrupt will immediately cause an interrupt. To avoid this, the corresponding PTF flag has to be cleared first.

1 = Interrupt of the corresponding PIT channel is enabled.
0 = Interrupt of the corresponding PIT channel is disabled.

3.1.6 PIT Time-out Flag Register

Register Address: $__05

	Bit 7	6	5	4	3	2	1	Bit 0
R	0	0	0	0	PTF3	PTF2	PTF1	PTF0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-6 PIT Time-out Flag Register (PITTF)

Read:anytime

Write:anytime (write to clear); writes to the reserved bits have no effect

PTF[3:0] — PIT Time-out Flag Bits for Timer Channel 3-0

PTF is set when the corresponding 16-bit timer modulus down-counter and the selected 8-bit micro timer modulus down-counter have counted to zero. The flag can be cleared by writing a one to the flag bit. Writing a zero has no effect. If flag clearing by writing a one and flag setting happen in the same bus clock cycle, the flag remains set. The flag bits are cleared if the PIT module is disabled or if the corresponding timer channel is disabled.

1 = Time-out of the corresponding PIT channel has occurred.

0 = Time-out of the corresponding PIT channel has not yet occurred.

3.1.7 PIT Micro Timer Load Register 0 to 1

Register Address: $__06, $__07

	Bit 7	6	5	4	3	2	1	Bit 0
R W	PMTLD7	PMTLD6	PMTLD5	PMTLD4	PMTLD3	PMTLD2	PMTLD1	PMTLD0
Reset:	0	0	0	0	0	0	0	0

Figure 3-7 PIT Micro Timer Load Register 0 to 1 (PITMTLD0-1)

Read:anytime

Write:anytime

PMTLD[7:0] — PIT Micro Timer Load Bits 7-0

These bits set the 8-bit modulus down-counter load value of the micro timers. Writing a new value into the PITMTLD register will not restart the timer. When the micro timer has counted down to zero the PMTLD register value will be loaded. The PFLMT bits in the PITCFLMT register can be used to immediately update the count register with the new value if an immediate load is desired.

3.1.8 PIT Load Register 0 to 3

Register Address: {$__08,$__09}, {$__0C,$__0D}, {$__10,$__11}, {$__14,$__15}

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
R W	PLD15	PLD14	PLD13	PLD12	PLD11	PLD10	PLD9	PLD8	PLD7	PLD6	PLD5	PLD4	PLD3	PLD2	PLD1	PLD0
Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 3-8 PIT Load Register 0 to 3 (PITLD0-3)

Read:anytime

Write:anytime

PLD[15:0] — PIT Load Bits 15-0

These bits set the 16-bit modulus down-counter load value. Writing a new value into the PITLD register must be a 16-bit access, to ensure data consistency. It will not restart the timer. When the timer has counted down to zero the PTF time-out flag will be set and the register value will be loaded. The PFLT bits in the PITFLT register can be used to immediately update the count register with the new value if an immediate load is desired.

3.1.9 PIT Count Register 0 to 3

Register Address: {$__0A,$__0B}, {$__0E,$__0F}, {$__12,$__13}, {$__16,$__17}

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
R W	PCNT15	PCNT14	PCNT13	PCNT12	PCNT11	PCNT10	PCNT9	PCNT8	PCNT7	PCNT6	PCNT5	PCNT4	PCNT3	PCNT2	PCNT1	PCNT0
Reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 3-9 PIT Count Register 0 to 3 (PITCNT0-3)

Read:anytime

Write:has no meaning or effect

PCNT[15:0] — PIT Count Bits 15-0

These bits represent the current 16-bit modulus down-counter value. The read access for the count register must take place in one clock cycle as a 16-bit access.

Section 4 Functional Description

4.1 General

Figure 4-1 shows a detailed block diagram of the PIT module. The main parts of the PIT are status, control and data registers, two 8-bit down-counters, four 16-bit down-counters and an interrupt/trigger interface.

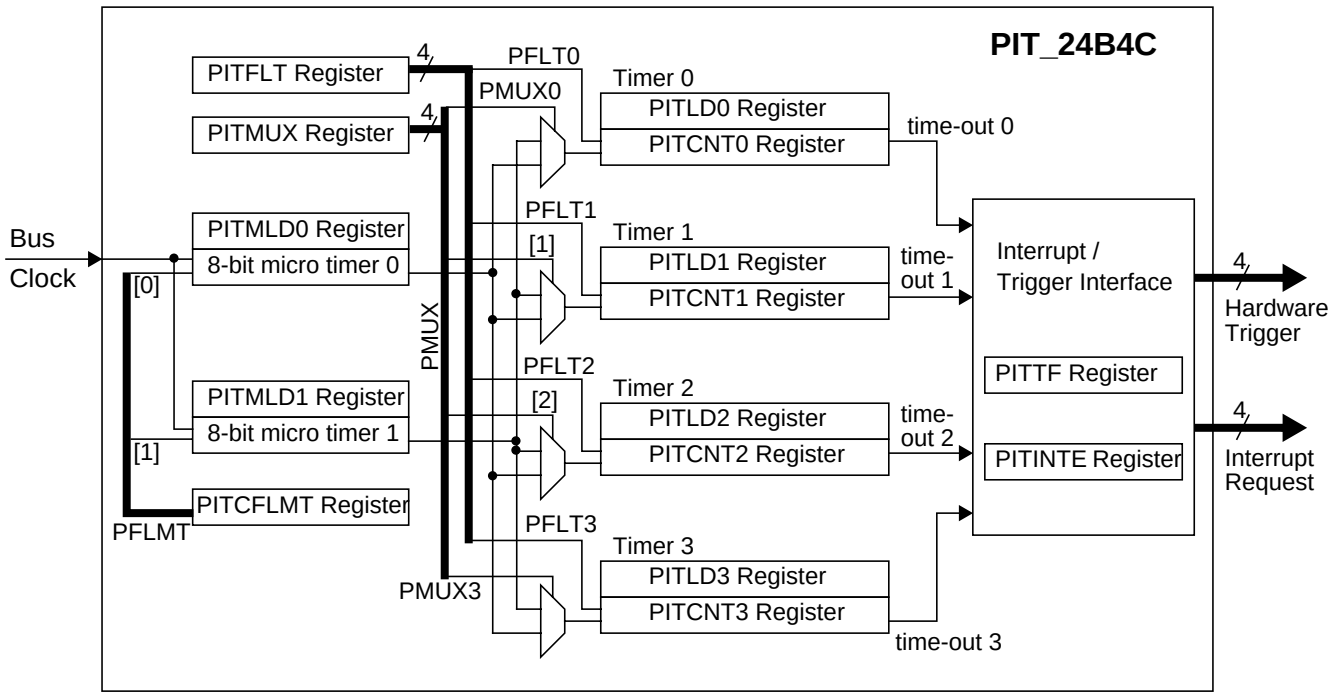


Figure 4-1 PIT_24B4C detailed Block Diagram

4.2 Timer

As shown in **Figure 1-1**and **Figure 4-1**the 24-bit timers are built in a two-stage architecture with four 16-bit modulus down-counters and two 8-bit modulus down-counters. The 16-bit timers are clocked with two selectable micro time bases which are generated with 8-bit modulus down-counters. Each 16-bit timer is connected to micro time base 0 or 1 via the PMUX[3:0] bit setting in the PIT Multiplex (PITMUX) register.

A timer channel is enabled if the module enable bit PITE in the PIT Control and Force Load Micro Timer (PITCFLMT) register is set and if the corresponding PCE bit in the PIT channel enable (PITCE) register is set. Two 8-bit modulus down-counters are used to generate two micro time bases. As soon as a micro time base is selected for an enabled timer channel, the corresponding micro timer modulus down-counter will load its start value as specified in the PITMTLD0 or PITMTLD1 register and will start down-counting. Whenever the micro timer down-counter has counted to zero the PITMTLD register is reloaded and the connected 16-bit modulus down-counters count one cycle.

Whenever a 16-bit timer counter and the connected 8-bit micro timer counter have counted to zero the PITLD register is reloaded and the corresponding time-out flag PTF in the PIT time-out flag (PITTF) register is set, as shown in **Figure 4-2**. The time-out period is a function of the timer load (PITLD) and micro timer load (PITMTLD) registers and the bus clock f_{BUS}:

$$\text{time-out period} = (\text{PITMTLD} + 1) * (\text{PITLD} + 1) / f_{BUS}.$$

E.g. for a 40MHz bus clock the maximum time-out period equals 256 * 65536 * 25ns = 419.43ms.

The current 16-bit modulus down-counter value can be read via the PITCNT register. The micro timer down-counter values cannot be read.

The 8-bit micro timers can individually be restarted by writing a one to the corresponding force load micro timer PFLMT bits in the PIT Control and Force Load Micro Timer (PITCFLMT) register. The 16-bit timers can individually be restarted by writing a one to the corresponding force load timer PFLT bits in the PIT Force Load Timer (PITFLT) register. If desired any group of timers and micro timers can be restarted at the same time by using one 16-bit write to the adjacent PITCFLMT and PITFLT registers with the relevant bits set, as shown in **Figure 4-2**.

4.3 Interrupt Interface

Each time-out event can be used to trigger an interrupt service request. For each timer channel an individual bit PINTE in the PIT Interrupt Enable (PITINTE) register exists to enable this feature. If PINTE is set an interrupt service is requested whenever the corresponding time-out flag PTF in the PIT time-out flag (PITTF) register is set. The flag can be cleared by writing a one to the flag bit.

NOTE: *Be careful when resetting the PITE, PINTE or PITCE bits in case of pending PIT interrupt requests, to avoid spurious interrupt requests!*

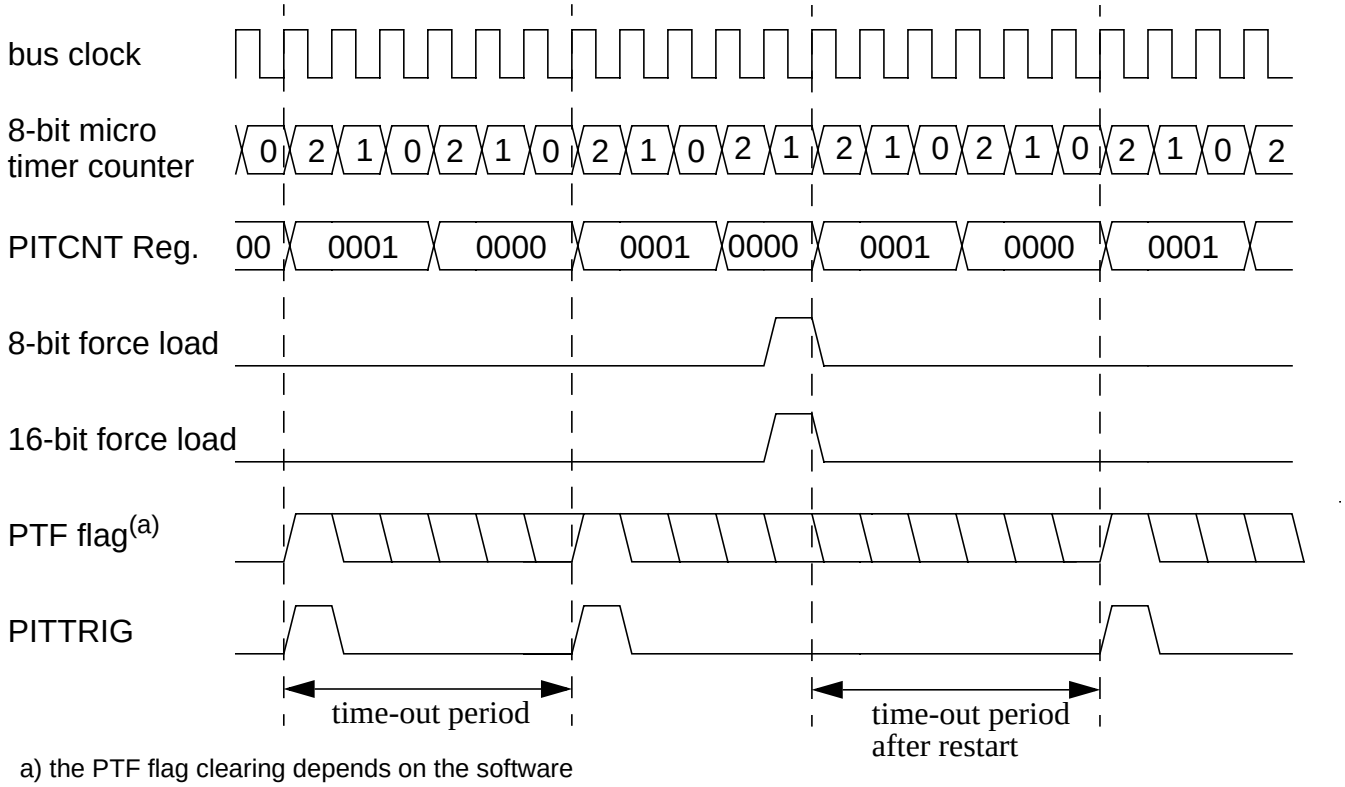
4.4 Hardware Trigger

The PIT module contains four hardware trigger signal lines PITTRIG[3:0], one for each timer channel. These signals can be connected on SoC level to peripheral modules enabling e.g. periodic ATD conversion (please refer to the SoC Guide for the mapping of PITTRIG[3:0] signals to peripheral modules).

Whenever a timer channel time-out is reached the corresponding PTF flag is set and the corresponding trigger signal PITTRIG triggers a rising edge. The trigger feature requires a minimum time-out period of two bus clock cycles because the trigger is asserted high for at least one bus clock cycle. For load register

values PITLD=$0001 and PITMTLD=$02 the flag setting, trigger timing and a restart with force load is shown in **Figure 4-2**.

Figure 4-2 PIT Trigger and Flag Signal Timing



a) the PTF flag clearing depends on the software

Section 5 Initialization/Application Information

5.1 Startup

Set the configuration registers before the PITE bit in the PITCFLMT register is set. Before PITE is set, the configuration registers can be written in arbitrary order.

5.2 Shutdown

When the PITCE register bits, the PITINTE register bits or the PITE bit in the PITCFLMT register are cleared, the corresponding PIT interrupt flags are cleared. In case of a pending PIT interrupt request a spurious interrupt can be generated. Two strategies, which avoid spurious interrupts, are recommended:

1. Reset the PIT interrupt flags only in an ISR. When entering the ISR the I Mask bit in the CCR is set automatically. The I Mask bit must not be cleared before the PIT interrupt flags are cleared.

2. After setting the I Mask bit with the SEI instruction, the PIT interrupt flags can be cleared. Then clear the I Mask bit with the CLI instruction to re-enable interrupts.

5.3 Flag Clearing

A flag is cleared by writing a one to the flag bit. Always use store or move instructions to write a one in certain bit positions. Do not use the bset instructions. Do not use any C-constructs that compile to bset instructions. “BSET flag_register, #mask” must not be used for flag clearing because bset is a read-modify-write instruction which writes back the “bit-wise or” of the flag_register and the mask into the flag_register. BSET would clear all flag bits that were set, independent from the mask.

E.g. to clear flag bit 0 use: MOVB #$01,PITTF.

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