S12X_EBI

Block Guide

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SPS/TSPG/816bit
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Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
01.28	13-Feb-03	13-Feb-03		Initial Customer Release
V01.29	25-Jun-03	25-Jun-03		Corrected document number. Removed "Controlled Copy" banners.

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Section 1 Introduction

This section describes the functionality of the External Bus Interface (EBI) sub-block of the s12x_core Platform. The functionality of the module is closely coupled with the s12x_cpu and the Memory Map Controller (s12x_mmc) sub-blocks.

Figure 1-1 is a block diagram of the EBI. In **Figure 1-1**, the signals on the right hand side represent pins that are associated to the port logic. Note there is a Port Interface Module (PIM) which is separate from the EBI and which may be configured for each chip. The user is advised to study this module for the particular chip being used in order to determine the exact functionality of the ports and pins. The block diagram shows the EBI and a PIM. A dotted line separates the two.

Figure 1-1 s12x_ebi Block Diagram

1.1 Overview

The EBI sub-block of the Core serves to provide access and/or visibility to internal Core data manipulation operations including timing reference information at the external boundary of the Core and/or system. The EBI supplies the address and data buses for external accesses and for internal data bus visibility.

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1.2 Features

The EBI includes these features:

- External bus controller designed to use six 8-bit Ports A, B, C, D, E, and K

- Generation of raw address, write data and control signals to be used with a non-muxed external bus

- Inputs for read data from external bus

- Control register to enable/disable alternate functions generally on Port E (determined by PIM)

- Mode control register

- Read Enable and Write Enable function

- Chip Selects

1.3 Modes of Operation

- Normal Expanded Mode

  Ports K, A and B are configured as a 23-bit address bus, Ports C and D are configured as a 16-bit data bus, and Port E provides bus control and status signals. This mode allows 16-bit external memory and peripheral devices to be interfaced to the system. The fastest external bus rate is divide by 2 from the internal bus rate. In this mode there is an external input which can cause the external bus to wait as desired by external logic.

- Normal Single-Chip Mode

  There is no external expansion bus in this mode. The processor program is executed from internal memory. Ports A, B,C,D, K, and most of E are available as general-purpose I/O.

- Special Single-Chip Mode

  This mode is generally used for debugging single-chip operation, boot-strapping, or security related operations. The active background mode is in control of CPU execution and BDM firmware is waiting for additional serial commands through the BKGD pin. There is no external expansion bus after reset in this mode.

- Emulation of Expanded Mode

  Developers use this mode for emulation systems in which the user's target application is Normal Expanded Mode.

- Emulation of Single-Chip Mode

  Developers use this mode for emulation systems in which the user's target application is Normal Single-Chip Mode. Code is executed from external memory if ROMON = 0 or from internal memory if ROMON = 1. The expansion bus is active in both cases to allow observation of the internal operation.

- Special Test Mode

Ports K, A and B are configured as a 23-bit address bus, Ports C and D are configured as a 16-bit data bus, and Port E provides bus control and status signals. In special test mode, the write protection of many control bits is lifted so that they can be thoroughly tested without needing to go through reset.

Section 2 External Signal Description

2.1 Overview

The user is advised to check the chip level document for port configuration and location of external bus signals. Some pins may not be bonded out in all implementations.

Table 2-1 outlines the pin names and functions and gives a brief description of their operation. Reset state of these pins and associated pull-ups or pull-downs is dependent on the mode of operation and on the integration of this block at the chip level (chip dependent).

Table 2-1 External System Signal Associated With EBI (Sheet 1 of 3)

Signal Functions	Signal mux	Description
MODC	MODC	At the rising edge on $\overline{\text{RESET}}$, the state of this pin is registered into the MODC bit to set the mode.
A15–A8	A15/IVD15 thru A8/IVD8	Mid address lines output in expanded modes. Addresses are not multiplexed with data when IVIS = 0.
IVD15–IVD8		High-order internal read data lines multiplexed outputs during visible internal data accesses (IVIS = 1) in special test mode and always in emulation modes.
A7–A1	A7/IVD7 thru A1/IVD1	Low-order address lines output in expanded modes. Addresses are not multiplexed with data when IVIS = 0.
IVD7–IVD1		Low-order internal read data lines multiplexed outputs during visible internal read accesses (IVIS = 1) in special test mode and always in emulation modes.
A0	A0/ $\overline{\text{UDS}}$/ IVD0	Low-order address lines output in expanded modes. Addresses are not multiplexed with data when IVIS = 0.
$\overline{\text{UDS}}$		Upper Data Strobe, active if there is a valid external access to the high byte D15:8
IVD0		Low-order internal read data lines multiplexed outputs during visible internal read accesses (IVIS = 1) in special test mode and always in emulation modes.
WD15–WD8	WD15 thru WD8	High-order output write data lines (even address).
WD7–WD0	WD7 thru WD0	Low-order output write data lines (odd address).
RD15–RD8	RD15 thru RD8	High-order input read data lines (even address).

Table 2-1 External System Signal Associated With EBI (Sheet 2 of 3)

Signal Functions	Signal mux	Description
RD7–RD0	RD7 thru RD0	Low-order input read data lines (odd address).
EWAIT	EWAIT/ ROMCTL	Maintain the external bus access until external device is ready to capture date (write) or provide data (read).
ROMCTL		At the rising edge of $\overline{RESET}$, the state of this pin is registered and selects the state of ROMON.
NOACC	NOACC/ A22	CPU No Access output. Indicates whether the current cycle is a free cycle. Only available in emulation and special test modes multiplexed with address.
A22		High order address in expanded modes.
A[21:20]	A[21:20]	High order addresses in expanded modes.
IQSTAT[3]	IQSTAT[3]/ A19	Queue Status: Advance and load. Only available in emulation and special test modes multiplexed with address.
A19		High order address in expanded modes.
IQSTAT[2]	IQSTAT[2]/ A18	Queue Status: Start even instruction. Only available in emulation and special test modes multiplexed with address.
A18		High order address in expanded modes.
IQSTAT[1]	IQSTAT[1]/ A17	Queue Status: Start odd instruction. Only available in emulation and special test modes multiplexed with address.
A17		High order address in expanded modes.
IQSTAT[0]	IQSTAT[0]/ A16	Queue Status: Start interrupt. Only available in emulation and special test modes multiplexed with address.
A16		High order address in expanded modes.
ECLKX2	ECLKX2	Bus timing reference clock in emulation and special test modes. A free-running clock at the cpu clock rate.
MODB	MODB	At the rising edge of $\overline{RESET}$, the state of this pin is registered into the MODB bit to set the mode.
MODA	MODA/ $\overline{RE}$	At the rising edge on $\overline{RESET}$, the state of this pin is registered into the MODA bit to set the mode.
$\overline{RE}$		Read Enable, active in normal expanded mode
ECLK	ECLK	Bus timing reference clock in emulation and special test modes. A free-running clock at the system clock rate or divided in other modes.
$\overline{LSTRB}$	$\overline{LSTRB}$/ $\overline{LDS}$	Low strobe bar, zero indicates valid data on D7–D0.
$\overline{LDS}$		Lower Data Strobe, active if there is a valid external access to the low byte D7:D0.

Table 2-1 External System Signal Associated With EBI (Sheet 3 of 3)

Signal Functions	Signal mux	Description
R/$\overline{\text{W}}$	R/$\overline{\text{W}}$/ $\overline{\text{WE}}$	Read/write, indicates the direction of internal data transfers. This is an output.
$\overline{\text{WE}}$		Write Enable, may be selected in expanded modes.
CS0	CS0	Chip select 0. See Device User Guide for availability and pin assignment
CS1	CS1	Chip select 1. See Device User Guide for availability and pin assignment
CS2	CS2	Chip select 2. See Device User Guide for availability and pin assignment

2.2 Detailed Signal Descriptions

Detailed descriptions of these pins can be found in the device specification for the particular chip being used.

Section 3 Memory Map/Register Definition

Many of the registers formally associated with the EBI are now located in the PIM. The registers associated with the EBI are shown in **Figure 3-1**.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
$000A	EIFCTL	Read / Write	CS2E	CS1E	CS0E	NECLK	EDIV1	EDIV0	NCLKX2	EWAIT
$000B	MODE	Read	MODC	MODB	MODA	ITHRS	IVIS	0	0	0
		Write	MODC	MODB	MODA	ITHRS	IVIS			
$000E	Reserved	Read	0	0	0	0	0	0	0	0
		Write								
$000F	Reserved	Read	0	0	0	0	0	0	0	0
		Write								

▨ = Unimplemented

Figure 3-1 EBI Register Map Summary

3.1 Register Descriptions

3.1.1 External Bus Interface Control Register (EIFCTL)

Address: $000A

	BIT 7	6	5	4	3	2	1	BIT 0	
Read: / Write:	CS2E	CS1E	CS0E	NECLK	EDIV1	EDIV0	NCLKX2	EWAIT	
Reset:	0	0	$\overline{ROMON}$	0	0	0	1	0	Normal Expanded
Reset:	0	0	0	1	0	0	1	0	Normal Single-Chip
Reset:	0	0	0	0	0	0	1	0	Special Single-Chip
Reset:	0	0	$\overline{ROMON}$	0	0	0	0	0	Emulation of Expanded
Reset:	0	0	$\overline{ROMON}$	0	0	0	0	0	Emulation of Single-Chip
Reset:	0	0	0	0	0	0	1	0	Special Test

▨ = Unimplemented

Figure 3-2 External Bus Interface Control Register (EIFCTL)

Read: Anytime in Single Chip, Special Test and Normal Expanded modes, Never in Emulation modes. In emulation modes, reads of this register are treated as external.

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Write: Anytime. Writes to some bits of this register may have no effect in certain operating modes. Please refer to the descriptions of each bit on the following pages.

The EIFCTL register is used to control external bus functions.

CS2E, CS1E, CS0E — Chip Select Enables 2, 1, 0

Each of these bits enables one of the external chip selects (only available in Normal Expanded, Emulation Expanded and Special Test modes).

Chip Select 2 is active in the global address range $14_0000 - $17_FFFF.

Chip Select 1 is active in the global address range $20_0000 - $3F_FFFF.

Chip Select 0 is active in the global address range $40_0000 - $7F_FFFF. If the on-chip Flash or ROM is enabled (ROMON = 1), then chip select 0 is not active in the space occupied by that on-chip memory.

Write anytime
1 = Chip Select is enabled (CSEx bits can only be written to a 1 in Normal Expanded, Emulation Expanded or Special Test mode).
0 = Chip Select is disabled.

NECLK — No External E Clock

Write anytime
1 = The associated pin is a general-purpose I/O pin. (NECLK can only be written to a 1 in Normal Expanded or Normal Single Chip mode)
0 = The associated pin is the external E clock pin.

EDIV1, EDIV0 — Divider for Free-Running External E Clock

These bits determine the rate of the free-running E clock. EDIVx bits can only be written to a 1 in Normal Expanded or Normal Single Chip mode. The usage of the bits is shown in **Table 3-1**.

Write anytime

Table 3-1 EDIV1:0, Free-Running E Clock Rate

EDIV1	EDIV0	Rate of Free-Running E Clock
0	0	ECLK = Internal bus rate
0	1	ECLK = Internal bus rate divided by 2
1	0	ECLK = Internal bus rate divided by 3
1	1	ECLK = Internal bus rate divided by 4

NCLKX2 — No External 2X (cpu) Clock

Special Test: Write Anytime

All other: Write Never
1 = The associated pin is a general-purpose I/O pin.
0 = The associated pin is the external 2x (cpu) clock pin.

EWAIT — External Wait Enable

This bit enables the external wait function (only available in Normal Expanded and Emulation modes).

Write anytime

1 = External Wait is enabled (EWAIT bit can only be written to a 1 in Normal Expanded or Emulation Expanded mode).
0 = External Wait is disabled.

3.1.2 MODE Register (MODE)

Address: $000B

	BIT 7	6	5	4	3	2	1	BIT 0	
Read:	MODC	MODB	MODA	ITHRS	IVIS	0	0	0	
Write:									
Reset:	0	0	0	0	0	0	0	0	Special Single-Chip
Reset:	0	0	1	1	1	0	0	0	Emulation Single-Chip
Reset:	0	1	0	0	0	0	0	0	Special Test
Reset:	0	1	1	1	1	0	0	0	Emulation Expanded
Reset:	1	0	0	0	0	0	0	0	Normal Single-Chip
Reset:	1	0	1	1	0	0	0	0	Normal Expanded
Reset:	1	1	0	0	0	0	0	0	Reserved
Reset:	1	1	1	0	0	0	0	0	Reserved

 = Unimplemented

Figure 3-3 MODE Register (MODE)

Read: Anytime in Single Chip, Special Test and Normal Expanded modes, Never in Emulation modes. In emulation modes, reads of this register are treated as external.

Write: Anytime. Writes to some bits of this register may have no effect in certain operating modes. Please refer to the descriptions of each bit on the following pages.

The MODE register is used to establish the operating mode and other miscellaneous functions (i.e., internal visibility and input threshold level).

Changes to bits in the MODE register are delayed one cycle after the write

MODC, MODB, and MODA — Mode Select Bits

These bits indicate the current operating mode. **Table 3-2** describes the write-ability of these bits in logical form. This is what is accomplished:

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There's one chance to change from Normal Single Chip to Normal Expanded or from Emulation Single Chip to Emulation Expanded. This operation is used for executing code from internal Flash or ROM and using the expanded bus.

Starting from reset in Normal Expanded Mode or Emulation of Expanded Mode means that is the mode until the next reset (no mode changes).

Special Single-Chip and Special Test allow changing to any other mode except reserved.

Reserved mode cannot be accessed.

Table 3-2 MODC, MODB, and MODA Write Capability[1]

MODC	MODB	MODA	Mode	MODx Write Capability
0	0	0	Special Single-Chip	MODC, MODB, and MODA write anytime but not to 11X[2]
0	0	1	Emulation of Single-Chip	MODC, MODA write never MODB write once[3]
0	1	0	Special Test	MODC, MODB, and MODA write anytime but not to 11X[2]
0	1	1	Emulation of Expanded	No write
1	0	0	Normal Single-Chip	MODC, MODB write never, MODA write once
1	0	1	Normal Expanded	No write
1	1	X	Reserved	No write

NOTES:
1. No writes to the MOD bits are allowed while operating in a SECURE mode. For more details, refer to the device user guide.
2. If you are in a special single-chip or special test mode and you write to this register, changing to normal single-chip mode, then one allowed write to this register remains. If you write to normal expanded or emulation mode, then no writes remain
3. Writing a 101 (Normal Expanded Mode) while in Emulation of Single Chip, will result in a transition to Emulation of Expanded (011). Writing any other value will have no effect and will block further write to this register.
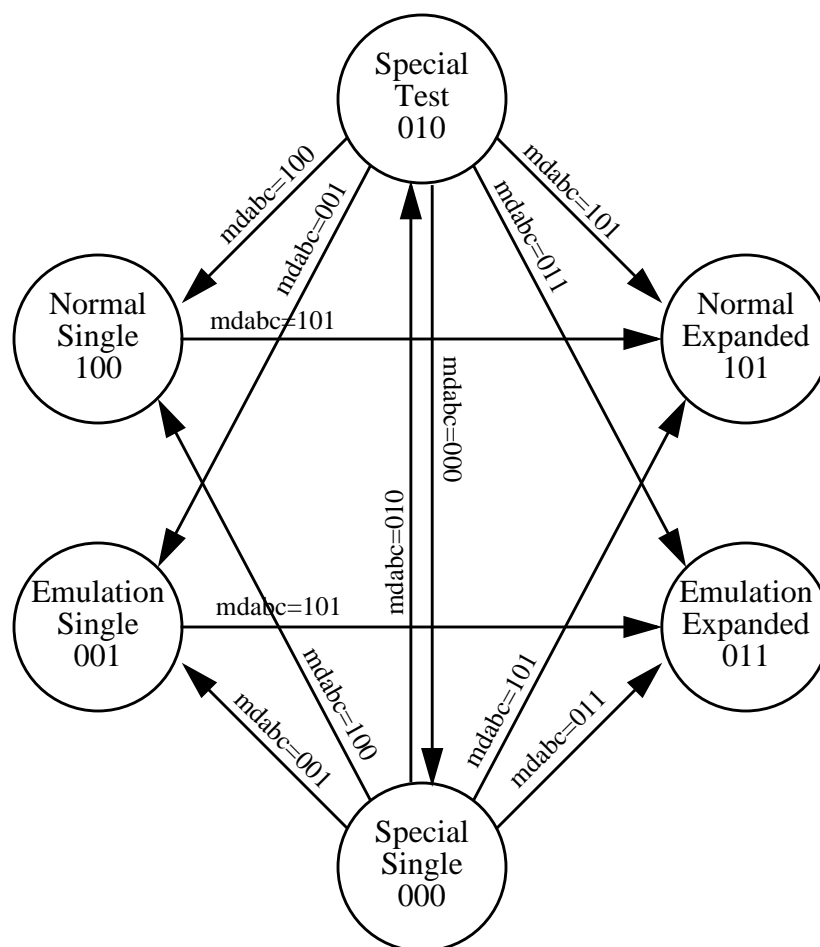
Figure 3-4 Mode Transition Diagram, only valid if MCU is unsecured

Table 3-3 Mode Select and State of Mode Bits

Input BKGD and Bit MODC	Input and Bit MODB	Input and Bit MODA	Mode Description
0	0	0	Special Single-Chip, BDM allowed and ACTIVE. BDM is "allowed" in all other modes but a serial command is required to make BDM "active".
0	0	1	Emulation of Normal Single-Chip, BDM allowed
0	1	0	Special Test (Expanded), BDM allowed
0	1	1	Emulation of Normal Expanded, BDM allowed
1	0	0	Normal Single-Chip, BDM allowed
1	0	1	Normal Expanded, BDM allowed
1	1	X	Reserved[1]

NOTES:
1. If mode inputs are set to the reserved state, the registers will load as Normal Single Chip equivalent to 100.

ITHRS — Input Threshold

Select Input Threshold for Ports C, D, E.

Write Anytime.
1 = Input Threshold is modified to allow receiving of correct data if external bus devices are operated at 3.3V and device is operated at 5V.
0 = Input Threshold is standard. (ITHRS bit cannot be written to a 0 in Emulation modes)

IVIS — Internal Data Bus Visibility

This bit determines whether internal data operations (reads and writes) mirrored on the external bus.

Special Test: Write Anytime

All other: Write Never
1 = Internal data bus operations are visible on external bus.
0 = No visibility of internal data bus operations on external bus.

Section 4 Functional Description

These are the main sub-blocks within the EBI:

- External bus interface related signals & control

- Control register bits to enable/disable alternate functions on expanded bus control pins.

- Mode control register.

- Secure mode control of bus signals.

4.1 External Bus Control

The external bus control generates, times or passes the miscellaneous control functions (pipe signals, ECLK, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$, $\overline{\text{WE}}$, $\overline{\text{RE}}$, $\overline{\text{CS0}}$, $\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$) that will be sent external on Port E or other pins. It also times the external addresses.

A general summary of the EBI functions for each mode is shown in

Table 4-1 Summary of EBI Functions

Properties	Normal Single Chip	Emulation Single Chip	Special Single Chip	Normal Expanded Mode	Emulation Expanded Mode	Special test Mode
Access Internal Address	1 cycle			1 cycle		1 cycle
Access Port AB…	2 cycles	2 cycles = PRU access	2 cycles	2 cycles N.A, since registers are irrelevant in these modes		2 cycles
Access External Address	X	1 cycle	X	2, 3, 4 cycles; E-WAIT controlled[1]		1 cycle
Access Emulation Flash Address[2]	X	1 cycle	X	X	1, 2, 3, 4 cycles; E-WAIT controlled[3]	1 cycle
IVIS	IVIS =0	IVIS = 1	IVIS = 0	IVIS = 0	IVIS = 1	IVIS = 0 out of reset, can be turned on
PE4 Behavior	off, /1, /2, /3, /4	/1= busclock always phase signal	/1= busclock always phase signal	off, /1, /2, /3, /4	/1= busclock always phase signal	/1= busclock always phase signal
LDS vs. LSTRB	X	A0, LSTRB	X	UDS, LDS	A0, LSTRB	A0, LSTRB
R/W vs. RE,WE	X	R/W	X	RE, WE	R/W	R/W
CS activateable	No			Yes		Yes
E-WAIT is achievable	No			Yes		No

NOTES:
1. If E-WAIT is selected, the minimum number of external bus cycles is 3.
2. This is an access to the address space which is normally internal Flash memory, but which can be emulated externally in certain modes. Accesses to all other external memory will be stretched.
3. Accesses to the external emulation Flash will be 1 cycle and not affected by EWAIT if EROMON = 0 and ROMON = 1 (see s12x_mmc Block Guide). If EROMON = ROMON = 1, the internal Flash will be on, and no external emulation Flash will be available. If ROMON = 0, then accesses to the external emulation Flash will be stretched like normal external accesses.

External means addressing an external resource this includes also the flash space in case of ROMON = 0.

ECLK means what is visible on PE4 pin

Port AB…, means all registers not in the map in emulation modes.

If said E-WAIT controlled, it means a minimum of the cycles shown in the ESTR register, plus as long as E-WAIT is asserted.

4.1.1 Detecting Access Type from External Signals

The external signals $\overline{\text{LSTRB}}$, R/$\overline{\text{W}}$, and AB0 indicate the type of bus access that is taking place. Accesses to the internal RAM module are the only type of access that would produce $\overline{\text{LSTRB}}$ = AB0 = 1, because the internal RAM is specifically designed to allow misaligned 16-bit accesses in a single cycle. In these cases the data for the address that was accessed is on the low half of the data bus and the data for address + 1 is on the high half of the data bus. This is summarized in **Table 4-2**. **Table 4-3** shows the access type functions when using $\overline{\text{UDS}}$, $\overline{\text{LDS}}$, $\overline{\text{RE}}$, $\overline{\text{WE}}$ in normal expanded mode.

Table 4-2 Access Type vs. Bus Control Pins in Emulation and Special Test modes

INT RAM access	$\overline{\text{LSTRB}}$	AB0	R/$\overline{\text{W}}$	Type of Access
x	1	0	1	8-bit read of an even address
x	0	1	1	8-bit read of an odd address
x	1	0	0	8-bit write of an even address
x	0	1	0	8-bit write of an odd address
x	0	0	1	16-bit read of an even address
0	0	1	1	16-bit read of an odd address (low/high data swapped)
1	1	1	1	16-bit read of an odd address (low/high data swapped)
x	0	0	0	16-bit write to an even address
0	0	1	0	16-bit write to an odd address (low/high data swapped)
1	1	1	0	16-bit write to an odd address (low/high data swapped)

Table 4-3 Access Type Bus vs. Control Pins in Normal Expanded mode

$\overline{\text{UDS}}$	$\overline{\text{LDS}}$	$\overline{\text{RE}}$	$\overline{\text{WE}}$	Type of Access
0	1	0	1	8-bit read of an even address
1	0	0	1	8-bit read of an odd address
0	1	1	0	8-bit write of an even address

Table 4-3 Access Type Bus vs. Control Pins in Normal Expanded mode

$\overline{\text{UDS}}$	$\overline{\text{LDS}}$	$\overline{\text{RE}}$	$\overline{\text{WE}}$	Type of Access
1	0	1	0	8-bit write of an odd address
0	0	0	1	16-bit read of an even address
0	0	1	0	16-bit write to an even address
X	X	1	1	No Access

4.1.2 Stretched Bus Cycles

In order to allow fast internal bus cycles to coexist in a system with slower external memory resources, the S12X supports the concept of stretched bus cycles (module timing reference clocks for timers and baud rate generators are not affected by this stretching). Control bits in the MISC register in the MMC sub-block of the Core specify the amount of stretch (0, 1, 2, or 3 additional periods of the internal bus-rate clock). While stretching, the CPU state machines are all held in their current state. At this point in the CPU bus cycle, write data would already be driven onto the data bus so the length of time write data is valid is extended in the case of a stretched bus cycle. Read data would not be captured by the system until the specified setup time before the $\overline{\text{RE}}$ rising edge.

4.1.3 Internal Visibility

Internal visibility is available when the system is operating in emulation modes and special test mode only. Internal visibility is enabled by setting the IVIS bit in the MODE register.

When internal visibility is enabled (IVIS = 1), certain internal cycles will be blocked from going external to prevent possible corruption of external devices. Specifically, during cycles when the BDM is selected, R/$\overline{\text{W}}$ will remain high, data will maintain its previous state, and address and $\overline{\text{LSTRB}}$ pins will be updated with the internal value. During CPU no access cycles when the BDM is not driving, R/$\overline{\text{W}}$ will remain high, and address, data, and the $\overline{\text{LSTRB}}$ pins will remain at their previous state.

4.1.4 Secure Mode

When the system is operating in a secure mode, internal visibility is not available (i.e., IVIS = 1 has no effect). Also, the IPIPE signals will not be visible, regardless of operating mode. IPIPEx will display zeroes. In addition, the MOD bits in the MODE control register cannot be written.

4.2 Control

The control block generates the register read/write control signals and miscellaneous port control signals.

4.2.1 Low-Power Options

The EBI does not contain any user-controlled options for reducing power consumption. The operation of the EBI in low-power modes is discussed in the following subsections.

4.2.1.1 Run Mode

The EBI does not contain any options for reducing power in run mode; however, the external addresses are conditioned to reduce power in single-chip modes. Expanded bus modes will increase power consumption.

4.2.1.2 Wait Mode

The EBI does not contain any options for reducing power in wait mode.

4.2.1.3 Stop Mode

The EBI will cease to function after execution of a CPU STOP instruction.

4.3 External Data Bus Interface

The external data bus interface block manages data transfers from/to the external pins to/from the internal read and write data buses. This block selectively couples 8-bit or 16-bit data to the internal data bus to implement a variety of data transfers including 8-bit, 16-bit, 16-bit swapped, and 8-bit external to 16-bit internal accesses. Modes, addresses, chip selects, etc. affect the type of accesses performed during each bus cycle.

4.4 Registers

The registers are described fully in **Section 3**.

Section 5 Application Information

This section will describe external bus interface timing and usage. The customer usage will be divided into three scenarios: normal mode operation without the ewait feature, normal mode operation with showing the ewait usage and emulation single chip mode operation.

Note that emulation expanded mode uses the same timing as normal mode. Special test mode uses the same timing as emulation single chip mode. Normal single chip and special single chip do not have an external bus.

5.1 Using the External Bus In Normal Mode

The normal bus operation requires a minimum of one cycle stretch for each external access. This method of using the external bus is straight forward and allows interfacing to external memories that have access times which are readily available in the commercial market.

5.1.1 Accesses to internal memory

These accesses will always be 1 cycle, except to the PRU registers, which are 2 cycles. The address bus, along with $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ will hold the previous state; $\overline{\text{RE}}$, $\overline{\text{WE}}$ and all $\overline{\text{CS}}$ pins will be negated. The data bus will drive the write data on a write cycle.

5.1.2 EWAIT Feature Turned Off

To start out simple, we start with the EWAIT feature unused. This first example of bus timing is shown in **Figure 5-1**. Systems designed this way rely on the internal programmable clock stretching. These systems have predictable external memory access times. Using 2 or 3 cycles of stretch is very similar and provides additional access time. The associated timing numbers are shown in **Table 5-1**.
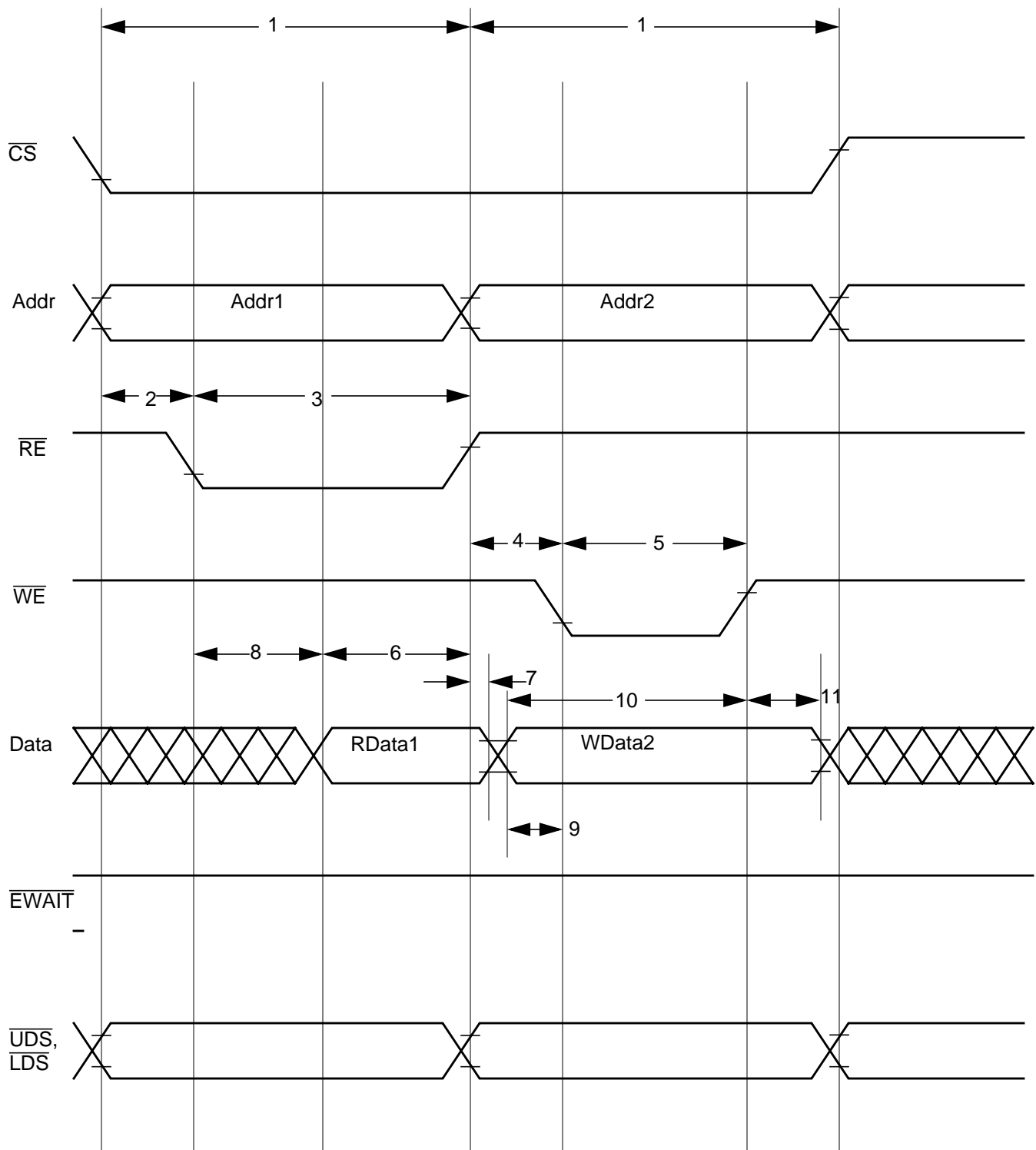
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Figure 5-1 Timing Diagram: Normal Mode - Read Followed by Write

Table 5-1: Normal Mode Expansion Bus Timing

No.	Characteristic [1] [2] [3] [4]	Symbol	40 MHz Min	Max	Unit
	Frequency of internal bus	f_i	D.C.	40.0	MHz
	Internal cycle time	t_{cyc}	25		ns
	Frequency of external bus	f_o	D.C.	20.0	MHz
1	External cycle time (selected by ESTR)	t_{cyce}	50		ns
2	Address valid to $\overline{RE}$ fall	t_{ADRE}		15	ns
3	Pulse width, $\overline{RE}$ (t_{cyce}-t_{ADRE})	PW_{RE}	35		ns
4	Address valid to $\overline{WE}$ fall	t_{ADWE}		15	ns
5	Pulse width, $\overline{WE}$ t_{cyce}	PW_{WE}	23		ns
6	Read data setup time	t_{DSR}	24		ns
7	Read data hold time	t_{DHR}	0		ns
8	Read enable access time (PW_{RE} - t_{DSR})	t_{ACCR}	11		ns
9	Write data valid to $\overline{WE}$ fall	t_{WDWE}	8		ns
10	Write data setup time (PW_{WE} +t_{WDWE})	t_{DSW}	31		ns
11	Write data hold time	t_{DHW}	8		ns

NOTES:
1. Crystal input is required to be within 45% to 55% duty.
2. Reduced drive must be off to meet these timings.
3. Unequal loading of pins will affect relative timing numbers.
4. The following signals are approximately line on line (change at the same time): Addr, UDS, LDS, & CS.

5.2 Using the External Bus With Bus Stretching and EWAIT

EWAIT operation is shown in the next examples. EWAIT can be used to increase the number of cycles of stretch over that which is programmed by ESTR. If the EWAIT signal is not asserted, the stretch is the same as programmed by ESTR. If EWAIT is asserted the minimum number of cycles is one more than programmed by ESTR. EWAIT can be held as long as desired to stretch the bus as needed.

Figure 5-2 shows one cycle of EWAIT stretch during a read access. **Figure 5-3** shows one cycle of EWAIT stretch during a write access. The associated timing numbers for both operations are shown in **Table 5-2**. It is recommended that the user use the free running E clock at the fastest rate (internal bus speed divided by 1) to time the EWAIT signal.
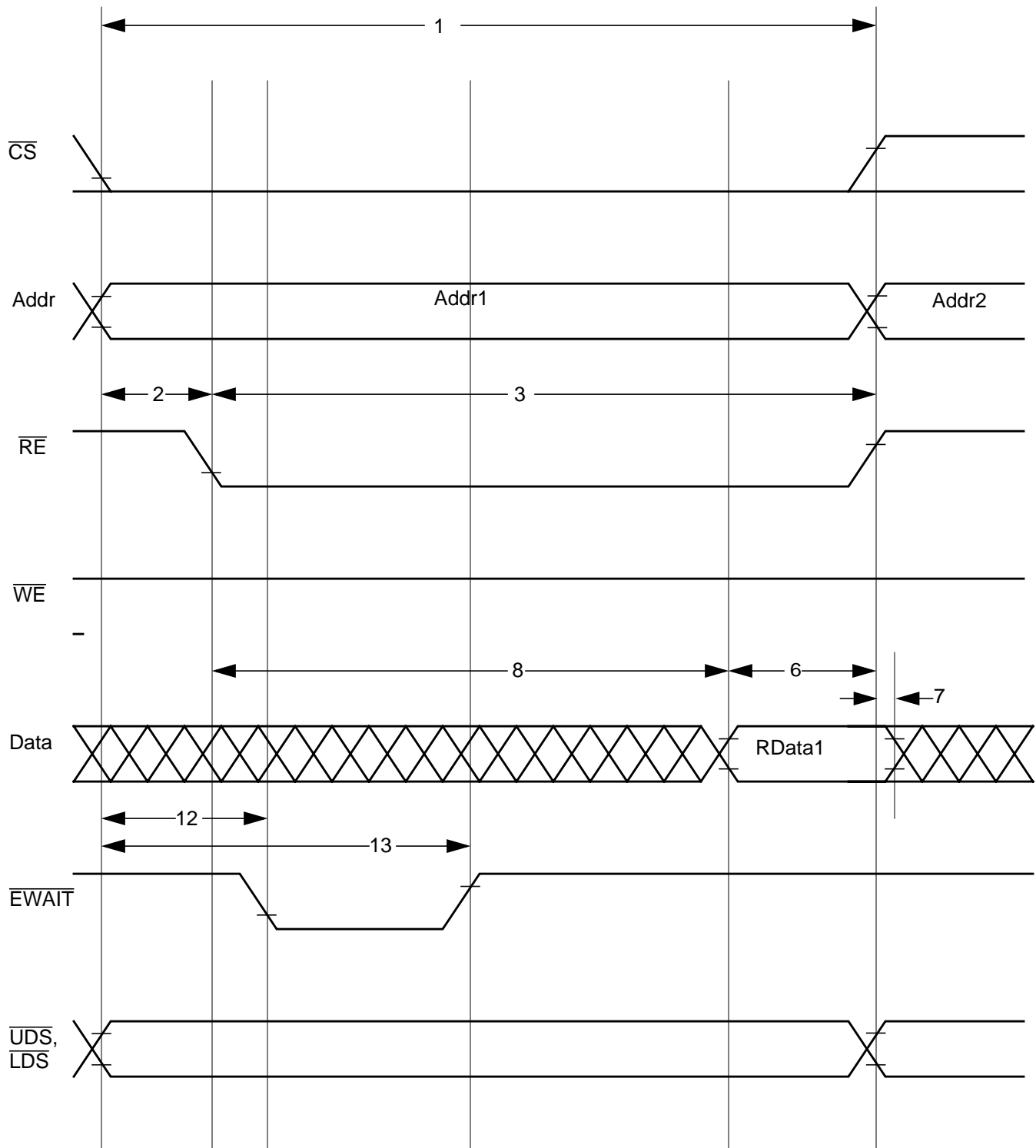
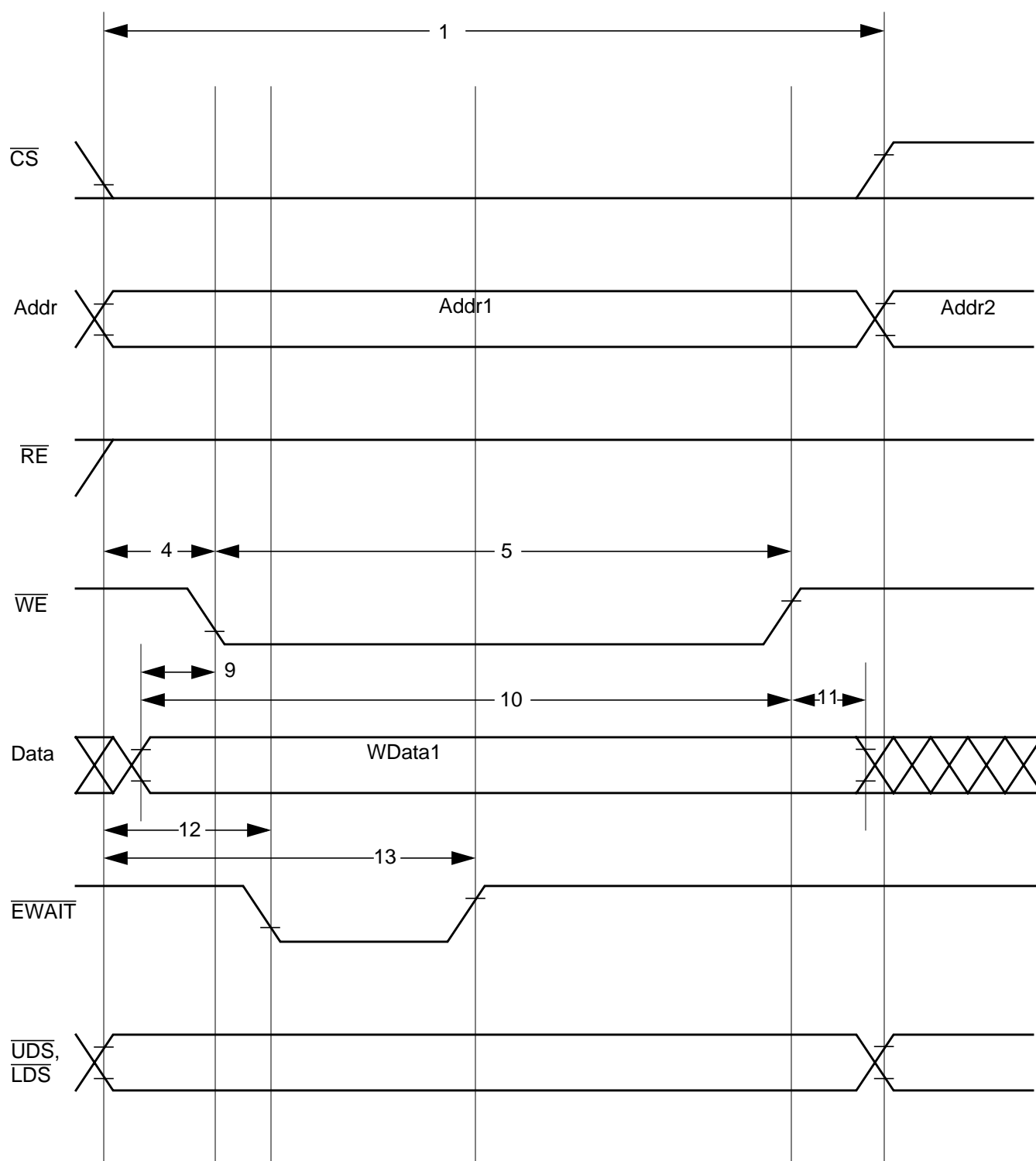**Figure 5-2 Timing Diagram: Normal Mode - Read with EWAIT**

Figure 5-3 Timing Diagram: Normal Mode - Write with EWAIT

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Table 5-2: Normal Mode Expansion Bus Timing with EWAIT

No.	Characteristic [1] [2] [3] [4]	Symbol	40 MHz 2 cycles stretch Min Max		40 MHz 3 cycles stretch Min Max		Unit
	Frequency of internal bus	f_i	D.C.	40.0	D.C.	40.0	MHz
	Internal cycle time	t_{cyc}	25		25		ns
	Frequency of external bus	f_o	D.C.	13.3	D.C.	10.0	MHz
	External cycle time (selected by ESTR)	t_{cyce}	75		100		ns
1	External cycle time (ESTR+1EWAIT)	t_{cycew}	100		125		ns
2	Address valid to $\overline{RE}$ fall	t_{ADRE}		15		15	ns
3	Pulse width, $\overline{RE}$ [5] (t_{cycew}-t_{ADRE})	PW_{RE}	85		110		ns
4	Address valid to $\overline{WE}$ fall	t_{ADWE}		15		15	ns
5	Pulse width, $\overline{WE}$ [5] t_{cycew}	PW_{WE}	73		98		ns
6	Read data setup time	t_{DSR}	24		24		ns
7	Read data hold time	t_{DHR}	0		0		ns
8	Read enable access time [5] (PW_{RE} - t_{DSR})	t_{ACCR}	71		86		ns
9	Write data valid to $\overline{WE}$ fall	t_{WDWE}	8		8		ns
10	Write data setup time [5] (PW_{WE} +t_{WDWE})	t_{DSW}	81		106		ns
11	Write data hold time	t_{DHW}	8		8		ns
12	Address to $\overline{EWAIT}$ fall	t_{ADWF}	0	20	0	45	ns
13	Address to $\overline{EWAIT}$ rise [6] t_{cyc}	t_{ADWR}	37	47	62	72	ns

NOTES:
1. Crystal input is required to be within 45% to 55% duty.
2. Reduced drive must be off to meet these timings.
3. Unequal loading of pins will affect relative timing numbers.
4. The following signals are approximately line on line (change at the same time): Addr, UDS, LDS, & CS.
5. Affected by $\overline{EWAIT}$.
6. These are the times $\overline{EWAIT}$ needs to be active for the internal strobe to detect it and add a cycle. Holding for additional cycles will cause the external bus to take additional cycles of WAIT.

5.3 Emulation Single-Chip Mode: External Bus with No Wait States

No wait state operation of the external bus is used in emulation single-chip and in special test mode. Making this timing work with external memory is a bit of a challenge. Using this mode to view internal

operation with a logic analyzer should be reasonable. The timing diagram for this operation is in **Figure 5-4** and the associated timing numbers are in **Table 5-3**.

Notes:

- Signals other than IVD, which are muxed with address will have the same timing as IVD.

- LSTR has the same timing as R/$\overline{W}$.

- ECLK2X rising edges are about line on line with ECLK edges.

- The timing for accesses to PRU registers, which take 2 cycles to complete, is the same as shown in **Figure 5-5** and **Figure 5-6** which show the timing for a read and write, respectively, with 1 cycle of stretch.
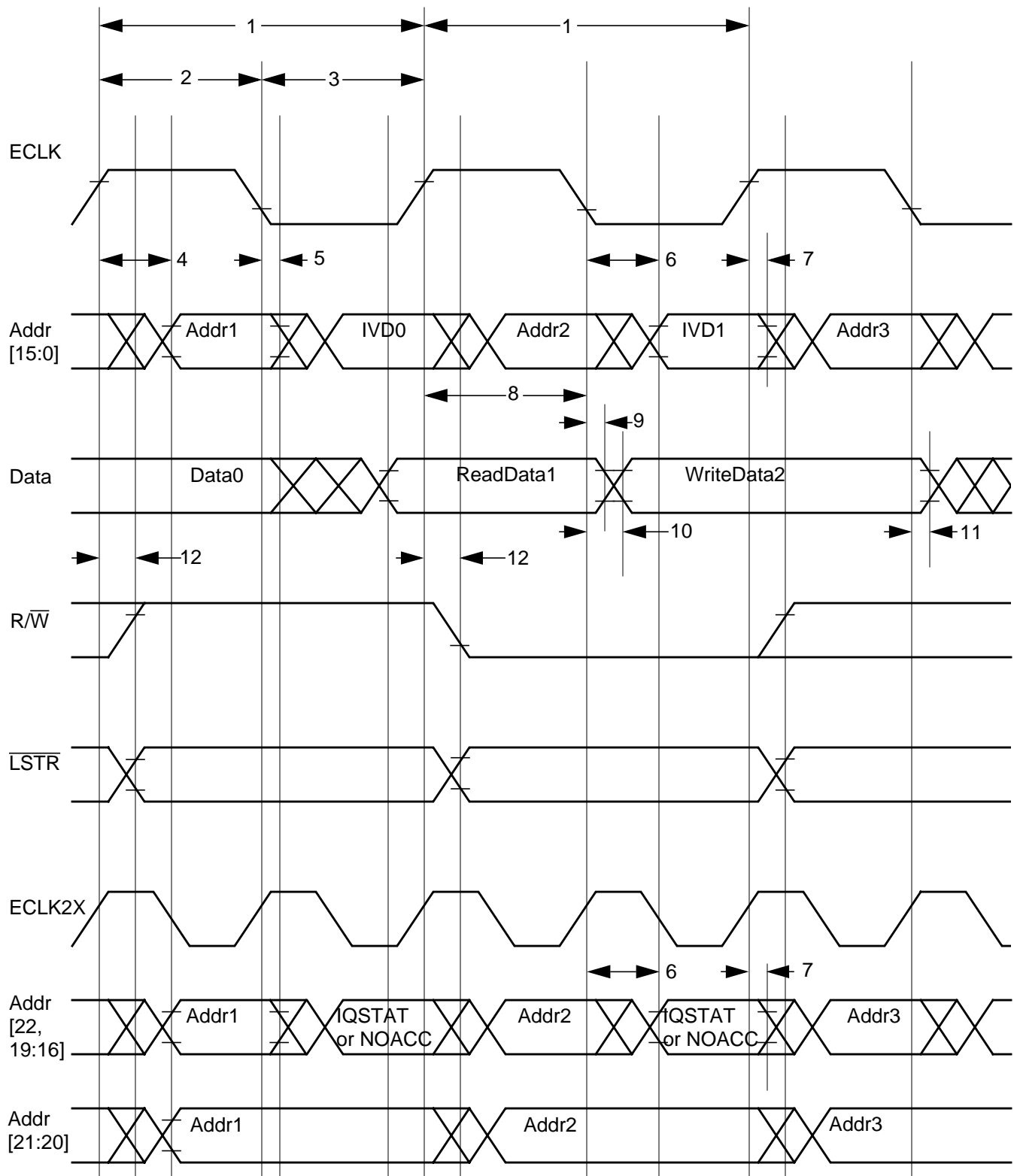
Figure 5-4 Timing Diagram: Emulation Single-Chip Mode - Read Followed by Write

Table 5-3: Emulation Single-Chip Mode Bus Timing - Typical Supply and Silicon, Room Temperature Only

Num	Characteristic [1] [2] [3]	Symbol	40 MHz Min	Max	Unit
	Frequency of internal bus	f_i	D.C.	40.0	MHz
1	Cycle time	t_{cyc}	25		ns
2	Pulse width, E high	PW_{EH}	11.5		ns
3	Pulse width, E low	PW_{EL}	11.5		ns
4	Address delay time	t_{AD}		5	ns
5	Address hold time	t_{AH}	0		ns
6	IVD delay time[4]	t_{IVDD}		4.5	ns
7	IVD hold time	t_{IVDH}	0		ns
8	Read data setup time	t_{DSR}	12		ns
9	Read data hold time	t_{DHR}	0		ns
10	Write data delay time	t_{DDW}		5	ns
11	Write data hold time	t_{DHW}	0		ns
12	Read/write data delay time	t_{RWD}	-1	5	ns

NOTES:
1. Crystal input is required to be within 45% to 55% duty.
2. Reduced drive must be off to meet these timings.
3. Unequal loading of pins will affect relative timing numbers.
4. Internal Visibility data is only brought out when the previous cycle was an internal read. On cycles where it is not brought out, address is held instead.

5.4 Emulation Expanded Mode: External Bus Wait State Capable

Designed to allow emulation of normal expanded mode, emulation expanded mode makes use of the earliest timing signals to allow external port replacement, external generation of selects and timing signals, and possible external emulation memory. If no stretch is imposed on the bus, the timing is the same as Emulation Single Chip shown in **Figure 5-4** and **Table 5-3**. The timing diagram for this operation when stretch is imposed is in **Figure 5-5** and **Figure 5-6**. These timing diagrams show a stretch of one cycle for read and write. The associated timing numbers are in **Table 5-4**.
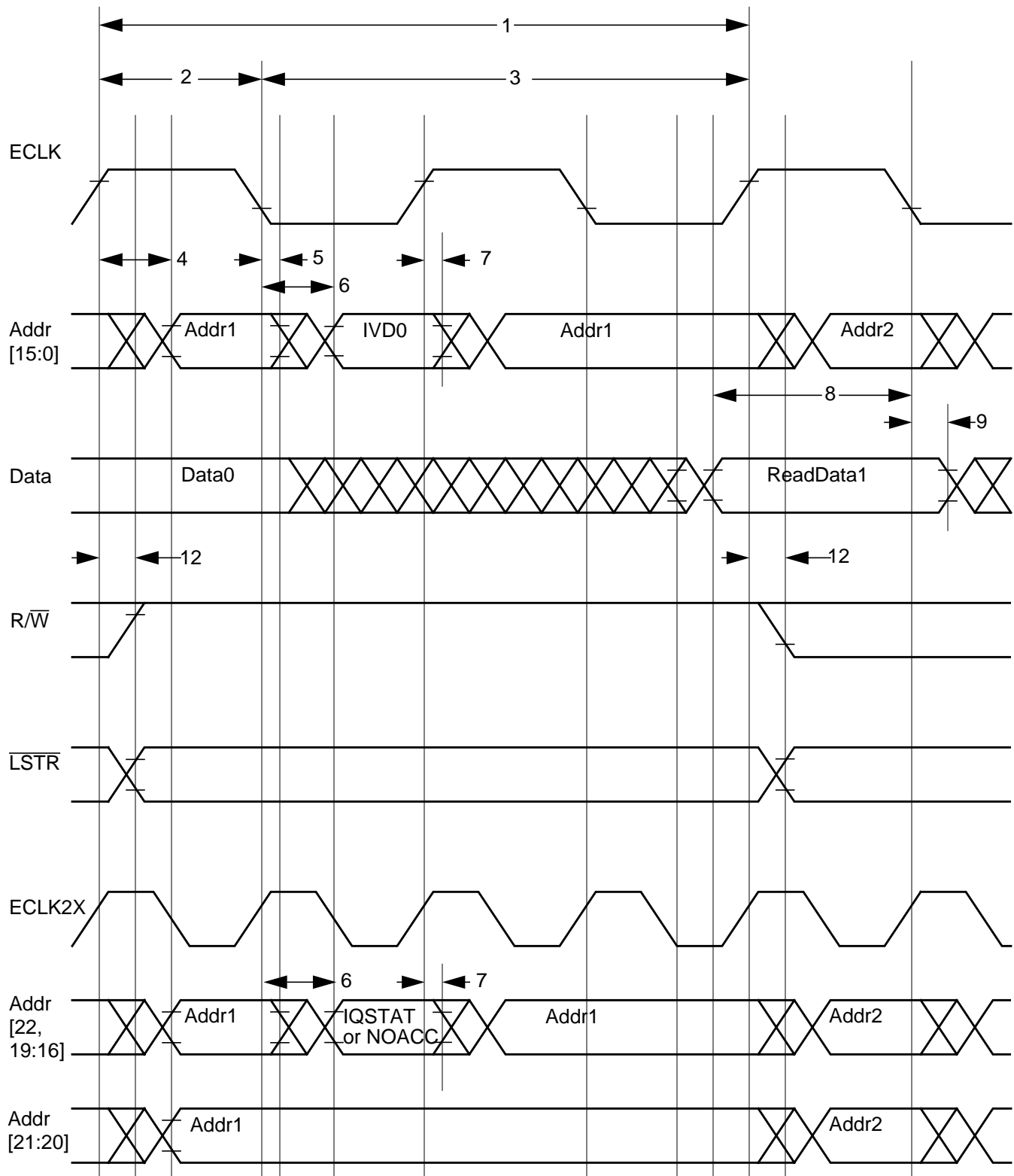
Figure 5-5 Timing Diagram: Emulation Expanded Mode - Read with One Cycle Stretch
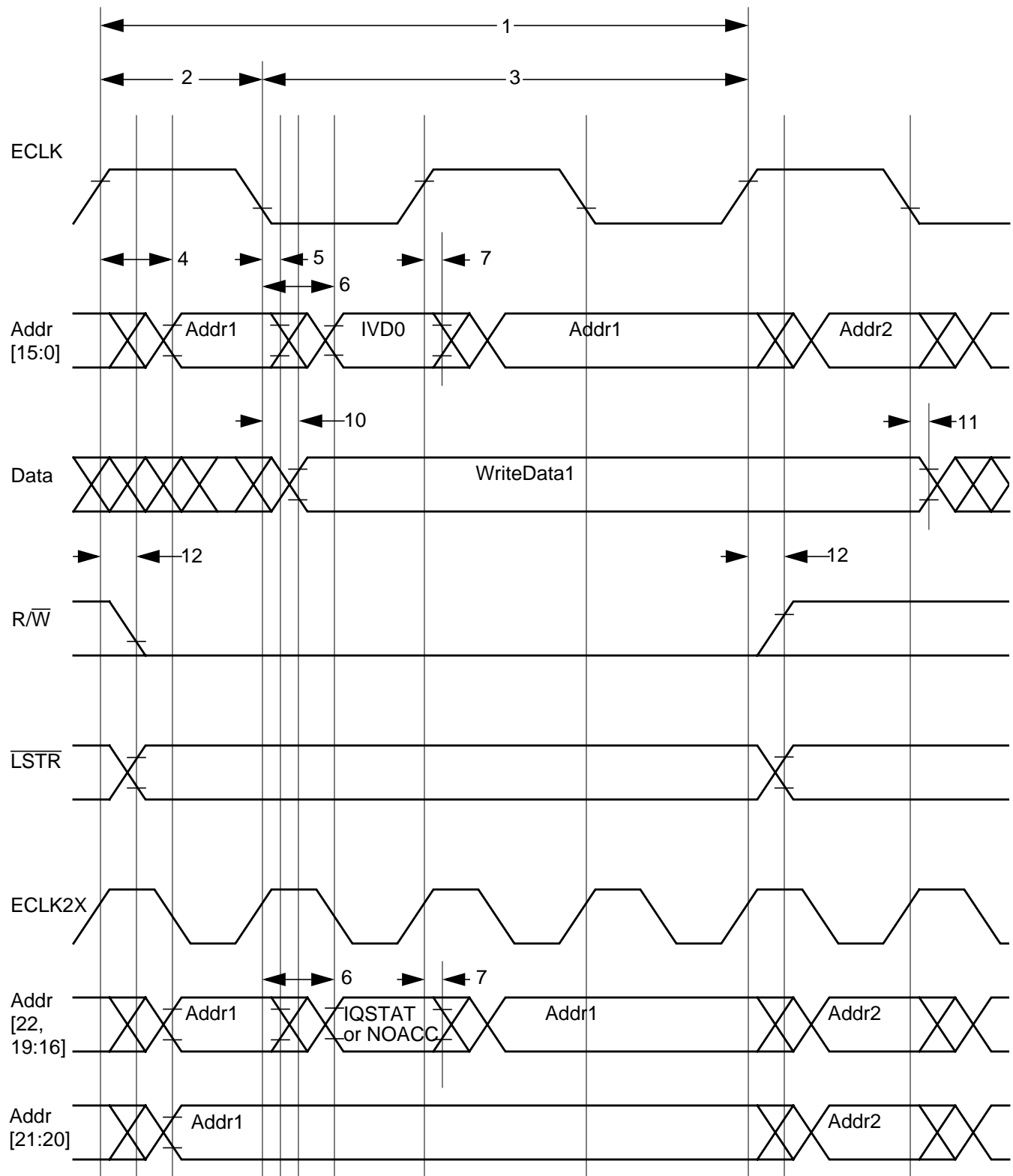
Figure 5-6 Timing Diagram: Emulation Expanded Mode - Write with One Cycle Stretch

Table 5-4: Emulation Expanded Mode Expansion Bus Timing - Typical Supply and Silicon, Room Temperature Only

No.	Characteristic [1] [2] [3] [4]	Symbol	40 MHz 1 cycle stretch Min	40 MHz 1 cycle stretch Max	40 MHz 2 cycles stretch Min	40 MHz 2 cycles stretch Max	40 MHz 3 cycles stretch Min	40 MHz 3 cycles stretch Max	Unit
	Internal cycle time	t_{cyc}	25	25	25	25	25	25	ns
1	Cycle time	t_{cyce}	50		75		100		ns
2	Pulse width, E high	PW_{EH}	11.5	14	11.5	14	11.5	14	ns
3	E falling to sampling E rising	t_{EFSR}	35	39.5	60	64.5	85	89.5	ns
4	Address delay time	t_{AD}		5		5		5	ns
5	Address hold time	t_{AH}	0		0		0		ns
6	IVD delay time[5]	t_{IVDD}		4.5		4.5		.54	ns
7	IVD hold time	t_{IVDH}	0		0		0		ns
8	Read data setup time	t_{DSR}	12		12		12		ns
9	Read data hold time	t_{DHR}	0		0		0		ns
10	Write data delay time	t_{DDW}		5		5		5	ns
11	Write data hold time	t_{DHW}	0		0		0		ns
12	Read/write data delay time	t_{RWD}	-1	5	-1	5	-1	5	ns

NOTES:

1. Crystal input is required to be within 45% to 55% duty.
2. Reduced drive must be off to meet these timings.
3. Unequal loading of pins will affect relative timing numbers.
4. The following signals are approximately line on line (change at the same time): Addr, UDS, LDS, & CS.
5. Internal Visibility data is only brought out when the previous cycle was an internal read. On cycles where it is not brought out, address is held instead.