PIM_9XDP512

Port Integration Module

Block Guide

V02.02

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Motorola, Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	03 Feb 2004	03 Feb 2004		Initial version.
V01.01	05 Apr 2004	05 Apr 2004		Renamed IVISDATA to IVD. Added I/O description to pin function table. Added info of reduced input threshold capability to specific pins. Added sensitivity to IRQ/XIRQ descriptions. Changed 'Upper/Lower Data Strobe' to '.. Select'.
V02.00	14 May 2004	14 May 2004		Added ECLKCTL register at address $001C. Detailed PRR descriptions.
V02.01	18 May 2004	18 May 2004		Removed "Controlled Copy" banners.
V02.02	30 Jul 2004	30 Jul 2004		Updated Expanded Bus Pin Functions table. Replaced NOACC with ACC[2:0]. Added CS3 output.

MOTOROLA

Table of Contents

MOTOROLA

Section 4 Functional Description

Section 5 Initialization/Application Information

List of Figures

MOTOROLA

List of Tables

Preface

Terminology

Acronyms and Abbreviations	
Logic level "1"	Voltage that corresponds to Boolean true state
Logic level "0"	Voltage that corresponds to Boolean false state
$	Represents hexadecimal number
x	Represents logic level 'don't care'
expanded modes	Normal Expanded Mode Emulation Single Chip Mode Emulation ExpandedMode Special Test Mode
single-chip modes	Normal Single Chip Mode Special Single Chip Mode
emulation modes	Emulation Single Chip Mode Emulation Expanded Mode
normal modes	Normal Single Chip Mode Normal Expanded Mode
special modes	Special Single Chip Mode Special Test Mode

Section 1 Introduction

1.1 Overview

The S12XD-family Port Integration Module establishes the interface between the peripheral modules including the non-multiplexed External Bus Interface module (S12X_EBI) and the I/O pins for all ports. It controls the electrical pin properties as well as the signal prioritization and multiplexing on shared pins.

This document covers the description of:

- Port A, B used as address output of the S12X_EBI

- Port C, D used as data I/O of the S12X_EBI

- Port E associated with the S12X_EBI control signals and the IRQ, XIRQ interrupt inputs

- Port K associated with address output and control signals of the S12X_EBI

- Port T connected to the Enhanced Capture Timer (ECT) module

- Port S associated with 2 SCI and 1 SPI modules

- Port M associated with 4 MSCAN modules and 1 SCI module

- Port P connected to the PWM and 2 SPI modules - inputs can be used as an external interrupt source

- Port H associated with 2 SCI modules - inputs can be used as an external interrupt source

- Port J associated with 1 MSCAN, 1 SCI and 2 IIC modules - inputs can be used as an external interrupt source

- Port AD0 and AD1 associated with one 8-channel and one 16-channel ATD module

Most I/O pins can be configured by register bits to select data direction and drive strength, to enable and select pull-up or pull-down devices. Interrupts can be enabled on specific pins resulting in status flags.

The I/O's of 2 MSCAN and all 3 SPI modules can be routed from their default location to alternative port pins.

> **NOTE:**   *The implementation of the S12XD-family Port Integration Module is device dependent. Therefore some functions are not available on certain derivatives or 112-pin and 80-pin package options.*

1.2 Features

A full-featured S12XD-family Port Integration Module includes these distinctive registers:

- Data and data direction registers for Ports A, B, C, D, E, K, T, S, M, P, H, J, AD0, and AD1 when used as general-purpose I/O

- Control registers to enable/disable pull-device and select pull-ups/pull-downs on Ports T, S, M, P, H, and J on per-pin basis

- Control registers to enable/disable pull-up devices on Ports AD0, and AD1 on per-pin basis

- Single control register to enable/disable pull-ups on Ports A, B, C, D, E, and K on per-port basis and on BKGD pin

- Control registers to enable/disable reduced output drive on Ports T, S, M, P, H, J, AD0, and AD1 on per-pin basis

- Single control register to enable/disable reduced output drive on Ports A, B, C, D, E, and K on per-port basis

- Control registers to enable/disable open-drain (wired-or) mode on Ports S and M

- Control registers to enable/disable pin interrupts on Ports P, H, and J

- Interrupt flag register for pin interrupts on Ports P, H, and J

- Control register to configure $\overline{\text{IRQ}}$ pin operation

- Free-running clock outputs

A standard port pin has the following minimum features:

- Input/output selection

- 5V output drive with two selectable drive strengths

- 5V digital and analog input

- Input with selectable pull-up or pull-down device

Optional features:

- Open drain for wired-or connections

- Interrupt inputs with glitch filtering

- Reduced input threshold to support low voltage applications

1.3 Block diagram

Figure 1-1 is a block diagram of the PIM_9XDP512.

- Signals shown in **Bold** are not available in 80-pin packages.

- Signals shown in ***Bold-Italics*** are neither available in 112-pin nor in 80-pin packages.

- Shaded labels denote alternative module routing ports.
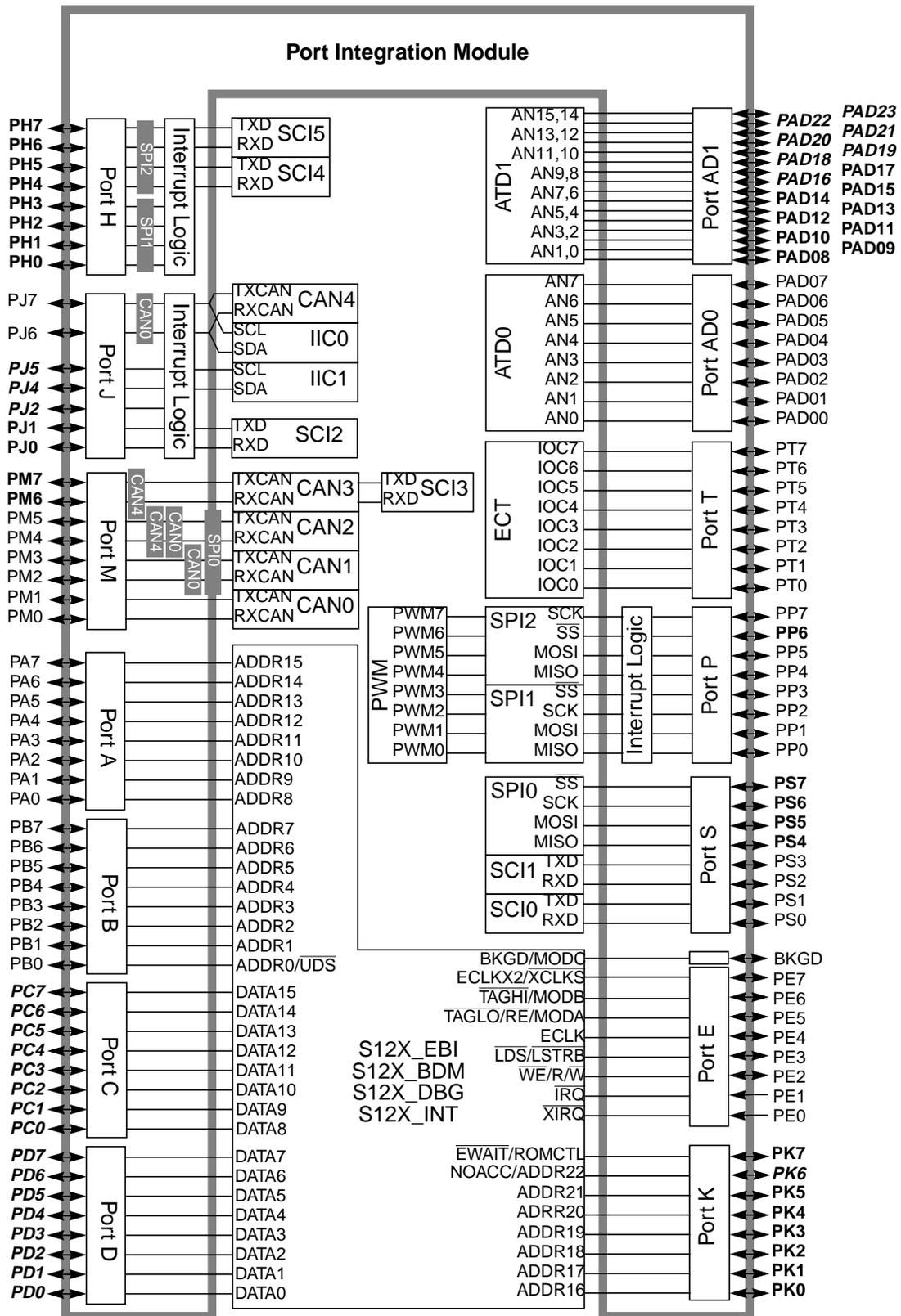
Figure 1-1 PIM_9XDP512 Block Diagram

Section 2 External Signal Description

2.1 Overview

This section lists and describes the signals that do connect off-chip.

2.2 Signal properties

Table 2-1 shows all the pins and their functions that are controlled by the PIM_9XDP512. *Refer to* **Section 4 Functional Description** *for the availability of the individual pins in the different package options.*

> **NOTE:** *If there is more than one function associated with a pin, the priority is indicated by the position in the table from top (highest priority) to bottom (lowest priority).*

Table 2-1 Pin Functions and Priorities

Port	Pin Name	Pin Function & Priority	I/O	Description	Pin Function after Reset
-	BKGD	MODC [1]	I	MODC input during $\overline{RESET}$	BKGD
		BKGD	I/O	S12X_BDM communication pin	
A	PA[7:0]	ADDR[15:8] mux IVD[15:8] [2]	O	High-order external bus address output (multiplexed with IVIS data)	Mode dependent [3]
		GPIO	I/O	General-purpose I/O	
B	PB[7:1]	ADDR[7:1] mux IVD[7:1] [2]	O	Low-order external bus address output (multiplexed with IVIS data)	Mode dependent [3]
		GPIO	I/O	General-purpose I/O	
	PB[0]	ADDR[0] mux IVD0 [2]	O	Low-order external bus address output (multiplexed with IVIS data)	
		$\overline{UDS}$	O	Upper data strobe	
		GPIO	I/O	General-purpose I/O	
C	PC[7:0]	DATA[15:8]	I/O	High-order bidirectional data input/output Configurable for reduced input threshold	Mode dependent [3]
		GPIO	I/O	General-purpose I/O	
D	PD[7:0]	DATA[7:0]	I/O	Low-order bidirectional data input/output Configurable for reduced input threshold	Mode dependent [3]
		GPIO	I/O	General-purpose I/O	

Port	Pin Name	Pin Function & Priority	I/O	Description	Pin Function after Reset
E	PE[7]	$\overline{\text{XCLKS}}$ [1]	I	External clock selection input during $\overline{\text{RESET}}$	Mode dependent [3]
		ECLKX2	I	Free-running clock output at Core Clock rate (ECLK x 2)	
		GPIO	I/O	General-purpose I/O	
	PE[6]	MODB [1]	I	MODB input during $\overline{\text{RESET}}$	
		$\overline{\text{TAGHI}}$	I	Instruction tagging low pin Configurable for reduced input threshold	
		GPIO	I/O	General-purpose I/O	
	PE[5]	MODA [1]	I	MODA input during $\overline{\text{RESET}}$	
		$\overline{\text{RE}}$	O	Read enable signal	
		$\overline{\text{TAGLO}}$	I	Instruction tagging low pin Configurable for reduced input threshold	
		GPIO	I/O	General-purpose I/O	
	PE[4]	ECLK	O	Free-running clock output at the Bus Clock rate or programmable divided in normal modes	
		GPIO	I/O	General-purpose I/O	
	PE[3]	EROMCTL [1]	I	EROMON bit control input during $\overline{\text{RESET}}$	
		$\overline{\text{LSTRB}}$	O	Low strobe bar output	
		$\overline{\text{LDS}}$	O	Lower data strobe	
		GPIO	I/O	General-purpose I/O	
	PE[2]	R/$\overline{\text{W}}$	O	Read/write output for external bus	
		$\overline{\text{WE}}$	O	Write enable signal	
		GPIO	I/O	General-purpose I/O	
	PE[1]	$\overline{\text{IRQ}}$	I	Maskable level- or falling edge-sensitive interrupt input	
		GPIO	I/O	General-purpose I/O	
	PE[0]	$\overline{\text{XIRQ}}$	I	Non-maskable level-sensitive interrupt input	
		GPIO	I/O	General-purpose I/O	
K	PK[7]	ROMCTL [1]	I	ROMON bit control input during $\overline{\text{RESET}}$	Mode dependent [3]
		$\overline{\text{EWAIT}}$	I	External Wait signal Configurable for reduced input threshold	
		GPIO	I/O	General-purpose I/O	
	PK[6:4]	ADDR[22:20] mux ACC[2:0] [2]	O	Extended external bus address output (multiplexed with access master output)	
		GPIO	I/O	General-purpose I/O	
	PK[3:0]	ADDR[19:16] mux IQSTAT[3:0] [2]	O	Extended external bus address output (multiplexed with instruction pipe status bits)	
		GPIO	I/O	General-purpose I/O	
T	PT[7:0]	IOC[7:0]	I/O	Enhanced Capture Timer Channels 7- 0 input/output	GPIO
		GPIO	I/O	General-purpose I/O	

Port	Pin Name	Pin Function & Priority	I/O	Description	Pin Function after Reset
S	PS7	$\overline{SS0}$	I/O	Serial Peripheral Interface 0 slave select output in master mode, input in slave mode or master mode.	GPIO
		GPIO	I/O	General-purpose I/O	
	PS6	SCK0	I/O	Serial Peripheral Interface 0 serial clock pin	
		GPIO	I/O	General-purpose I/O	
	PS5	MOSI0	I/O	Serial Peripheral Interface 0 master out/slave in pin	
		GPIO	I/O	General-purpose I/O	
	PS4	MISO0	I/O	Serial Peripheral Interface 0 master in/slave out pin	
		GPIO	I/O	General-purpose I/O	
	PS3	TXD1	O	Serial Communication Interface 1 transmit pin	
		GPIO	I/O	General-purpose I/O	
	PS2	RXD1	I	Serial Communication Interface 1 receive pin	
		GPIO	I/O	General-purpose I/O	
	PS1	TXD0	O	Serial Communication Interface 0 transmit pin	
		GPIO	I/O	General-purpose I/O	
	PS0	RXD0	I	Serial Communication Interface 0 receive pin	
		GPIO	I/O	General-purpose I/O	

Port	Pin Name	Pin Function & Priority	I/O	Description	Pin Function after Reset
M	PM7	TXCAN3	O	MSCAN3 transmit pin	GPIO
		TXCAN4	O	MSCAN4 transmit pin	
		TXD3	O	Serial Communication Interface 3 transmit pin	
		GPIO	I/O	General-purpose I/O	
	PM6	RXCAN3	I	MSCAN3 receive pin	
		RXCAN4	I	MSCAN4 receive pin	
		RXD3	I	Serial Communication Interface 3 receive pin	
		GPIO	I/O	General-purpose I/O	
	PM5	TXCAN2	O	MSCAN2 transmit pin	
		TXCAN0	O	MSCAN0 transmit pin	
		TXCAN4	O	MSCAN4 transmit pin	
		SCK0	I/O	Serial Peripheral Interface 0 serial clock pin *If CAN0 is routed to PM[3:2] the SPI0 can still be used in bidirectional master mode.*	
		GPIO	I/O	General-purpose I/O	
	PM4	RXCAN2	I	MSCAN2 receive pin	
		RXCAN0	I	MSCAN0 receive pin	
		RXCAN4	I	MSCAN4 receive pin	
		MOSI0	I/O	Serial Peripheral Interface 0 master out/slave in pin *If CAN0 is routed to PM[3:2] the SPI0 can still be used in bidirectional master mode.*	
		GPIO	I/O	General-purpose I/O	
	PM3	TXCAN1	O	MSCAN1 transmit pin	
		TXCAN0	O	MSCAN0 transmit pin	
		$\overline{SS0}$	I/O	Serial Peripheral Interface 0 slave select output in master mode, input for slave mode or master mode.	
		GPIO	I/O	General-purpose I/O	
	PM2	RXCAN1	I	MSCAN1 receive pin	
		RXCAN0	I	MSCAN0 receive pin	
		MISO0	I/O	Serial Peripheral Interface 0 master in/slave out pin	
		GPIO	I/O	General-purpose I/O	
	PM1	TXCAN0	O	MSCAN0 transmit pin	
		GPIO	I/O	General-purpose I/O	
	PM0	RXCAN0	I	MSCAN0 receive pin	
		GPIO	I/O	General-purpose I/O	

MOTOROLA

Port	Pin Name	Pin Function & Priority	I/O	Description	Pin Function after Reset
P	PP7	PWM7	I/O	Pulse Width Modulator input/output channel 7	GPIO
		SCK2	I/O	Serial Peripheral Interface 2 serial clock pin	
		GPIO/KWP7	I/O	General-purpose I/O with interrupt	
	PP6	PWM6	O	Pulse Width Modulator output channel 6	
		$\overline{SS2}$	I/O	Serial Peripheral Interface 2 slave select output in master mode, input for slave mode or master mode.	
		GPIO/KWP6	I/O	General-purpose I/O with interrupt	
	PP5	PWM5	O	Pulse Width Modulator output channel 5	
		MOSI2	I/O	Serial Peripheral Interface 2 master out/slave in pin	
		GPIO/KWP5	I/O	General-purpose I/O with interrupt	
	PP4	PWM4	O	Pulse Width Modulator output channel 4	
		MISO2	I/O	Serial Peripheral Interface 2 master in/slave out pin	
		GPIO/KWP4	I/O	General-purpose I/O with interrupt	
	PP3	PWM3	O	Pulse Width Modulator output channel 3	
		$\overline{SS1}$	I/O	Serial Peripheral Interface 1 slave select output in master mode, input for slave mode or master mode.	
		GPIO/KWP3	I/O	General-purpose I/O with interrupt	
	PP2	PWM2	O	Pulse Width Modulator output channel 2	
		SCK1	I/O	Serial Peripheral Interface 1 serial clock pin	
		GPIO/KWP2	I/O	General-purpose I/O with interrupt	
	PP1	PWM1	O	Pulse Width Modulator output channel 1	
		MOSI1	I/O	Serial Peripheral Interface 1 master out/slave in pin	
		GPIO/KWP1	I/O	General-purpose I/O with interrupt	
	PP0	PWM0	O	Pulse Width Modulator output channel 0	
		MISO1	I/O	Serial Peripheral Interface 1 master in/slave out pin	
		GPIO/KWP0	I/O	General-purpose I/O with interrupt	

Port	Pin Name	Pin Function & Priority	I/O	Description	Pin Function after Reset
H	PH7	$\overline{SS2}$	I/O	Serial Peripheral Interface 2 slave select output in master mode, input for slave mode or master mode	GPIO
		TXD5	O	Serial Communication Interface 5 transmit pin	
		GPIO/KWH7	I/O	General-purpose I/O with interrupt	
	PH6	SCK2	I/O	Serial Peripheral Interface 2 serial clock pin	
		RXD5	I	Serial Communication Interface 5 receive pin	
		GPIO/KWH6	I/O	General-purpose I/O with interrupt	
	PH5	MOSI2	I/O	Serial Peripheral Interface 2 master out/slave in pin	
		TXD4	O	Serial Communication Interface 4 transmit pin	
		GPIO/KWH5	I/O	General-purpose I/O with interrupt	
	PH4	MISO2	I/O	Serial Peripheral Interface 2 master in/slave out pin	
		RXD4	I	Serial Communication Interface 4 receive pin	
		GPIO/KWH4	I/O	General-purpose I/O with interrupt	
	PH3	$\overline{SS1}$	I/O	Serial Peripheral Interface 1 slave select output in master mode, input for slave mode or master mode.	
		GPIO/KWH3	I/O	General-purpose I/O with interrupt	
	PH2	SCK1	I/O	Serial Peripheral Interface 1 serial clock pin	
		GPIO/KWH2	I/O	General-purpose I/O with interrupt	
	PH1	MOSI1	I/O	Serial Peripheral Interface 1 master out/slave in pin	
		GPIO/KWH1	I/O	General-purpose I/O with interrupt	
	PH0	MISO1	I/O	Serial Peripheral Interface 1 master in/slave out pin	
		GPIO/KWH0	I/O	General-purpose I/O with interrupt	

Port	Pin Name	Pin Function & Priority	I/O	Description	Pin Function after Reset
J	PJ7	TXCAN4	O	MSCAN4 transmit pin	GPIO
		SCL0	O	Inter Integrated Circuit 0 serial clock line	
		TXCAN0	O	MSCAN0 transmit pin	
		GPIO/KWJ7	I/O	General-purpose I/O with interrupt	
	PJ6	RXCAN4	I	MSCAN4 receive pin	
		SDA0	I/O	Inter Integrated Circuit 0 serial data line	
		RXCAN0	I	MSCAN0 receive pin	
		GPIO/KWJ6	I/O	General-purpose I/O with interrupt	
	PJ5	SCL1	O	Inter Integrated Circuit 1 serial clock line	
		$\overline{CS2}$	O	Chip select 2	
		GPIO/KWJ7	I/O	General-purpose I/O with interrupt	
	PJ4	SDA1	I/O	Inter Integrated Circuit 1 serial data line	
		$\overline{CS0}$	O	Chip select 0	
		GPIO/KWJ6	I/O	General-purpose I/O with interrupt	
	PJ2	$\overline{CS1}$	O	Chip select 1	
		GPIO/KWJ2	I/O	General-purpose I/O with interrupt	
	PJ1	TXD2	O	Serial Communication Interface 2 transmit pin	
		GPIO/KWJ1	I/O	General-purpose I/O with interrupt	
	PJ0	RXD2	I	Serial Communication Interface 2 receive pin	
		$\overline{CS3}$	O	Chip select 3	
		GPIO/KWJ0	I/O	General-purpose I/O with interrupt	
AD0	PAD[07:00]	GPIO	I/O	General-purpose I/O	GPIO
		AN[7:0]	I	ATD0 analog inputs	
AD1	PAD[23:08]	GPIO	I/O	General-purpose I/O	GPIO
		AN[15:0]	I	ATD1 analog inputs	

NOTES:

1. Function active when $\overline{RESET}$ asserted.
2. Only available in emulation modes or in Special Test Mode with IVIS on.
3. Refer also to **Table 4-4** and S12X_EBI Block Guide.

Section 3 Memory Map/Register Definition

This section provides a detailed description of all PIM_9XDP512 registers.

3.1 Memory map

Table 3-1 shows the register map of the Port Integration Module.

Table 3-1 Memory Map

Address	Use	Access
$0000	Port A Data Register (PORTA)	Read / Write
$0001	Port B Data Register (PORTB)	Read / Write
$0002	Port A Data Direction Register (DDRA)	Read / Write
$0003	Port B Data Direction Register (DDRB)	Read / Write
$0004	Port C Data Register (PORTC)	Read / Write
$0005	Port D Data Register (PORTD)	Read / Write
$0006	Port C Data Direction Register (DDRC)	Read / Write
$0007	Port D Data Direction Register (DDRD)	Read / Write
$0008	Port E Data Register (PORTE)	Read / Write [1]
$0009	Port E Data Direction Register (DDRE)	Read / Write [1]
$000A : $000B	Non-PIM address range	-
$000C	Pull-up Up Control Register (PUCR)	Read / Write [1]
$000D	Reduced Drive Register (RDRIV)	Read / Write [1]
$000E : $001B	Non-PIM address range	-
$001C	ECLK Control Register (ECLKCTL)	Read / Write [1]
$001D	PIM Reserved	-
$001E	IRQ Control Register (IRQCR)	Read / Write [1]
$001F	PIM Reserved	-
$0020 : $0031	Non-PIM address range	-
$0032	Port K Data Register (PORTK)	Read / Write
$0033	Port K Data Direction Register (DDRK)	Read / Write
$0034 : $023F	Non-PIM address range	-
$0240	Port T Data Register (PTT)	Read / Write
$0241	Port T Input Register (PTIT)	Read
$0242	Port T Data Direction Register (DDRT)	Read / Write
$0243	Port T Reduced Drive Register (RDRT)	Read / Write
$0244	Port T Pull Device Enable Register (PERT)	Read / Write
$0245	Port T Polarity Select Register (PPST)	Read / Write

$0246	Reserved	-
$0247	Reserved	-
$0248	Port S Data Register (PTS)	Read / Write
$0249	Port S Input Register (PTIS)	Read
$024A	Port S Data Direction Register (DDRS)	Read / Write
$024B	Port S Reduced Drive Register (RDRS)	Read / Write
$024C	Port S Pull Device Enable Register (PERS)	Read / Write
$024D	Port S Polarity Select Register (PPSS)	Read / Write
$024E	Port S Wired-Or Mode Register (WOMS)	Read / Write
$024F	Reserved	-
$0250	Port M Data Register (PTM)	Read / Write
$0251	Port M Input Register (PTIM)	Read
$0252	Port M Data Direction Register (DDRM)	Read / Write
$0253	Port M Reduced Drive Register (RDRM)	Read / Write
$0254	Port M Pull Device Enable Register (PERM)	Read / Write
$0255	Port M Polarity Select Register (PPSM)	Read / Write
$0256	Port M Wired-Or Mode Register (WOMM)	Read / Write
$0257	Module Routing Register (MODRR)	Read / Write
$0258	Port P Data Register (PTP)	Read / Write
$0259	Port P Input Register (PTIP)	Read
$025A	Port P Data Direction Register (DDRP)	Read / Write
$025B	Port P Reduced Drive Register (RDRP)	Read / Write
$025C	Port P Pull Device Enable Register (PERP)	Read / Write
$025D	Port P Polarity Select Register (PPSP)	Read / Write
$025E	Port P Interrupt Enable Register (PIEP)	Read / Write
$025F	Port P Interrupt Flag Register (PIFP)	Read / Write
$0260	Port H Data Register (PTH)	Read / Write
$0261	Port H Input Register (PTIH)	Read
$0262	Port H Data Direction Register (DDRH)	Read / Write
$0263	Port H Reduced Drive Register (RDRH)	Read / Write
$0264	Port H Pull Device Enable Register (PERH)	Read / Write
$0265	Port H Polarity Select Register (PPSH)	Read / Write
$0266	Port H Interrupt Enable Register (PIEH)	Read / Write
$0267	Port H Interrupt Flag Register (PIFH)	Read / Write
$0268	Port J Data Register (PTJ)	Read / Write [1]
$0269	Port J Input Register (PTIJ)	Read
$026A	Port J Data Direction Register (DDRJ)	Read / Write [1]
$026B	Port J Reduced Drive Register (RDRJ)	Read / Write [1]
$026C	Port J Pull Device Enable Register (PERJ)	Read / Write [1]
$026D	Port J Polarity Select Register (PPSJ)	Read / Write [1]
$026E	Port J Interrupt Enable Register (PIEJ)	Read / Write [1]
$026F	Port J Interrupt Flag Register (PIFJ)	Read / Write [1]
$0270	Reserved	-
$0271	Port AD0 Data Register 1 (PT1AD0)	Read / Write
$0272	Reserved	-

$0273	Port AD0 Data Direction Register 1 (DDR1AD0)	Read / Write
$0274	Reserved	-
$0275	Port AD0 Reduced Drive Register 1 (RDR1AD0)	Read / Write
$0276	Reserved	-
$0277	Port AD0 Pull Up Enable Register 1 (PER1AD0)	Read / Write
$0278	Port AD1 Data Register 0 (PT0AD1)	Read / Write
$0279	Port AD1 Data Register 1 (PT1AD1)	Read / Write
$027A	Port AD1 Data Direction Register 0 (DDR0AD1)	Read / Write
$027B	Port AD1 Data Direction Register 1 (DDR1AD1)	Read / Write
$027C	Port AD1 Reduced Drive Register 0 (RDR0AD1)	Read / Write
$027D	Port AD1 Reduced Drive Register 1 (RDR1AD1)	Read / Write
$027E	Port AD1 Pull Up Enable Register 0 (PER0AD1)	Read / Write
$027F	Port AD1 Pull Up Enable Register 1 (PER1AD1)	Read / Write

NOTES:

1. Write access not applicable for one or more register bits. *Refer to register description.*

MOTOROLA

3.2 Register descriptions

The following table summarizes the effect on the various configuration bits, data direction (DDR), output level (IO), reduced drive (RDR), pull enable (PE), pull select (PS) and interrupt enable (IE) for the ports.

The configuration bit PS is used for two purposes:

1. Configure the sensitive interrupt edge (rising or falling), if interrupt is enabled.
2. Select either a pull-up or pull-down device if PE is active.

Table 3-2 Pin Configuration Summary

DDR	IO	RDR	PE	PS [1]	IE [2]	Function	Pull Device	Interrupt
0	X	X	0	X	0	Input	Disabled	Disabled
0	X	X	1	0	0	Input	Pull Up	Disabled
0	X	X	1	1	0	Input	Pull Down	Disabled
0	X	X	0	0	1	Input	Disabled	Falling edge
0	X	X	0	1	1	Input	Disabled	Rising edge
0	X	X	1	0	1	Input	Pull Up	Falling edge
0	X	X	1	1	1	Input	Pull Down	Rising edge
1	0	0	X	X	0	Output, full drive to 0	Disabled	Disabled
1	1	0	X	X	0	Output, full drive to 1	Disabled	Disabled
1	0	1	X	X	0	Output, reduced drive to 0	Disabled	Disabled
1	1	1	X	X	0	Output, reduced drive to 1	Disabled	Disabled
1	0	0	X	0	1	Output, full drive to 0	Disabled	Falling edge
1	1	0	X	1	1	Output, full drive to 1	Disabled	Rising edge
1	0	1	X	0	1	Output, reduced drive to 0	Disabled	Falling edge
1	1	1	X	1	1	Output, reduced drive to 1	Disabled	Rising edge

NOTES:
1. Always "0" on Port A, B, C, D, E, K, AD0, and AD1.
2. Applicable only on Port P, H and J.

NOTE: *All register bits in this module are completely synchronous to internal clocks during a register read.*

3.2.1 Port A Data Register (PORTA)

Address Offset: $0000 (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Alt. Func.:	ADDR15 mux IVD15	ADDR14 mux IVD14	ADDR13 mux IVD13	ADDR12 mux IVD12	ADDR11 mux IVD11	ADDR10 mux IVD10	ADDR9 mux IVD9	ADDR8 mux IVD8
Reset:	0	0	0	0	0	0	0	0

[ ] = Reserved or unimplemented

Figure 3-1 Port A Data Register (PORTA)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data source is depending on the data direction value.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

Port A pins 7 through 0 are associated with address outputs ADDR15 through ADDR8 respectively in expanded modes. When this port is not used for external addresses, these pins can be used as general purpose I/O.

If the data direction bits of the associated I/O pins are set to logic level "1", a read returns the value of the port register, otherwise the buffered pin input state is read.

3.2.2 Port B Data Register (PORTB)

Address Offset: $0001 (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Alt. Func.:	ADDR7 mux IVD7	ADDR6 mux IVD6	ADDR5 mux IVD5	ADDR4 mux IVD4	ADDR3 mux IVD3	ADDR2 mux IVD2	ADDR1 mux IVD1	ADDR0 mux IVD0 or $\overline{UDS}$
Reset:	0	0	0	0	0	0	0	0

[ ] = Reserved or unimplemented

Figure 3-2 Port B Data Register (PORTB)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data source is depending on the data direction value.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

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Port B pins 7 through 1 are associated with address outputs ADDR7 through ADDR1 respectively in expanded modes. Pin 0 is associated with output ADDR0 in emulation modes and special test mode and with Upper Data Select ($\overline{UDS}$) in normal expanded mode. When this port is not used for external addresses, these pins can be used as general purpose I/O.

If the data direction bits of the associated I/O pins are set to logic level "1", a read returns the value of the port register, otherwise the buffered pin input state is read.

3.2.3 Port A Data Direction Register (DDRA)

Address Offset: $0002 (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-3 Port A Data Direction Register (DDRA)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data are read from this register.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

This register controls the data direction for Port A. When Port A is operating as a general purpose I/O port, DDRA determines whether each pin is an input or output. A logic level "1" causes the associated port pin to be an output and a logic level "0" causes the associated pin to be a high-impedance input.

DDRA[7:0] — Data Direction Port A
    1 = Associated pin is configured as output.
    0 = Associated pin is configured as input.

> **NOTE:** *Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PORTA after changing the DDRA register.*

3.2.4 Port B Data Direction Register (DDRB)

Address Offset: $0003 (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Reset:	0	0	0	0	0	0	0	0
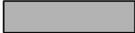
= Reserved or unimplemented

Figure 3-4 Port B Data Direction Register (DDRB)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data are read from this register.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

This register controls the data direction for Port B. When Port B is operating as a general purpose I/O port, DDRB determines whether each pin is an input or output. A logic level "1" causes the associated port pin to be an output and a logic level "0" causes the associated pin to be a high-impedance input.

DDRB[7:0] — Data Direction Port B
      1 = Associated pin is configured as output.
      0 = Associated pin is configured as input.

NOTE: *Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PORTB after changing the DDRB register.*

3.2.5 Port C Data Register (PORTC)

Address Offset: $0004 (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Exp.:	DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8
Reset:	0	0	0	0	0	0	0	0

                 = Reserved or unimplemented

Figure 3-5 Port C Data Register (PORTC)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data source is depending on the data direction value.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus..

Port C pins 7 through 0 are associated with data I/O lines DATA15 through DATA8 respectively in expanded modes. When this port is not used for external data, these pins can be used as general purpose I/O.

If the data direction bits of the associated I/O pins are set to logic level "1", a read returns the value of the port register, otherwise the buffered pin input state is read.

3.2.6 Port D Data Register (PORTD)

Address Offset: $0005 (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Exp.:	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented

Figure 3-6 Port D Data Register (PORTD)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data source is depending on the data direction value.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

Port D pins 7 through 0 are associated with data I/O lines DATA7 through DATA0 respectively in expanded modes. When this port is not used for external data, these pins can be used as general purpose I/O.

If the data direction bits of the associated I/O pins are set to logic level "1", a read returns the value of the port register, otherwise the buffered pin input state is read.

3.2.7 Port C Data Direction Register (DDRC)

Address Offset: $0006 (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented

Figure 3-7 Port C Data Direction Register (DDRC)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data are read from this register.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

This register controls the data direction for Port C. When Port C is operating as a general purpose I/O port, DDRC determines whether each pin is an input or output. A logic level "1" causes the associated port pin to be an output and a logic level "0" causes the associated pin to be a high-impedance input.

DDRC[7:0] — Data Direction Port C
      1 = Associated pin is configured as output.
      0 = Associated pin is configured as input.

> **_NOTE:_** _Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PORTC after changing the DDRC register._

3.2.8 Port D Data Direction Register (DDRD)

Address Offset: $0007 (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
Reset:	0	0	0	0	0	0	0	0

               = Reserved or unimplemented

Figure 3-8 Port D Data Direction Register (DDRD)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data are read from this register.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

This register controls the data direction for Port D. When Port D is operating as a general purpose I/O port, DDRD determines whether each pin is an input or output. A logic level "1" causes the associated port pin to be an output and a logic level "0" causes the associated pin to be a high-impedance input.

DDRD[7:0] — Data Direction Port D
      1 = Associated pin is configured as output.
      0 = Associated pin is configured as input.

> **_NOTE:_** _Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PORTD after changing the DDRD register._

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3.2.9 Port E Data Register (PORTE)

Address Offset: $0008 (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Alt. Func.:	$\overline{\text{XCLKS}}$ or ECLKX2	MODB or $\overline{\text{TAGHI}}$	MODA or $\overline{\text{RE}}$ or $\overline{\text{TAGLO}}$	ECLK	EROMCTL or $\overline{\text{LSTRB}}$ or $\overline{\text{LDS}}$	R/$\overline{\text{W}}$ or $\overline{\text{WE}}$	$\overline{\text{IRQ}}$	$\overline{\text{XIRQ}}$
Reset:	0	0	0	0	0	0	-[1]	-[1]

☐ = Reserved or unimplemented

NOTES:

1. These registers are reset to zero. Two bus clock cycles after reset release the register values are updated with the associated pin values.

Figure 3-9 Port E Data Register (PORTE)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data source is depending on the data direction value.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

Port E bits 7 through 0 are associated with external bus control signals and interrupt inputs. These include mode select (MODB, MODA), E clock, double frequency E clock, Instruction Tagging High and Low ($\overline{\text{TAGHI}}$, $\overline{\text{TAGLO}}$), Read/Write (R/$\overline{\text{W}}$), Read Enable and Write Enable ($\overline{\text{RE}}$, $\overline{\text{WE}}$), Lower Data Select ($\overline{\text{LDS}}$), $\overline{\text{IRQ}}$, and $\overline{\text{XIRQ}}$.

When not used for any of these specific functions, Port E pins 7-2 can be used as general purpose I/O and pins 1-0 can be used as general purpose inputs.

If the data direction bits of the associated I/O pins are set to logic level "1", a read returns the value of the port register, otherwise the buffered pin input state is read.

Pins 6 and 5 are inputs with enabled pull-down devices while RESET pin is low.

Pins 7 and 3 are inputs with enabled pull-up devices while RESET pin is low.

3.2.10 Port E Data Direction Register (DDRE)

Address Offset: $0009 (PRR)

|	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRE7	DDRE6	DDRE5	DDRE4	DDRE3	DDRE2	0	0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented

Figure 3-10 Port E Data Direction Register (DDRE)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data are read from this register.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

This register controls the data direction for Port E. When Port E is operating as a general purpose I/O port, DDRE determines whether each pin is an input or output. A logic level "1" causes the associated port pin to be an output and a logic level "0" causes the associated pin to be a high-impedance input.

Port E bit 1 (associated with $\overline{\text{IRQ}}$) and bit 0 (associated with $\overline{\text{XIRQ}}$) cannot be configured as outputs. Port E, bits 1 and 0, can be read regardless of whether the alternate interrupt function is enabled.

DDRE[7:2]   Data Direction Port E
      1 = Associated pin is configured as output.
      0 = Associated pin is configured as input.

> **NOTE:**   *Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PORTE after changing the DDRE register.*

3.2.11 S12X_EBI ports, BKGD, VREGEN pin Pull-up Control Register (PUCR)

Address Offset: $000C (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PUPKE	BKPUE	0	PUPEE	PUPDE	PUPCE	PUPBE	PUPAE
Reset:	1	1	0	1	0	0	0	0

[   ] = Reserved or unimplemented
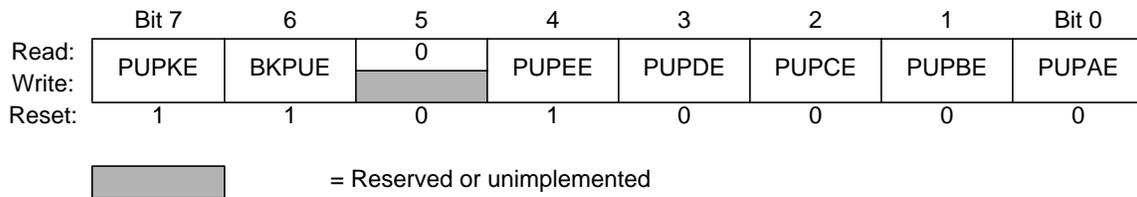
Figure 3-11 S12X_EBI ports, BKGD, VREGEN pin Pull-up Control Register (PUCR)

Read: Anytime in single-chip modes.

Write: Anytime, except BKPUE which is writable in Special Test Mode only.

This register is used to enable pull-up devices for the associated ports A, B, C, D, E, and K. Pull-up devices are assigned on a per-port basis and apply to any pin in the corresponding port that is currently configured as an input.

PUPKE - Pull-up Port K Enable
      1 = Enable pull-up devices for Port K input pins.
      0 = Port K pull-up devices are disabled.

BKPUE - BKGD and VREGEN pin pull-up enable
      1 = Enable pull-up devices on BKGD and VREGEN pins.
      0 = BKGD and VREGEN pull-up devices are disabled.

PUPEE - Pull-up Port E Enable
      1 = Enable pull-up devices for Port E input pins bits 7, 4-0.
      0 = Port E pull-up devices on bit 7, 4-0 are disabled.

NOTE: *Bits 5 and 6 of Port E have pull-down devices which are only enabled during reset.*
This bit has no effect on these pins.

PUPDE - Pull-up Port D Enable
　　　1 = Enable pull-up devices for all Port D input pins.
　　　0 = Port D pull-up devices are disabled.

PUPCE - Pull-up Port C Enable
　　　1 = Enable pull-up devices for all Port C input pins.
　　　0 = Port C pull-up devices are disabled.

PUPBE - Pull-up Port B Enable
　　　1 = Enable pull-up devices for all Port B input pins.
　　　0 = Port B pull-up devices are disabled.

PUPAE - Pull-up Port A Enable
　　　1 = Enable pull-up devices for all Port A input pins.
　　　0 = Port A pull-up devices are disabled.

3.2.12 S12X_EBI ports Reduced Drive Register (RDRIV)

Address Offset: $000D (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RDPK	0	0	RDPE	RDPD	RDPC	RDPB	RDPA
Write:	RDPK			RDPE	RDPD	RDPC	RDPB	RDPA
Reset:	0	0	0	0	0	0	0	0

　　　　　　　　　　= Reserved or unimplemented

Figure 3-12 S12X_EBI ports Reduced Drive Register (RDRIV)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data are read from this register.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

This register is used to select reduced drive for the pins associated with the S12X_EBI ports A, B, C, D, E, and K. If enabled, the pins drive at about 1/6 of the full drive strength. The reduced drive function is independent of which function is being used on a particular pin.

The reduced drive functionality does not take effect on the pins in emulation modes.

RDPK - Reduced Drive of Port K
　　　1 = All Port K output pins have reduced drive enabled.
　　　0 = All Port K output pins have full drive enabled.

RDPE - Reduced Drive of Port E
　　　1 = All Port E output pins have reduced drive enabled.
　　　0 = All Port E output pins have full drive enabled.

RDPD - Reduced Drive of Port D

      1 = All Port D output pins have reduced drive enabled.

      0 = All Port D output pins have full drive enabled.

RDPC - Reduced Drive of Port C

      1 = All Port C output pins have reduced drive enabled.

      0 = All Port C output pins have full drive enabled.

RDPB - Reduced Drive of Port B

      1 = All Port B output pins have reduced drive enabled.

      0 = All Port B output pins have full drive enabled.

RDPA - Reduced Drive of Ports A

      1 = All Port A output pins have reduced drive enabled.

      0 = All Port A output pins have full drive enabled.

3.2.13 ECLK Control Register (ECLKCTL)

Address Offset: $001C (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0	
Read:	NECLK	NCLKX2	0	0	0	0	EDIV1	EDIV0	
Write:							EDIV1	EDIV0	
Reset[1]:	(mode depend-dent)	1	0	0	0	0	0	0	Mode
SS	0	1	0	0	0	0	0	0	Special Single-Chip
ES	1	1	0	0	0	0	0	0	Emulation Single-Chip
ST	0	1	0	0	0	0	0	0	Special Test
EX	0	1	0	0	0	0	0	0	Emulation Expanded
NS	1	1	0	0	0	0	0	0	Normal Single-Chip
NX	0	1	0	0	0	0	0	0	Normal Expanded

         = Reserved or unimplemented

NOTES:

1. Reset values in emulation modes are identical to those of the target mode.

**Figure 3-13 ECLK Control Register (ECLKCTL)**

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data are read from this register.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

The ECLKCTL register is used to control the availability of the free-running clocks and the free-running clock divider.

NECLK — No ECLK

This bit controls the availability of a free-running clock on the ECLK pin.

Clock output is always active in emulation modes and if enabled in all other operating modes.
1 = ECLK disabled
0 = ECLK enabled

NCLKX2 — No ECLKX2

This bit controls the availability of a free-running clock on the ECLKX2 pin. This clock has a fixed rate of twice the internal Bus Clock.

Clock output is always active in emulation modes and if enabled in all other operating modes.
1 = ECLKX2 is disabled
0 = ECLKX2 is enabled

EDIV1, EDIV0 — Free-running ECLK Divider

These bits determine the rate of the free-running clock on the ECLK pin. The usage of the bits is shown in **Table 3-3**.

Divider is always disabled in emulation modes and active as programmed in all other operating modes.

Table 3-3 Free-Running ECLK Clock Rate

EDIV[1:0]	Rate of Free-Running ECLK
00	ECLK = Bus Clock rate
01	ECLK = Bus Clock rate divided by 2
10	ECLK = Bus Clock rate divided by 3
11	ECLK = Bus Clock rate divided by 4

3.2.14 IRQ Control Register (IRQCR)

Address Offset: $001E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQE	IRQEN	0	0	0	0	0	0
Write:								
Reset:	0	1	0	0	0	0	0	0

= Reserved or unimplemented
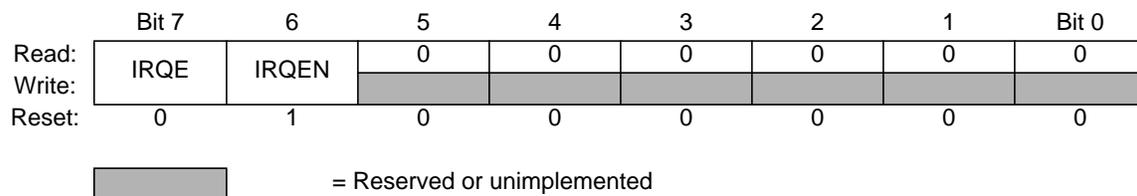
Figure 3-14 IRQ Control Register (IRQCR)

Read: See individual bit descriptions below.

Write: See individual bit descriptions below.

IRQE - IRQ select edge sensitive only

Special modes: Read or write anytime.

Normal & emulation modes: Read anytime, write once.

1 = $\overline{\text{IRQ}}$ configured to respond only to falling edges. Falling edges on the $\overline{\text{IRQ}}$ pin will be detected anytime IRQE = 1 and will be cleared only upon a reset or the servicing of the $\overline{\text{IRQ}}$ interrupt.

0 = $\overline{\text{IRQ}}$ configured for low level recognition.

IRQEN - External IRQ enable

Read or write anytime.

1 = External $\overline{\text{IRQ}}$ pin is connected to interrupt logic.

0 = External $\overline{\text{IRQ}}$ pin is disconnected from interrupt logic.

3.2.15 Port K Data Register (PORTK)

Address Offset: $0032 (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0
Alt. Func.:	ROMCTL or $\overline{\text{EWAIT}}$	ADDR22 mux NOACC	ADDR21	ADDR20	ADDR19 mux IQSTAT3	ADDR18 mux IQSTAT2	ADDR17 mux IQSTAT1	ADDR16 mux IQSTAT0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented

Figure 3-15 Port K Data Register (PORTK)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data source is depending on the data direction value.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

Port K pins 7 through 0 are associated with external bus control signals and internal memory expansion emulation pins. These include ADDR22-ADDR16, No-Access (NOACC), External Wait ($\overline{\text{EWAIT}}$) and instruction pipe signals IQSTAT3-IQSTAT0. Bits 6-0 carry the external addresses in all expanded modes. In emulation or special test mode with internal visibility enabled the address is multiplexed with the alternate functions NOACC and IQSTAT on the respective pins. In single-chip modes the port pins can be used as general-purpose I/O.

If the data direction bits of the associated I/O pins are set to logic level "1", a read returns the value of the port register, otherwise the buffered pin input state is read.

3.2.16 Port K Data Direction Register (DDRK)

Address Offset: $0033 (PRR)

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRK7	DDRK6	DDRK5	DDRK4	DDRK3	DDRK2	DDRK1	DDRK0
Reset:	0	0	0	0	0	0	0	0

　 = Reserved or unimplemented

Figure 3-16 Port K Data Direction Register (DDRK)

Read: Anytime. In emulation modes, read operations will return the data from the external bus, in all other modes the data are read from this register.

Write: Anytime. In emulation modes, write operations will also be directed to the external bus.

This register controls the data direction for Port K. When Port K is operating as a general purpose I/O port, DDRK determines whether each pin is an input or output. A logic level "1" causes the associated port pin to be an output and a logic level "0" causes the associated pin to be a high-impedance input.

DDRK[7:0]   Data Direction Port K
　　 1 = Associated pin is configured as output.
　　 0 = Associated pin is configured as input.

> **NOTE:** *Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PORTK after changing the DDRK register.*

3.2.17 Port T Data Register (PTT)

Address Offset: $0240

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
ECT:	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
Reset:	0	0	0	0	0	0	0	0

　 = Reserved or unimplemented

Figure 3-17 Port T Data Register (PTT)

Read:Anytime.

Write:Anytime.

Port T bits 7 through 0 are associated with ECT channels IOC7 through IOC0 (*refer to ECT Block Guide*). When not used with the ECT, these pins can be used as general purpose I/O.

If the data direction bits of the associated I/O pins are set to logic level "1", a read returns the value of the port register, otherwise the buffered pin input state is read.

3.2.18 Port T Input Register (PTIT)

Address Offset: $0241

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
Write:								
Reset[1]:	-	-	-	-	-	-	-	-

☐ = Reserved or unimplemented

NOTES:
1. These registers are reset to zero. Two bus clock cycles after reset release the register values are updated with the associated pin values.

Figure 3-18 Port T Input Register (PTIT)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the buffered state of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

3.2.19 Port T Data Direction Register (DDRT)

Address Offset: $0242

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRT7	DDRT6	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented

Figure 3-19 Port T Data Direction Register (DDRT)

Read:Anytime.

Write:Anytime.

This register configures each Port T pin as either input or output.

The ECT forces the I/O state to be an output for each timer port associated with an enabled output compare. In this case the data direction bits will not change.

The DDRT bits revert to controlling the I/O direction of a pin when the associated timer output compare is disabled.

The timer Input Capture always monitors the state of the pin.

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DDRT[7:0] — Data Direction Port T

    1 = Associated pin is configured as output.

    0 = Associated pin is configured as input.

> ***NOTE:*** *Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTT or PTIT registers, when changing the DDRT register.*

3.2.20 Port T Reduced Drive Register (RDRT)

Address Offset: $0243

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
Reset:	0	0	0	0	0	0	0	0

    ■ = Reserved or unimplemented
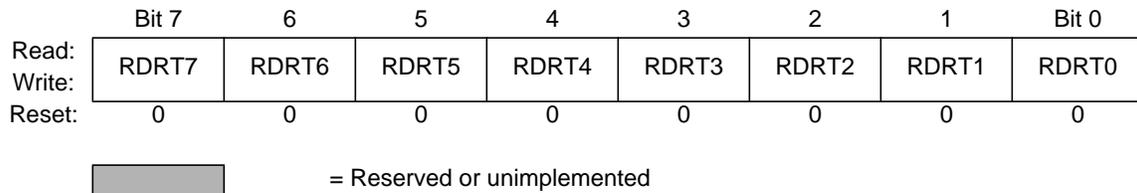
Figure 3-20 Port T Reduced Drive Register (RDRT)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each Port T output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRT[7:0] — Reduced Drive Port T

    1 = Associated pin drives at about 1/6 of the full drive strength.

    0 = Full drive strength at output.

3.2.21 Port T Pull Device Enable Register (PERT)

Address Offset: $0244

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
Reset:	0	0	0	0	0	0	0	0

    ■ = Reserved or unimplemented
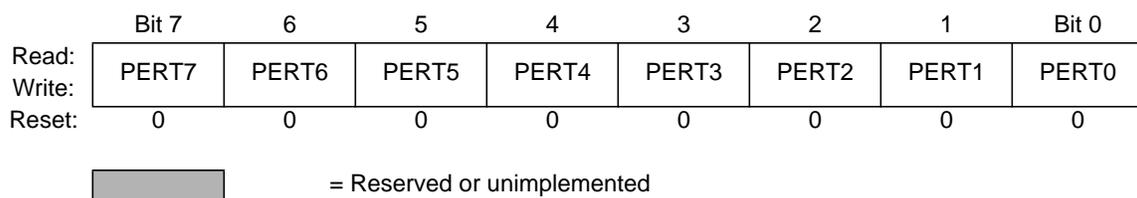
Figure 3-21 Port T Pull Device Enable Register (PERT)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERT[7:0] — Pull Device Enable Port T
> 1 = Either a pull-up or pull-down device is enabled.
> 0 = Pull-up or pull-down device is disabled.

3.2.22 Port T Polarity Select Register (PPST)

Address Offset: $0245

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
Reset:	0	0	0	0	0	0	0	0

                = Reserved or unimplemented
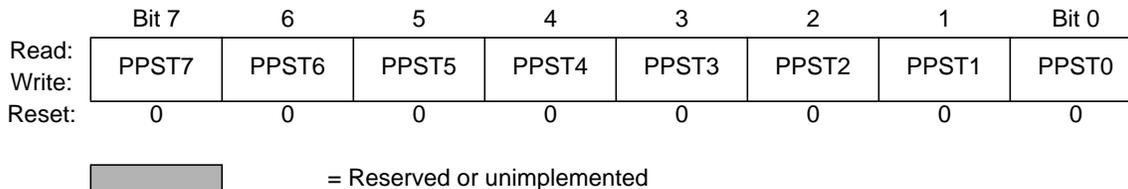
Figure 3-22 Port T Polarity Select Register (PPST)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPST[7:0] — Pull Select Port T
> 1 = A pull-down device is connected to the associated Port T pin, if enabled by the associated bit in register PERT and if the port is used as input.
> 0 = A pull-up device is connected to the associated Port T pin, if enabled by the associated bit in register PERT and if the port is used as input.

3.2.23 Port S Data Register (PTS)

Address Offset: $0248

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
SCI/SPI	SS0	SCK0	MOSI0	MISO0	TXD1	RXD1	TXD0	RXD0
Reset:	0	0	0	0	0	0	0	0

                = Reserved or unimplemented
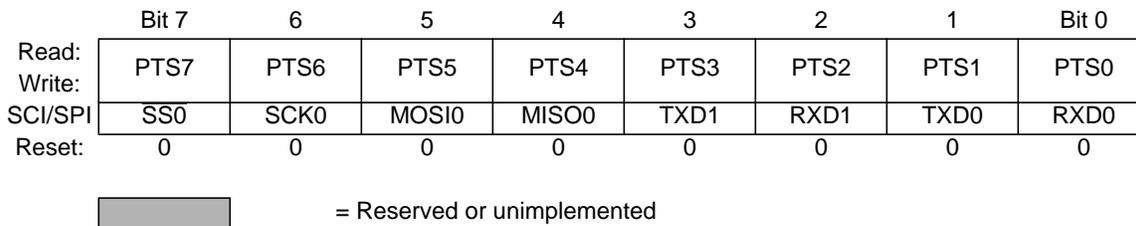
Figure 3-23 Port S Data Register (PTS)

Read:Anytime.

Write:Anytime.

Port S pins 7 through 4 are associated with the SPI0. The SPI0 pin configuration is determined by several status bits in the SPI0 module. *Refer to SPI Block Guide for details.* When not used with the SPI0, these pins can be used as general purpose I/O.

Port S bits 3 through 0 are associated with the SCI1 and SCI0. The SCI ports associated with transmit pins 3 and 1 are configured as outputs if the transmitter is enabled. The SCI ports associated with receive pins 2 and 0 are configured as inputs if the receiver is enabled. *Refer to SCI Block Guide for details.* When not used with the SCI, these pins can be used as general purpose I/O.

If the data direction bits of the associated I/O pins are set to logic level "1", a read returns the value of the port register, otherwise the buffered pin input state is read.

3.2.24 Port S Input Register (PTIS)

Address Offset: $0249

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
Write:								
Reset[1]:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

NOTES:
1. These registers are reset to zero. Two bus clock cycles after reset release the register values are updated with the associated pin values.

Figure 3-24 Port S Input Register (PTIS)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the buffered state of the associated pins. This also can be used to detect overload or short circuit conditions on output pins.

3.2.25 Port S Data Direction Register (DDRS)

Address Offset: $024A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRS7	DDRS6	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-25 Port S Data Direction Register (DDRS)

Read:Anytime.

Write:Anytime.

This register configures each Port S pin as either input or output.

If SPI0 is enabled, the SPI0 determines the pin direction. *Refer to SPI Block Guide for details.*

If the associated SCI transmit or receive channel is enabled this register has no effect on the pins. The pin is forced to be an output if a SCI transmit channel is enabled, it is forced to be an input if the SCI receive channel is enabled.

The DDRS bits revert to controlling the I/O direction of a pin when the associated channel is disabled.

DDRS[7:0] — Data Direction Port S
   1 = Associated pin is configured as output.
   0 = Associated pin is configured as input.

*NOTE:*   *Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTS or PTIS registers, when changing the DDRS register.*

3.2.26 Port S Reduced Drive Register (RDRS)

Address Offset: $024B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-26 Port S Reduced Drive Register (RDRS)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each Port S output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRS[7:0] — Reduced Drive Port S
   1 = Associated pin drives at about 1/6 of the full drive strength.
   0 = Full drive strength at output.

3.2.27 Port S Pull Device Enable Register (PERS)

Address Offset: $024C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
Reset:	1	1	1	1	1	1	1	1

= Reserved or unimplemented
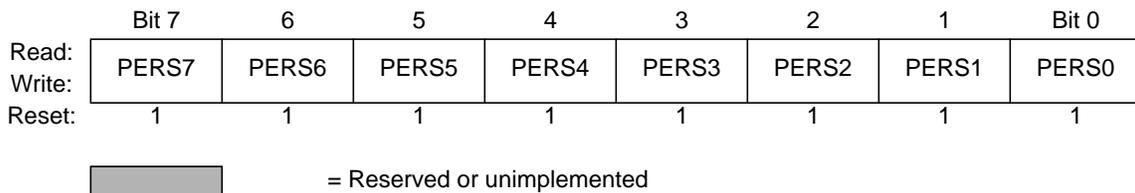
Figure 3-27 Port S Pull Device Enable Register (PERS)

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Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as output in wired-or (open drain) mode. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled.

PERS[7:0] — Pull Device Enable Port S
     1 = Either a pull-up or pull-down device is enabled.
     0 = Pull-up or pull-down device is disabled.

3.2.28 Port S Polarity Select Register (PPSS)

Address Offset: $024D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
Reset:	0	0	0	0	0	0	0	0

             = Reserved or unimplemented

Figure 3-28 Port S Polarity Select Register (PPSS)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin.

PPSS[7:0] — Pull Select Port S
     1 = A pull-down device is connected to the associated Port S pin, if enabled by the associated bit in register PERS and if the port is used as input.
     0 = A pull-up device is connected to the associated Port S pin, if enabled by the associated bit in register PERS and if the port is used as input or as wired-or output.

3.2.29 Port S Wired-Or Mode Register (WOMS)

Address Offset: $024E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
Reset:	0	0	0	0	0	0	0	0

             = Reserved or unimplemented

Figure 3-29 Port S Wired-Or Mode Register (WOMS)

Read:Anytime.

Write:Anytime.

This register configures the output pins as wired-or. If enabled the output is driven active low only (open-drain). A logic level of "1" is not driven. It applies also to the SPI and SCI outputs and allows a multipoint connection of several serial modules. These bits have no influence on pins used as inputs.

WOMS[7:0] — Wired-Or Mode Port S
        1 = Output buffers operate as open-drain outputs.
        0 = Output buffers operate as push-pull outputs.

3.2.30 Port M Data Register (PTM)

Address Offset: $0250

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTM7	PTM6	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
CAN:	TXCAN3	RXCAN3	TXCAN2	RXCAN2	TXCAN1	RXCAN1	TXCAN0	RXCAN0
Routed CAN0:			TXCAN0	RXCAN0	TXCAN0	RXCAN0		
Routed CAN4:	TXCAN4	RXCAN4	TXCAN4	RXCAN4				
Routed SPI0:			SCK0	MOSI0	$\overline{SS0}$	MISO0		
SCI:	TXD3	RXD3						
Reset	0	0	0	0	0	0	0	0

▢	= Reserved or unimplemented

Figure 3-30 Port M Data Register (PTM)

Read:Anytime.

Write:Anytime.

Port M pins 75 through 0 are associated with the CAN0, CAN1, CAN2, CAN3, SCI3, as well as the routed CAN0, CAN4, and SPI0 modules. When not used with any of the peripherals, these pins can be used as general purpose I/O.

If the data direction bits of the associated I/O pins are set to logic level "1", a read returns the value of the port register, otherwise the buffered pin input state is read.

PM[7:6]

The CAN3 function (TXCAN3 and RXCAN3) takes precedence over the CAN4, SCI3 and the general purpose I/O function if the CAN3 module is enabled. *Refer to MSCAN Block Guide for details.*

The CAN4 function (TXCAN4 and RXCAN4) takes precedence over the SCI3 and the general purpose I/O function if the CAN4 module is enabled. *Refer to MSCAN Block Guide for details.*

The SCI3 function (TXD3 and RXD3) takes precedence over the general purpose I/O function if the SCI3 module is enabled. *Refer to SCI Block Guide for details.*

PM[5:4]

The CAN2 function (TXCAN2 and RXCAN2) takes precedence over the routed CAN0, routed CAN4, the routed SPI0 and the general purpose I/O function if the CAN2 module is enabled{pim_9xd_prio.m}.

The routed CAN0 function (TXCAN0 and RXCAN0) takes precedence over the routed CAN4, the routed SPI0 and the general purpose I/O function if the routed CAN0 module is enabled.

The routed CAN4 function (TXCAN4 and RXCAN4) takes precedence over the routed SPI0 and general purpose I/O function if the routed CAN4 module is enabled. *Refer to MSCAN Block Guide for details.*

The routed SPI0 function (SCK0 and MOSI0) takes precedence of the general purpose I/O function if the routed SPI0 is enabled. *Refer to SPI Block Guide for details.*

PM[3:2]

The CAN1 function (TXCAN1 and RXCAN1) takes precedence over the routed CAN0, the routed SPI0 and the general purpose I/O function if the CAN1 module is enabled.

The routed CAN0 function (TXCAN0 and RXCAN0) takes precedence over the routed SPI0 and the general purpose I/O function if the routed CAN0 module is enabled. *Refer to MSCAN Block Guide for details.*

The routed SPI0 function ($\overline{SS0}$ and MISO0) takes precedence of the general purpose I/O function if the routed SPI0 is enabled and not in bidirectional mode. *Refer to SPI Block Guide for details.*

PM[1:0]

The CAN0 function (TXCAN0 and RXCAN0) takes precedence over the general purpose I/O function if the CAN0 module is enabled. *Refer to MSCAN Block Guide for details.*

3.2.31 Port M Input Register (PTIM)

Address Offset: $0251

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIM7	PTIM6	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
Write:								
Reset[1]:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

NOTES:
1. These registers are reset to zero. Two bus clock cycles after reset release the register values are updated with the associated pin values.

Figure 3-31 Port M Input Register (PTIM)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the buffered state of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

3.2.32 Port M Data Direction Register (DDRM)

Address Offset: $0252

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRM7	DDRM6	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
Reset:	0	0	0	0	0	0	0	0

 = Reserved or unimplemented
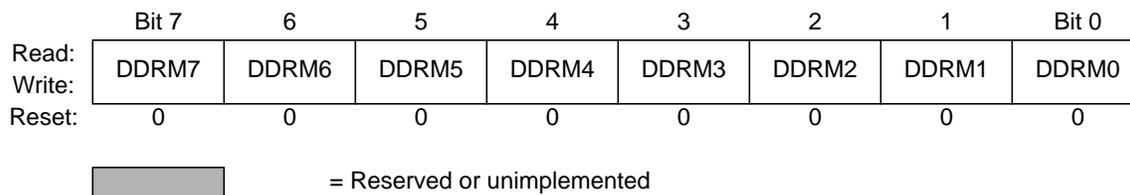
Figure 3-32 Port M Data Direction Register (DDRM)

Read:Anytime.

Write:Anytime.

This register configures each Port M pin as either input or output.

The CAN/SCI3 forces the I/O state to be an output for each port line associated with an enabled output (TXCAN[3:0], TXD3). They also forces the I/O state to be an input for each port line associated with an enabled input (RXCAN[3:0], RXD3). In those cases the data direction bits will not change.

The DDRM bits revert to controlling the I/O direction of a pin when the associated peripheral module is disabled.

DDRM[7:0] — Data Direction Port M
   1 = Associated pin is configured as output.
   0 = Associated pin is configured as input.

NOTE: *Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTM or PTIM registers, when changing the DDRM register.*

3.2.33 Port M Reduced Drive Register (RDRM)

Address Offset: $0253

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRM7	RDRM6	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
Reset:	0	0	0	0	0	0	0	0

 = Reserved or unimplemented

Figure 3-33 Port M Reduced Drive Register (RDRM)

Read:Anytime.

Write:Anytime.

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This register configures the drive strength of each Port M output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRM[7:0] — Reduced Drive Port M
    1 = Associated pin drives at about 1/6 of the full drive strength.
    0 = Full drive strength at output.

## 3.2.34 Port M Pull Device Enable Register (PERM)

Address Offset: $0254

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERM7	PERM6	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
Reset:	0	0	0	0	0	0	0	0

        [ ] = Reserved or unimplemented
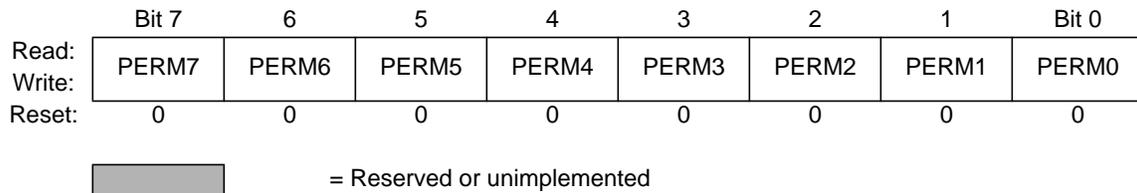
Figure 3-34 Port M Pull Device Enable Register (PERM)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or wired-or output. This bit has no effect if the port is used as push-pull output. Out of reset no pull device is enabled.

PERM[7:0] — Pull Device Enable Port M
    1 = Either a pull-up or pull-down device is enabled.
    0 = Pull-up or pull-down device is disabled.

3.2.35 Port M Polarity Select Register (PPSM)

Address Offset: $0255

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
Reset:	0	0	0	0	0	0	0	0

        [ ] = Reserved or unimplemented
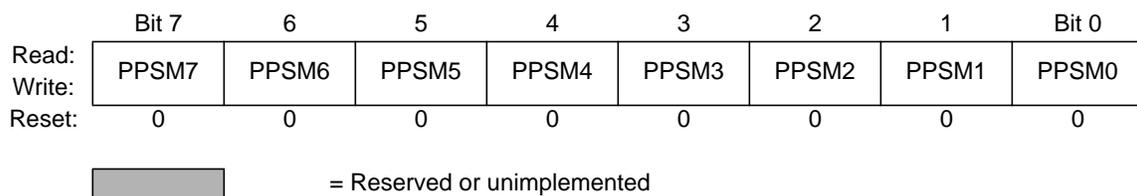
Figure 3-35 Port M Polarity Select Register (PPSM)

Read:Anytime.

Write:Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin. If CAN is active a pull-up device can be activated on the RXCAN[3:0] inputs, but not a pull-down.

PPSM[7:0] — Pull Select Port M
- 1 = A pull-down device is connected to the associated Port M pin, if enabled by the associated bit in register PERM and if the port is used as a general purpose but not as RXCAN.
- 0 = A pull-up device is connected to the associated Port M pin, if enabled by the associated bit in register PERM and if the port is used as general purpose or RXCAN input.

3.2.36 Port M Wired-Or Mode Register (WOMM)

Address Offset: $0256

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented
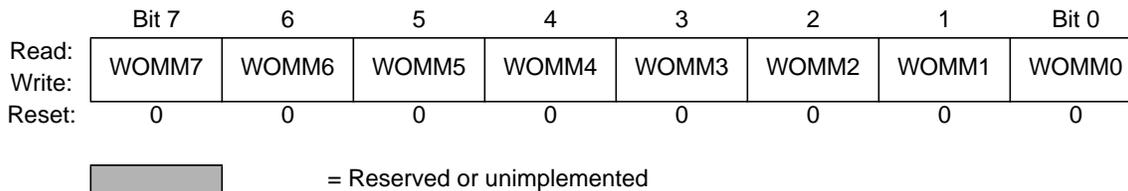
Figure 3-36 Port M Wired-Or Mode Register (WOMM)

Read:Anytime.

Write:Anytime.

This register configures the output pins as wired-or. If enabled the output is driven active low only (open-drain). A logic level of "1" is not driven. It applies also to the CAN outputs and allows a multipoint connection of several serial modules. This bit has no influence on pins used as inputs.

WOMM[7:0] — Wired-Or Mode Port M
- 1 = Output buffers operate as open-drain outputs.
- 0 = Output buffers operate as push-pull outputs.

3.2.37 Module Routing Register (MODRR)

Address Offset: $0257

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	MODRR6	MODRR5	MODRR4	MODRR3	MODRR2	MODRR1	MODRR0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented
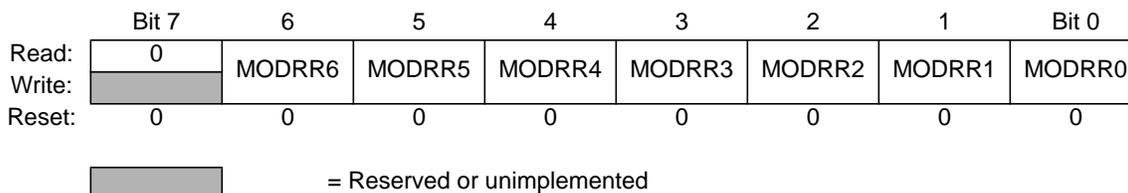
Figure 3-37 Module Routing Register (MODRR)

Read:Anytime.

Write:Anytime.

This register configures the re-routing of CAN0, CAN4, SPI0, SPI1, and SPI2 on alternative ports.

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Table 3-4 Module Routing Summary

Module	MODRR							Related Pins			
	6	5	4	3	2	1	0				
								RXCAN		TXCAN	
CAN0	x	x	x	x	x	0	0	PM0		PM1	
	x	x	x	x	x	0	1	PM2		PM3	
	x	x	x	x	x	1	0	PM4		PM5	
	x	x	x	x	x	1	1	PJ6		PJ7	
CAN4	x	x	x	0	0	x	x	PJ6		PJ7	
	x	x	x	0	1	x	x	PM4		PM5	
	x	x	x	1	0	x	x	PM6		PM7	
	x	x	x	1	1	x	x	Reserved			
								MISO	MOSI	SCK	$\overline{\overline{SS}}$
SPI0	x	x	0	x	x	x	x	PS4	PS5	PS6	PS7
	x	x	1	x	x	x	x	PM2	PM4	PM5	PM3
SPI1	x	0	x	x	x	x	x	PP0	PP1	PP2	PP3
	x	1	x	x	x	x	x	PH0	PH1	PH2	PH3
SPI2	0	x	x	x	x	x	x	PP4	PP5	PP7	PP6
	1	x	x	x	x	x	x	PH4	PH5	PH6	PH7

3.2.38 Port P Data Register (PTP)

Address Offset: $0258

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTP7	PTP6	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
PWM:	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
SPI:	SCK2	SS2	MOSI2	MISO2	SS1	SCK1	MOSI1	MISO1
Reset:	0	0	0	0	0	0	0	0

[ ] = Reserved or unimplemented

Figure 3-38 Port P Data Register (PTP)

Read: Anytime.

Write: Anytime.

Port P pins 7, and 5 through 0 are associated with the PWM as well as the SPI1 and SPI2 modules. These pins can be used as general purpose I/O when not used with any of the peripherals.

If the data direction bits of the associated I/O pins are set to logic level "1", a read returns the value of the port register, otherwise the buffered pin input state is read.

The PWM function takes precedence over the general purpose I/O and the SPI2 or SPI1 function if the associated PWM channel is enabled. While channels 6 and 5-0 are output only if the respective channel is enabled, channel 7 can be PWM output or input if the shutdown feature is enabled. *Refer to PWM Block Guide for details.*

The SPI2 function takes precedence over the general purpose I/O function if enabled. *Refer to SPI Block Guide for details.*

The SPI1 function takes precedence over the general purpose I/O function if enabled. *Refer to SPI Block Guide for details.*

3.2.39 Port P Input Register (PTIP)

Address Offset: $0259

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIP7	PTIP6	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
Write:								
Reset[1]:	-	-	-	-	-	-	-	-

        = Reserved or unimplemented

NOTES:
1. These registers are reset to zero. Two bus clock cycles after reset release the register values are updated with the associated pin values.

Figure 3-39 Port P Input Register (PTIP)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the buffered state of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

3.2.40 Port P Data Direction Register (DDRP)

Address Offset: $025A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRP7	DDRP6	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
Reset:	0	0	0	0	0	0	0	0

        = Reserved or unimplemented

Figure 3-40 Port P Data Direction Register (DDRP)

Read:Anytime.

Write:Anytime.

This register configures each Port P pin as either input or output.

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If the associated PWM channel or SPI module is enabled this register has no effect on the pins.

The PWM forces the I/O state to be an output for each port line associated with an enabled PWM7-0 channel. Channel 7 can force the pin to input if the shutdown feature is enabled. *Refer to PWM Block Guide for details.*

If a SPI module is enabled, the SPI determines the pin direction. *Refer to SPI Block Guide for details.*

The DDRP bits revert to controlling the I/O direction of a pin when the associated peripherals are disabled.

DDRP[7:0] — Data Direction Port P
      1 = Associated pin is configured as output.
      0 = Associated pin is configured as input.

> **NOTE:** *Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTP or PTIP registers, when changing the DDRP register.*

3.2.41 Port P Reduced Drive Register (RDRP)

Address Offset: $025B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRP7	RDRP6	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
Reset:	0	0	0	0	0	0	0	0

                        = Reserved or unimplemented

Figure 3-41 Port P Reduced Drive Register (RDRP)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each Port P output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRP[7:0] — Reduced Drive Port P
      1 = Associated pin drives at about 1/6 of the full drive strength.
      0 = Full drive strength at output.

3.2.42 Port P Pull Device Enable Register (PERP)

Address Offset: $025C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERP7	PERP6	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented
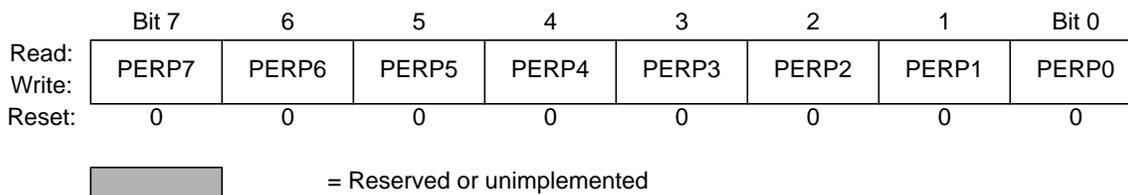
Figure 3-42 Port P Pull Device Enable Register (PERP)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERP[7:0] — Pull Device Enable Port P
    1 = Either a pull-up or pull-down device is enabled.
    0 = Pull-up or pull-down device is disabled.

3.2.43 Port P Polarity Select Register (PPSP)

Address Offset: $025D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSP7	PPSP6	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented
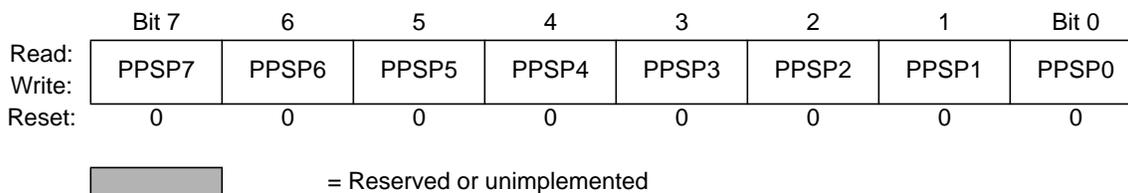
Figure 3-43 Port P Polarity Select Register (PPSP)

Read:Anytime.

Write:Anytime.

This register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.

PPSP[7:0] — Polarity Select Port P
    1 = Rising edge on the associated Port P pin sets the associated flag bit in the PIFP register.A
        pull-down device is connected to the associated Port P pin, if enabled by the associated bit in
        register PERP and if the port is used as input.
    0 = Falling edge on the associated Port P pin sets the associated flag bit in the PIFP register.A
        pull-up device is connected to the associated Port P pin, if enabled by the associated bit in
        register PERP and if the port is used as input.

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3.2.44 Port P Interrupt Enable Register (PIEP)

Address Offset: $025E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIEP7	PIEP6	PIEP5	PIEP4	PIEP3	PIEP2	PIEP1	PIEP0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented
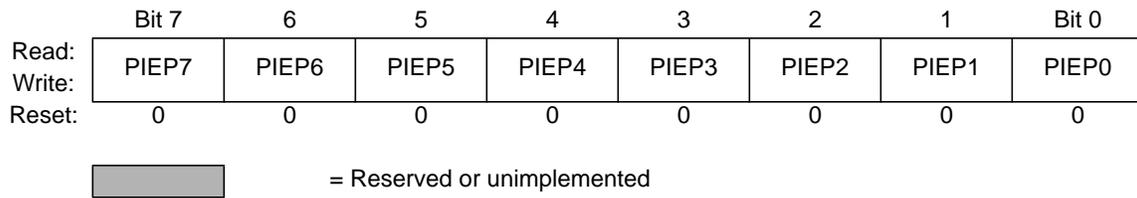
Figure 3-44 Port P Interrupt Enable Register (PIEP)

Read:Anytime.

Write:Anytime.

This register disables or enables on a per-pin basis the edge sensitive external interrupt associated with Port P.

PIEP[7:0] — Interrupt Enable Port P
    1 = Interrupt is enabled.
    0 = Interrupt is disabled (interrupt flag masked).

3.2.45 Port P Interrupt Flag Register (PIFP)

Address Offset: $025F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIFP7	PIFP6	PIFP5	PIFP4	PIFP3	PIFP2	PIFP1	PIFP0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented
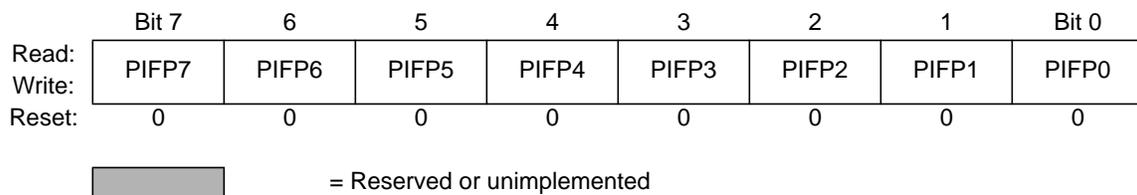
Figure 3-45 Port P Interrupt Flag Register (PIFP)

Read:Anytime.

Write:Anytime.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSP register. To clear this flag, write logic level "1" to the corresponding bit in the PIFP register. Writing a "0" has no effect.

PIFP[7:0] — Interrupt Flags Port P
    1 = Active edge on the associated bit has occurred (an interrupt will occur if the associated enable
        bit is set).
        Writing a logic level "1" clears the associated flag.
    0 = No active edge pending.
        Writing a "0" has no effect.

3.2.46 Port H Data Register (PTH)

Address Offset: $0260

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
Routed SPI:	$\overline{SS2}$	SCK2	MOSI2	MISO2	$\overline{SS1}$	SCK1	MOSI1	MISO1
SCI:	TXD5	RXD5	TXD4	RXD4				
Reset:	0	0	0	0	0	0	0	0
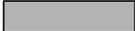
= Reserved or unimplemented

Figure 3-46 Port H Data Register (PTH)

Read:Anytime.

Write:Anytime.

Port H pins 7 through 0 are associated with the SCI4 and SCI5 as well as the routed SPI1 and SPI2 modules. These pins can be used as general purpose I/O when not used with any of the peripherals.

If the data direction bits of the associated I/O pins are set to logic level "1", a read returns the value of the port register, otherwise the buffered pin input state is read.

The routed SPI2 function takes precedence over the SCI4 and SCI5 and the general purpose I/O function if the routed SPI2 module is enabled. *Refer to SPI Block Guide for details.*

The routed SPI1 function takes precedence over the general purpose I/O function if the routed SPI1 is enabled. *Refer to SPI Block Guide for details.*

The SCI4 and SCI5 function takes precedence over the general purpose I/O function if the SCI4 or SCI5 is enabled. *Refer to SCI Block Guide for details.*

3.2.47 Port H Input Register (PTIH)

Address Offset: $0261

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
Write:								
Reset[1]:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

NOTES:
1. These registers are reset to zero. Two bus clock cycles after reset release the register values are updated with the associated pin values.

Figure 3-47 Port H Input Register (PTIH)

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Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the buffered state of the associated pins. This can also be used to detect overload or short circuit conditions on output pins.

3.2.48 Port H Data Direction Register (DDRH)

Address Offset: $0262

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRH7	DDRH6	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented
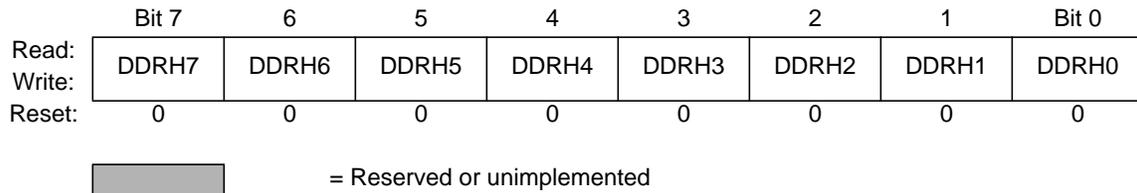
Figure 3-48 Port H Data Direction Register (DDRH)

Read:Anytime.

Write:Anytime.

This register configures each Port H pin as either input or output.

If the associated SCI channel or routed SPI module is enabled this register has no effect on the pins.

The SCI forces the I/O state to be an output for each port line associated with an enabled output (TXD5, TXD4). It also forces the I/O state to be an input for each port line associated with an enabled input (RXD5, RXD4). In those cases the data direction bits will not change.

If a SPI module is enabled, the SPI determines the pin direction. *Refer to SPI Block Guide for details.*

The DDRH bits revert to controlling the I/O direction of a pin when the associated peripheral modules are disabled.

DDRH[7:0] — Data Direction Port H
      1 = Associated pin is configured as output.
      0 = Associated pin is configured as input.

NOTE: *Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTH or PTIH registers, when changing the DDRH register.*

3.2.49 Port H Reduced Drive Register (RDRH)

Address Offset: $0263

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-49 Port H Reduced Drive Register (RDRH)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each Port H output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRH[7:0] — Reduced Drive Port H
    1 = Associated pin drives at about 1/6 of the full drive strength.
    0 = Full drive strength at output.

3.2.50 Port H Pull Device Enable Register (PERH)

Address Offset: $0264

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented
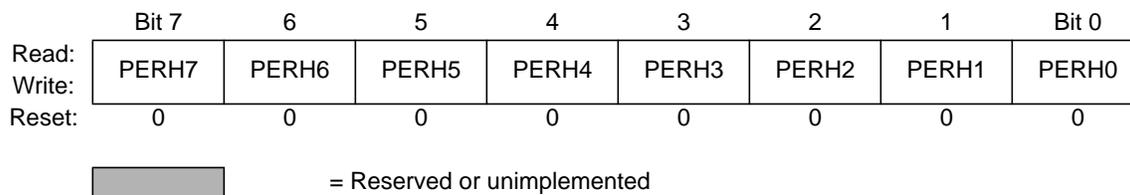
Figure 3-50 Port H Pull Device Enable Register (PERH)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PERH[7:0] — Pull Device Enable Port H
    1 = Either a pull-up or pull-down device is enabled.
    0 = Pull-up or pull-down device is disabled.

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3.2.51 Port H Polarity Select Register (PPSH)

Address Offset: $0265

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-51 Port H Polarity Select Register (PPSH)

Read:Anytime.

Write:Anytime.

This register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.

PPSH[7:0] — Polarity Select Port H
    1 = Rising edge on the associated Port H pin sets the associated flag bit in the PIFH register.
        A pull-down device is connected to the associated Port H pin, if enabled by the associated bit
        in register PERH and if the port is used as input.
    0 = Falling edge on the associated Port H pin sets the associated flag bit in the PIFH register.
        A pull-up device is connected to the associated Port H pin, if enabled by the associated bit in
        register PERH and if the port is used as input.

3.2.52 Port H Interrupt Enable Register (PIEH)

Address Offset: $0266

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-52 Port H Interrupt Enable Register (PIEH)

Read:Anytime.

Write:Anytime.

This register disables or enables on a per-pin basis the edge sensitive external interrupt associated with Port H.

PIEH[7:0] — Interrupt Enable Port H
    1 = Interrupt is enabled.
    0 = Interrupt is disabled (interrupt flag masked).

3.2.53 Port H Interrupt Flag Register (PIFH)

Address Offset: $0267

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-53 Port H Interrupt Flag Register (PIFH)

Read:Anytime.

Write:Anytime.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSH register. To clear this flag, write logic level "1" to the corresponding bit in the PIFH register. Writing a "0" has no effect.

PIFH[7:0] — Interrupt Flags Port H
    1 = Active edge on the associated bit has occurred (an interrupt will occur if the associated enable
       bit is set).
       Writing a logic level "1" clears the associated flag.
    0 = No active edge pending.
       Writing a "0" has no effect.

3.2.54 Port J Data Register (PTJ)

Address Offset: $0268

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTJ7	PTJ6	PTJ5	PTJ4	0	PTJ2	PTJ1	PTJ0
CAN4/ SCI2:	TXCAN4	RXCAN4					TXD2	RXD2
IIC0:	SCL0	SDA0						
IIC1:			SCL1	SDA1				
Routed CAN0:	TXCAN0	RXCAN0						
Alt. Func.:			$\overline{CS2}$	$\overline{CS0}$		$\overline{CS1}$		$\overline{CS3}$
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-54 Port J Data Register (PTJ)

Read:Anytime.

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PIM_9XDP512 Block Guide V02.02

Write:Anytime.

Port J pins 7 - 4 and 2 - 0 are associated with the CAN4, SCI2, IIC0 and IIC1, the routed CAN0 modules and chip select signals ($\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$). These pins can be used as general purpose I/O when not used with any of the peripherals.

If the data direction bits of the associated I/O pins are set to logic level "1", a read returns the value of the port register, otherwise the buffered pin input state is read.

PJ[7:6]

The CAN4 function (TXCAN4 and RXCAN4) takes precedence over the IIC0, the routed CAN0 and the general purpose I/O function if the CAN4 module is enabled.

The IIC0 function (SCL0 and SDA0) takes precedence over the routed CAN0 and the general purpose I/O function if the IIC0 is enabled. If the IIC0 module takes precedence the SDA0 and SCL0 outputs are configured as open drain outputs. *Refer to IIC Block Guide for details.*

The routed CAN0 function (TXCAN0 and RXCAN0) takes precedence over the general purpose I/O function if the routed CAN0 module is enabled. *Refer to MSCAN Block Guide for details.*

PJ[5:4]

The IIC1 function (SCL1 and SDA1) takes precedence over the chip select ($\overline{CS0}$, $\overline{CS2}$) and general purpose I/O function if the IIC1 is enabled. The chip selects ($\overline{CS0}$, $\overline{CS2}$) take precedence over the general purpose I/O. If the IIC1 module takes precedence the SDA1 and SCL1 outputs are configured as open drain outputs. *Refer to IIC Block Guide for details.*

PJ[2]

The chip select function ($\overline{CS1}$) takes precedence over the general purpose I/O.

PJ[1]

The SCI2 function takes precedence over the general purpose I/O function if the SCI2 module is enabled. *Refer to SCI Block Guide for details.*

PJ[0]

The SCI2 function takes precedence over the chip select ($\overline{CS3}$) and the general purpose I/O function if the SCI2 module is enabled. The chip select ($\overline{CS3}$) takes precedence over the general purpose I/O function. *Refer to SCI Block Guide for details.*

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3.2.55 Port J Input Register (PTIJ)

Address Offset: $0269

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTIJ7	PTIJ6	PTIJ5	PTIJ4	0	PTIJ2	PTIJ1	PTIJ0
Write:								
Reset[1]:	-	-	-	-	-	-	-	-

= Reserved or unimplemented

NOTES:
  1. These registers are reset to zero. Two bus clock cycles after reset release the register values are updated with the associated pin values.

Figure 3-55 Port J Input Register (PTIJ)

Read:Anytime.

Write:Never, writes to this register have no effect.

This register always reads back the buffered state of the associated pins. This can be used to detect overload or short circuit conditions on output pins.

3.2.56 Port J Data Direction Register (DDRJ)

Address Offset: $026A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	DDRJ7	DDRJ6	DDRJ5	DDRJ4	0	DDRJ2	DDRJ1	DDRJ0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-56 Port J Data Direction Register (DDRJ)

Read:Anytime.

Write:Anytime.

This register configures each Port J pin as either input or output.

The CAN forces the I/O state to be an output on PJ7 (TXCAN4) and an input on pin PJ6 (RXCAN4). The IIC takes control of the I/O if enabled. In these cases the data direction bits will not change.

The SCI2 forces the I/O state to be an output for each port line associated with an enabled output (TXD2). It also forces the I/O state to be an input for each port line associated with an enabled input (RXD2). In these cases the data direction bits will not change.

The DDRJ bits revert to controlling the I/O direction of a pin when the associated peripheral module is disabled.

DDRJ[7:4][2:0] — Data Direction Port J

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1 = Associated pin is configured as output.
0 = Associated pin is configured as input.

NOTE: *Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTJ or PTIJ registers, when changing the DDRJ register.*

3.2.57 Port J Reduced Drive Register (RDRJ)

Address Offset: $026B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDRJ7	RDRJ6	RDRJ5	RDRJ4	0	RDRJ2	RDRJ1	RDRJ0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented

Figure 3-57 Port J Reduced Drive Register (RDRJ)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each Port J output pin as either full or reduced. If the port is used as input this bit is ignored.

RDRJ[7:4][2:0] — Reduced Drive Port J
    1 = Associated pin drives at about 1/6 of the full drive strength.
    0 = Full drive strength at output.

3.2.58 Port J Pull Device Enable Register (PERJ)

Address Offset: $026C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PERJ7	PERJ6	PERJ5	PERJ4	0	PERJ2	PERJ1	PERJ0
Reset:	1	1	1	1	0	1	1	1

☐ = Reserved or unimplemented

Figure 3-58 Port J Pull Device Enable Register (PERJ)

Read:Anytime.

Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated, if the port is used as input or as wired-or output. This bit has no effect if the port is used as push-pull output. Out of reset a pull-up device is enabled.

PERJ[7:4][2:0] — Pull Device Enable Port J
    1 = Either a pull-up or pull-down device is enabled.
    0 = Pull-up or pull-down device is disabled.

3.2.59 Port J Polarity Select Register (PPSJ)

Address Offset: $026D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PPSJ7	PPSJ6	PPSJ5	PPSJ4	0	PPSJ2	PPSJ1	PPSJ0
Reset:	0	0	0	0	0	0	0	0

           = Reserved or unimplemented
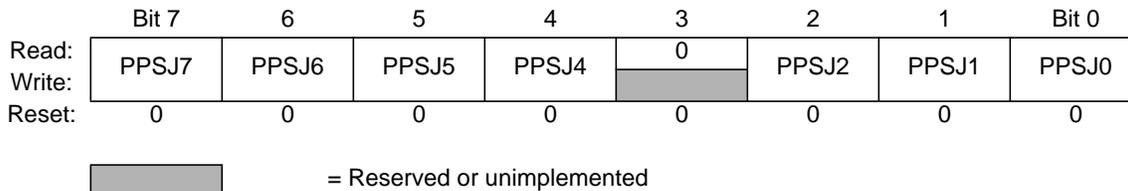
Figure 3-59 Port J Polarity Select Register (PPSJ)

Read:Anytime.

Write:Anytime.

This register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled.

PPSJ[7:4][2:0] — Polarity Select Port J
    1 = Rising edge on the associated Port J pin sets the associated flag bit in the PIFJ register.
       A pull-down device is connected to the associated Port J pin, if enabled by the associated bit in
       register PERJ and if the port is used as input.
    0 = Falling edge on the associated Port J pin sets the associated flag bit in the PIFJ register.
       A pull-up device is connected to the associated Port J pin, if enabled by the associated bit in
       register PERJ and if the port is used as general purpose input or as IIC port.

3.2.60 Port J Interrupt Enable Register (PIEJ)

Address Offset: $026E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIEJ7	PIEJ6	PIEJ5	PIEJ4	0	PIEJ2	PIEJ1	PIEJ0
Reset:	0	0	0	0	0	0	0	0

           = Reserved or unimplemented

Figure 3-60 Port J Interrupt Enable Register (PIEJ)

This register disables or enables on a per-pin basis the edge sensitive external interrupt associated with Port J.

PIEJ[7:4][2:0] — Interrupt Enable Port J
    1 = Interrupt is enabled.

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0 = Interrupt is disabled (interrupt flag masked).

3.2.61 Port J Interrupt Flag Register (PIFJ)

Address Offset: $026F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PIFJ7	PIFJ6	PIFJ5	PIFJ4	0	PIFJ2	PIFJ1	PIFJ0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented

Figure 3-61 Port J Interrupt Flag Register (PIFJ)

Read:Anytime.

Write:Anytime.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSJ register. To clear this flag, write logic level "1" to the corresponding bit in the PIFJ register. Writing a "0" has no effect.

PIFJ[7:4][2:0] — Interrupt Flags Port J
>   1 = Active edge on the associated bit has occurred (an interrupt will occur if the associated enable
>   bit is set).
>   Writing a logic level "1" clears the associated flag.
>   0 = No active edge pending.
>   Writing a "0" has no effect.

3.2.62 Port AD0 Data Register 1 (PT1AD0)

Address Offset: $0271

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PT1AD0 7	PT1AD0 6	PT1AD0 5	PT1AD0 4	PT1AD0 3	PT1AD0 2	PT1AD0 1	PT1AD0 0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented

Figure 3-62 Port AD0 Data Register 1 (PT1AD0)

Read:Anytime.

Write:Anytime.

This register is associated with AD0 pins PAD[23:10]. These pins can also be used as general purpose I/O.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

3.2.63 Port AD0 Data Direction Register 1 (DDR1AD0)

Address Offset: $0273

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	DDR1AD0	DDR1AD0	DDR1AD0	DDR1AD0	DDR1AD0	DDR1AD0	DDR1AD0	DDR1AD0
Write:	7	6	5	4	3	2	1	0
Reset:	0	0	0	0	0	0	0	0

◻ = Reserved or unimplemented

Figure 3-63 Port AD0 Data Direction Register 1 (DDR1AD0)

Read:Anytime.

Write:Anytime.

This register configures pins PAD[07:00] as either input or output.

DDR1AD0[7:0] — Data Direction Port AD0 Register 1
    1 = Associated pin is configured as output.
    0 = Associated pin is configured as input.

> **NOTE:** *Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTAD01 register, when changing the DDR1AD0 register.*

> **NOTE:** *To use the digital input function on Port AD0 the ATD0 Digital Input Enable Register (ATD0DIEN) has to be set to logic level "1".*

3.2.64 Port AD0 Reduced Drive Register 1 (RDR1AD0)

Address Offset: $0275

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RDR1AD0	RDR1AD0	RDR1AD0	RDR1AD0	RDR1AD0	RDR1AD0	RDR1AD0	RDR1AD0
Write:	7	6	5	4	3	2	1	0
Reset:	0	0	0	0	0	0	0	0

◻ = Reserved or unimplemented

Figure 3-64 Port AD0 Reduced Drive Register 1 (RDR1AD0)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each output pin PAD[07:00] as either full or reduced. If the port is used as input this bit is ignored.

RDR1AD0[7:0] — Reduced Drive Port AD0 Register 1
    1 = Associated pin drives at about 1/6 of the full drive strength.

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0 = Full drive strength at output.

3.2.65 Port AD0 Pull Up Enable Register 1 (PER1AD0)

Address Offset: $0277

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PER1AD0	PER1AD0	PER1AD0	PER1AD0	PER1AD0	PER1AD0	PER1AD0	PER1AD0
Write:	7	6	5	4	3	2	1	0
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented

Figure 3-65 Port AD0 Pull Up Enable Register 1 (PER1AD0)

Read:Anytime.

Write:Anytime.

This register activates a pull-up device on the respective pin PAD[07:00] if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull device is enabled.

PER1AD0[7:0] — Pull Device Enable Port AD0 Register 1
    1 = Pull-up device is enabled.
    0 = Pull-up device is disabled.

3.2.66 Port AD1 Data Register 0 (PT0AD1)

Address Offset: $0278

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PT0AD1	PT0AD1	PT0AD1	PT0AD1	PT0AD1	PT0AD1	PT0AD1	PT0AD1
Write:	23	22	21	20	19	18	17	16
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented

Figure 3-66 Port AD1 Data Register 0 (PT0AD1)

Read:Anytime.

Write:Anytime.

This register is associated with AD1 pins PAD[23:16]. These pins can also be used as general purpose I/O.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

3.2.67 Port AD1 Data Register 1 (PT1AD1)

Address Offset: $0279

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PT1AD1	PT1AD1	PT1AD1	PT1AD1	PT1AD1	PT1AD1	PT1AD1	PT1AD1
Write:	15	14	13	12	11	10	9	8
Reset:	0	0	0	0	0	0	0	0

          = Reserved or unimplemented

Figure 3-67 Port AD1 Data Register 1 (PT1AD1)

Read:Anytime.

Write:Anytime.

This register is associated with AD1 pins PAD[15:08]. These pins can also be used as general purpose I/O.

If the data direction bits of the associated I/O pins are set to 1, a read returns the value of the port register, otherwise the value at the pins is read.

3.2.68 Port AD1 Data Direction Register 0 (DDR0AD1)

Address Offset: $027A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	DDR0AD1	DDR0AD1	DDR0AD1	DDR0AD1	DDR0AD1	DDR0AD1	DDR0AD1	DDR0AD1
Write:	23	22	21	20	19	18	17	16
Reset:	0	0	0	0	0	0	0	0

          = Reserved or unimplemented

Figure 3-68 Port AD1 Data Direction Register 0 (DDR0AD1)

Read:Anytime.

Write:Anytime.

This register configures pin PAD[23:16] as either input or output.

DDR0AD1[23:16] — Data Direction Port AD1 Register 0
        1 = Associated pin is configured as output.
        0 = Associated pin is configured as input.

> **NOTE:** *Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTAD10 register, when changing the DDR0AD1 register.*

> **NOTE:** *To use the digital input function on Port AD1 the ATD1 Digital Input Enable Register (ATD1DIEN0) has to be set to logic level "1".*

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3.2.69 Port AD1 Data Direction Register 1 (DDR1AD1)

Address Offset: $027B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	DDR1AD1	DDR1AD1	DDR1AD1	DDR1AD1	DDR1AD1	DDR1AD1	DDR1AD1	DDR1AD1
Write:	15	14	13	12	11	10	9	8
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented

Figure 3-69 Port AD1 Data Direction Register 1 (DDR1AD1)

Read:Anytime.

Write:Anytime.

This register configures pins PAD[15:08] as either input or output.

DDR1AD1[15:8] — Data Direction Port AD1 Register 1
    1 = Associated pin is configured as output.
    0 = Associated pin is configured as input.

> **NOTE:**   *Due to internal synchronization circuits, it can take up to 2 bus clock cycles until the correct value is read on PTAD11 register, when changing the DDR1AD1 register.*

> **NOTE:**   *To use the digital input function on Port AD1 the ATD1 Digital Input Enable Register (ATD1DIEN1) has to be set to logic level "1".*

3.2.70 Port AD1 Reduced Drive Register 0 (RDR0AD1)

Address Offset: $027C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RDR0AD1	RDR0AD1	RDR0AD1	RDR0AD1	RDR0AD1	RDR0AD1	RDR0AD1	RDR0AD1
Write:	23	22	21	20	19	18	17	16
Reset:	0	0	0	0	0	0	0	0

☐ = Reserved or unimplemented

Figure 3-70 Port AD1 Reduced Drive Register 0 (RDR0AD1)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each PAD[23:16] output pin as either full or reduced. If the port is used as input this bit is ignored.

RDR0AD1[23:16] — Reduced Drive Port AD1 Register 0
    1 = Associated pin drives at about 1/6 of the full drive strength.

0 = Full drive strength at output.

3.2.71 Port AD1 Reduced Drive Register 1 (RDR1AD1)

Address Offset: $027D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RDR1AD1 15	RDR1AD1 14	RDR1AD1 13	RDR1AD1 12	RDR1AD1 11	RDR1AD1 10	RDR1AD1 9	RDR1AD1 8
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-71 Port AD1 Reduced Drive Register 1 (RDR1AD1)

Read:Anytime.

Write:Anytime.

This register configures the drive strength of each PAD[15:08] output pin as either full or reduced. If the port is used as input this bit is ignored.

RDR1AD1[15:8] — Reduced Drive Port AD1 Register 1
    1 = Associated pin drives at about 1/6 of the full drive strength.
    0 = Full drive strength at output.

3.2.72 Port AD1 Pull Up Enable Register 0 (PER0AD1)

Address Offset: $027E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PER0AD1 23	PER0AD1 22	PER0AD1 21	PER0AD1 20	PER0AD1 19	PER0AD1 18	PER0AD1 17	PER0AD1 16
Reset:	0	0	0	0	0	0	0	0

= Reserved or unimplemented

Figure 3-72 Port AD1 Pull Up Enable Register 0 (PER0AD1)

Read:Anytime.

Write:Anytime.

This register activates a pull-up device on the respective PAD[23:16] pin if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull-up device is enabled.

PER0AD1[23:16] — Pull Device Enable Port AD1 Register 0
    1 = Pull-up device is enabled.
    0 = Pull-up device is disabled.

MOTOROLA

3.2.73 Port AD1 Pull Up Enable Register 1 (PER1AD1)

Address Offset: $027F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PER1AD1	PER1AD1	PER1AD1	PER1AD1	PER1AD1	PER1AD1	PER1AD1	PER1AD1
Write:	15	14	13	12	11	10	9	8
Reset:	0	0	0	0	0	0	0	0

 = Reserved or unimplemented

Figure 3-73 Port AD1 Pull Up Enable Register 1 (PER1AD1)

Read:Anytime.

Write:Anytime.

This register activates a pull-up device on the respective PAD[15:08] pin if the port is used as input. This bit has no effect if the port is used as output. Out of reset no pull-up device is enabled.

PER1AD1[15:8] — Pull Device Enable Port AD1 Register 1
 1 = Pull-up device is enabled.
 0 = Pull-up device is disabled.

Section 4 Functional Description

4.1 General

Each pin except PE0, PE1, and BKGD can act as general purpose I/O. In addition each pin can act as an output from the external bus interface module or a peripheral module or an input to the external bus interface module or a peripheral module.

A set of configuration registers is common to all ports with exceptions in the expanded bus interface and ATD ports (**Table 4-1**). All registers can be written at any time, however a specific configuration might not become active.

Example: Selecting a pull-up device

This device does not become active while the port is used as a push-pull output.

Table 4-1 Register availability per port[1]

Port	Data	Data Direction	Input	Reduced Drive	Pull Enable	Polarity Select	Wired-Or Mode	Interrupt Enable	Interrupt Flag
A	✔	✔	-	✔	✔	-	-	-	-
B	✔	✔	-			-	-	-	-
C	✔	✔	-			-	-	-	-
D	✔	✔	-			-	-	-	-
E	✔	✔	-			-	-	-	-
K	✔	✔	-			-	-	-	-
T	✔	✔	✔	✔	✔	✔	-	-	-
S	✔	✔	✔	✔	✔	✔	✔	-	-
M	✔	✔	✔	✔	✔	✔	✔	-	-
P	✔	✔	✔	✔	✔	✔	-	✔	✔
H	✔	✔	✔	✔	✔	✔	-	✔	✔
J	✔	✔	✔	✔	✔	✔	-	✔	✔
AD0	✔	✔	-	✔	✔	-	-	-	-
AD1	✔	✔	-	✔	✔	-	-	-	-

NOTES:
1. Each cell represents one register with individual configuration bits

4.2 Registers

4.2.1 Data register

This register holds the value driven out to the pin if the pin is used as a general purpose I/O.

Writing to this register has only an effect on the pin if the pin is used as general purpose output. When reading this address, the buffered state of the pin is returned if the associated data direction register bit is set to "0".

If the data direction register bits are set to logic level "1", the contents of the data register is returned. This is independent of any other configuration (**Figure 4-1**).

4.2.2 Input register

This is a read-only register and always returns the buffered state of the pin (**Figure 4-1**).

4.2.3 Data direction register

This register defines whether the pin is used as an input or an output.

If a peripheral module controls the pin the contents of the data direction register is ignored (**Figure 4-1**).
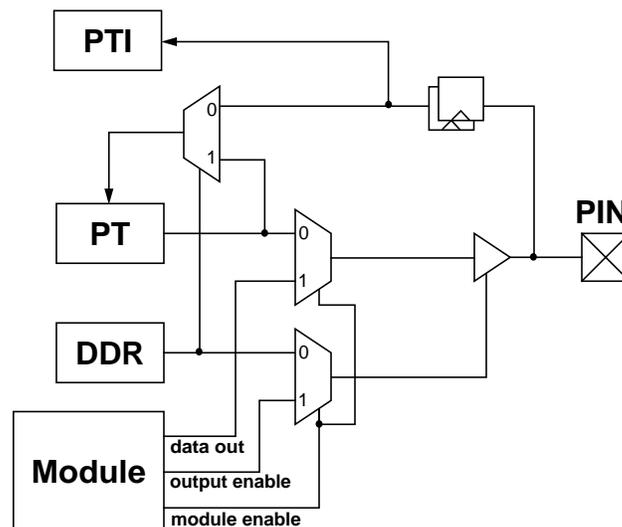
Figure 4-1 Illustration of I/O pin functionality

4.2.4 Reduced drive register

If the pin is used as an output this register allows the configuration of the drive strength.

4.2.5 Pull device enable register

This register turns on a pull-up or pull-down device.

It becomes active only if the pin is used as an input or as a wired-or output.

4.2.6 Polarity select register

This register selects either a pull-up or pull-down device if enabled.

It becomes only active if the pin is used as an input. A pull-up device can be activated if the pin is used as a wired-or output.

If the pin is used as an interrupt input this register selects the active interrupt edge.

4.2.7 Wired-or mode register

If the pin is used as an output this register turns off the active high drive. This allows wired-or type connections of outputs.

4.2.8 Interrupt enable register

If the pin is used as an interrupt input this register serves as a mask to the interrupt flag to enable/disable the interrupt.

4.2.9 Interrupt flag register

If the pin is used as an interrupt input this register holds the interrupt flag after a valid pin event.

4.2.10 Module routing register

This register supports the re-routing of the CAN0, CAN4, SPI0, SPI1, and SPI2 pins to alternative ports. This allows a software re-configuration of the pinouts of the different package options with respect to above peripherals.

> **NOTE:**   *The purpose of the Module Routing Register is to provide maximum flexibility for derivatives with a lower number of MSCAN and SPI modules.*

Table 4-2 Module implementations on derivatives

Number of modules	MSCAN modules					SPI modules		
	CAN0	CAN1	CAN2	CAN3	CAN4	SPI0	SPI1	SPI2
5	✔	✔	✔	✔	✔	-	-	-
4	✔	✔	✔	-	✔	-	-	-
3	✔	✔	-	-	✔	✔	✔	✔
2	✔	-	-	-	✔	✔	✔	-
1	✔	-	-	-	-	✔	-	-

MOTOROLA

4.3 Ports

4.3.1 BKGD pin

The BKGD pin is associated with the S12X_BDM and S12X_EBI modules.

During reset, the BKGD pin is used as MODC input.

4.3.2 Port A, B

Port A pins PA[7:0] and Port B pins PB[7:0] can be used for either general-purpose I/O, or, in 144-pin packages, also with the external bus interface. In this case Port A and Port B are associated with the external address bus outputs ADDR15-ADDR8 and ADDR7-ADDR0, respectively. PB0 is the ADDR0 or $\overline{\text{UDS}}$ output.

4.3.3 Port C, D

Port C pins PC[7:0] and Port D pins PD[7:0] can be used for either general-purpose I/O, or, in 144-pin packages, also with the external bus interface. In this case Port C and Port D are associated with the external data bus inputs/outputs DATA15-DATA8 and DATA7-DATA0, respectively.

These pins are configured for reduced input threshold in certain operating modes (refer to S12X_EBI Block Guide).

>   **NOTE:**   *Port C and D are neither available in 112-pin nor in 80-pin packages.*

4.3.4 Port E

Port E is associated with the external bus control outputs R/$\overline{\text{W}}$, $\overline{\text{LSTRB}}$, $\overline{\text{LDS}}$ and $\overline{\text{RE}}$, the free-running clock outputs ECLK and ECLK2X, as well as with the $\overline{\text{TAGHI}}$, $\overline{\text{TAGLO}}$, MODA and MODB and interrupt inputs $\overline{\text{IRQ}}$ and $\overline{\text{XIRQ}}$.

Port E pins PE[7:2] can be used for either general-purpose I/O or with the alternative functions.

Port E pin PE[7] an be used for either general-purpose I/O or as the free-running clock ECLKX2 output running at the Core Clock rate. The clock output is always enabled in emulation modes.

Port E pin PE[4] an be used for either general-purpose I/O or as the free-running clock ECLK output running at the Bus Clock rate or at the programmed divided clock rate. The clock output is always enabled in emulation modes.

Port E pin PE[1] can be used for either general-purpose input or as the level- or falling edge-sensitive $\overline{\text{IRQ}}$ interrupt input. $\overline{\text{IRQ}}$ will be enabled by setting the IRQEN configuration bit (**3.2.14 IRQ Control Register (IRQCR)**) and clearing the I-bit in the CPU's condition code register. It is inhibited at reset so this pin is initially configured as a simple input with a pull-up.

Port E pin PE[0] can be used for either general-purpose input or as the level-sensitive $\overline{\text{XIRQ}}$ interrupt input. $\overline{\text{XIRQ}}$ can be enabled by clearing the X-bit in the CPU's condition code register. It is inhibited at reset so this pin is initially configured as a high-impedance input with a pull-up.

Port E pins PE[5] and PE[6] are configured for reduced input threshold in certain modes (refer to S12X_EBI Block Guide).

4.3.5 Port K

Port K pins PK[7:0] can be used for either general-purpose I/O, or, in 144-pin packages, also with the external bus interface. In this case Port K pins PK[6:0] are associated with the external address bus outputs ADDR22-ADDR16 and PK7 is associated to the $\overline{\text{EWAIT}}$ input.

Port K pin PE[7] is configured for reduced input threshold in certain modes (refer to S12X_EBI Block Guide).

> **NOTE:**   *Port K is not available in 80-pin packages.*
> *PK[6] is not available in 112-pin packages.*

4.3.6 Port T

This port is associated with the ECT module.

Port T pins PT[7:0] can be used for either general-purpose I/O, or with the channels of the Enhanced Capture Timer.

4.3.7 Port S

This port is associated with SCI0, SCI1 and SPI0.

Port S pins PS[7:0] can be used either for general-purpose I/O, or with the SCI and SPI subsystems.

The SPI0 pins can be re-routed. *Refer to* **3.2.37 Module Routing Register (MODRR)**.

> **NOTE:**   *PS[7:4] are not available in 80-pin packages.*

4.3.8 Port M

This port is associated with the SCI3, CAN4-0 and SPI0.

Port M pins PM[7:0] can be used for either general purpose I/O, or with the CAN, SCI and SPI subsystems.

The CAN0, CAN4 and SPI0 pins can be re-routed. *Refer to* **3.2.37 Module Routing Register (MODRR)**.

> **NOTE:**   *PM[7:6] are not available in 80-pin packages.*

MOTOROLA

4.3.9 Port P

This port is associated with the PWM, SPI1 and SPI2.

Port P pins PP[7:0] can be used for either general purpose I/O, or with the PWM and SPI subsystems.

The pins are shared between the PWM channels and the SPI1 and SPI2 modules. If the PWM is enabled the pins become PWM output channels with the exception of pin 7 which can be PWM input or output. If SPI1 or SPI2 are enabled and PWM is disabled, the respective pin configuration is determined by status bits in the SPI modules.

The SPI1 and SPI2 pins can be re-routed. *Refer to* **3.2.37 Module Routing Register (MODRR)**.

Port P offers 8 I/O pins with edge triggered interrupt capability in wired-or fashion (**4.4 Pin interrupts**).

> **NOTE:**   *PP[6] is not available in 80-pin packages.*

4.3.10 Port H

This port is associated with the SPI1, SPI2, SCI4, and SCI5.

Port H pins PH[7:0] can be used for either general purpose I/O, or with the SPI and SCI subsystems.

Port H pins can be used with the routed SPI1 and SPI2 modules. *Refer to* **3.2.37 Module Routing Register (MODRR)**.

Port H offers 8 I/O pins with edge triggered interrupt capability (**4.4 Pin interrupts**).

> **NOTE:**   *Port H is not available in 80-pin packages.*

4.3.11 Port J

This port is associated with the chip selects $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ as well as with CAN4, CAN0, IIC1, IIC0, and SCI2.

Port J pins PJ[7:4] and PJ[2:0] can be used for either general purpose I/O, or with the CAN, IIC, or SCI subsystems.

If IIC takes precedence the associated pins become IIC open-drain output pins.

The CAN4 pins can be re-routed. *Refer to* **3.2.37 Module Routing Register (MODRR)**.

Port J pins can be used with the routed CAN0 modules. *Refer to* **3.2.37 Module Routing Register (MODRR)**.

Port J offers 7 I/O pins with edge triggered interrupt capability (**4.4 Pin interrupts**).

> **NOTE:**   *PJ[5,4,2] are not available in 112-pin packages.*
> *PJ[5,4,2,1,0] are not available in 80-pin packages.*

4.3.12 Port AD0

This port is associated with the ATD0.

Port AD0 pins PAD07-PAD00 can be used for either general purpose I/O, or with the ATD0 subsystem.

4.3.13 Port AD1

This port is associated with the ATD1.

Port AD1 pins PAD23-PAD08 can be used for either general purpose I/O, or with the ATD1 subsystem.

> **NOTE:**   *PAD[23:16] are not available in 112-pin packages.*
> *PAD[23:08] are not available in 80-pin packages.*

4.4 Pin interrupts

Ports P, H and J offer pin interrupt capability. The interrupt enable as well as the sensitivity to rising or falling edges can be individually configured on per-pin basis. All bits/pins in a port share the same interrupt vector. Interrupts can be used with the pins configured as inputs or outputs.

An interrupt is generated when a bit in the port interrupt flag register and its corresponding port interrupt enable bit are both set. The pin interrupt feature is also capable to wake up the CPU when it is in STOP or WAIT mode.

A digital filter on each pin prevents pulses (**Figure 4-3**) shorter than a specified time from generating an interrupt. The minimum time varies over process conditions, temperature and voltage (**Figure 4-2** and **Table 4-3**).

Glitch, filtered out, no interrupt flag set

Valid pulse, interrupt flag set   uncertain

t_{pign}

t_{pval}
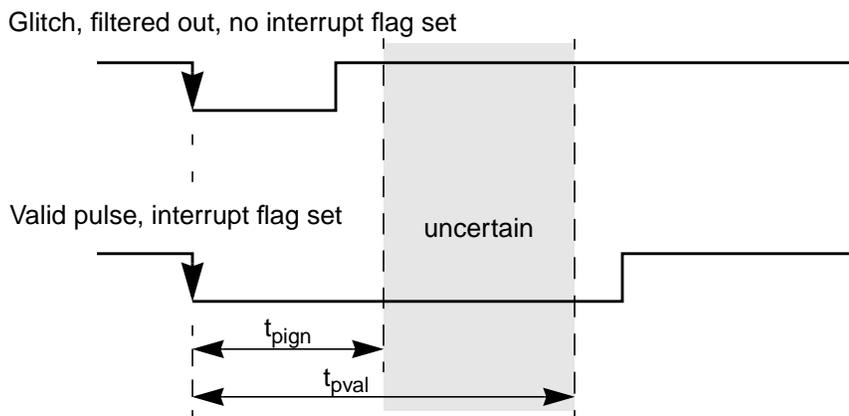
Figure 4-2 Interrupt Glitch Filter on Port P, H and J (PPS=0)

MOTOROLA

Table 4-3 Pulse Detection Criteria

Pulse	Mode		
	$\overline{STOP}$		STOP[1]
		Unit	
Ignored	$t_{pulse} \leq 3$	bus clocks	$t_{pulse} \leq t_{pign}$
Uncertain	$3 < t_{pulse} < 4$	bus clocks	$t_{pign} < t_{pulse} < t_{pval}$
Valid	$t_{pulse} \geq 4$	bus clocks	$t_{pulse} \geq t_{pval}$

NOTES:
1. These values include the spread of the oscillator frequency over temperature, voltage and process.
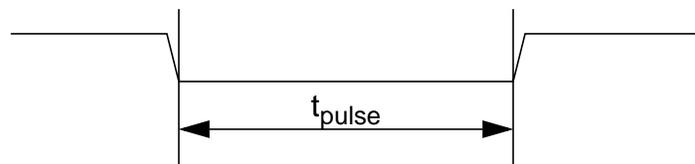
Figure 4-3 Pulse Illustration

A valid edge on an input is detected if 4 consecutive samples of a passive level are followed by 4 consecutive samples of an active level directly or indirectly.

The filters are continuously clocked by the bus clock in RUN and WAIT mode. In STOP mode the clock is generated by an RC-oscillator in the Port Integration Module. To maximize current saving the RC oscillator runs only if the following condition is true on any pin individually:

Sample count <= 4 and interrupt enabled (PIE=1) and interrupt flag not set (PIF=0).

4.5 Expanded bus pin functions

All peripheral ports T, S, M, P, H, J, AD0 and AD1 start up as general purpose inputs after reset.

Depending on the external mode pin condition, the external bus interface related ports A, B, C, D, E, and K start up as general purpose inputs on reset or are configured for their alternate functions.

Table 4-4 lists the pin functions in relationship with the different operating modes. If two entries per pin are displayed, a "mux" indicates time-multiplexing between the two functions and an "or" means that a configuration bit exists which can be altered after reset to select the respective function (displayed in *italics*). *Refer to S12X_EBI Block Guide for details.*

Table 4-4 Expanded Bus Pin Functions vs. Operating Modes

Pin	single-chip modes		expanded modes			
	Normal Single-Chip	Special Single-Chip	Normal Expanded	Emulation Single-Chip	Emulation Expanded	Special Test
PK7	GPIO	GPIO	GPIO *or* $\overline{EWAIT}$	GPIO	GPIO *or* $\overline{EWAIT}$	GPIO
PK[6:4]	GPIO	GPIO	ADDR[22:20] *or* *GPIO*	ADDR[22:20] mux ACC[2:0]	ADDR[22:20] mux ACC[2:0]	ADDR[22:20]
PK[3:0]	GPIO	GPIO	ADDR[19:16] *or* *GPIO*	ADDR[19:16] mux IQSTAT[3:0]	ADDR[19:16] mux IQSTAT[3:0]	ADDR[19:16]
PA[7:0]	GPIO	GPIO	ADDR[15:8] *or* *GPIO*	ADDR[15:8] mux IVD[15:8]	ADDR[15:8] mux IVD[15:8]	ADDR[15:8]
PB[7:1]	GPIO	GPIO	ADDR[7:1] *or* *GPIO*	ADDR[7:1] mux IVD[7:1]	ADDR[7:1] mux IVD[7:1]	ADDR[7:1]
PB0	GPIO	GPIO	$\overline{UDS}$ *or* *GPIO*	ADDR0 mux IVD0	ADDR0 mux IVD0	ADDR0
PC[7:0]	GPIO	GPIO	DATA[15:8] *or* *GPIO*	DATA[15:8]	DATA[15:8]	DATA[15:8] *or* *GPIO*
PD[7:0]	GPIO	GPIO	DATA[7:0]	DATA[7:0]	DATA[7:0]	DATA[7:0]
PE7	GPIO *or* ECLKX2	GPIO *or* ECLKX2	GPIO *or* ECLKX2	ECLKX2	ECLKX2	GPIO *or* ECLKX2
PE6	GPIO	GPIO	GPIO	$\overline{TAGHI}$	$\overline{TAGHI}$	GPIO
PE5	GPIO	GPIO	$\overline{RE}$	$\overline{TAGLO}$	$\overline{TAGLO}$	GPIO
PE4	GPIO *or* ECLK	ECLK *or* *GPIO*	ECLK *or* *GPIO*	ECLK	ECLK	ECLK *or* *GPIO*
PE3	GPIO	GPIO	$\overline{LDS}$ *or* *GPIO*	$\overline{LSTRB}$	$\overline{LSTRB}$	$\overline{LSTRB}$
PE2	GPIO	GPIO	$\overline{WE}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$
PJ5	GPIO	GPIO	GPIO *or* $\overline{CS2}$	GPIO	GPIO *or* $\overline{CS2}$	GPIO *or* $\overline{CS2}$
PJ4	GPIO	GPIO	GPIO or $\overline{CS0}$ [1]	GPIO	GPIO or $\overline{CS0}$ [1]	GPIO *or* $\overline{CS0}$
PJ2	GPIO	GPIO	GPIO *or* $\overline{CS1}$	GPIO	GPIO *or* $\overline{CS1}$	GPIO *or* $\overline{CS1}$
PJ0	GPIO	GPIO	GPIO *or* $\overline{CS3}$	GPIO	GPIO *or* $\overline{CS3}$	GPIO *or* $\overline{CS3}$

MOTOROLA

NOTES:
  1. Depending on ROMON bit. *Refer to Device Guide, S12X_EBI Block Guide and S12X_MMC Block Guide for details.*

4.6 Low Power Options

4.6.1 Run Mode

No low power options exist for this module in run mode.

4.6.2 Wait Mode

No low power options exist for this module in wait mode.

4.6.3 Stop Mode

All clocks are stopped. There are asynchronous paths to generate interrupts from STOP on Port P, H and J.

Section 5 Initialization/Application Information

5.1 Port Data and Data Direction Register writes

It is not recommended to write PORTx and DDRx in a word access. When changing the register pins from inputs to outputs, the data may have extra transitions during the write access. Initialize the port data register before enabling the outputs.

Index

–B–

block diagram 16

–D–

Data direction register 75
Data register 74

–E–

EBI 15
Expanded bus 81

–G–

Glitch Filter 80

–I–

Input register 75
Interrupt enable register 76
Interrupt flag register 76

–M–

Module Routing 52
Module routing register 76

–P–

Pin Configuration 29
Pin interrupts 80
Polarity select register 76
priority 19
Pull device enable register 75

–R–

Reduced drive register 75
register map 26

–W–

Wired-or mode register 76

Block Guide End Sheet

FINAL PAGE OF

88

PAGES

MOTOROLA