OSC_LCP
Block Guide
V01.04

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Motorola, Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
01.00	17-Jul-02	17-Jul-02		Initial Release
01.01	18-Jul-02	18-Jul-02		Format changed to SRS 3.0 Standard
01.02	18-Feb-03	18-Feb-03		- Document number was changed - Author's name was made conditional text. - Sect. 2.3.2: General recommendation for qualification and two disclaimers for overtone resonators were added.
01.03	22-Mar-04	22-Mar-04		The description of the XCLKS signal sampling was substituted by a reference to the DUG.
01.04	17-Jun-04	17-Jun-04		The "Controlled Copy" statement on each page was removed

Table of Contents

List of Figures

List of Tables

Preface

Terminology

ALC = Amplitude Limitation Control

CM = Clock Monitor

CME = Clock Monitor Enable

CRG = Clock and Reset Generator module

LC = Loop Control

RC = Resistor-Capacitor

SCME = Self Clock Mode Enable

VC = Virtual Component

Section 1 Introduction

Figure 1-1 shows a block diagram of the OSC_LCP.

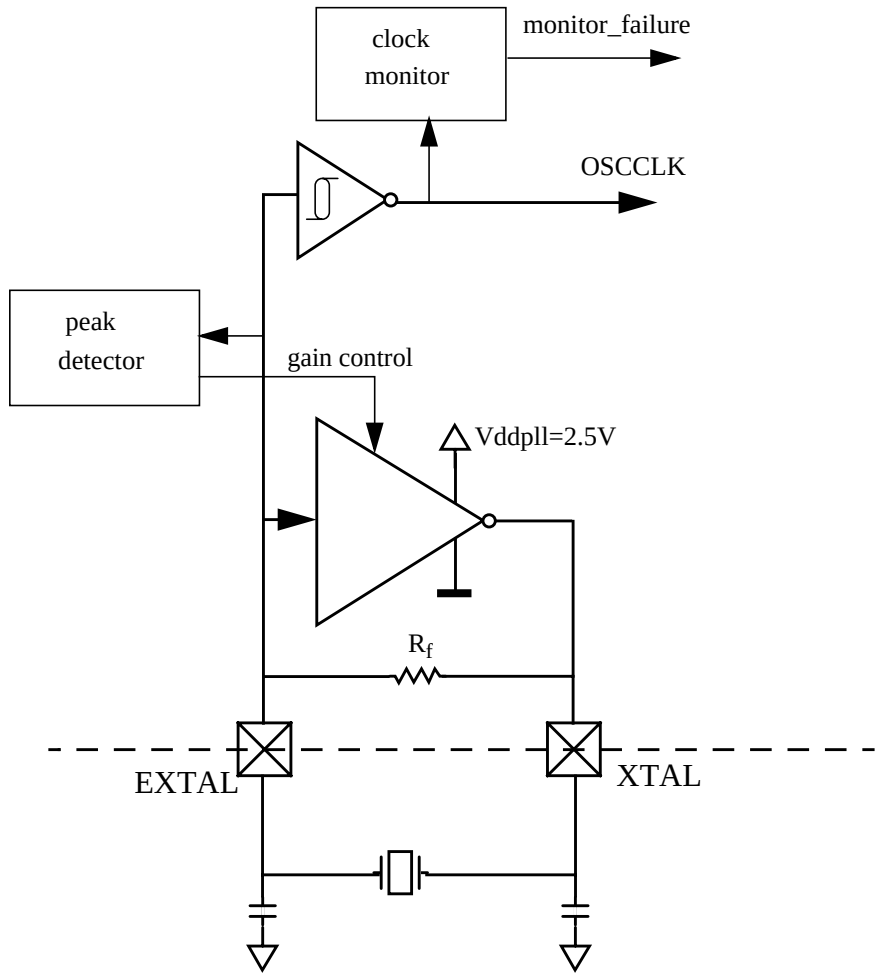


Figure 1-1 OSC_LCP Block Diagram

1.1 Overview

The Pierce Oscillator (OSC_LCP) module provides a robust, low-noise and low-power clock source. The module will be operated from the Vddpll supply rail (2.5 V nominal) and require the minimum number of external components. It is designed for optimal start-up margin with typical crystal oscillators.

1.2 Features

The OSC_LCP will contain circuitry to dynamically control current gain in the output amplitude. This ensures a signal with low harmonic distortion, low power and good noise immunity.

- High noise immunity due to input hysteresis.
- Low RF emissions with peak to peak swing limited dynamically.
- Transconductance (gm) sized for optimum start-up margin for typical oscillators.
- Dynamic gain control eliminates the need for external current limiting resistor.
- Integrated resistor eliminates the need for external bias resistor.
- Low power consumption:
  - Operates from 2.5 V (nominal) supply
  - Amplitude control limits power
- Clock monitor

1.3 Modes of Operation

Two modes of operation exist:

- Loop controlled Pierce oscillator.
- External square wave mode featuring also full swing Pierce without internal feedback resistor.

Section 2 External Signal Description

2.1 Overview

This section lists and describes the signals that connect off chip

2.2 Detailed Signal Descriptions

2.3 Detailed Signal Descriptions

2.3.1 VDDPLL, VSSPLL

Theses pins provides operating voltage (VDDPLL) and ground (VSSPLL) for the OSC_LCP circuitry. This allows the supply voltage to the OSC_LCP to be independently bypassed.

2.3.2 EXTAL, XTAL

These pins provide the interface for either a crystal or a CMOS compatible clock to control the internal clock generator circuitry. EXTAL is the external clock input or the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. The MCU internal system clock is derived from the EXTAL input frequency. In Full Stop Mode (PSTP=0) the EXTAL pin is pulled down by an internal resistor of typical 200k Ohms.

NOTE: *Motorola recommends an evaluation of the application board and chosen resonator or crystal by the resonator or crystal supplier!*

NOTE: *Loop controlled circuit is not suited for overtone resonators and crystals!*

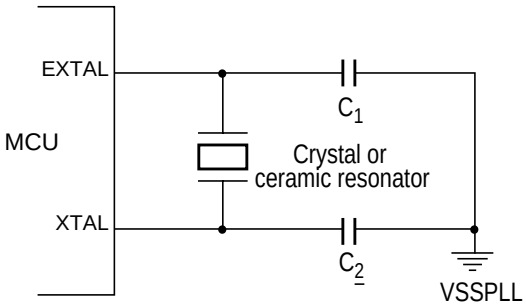
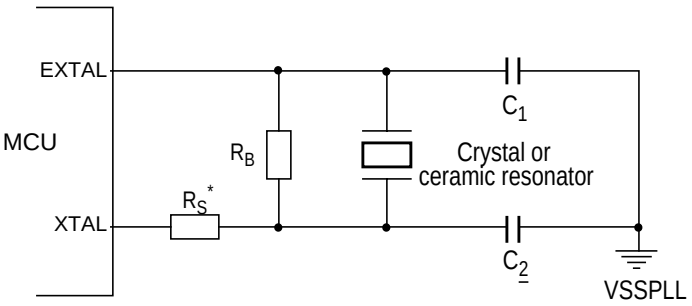


Figure 2-1 Loop Controlled Pierce Oscillator Connections (XCLKS=0)

NOTE: *Full swing Pierce circuit is not suited for overtone resonators and crystals without a careful component selection!*



* R_S can be zero (shorted) when use with higher frequency crystals. Refer to manufacturer's data.

Figure 2-2 Full Swing Pierce Oscillator Connections (XCLKS=1)

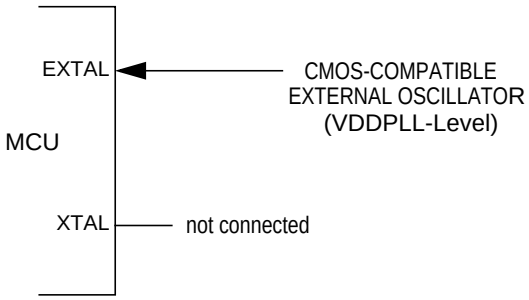


Figure 2-3 External Clock Connections (XCLKS=1)

2.3.3 XCLKS

The XCLKS is an input signal which controls whether a crystal in combination with the internal loop controlled (low power) Pierce oscillator is used or whether full swing Pierce oscillator/external clock circuitry is used. **Refer to device specification for polarity and sampling conditions of the XCLKS pin.** **Table 2-1** lists the state coding of the sampled XCLKS signal.

Table 2-1 Clock Selection Based on XCLKS

XCLKS	Description
0	loop controlled Pierce Oscillator selected
1	full swing Pierce Oscillator/external clock selected

Section 3 Memory Map/Register Definition

The CRG contains the registers and associated bits for controlling and monitoring the oscillator module.

Section 4 Functional Description

The OSC_LCP module has control circuitry to maintain the crystal oscillator circuit voltage level to an optimal level which is determined by the amount of hysteresis being used and the maximum oscillation range.

The oscillator block has two external pins, EXTAL and XTAL. The oscillator input pin, EXTAL, is intended to be connected to either a crystal or an external clock source. The selection of loop controlled Pierce oscillator or full swing Pierce Oscillator/external clock depends on the XCLKS signal which is sampled during reset. The XTAL pin is an output signal that provides crystal circuit feedback.

A buffered EXTAL signal becomes the internal clock. To improve noise immunity, the oscillator is powered by the VDDPLL and VSSPLL power supply pins.

4.1 Gain control

A closed loop control system will be utilized whereby the amplifier is modulated to keep the output waveform sinusoidal and to limit the oscillation amplitude. The output peak to peak voltage will be kept above twice the maximum hysteresis level of the input buffer. Electrical specification details are provided in the Device User Guide Appendix A “Electrical Characteristics”.

4.2 Clock Monitor

The clock monitor circuit is based on an internal RC time delay so that it can operate without any MCU clocks. If no OSCCLK edges are detected within this RC time delay, the clock monitor indicates failure which asserts self clock mode or generates a system reset depending on the state of SCME bit. If the clock monitor is disabled or the presence of clocks is detected no failure is indicated.The clock monitor function is enabled/disabled by the CME control bit, described in the CRG block user guide.

4.3 Wait Mode Operation

During wait mode OSC_LCP is not impacted.

4.4 Stop Mode Operation

OSC_LCP is placed in a static state when the part is in STOP mode except when Pseudo-Stop mode is enabled. During Pseudo-Stop mode OSC_LCP is not impacted.

Section 5 Initialization/Application Information

NA.

Index

Block Guide End Sheet

FINAL PAGE OF
20
PAGES