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MC6805R6

Technical Summary
8-Bit Microcontroller Unit

Introduction

The MC6805R6 is a member of the low-cost, high-performance M6805 Family of 8-bit microcontroller units (MCUs). The M6805 Family is based on the customer specified integrated circuit (CSIC) design strategy. All MCUs in the family use the popular M6805 central processor unit (CPU) and are available with several different subsystems, memory sizes and types, and package types.

The MC6805R6 is a 40-pin device based on the MC6805R3 design. On-chip memory has 3776 bytes of ROM and 112 bytes of static RAM (SRAM). The analog-to-digital (A/D) converter has been expanded to eight channels, and a computer operating properly (COP) system has been added.

Refer to this technical summary for the architecture of the MC6805R6 and a brief description of its subsystems and memory map. For MC6805R6 evaluation support tools, refer to *Evaluation Products*, Motorola document number BR292/D.

Features

- Popular M6805 CPU
- Memory-Mapped Input/Output (I/O) Registers
- 3776 Bytes of ROM
- 112 Bytes of User SRAM
- 24 Bidirectional I/O Pins
- Eight Input-Only Pins
- Eight-Channel Analog-to-Digital (A/D) Converter
- Eight-Bit Timer with Programmable Seven-Bit Prescaler
- Self-Check Mode
- Computer Operating Properly (COP) Watchdog Reset
- On-Chip Oscillator
- Low-Voltage Inhibit Circuit
- 40-Pin Dual In-Line Package (DIP)
- 44-Pin Plastic Leaded Chip Carrier (PLCC)

Ordering Information

Package Type	Order Number
40-Pin DIP	MC6805R6
44-Pin PLCC	MC6805R6FN

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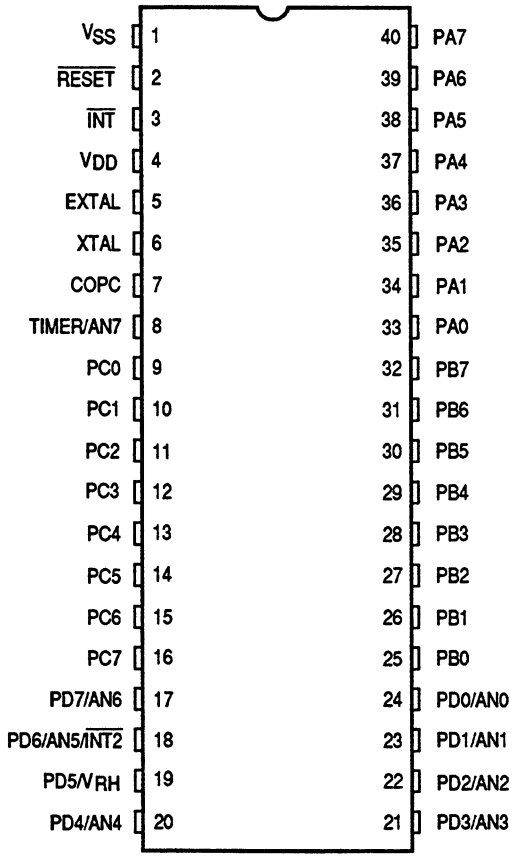
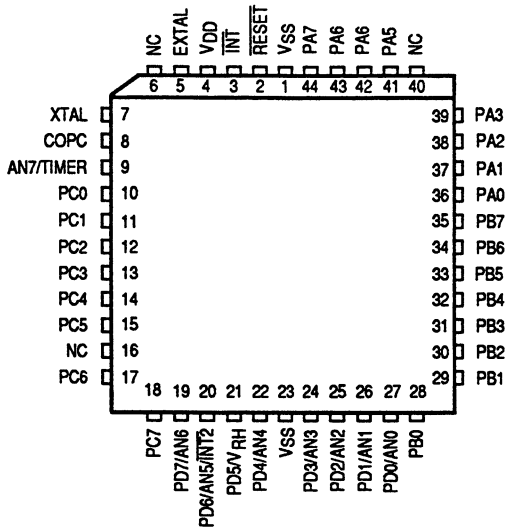
Register Index

Pin Assignments

The following figures show the pin assignments of the DIP and PLCC packages.

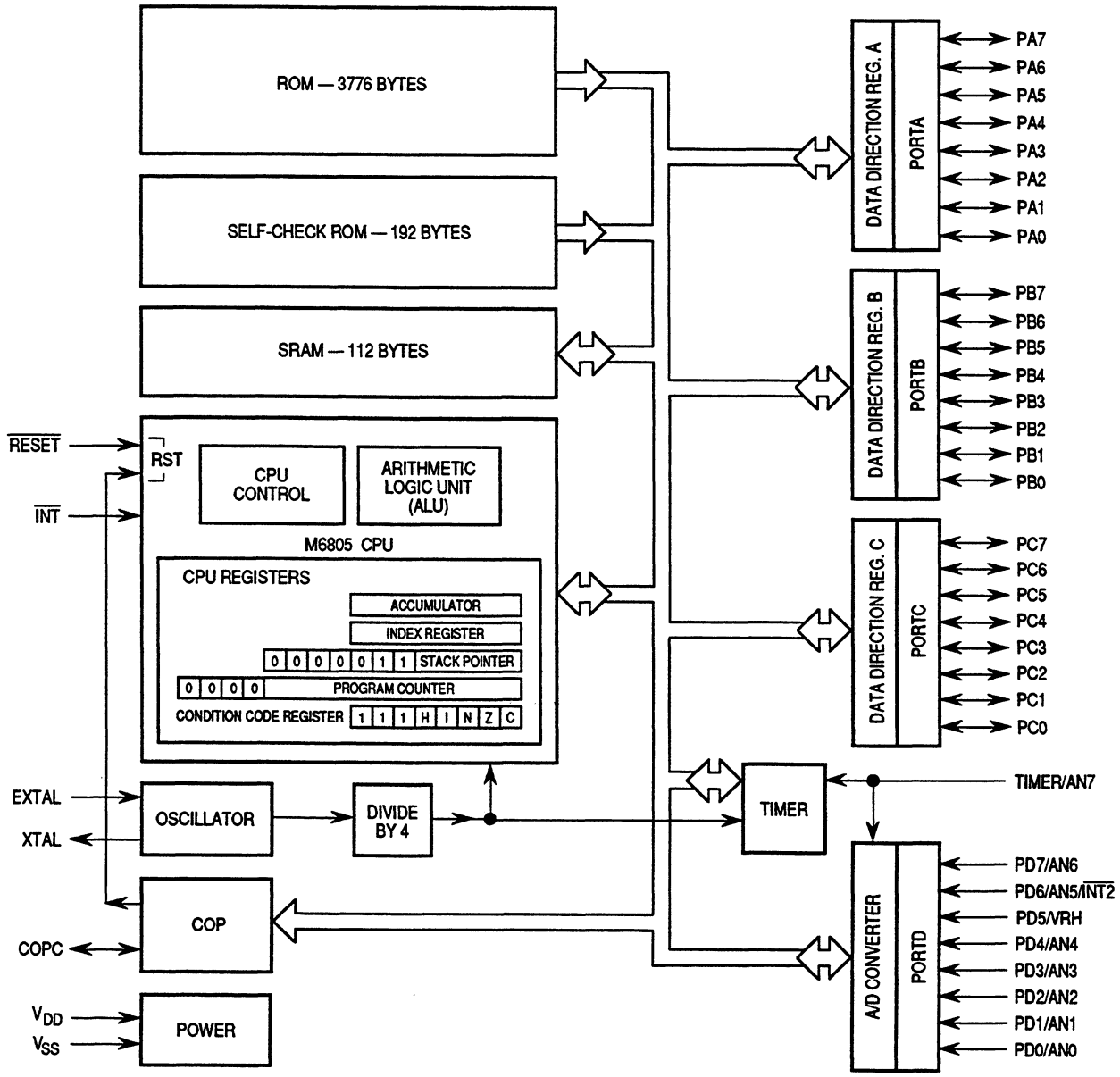




Pin Assignments

MCU Structure

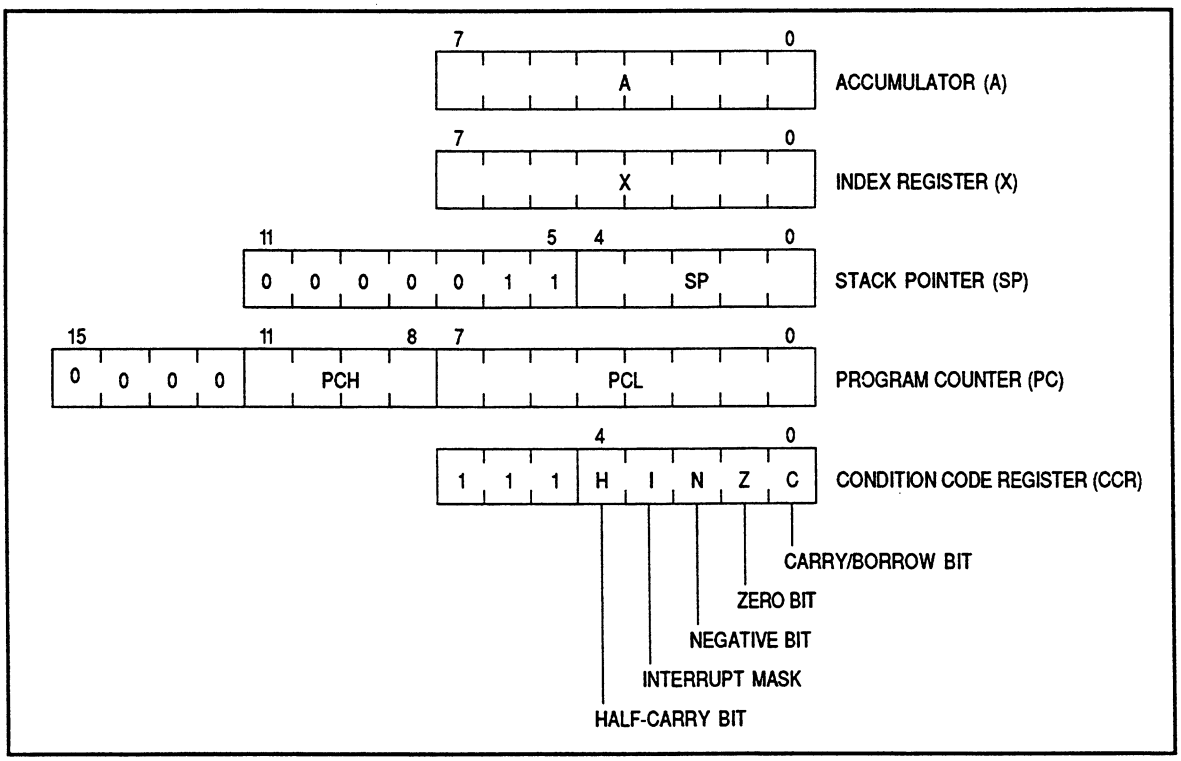
The following figure shows the structure of the MC6805R6 MCU.



Block Diagram

Central Processor Unit Registers

Five CPU registers are available to the programmer.



CPU Registers

The 8-bit accumulator holds operands and results of arithmetic and non-arithmetic operations.

The 8-bit index register is used for indexed addressing.

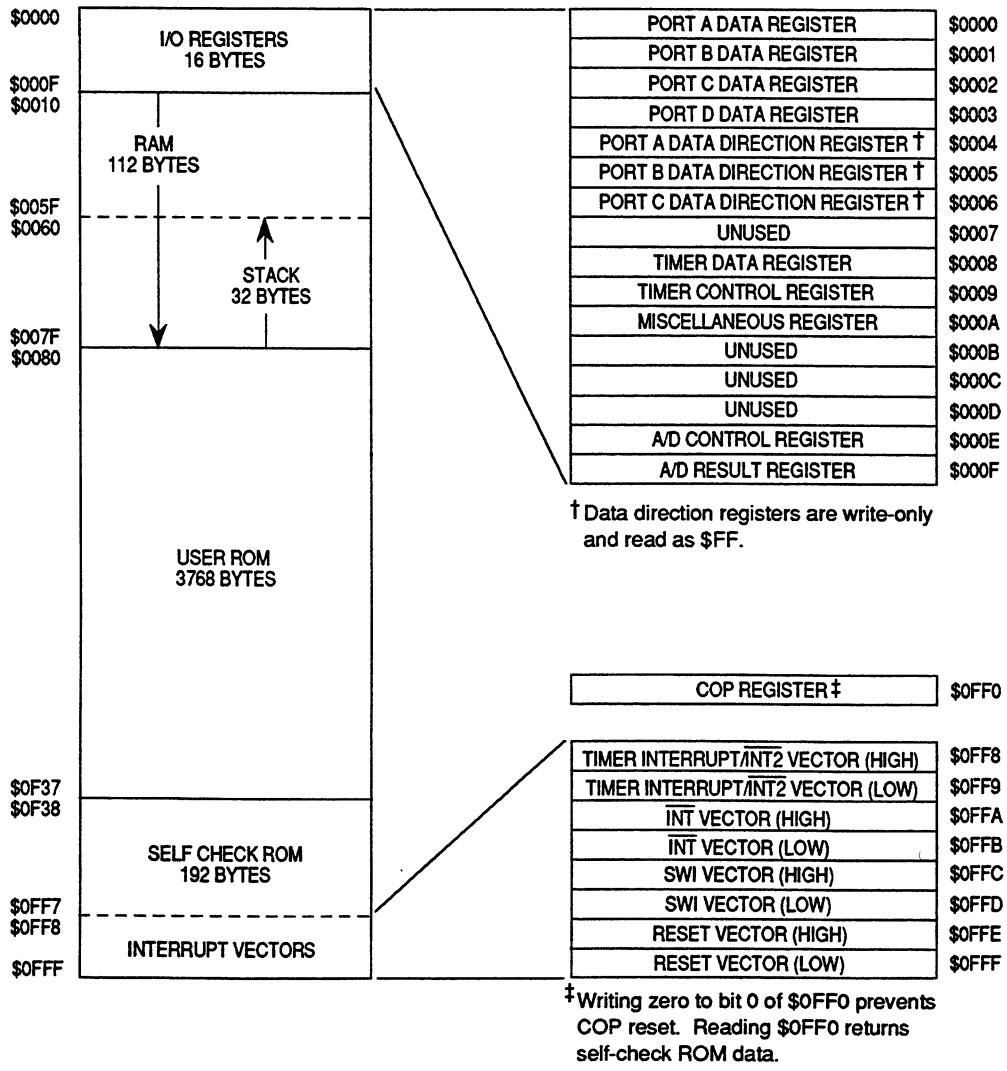
The 12-bit program counter contains the address of the next byte to be fetched.

The 12-bit stack pointer contains the address of the next free location on the stack.

The 5-bit condition code register has four bits that indicate the results of the instruction just executed. A fifth bit is the interrupt mask.

Memory Map

The MCU can address 4096 bytes of memory space. The following figures show the organization of the on-chip memory.



Memory Map

Register and Control Bit Assignments

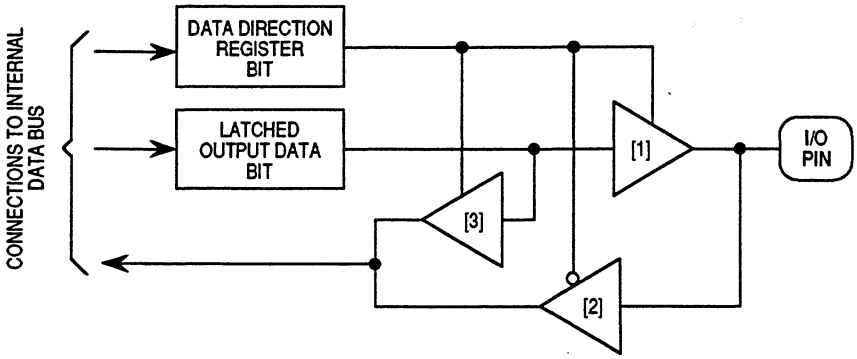
	Bit 7	6	5	4	3	2	1	Bit 0	
$0000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$0001	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$0002	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$0004	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0	DDRA
$0005	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0	DDRB
$0006	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0	DDRC
$0007	—	—	—	—	—	—	—	—	UNUSED
$0008	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0	TDR
$0009	TIR	TIM	TIN	TIE	PSC	PS2	PS1	PS0	TCR
$000A	IR	IM	—	—	—	—	—	—	MR
$000B	—	—	—	—	—	—	—	—	UNUSED
$000C	—	—	—	—	—	—	—	—	UNUSED
$000D	—	—	—	—	—	—	—	—	UNUSED
$000E	CCF	—	—	—	ACR3	ACR2	ACR1	ACR0	ACR
$000F	ARR7	ARR6	ARR5	ARR4	ARR3	ARR2	ARR1	ARR0	ARR

I/O Port Registers

The 8-bit ports A, B, and C are bidirectional. To configure any port pin as an output, set the corresponding data direction register (DDR) bit to a logical one. To use a port pin as an input, clear its DDR bit. A reset clears all DDR bits, configuring all I/O pins as inputs.

The DDRs are write-only registers that always read as $FF.

The 8-bit port D is an input-only port that shares its pins with the A/D converter.



[1] This output buffer enables the latched output to drive the pin when DDR bit is 1 (output mode).
[2] This input buffer is enabled when DDR bit is 0 (input mode).
[3] This input buffer is enabled when DDR bit is 1 (output mode).

I/O Port Circuit

I/O Pin Functions

R/$\overline{W}$*	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch, which drives the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in output mode. The output data latch is read.

*R/$\overline{W}$ is an internal signal.

PORT A — Port A Data Register **$0000**

	Bit 7	6	5	4	3	2	1	Bit 0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	NOT CHANGED BY RESET							

DDRA — Data Direction Register for Port A **$0004**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
RESET:	0	0	0	0	0	0	0	0

DDRA7–DDRA0 — Port A Data Direction

These write-only bits determine whether the PA7–PA0 pins are inputs or outputs.

1 = Corresponding port pin configured as output
0 = Corresponding port pin configured as input

PORT B — Port B Data Register **$0001**

	Bit 7	6	5	4	3	2	1	Bit 0
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
RESET:	NOT CHANGED BY RESET							

DDRB — Data Direction Register for Port B **$0005**

	Bit 7	6	5	4	3	2	1	0
	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
RESET:	0	0	0	0	0	0	0	0

DDRB7–DDRB0 — Port B Data Direction

These write-only bits determine whether the PB7–PB0 pins are inputs or outputs.

1 = Corresponding port pin configured as output

0 = Corresponding port pin configured as input

PORT C — Port C Data Register **$0002**

	Bit 7	6	5	4	3	2	1	0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	NOT CHANGED BY RESET							

DDRC — Data Direction Register for Port C **$0006**

	Bit 7	6	5	4	3	2	1	0
	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
RESET:	0	0	0	0	0	0	0	0

DDRC7–DDRC0 — Port C Data Direction

These write-only bits determine whether the PC7–PC0 pins are inputs or outputs.

1 = Corresponding port pin configured as output

0 = Corresponding port pin configured as input

PORT D — Port D Data Register **$0003**

	Bit 7	6	5	4	3	2	1	Bit 0
	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	NOT CHANGED BY RESET							

Resets and Interrupts

A CPU reset occurs under the following conditions:

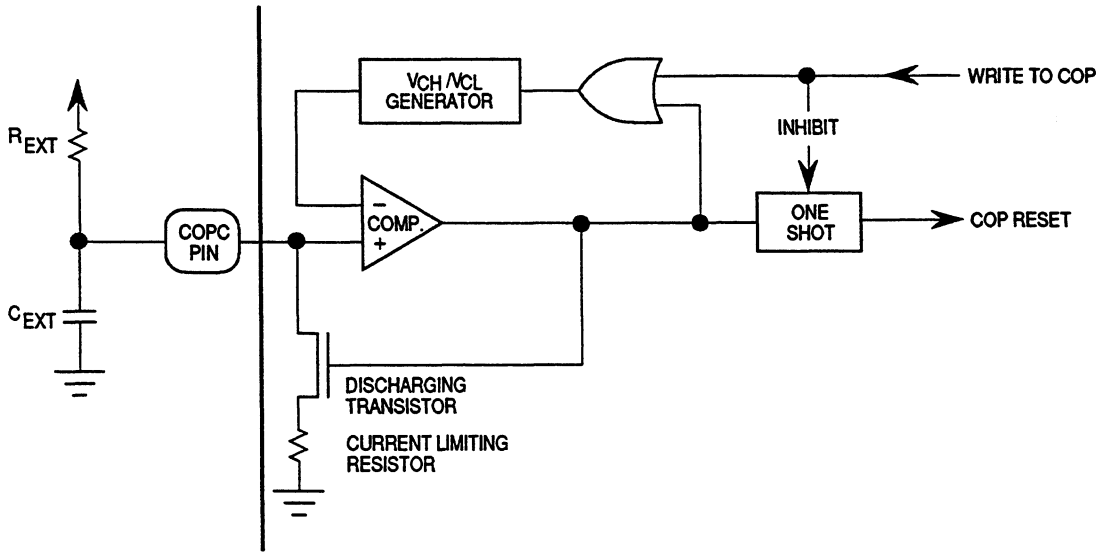
- A power-on reset (POR) is generated when a positive transition occurs on the V_{DD} pin.
- A reset is generated when an external logical zero is applied to the $\overline{\text{RESET}}$ pin.
- The computer operating properly (COP) circuit resets the CPU if the CPU is not serviced by a program sequence within a specific period of time. When the voltage on the COPC pin, generated by an external resistor capacitor (RC) circuit, rises above the internal comparator's reference, a COP reset occurs. Clearing bit 0 of the COP register, located at $0FF0, discharges the voltage on the COPC pin.

COP — Computer Operating Properly Register **$0FF0**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	—	—	—	—	—	COPR
RESET:	—	—	—	—	—	—	—	0

COPR — COP Reset

Clearing this bit discharges the voltage on the COPC pin, preventing a COP reset.



COP Circuit

The following internal actions occur on reset:

- The interrupt mask (I) in the condition code register is set, inhibiting interrupts.
- The stack pointer is loaded with $7F.
- Data direction bits are cleared, making all I/O pins inputs.
- The $\overline{\text{INT}}$ logic is cleared.
- The timer is loaded with $FF.
- The timer prescaler is loaded with $7F.
- The timer control register is loaded with $7F.
- The miscellaneous register is loaded with $7F.
- The program counter is loaded with the reset vector.

The CPU can be interrupted in the following ways:

- An interrupt is executed by the nonmaskable software interrupt instruction (SWI).
- A timer interrupt is requested when the timer decrements to zero. Setting the timer interrupt mask (TIM) in the timer control register disables timer interrupts. Refer to **Timer**.
- An external interrupt is requested when a falling edge occurs on the $\overline{\text{INT}}$ pin.
- An external interrupt is requested when a falling edge occurs on the $\overline{\text{INT2}}$ pin. Setting the interrupt mask (IM) in the miscellaneous register disables $\overline{\text{INT2}}$ interrupts.

MR — Miscellaneous Register **$000A**

	Bit 7	6	5	4	3	2	1	Bit 0
	IR	IM	—	—	—	—	—	—
RESET:	0	1	U	U	U	U	U	U

IR — Interrupt 2 Request
1 = $\overline{\text{INT2}}$ interrupt requested
0 = $\overline{\text{INT2}}$ interrupt not requested

IM — Interrupt 2 Mask
1 = $\overline{\text{INT2}}$ interrupt inhibited
0 = $\overline{\text{INT2}}$ interrupt enabled

The following actions occur as a result of an interrupt:

- The CPU registers are stored in the stack in the order PCL, PCH, X, A, CCR.
- The interrupt mask (I) in the condition code register is set to prevent additional interrupts.
- The program counter is loaded with the appropriate interrupt vector (SWI, $\overline{\text{INT}}$, or timer/$\overline{\text{INT2}}$).
- The RTI (return from interrupt) instruction causes the CPU registers to be recovered from the stack in the order CCR, A, X, PCH, PCL. Normal processing resumes.

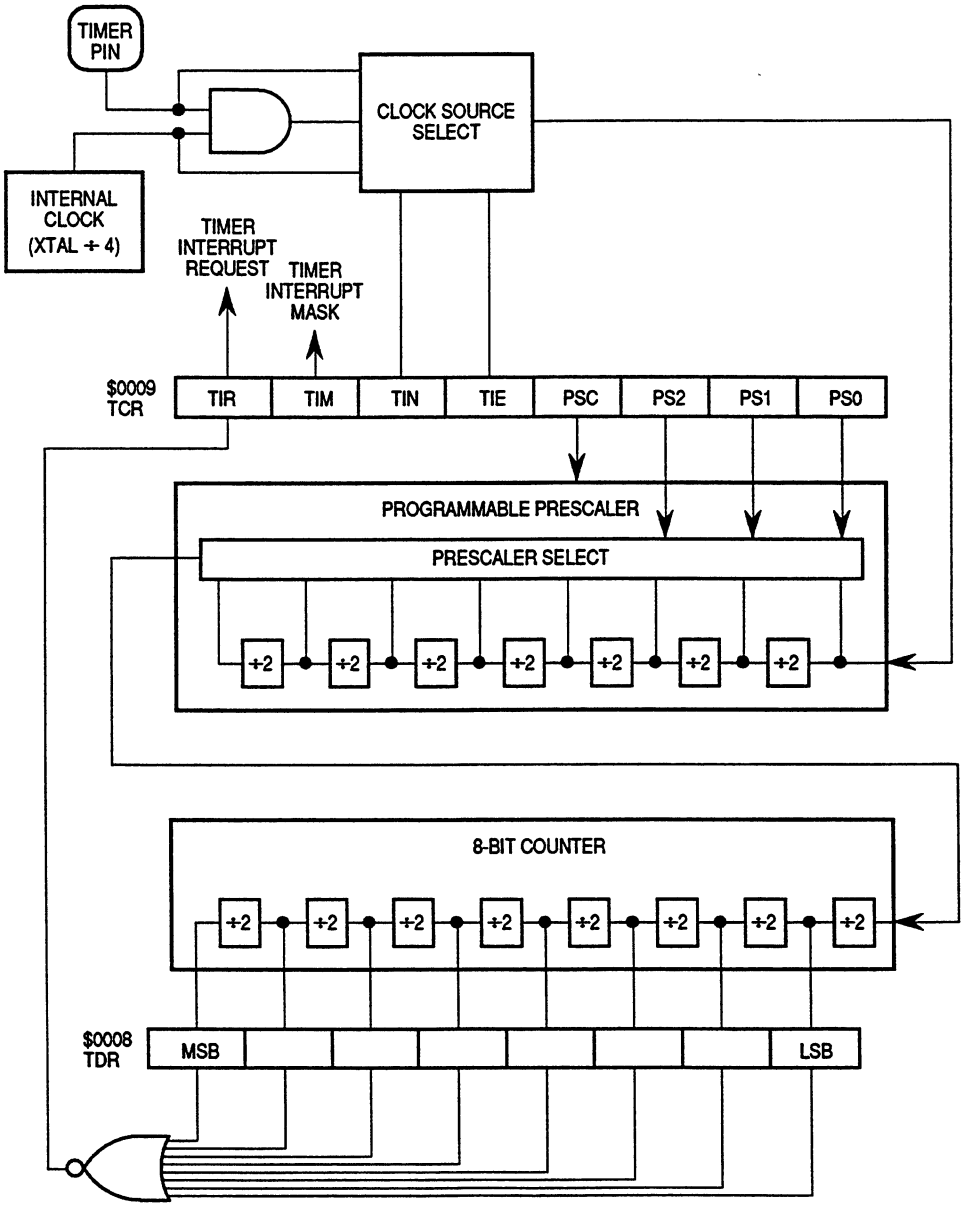
Low-Voltage Inhibit

The optional low-voltage detection circuit is a mask option that causes a reset of the MCU when the power supply voltage falls below a certain level (V_{LVI}). The output from the low-voltage detector is connected to the internal reset circuitry directly. It forces the $\overline{\text{RESET}}$ pin low with a strong discharge device through a resistor. The internal reset is removed once the power supply voltage rises above a recovery level (V_{LVR}), at which time a normal power-on reset occurs.

Timer

The timer consists of an 8-bit software-programmable counter driven by a 7-bit software-programmable prescaler.

The counter is loaded under program control and decrements toward $00. When the counter reaches $00, the timer interrupt request bit (TIR) in the timer control register (TCR) is set. Refer to the timer block diagram.



Timer Block Diagram

TDR — Timer Data Register **$0008**

	Bit 7	6	5	4	3	2	1	Bit 0
	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
RESET:	1	1	1	1	1	1	1	1

The read-only TDR contains the current counter value. Reading the TDR does not disturb the counting process.

TCR — Timer Control Register **$0009**

	Bit 7	6	5	4	3	2	1	Bit 0
	TIR	TIM	TIE	TPE	PSC	PS2	PS1	PS0
RESET:	0	1	1	1	U	1	1	1

U = UNAFFECTED

TIR — Timer Interrupt Request

This read/write bit is automatically set when the counter rolls over from $FF to $00. TIR must be cleared by software.

TIM — Timer Interrupt Mask

This read/write bit enables timer interrupts.

1 = Interrupt inhibited
0 = Interrupt enabled

TIE— Timer Internal/External

This read/write bit selects either the internal or the external clock.

1 = External clock selected
0 = Internal clock selected

TPE — Timer Pin Enable

This read/write bit enables the timer pin.

1 = Timer pin enabled
0 = Timer pin disabled

Clock Selection

TIE:TPE	Clock Source
00	Internal Clock
01	AND of Internal and External Clocks
10	No Clock
11	External Clock

PSC — Prescaler Clear

This write-only bit resets the prescaler. PSC always reads as zero.

1 = Prescaler cleared
0 = No effect

PS[2:0] — Prescaler

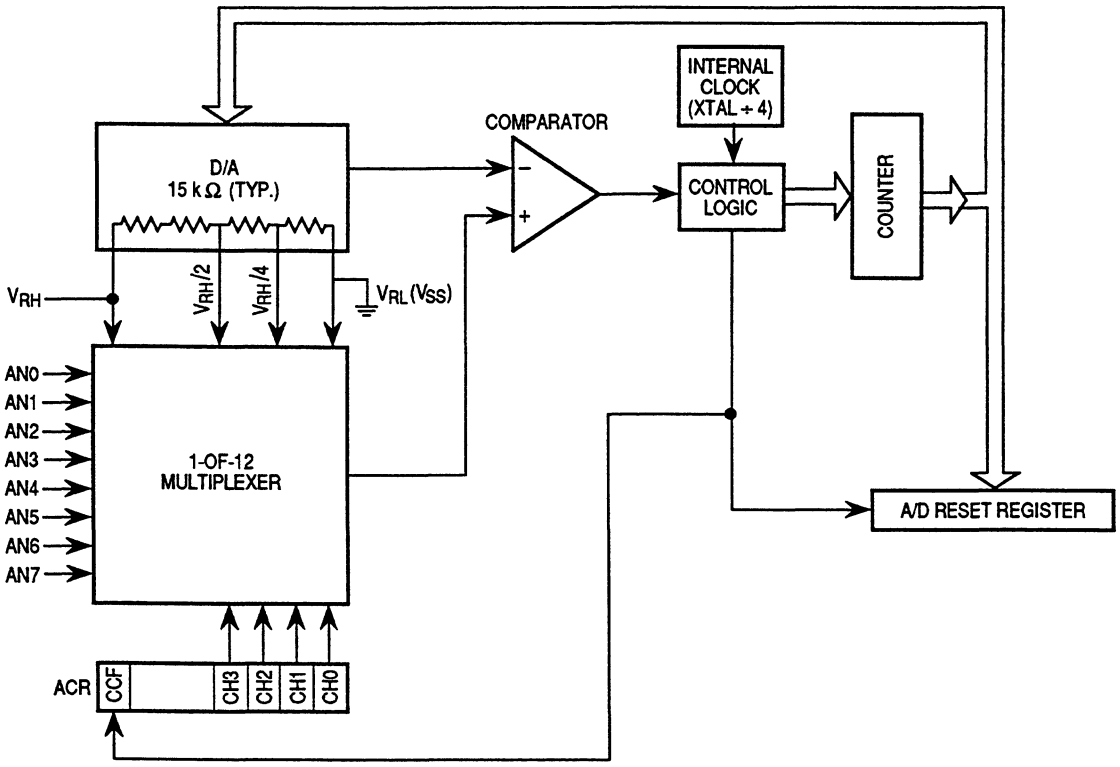
These read/write bits select one of the seven prescaler outputs.

Prescaler Select

PS[2:0]	Divide By
000	1 (Bypass Prescaler)
001	2
010	4
011	8
100	16
101	32
110	64
111	128

Analog-to-Digital Converter

The 8-bit analog-to-digital (A/D) converter uses a successive approximation technique to convert selected analog inputs continuously. One of eight analog inputs can be multiplexed to the A/D converter through AN0–AN7. A conversion of the sampled analog input occurs every 30 internal clock cycles. Whenever the A/D control register is written to, the conversion complete flag (CCF) is cleared and a new conversion begins. When the conversion is complete, the digitized value of the analog sample is placed in the A/D result register.



A/D Converter Block Diagram

ACR — A/D Control Register **$000E**

	Bit 7	6	5	4	3	2	1	Bit 0
	CCF	—	—	—	CH3	CH2	CH1	CH0
RESET:	0	—	—	—	0	0	0	0

CCF — Conversion Complete Flag
1 = Conversion result available in A/D result register
0 = Conversion result not yet available

CH[3:0] — Channel Select Bits

These read/write bits select one of the 12 A/D channels.

ACR Channel Select Map

CH[3:0]	Channel
0000	AN0
0000	AN1
0010	AN2
0011	AN3
0100	VRH
0101	VRL
0110	VRH ÷ 4
0111	VRH ÷ 2
1000	AN4
1001	AN5
1010	AN6
1011	AN7
1100	VRH
1101	VRL
1110	VRH ÷ 4
1111	VRH ÷ 2

ARR — A/D Result Register **$000F**

	Bit 7	6	5	4	3	2	1	Bit 0
	ARR7	ARR6	ARR5	ARR4	ARR3	ARR2	ARR1	ARR0
RESET:	NOT CHANGED BY RESET							

This 8-bit register contains the result of the most recent A/D conversion.

Notes

Notes

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