MC9S12XD-Family

Product Brief

NeXt Generation 16-Bit Microcontroller Family

Targeted at automotive multiplexing applications, the MC9S12X MCU family will deliver 32-bit performance with all the advantages and efficiencies of a 16 bit MCU. The design goal is to retain the low cost, power consumption, EMC and code-size efficiency advantages currently enjoyed by users of Motorola's existing 16-Bit MC9S12 MCU family.

Based around an enhanced S12 core, the MC9S12XD-Family will deliver 2 to 5 times the performance of a 25MHz S12 whilst retaining a high degree of pin and code compatibility with the S12.

The MC9S12XD-Family introduces the performance boosting **XGATE** module. Using enhanced DMA functionality, this parallel processing module offloads the CPU by providing high speed data processing and transfer between peripheral modules, RAM and I/O ports. Providing up to 80MIPS of performance additional to the CPU, the XGATE can handle 64 channels and is fully user programmable.

The MC9S12XD-Family will feature the enhanced **MXCAN** module which, when used in conjunction with XGATE, delivers **FULL CAN** performance with virtually unlimited number of mailboxes and retains backwards compatibility with the MSCAN module featured on existing S12 products.

Memory options will initially range from 128K to 1MByte of Motorola's industry-leading, full automotive spec SG-Flash with additional integrated EEPROM. In addition to the rich S12 peripheral set, the MC9S12XD-Family will feature more RAM, extra A/D channels, new timer features and additional LIN-compatible SCI ports compared with the S12 D-Family. The MC9S12XD-Family also features a new flexible interrupt handler which allows multilevel nested interrupts.

The MC9S12XD-Family has full 16-bit data paths throughout. The non-multiplexed expanded bus interface available on the 144-Pin versions allows an easy interface to external memories. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. System power consumption is further improved with the new “fast exit from STOP mode” feature and an ultra low power wake-up timer.

In addition to the I/O ports available in each module, up to 25 further I/O ports are available with interrupt capability allowing Wake-Up from STOP or WAIT mode.

The MC9S12XD-Family will be available in 144-Pin LQFP (with optional external bus), 112-Pin or 80-Pin options.

Feature Detail

- **16-Bit CPU (Enhanced S12 Core – CPU12)**
  - — Additional (superset) instructions to improve 32 bit calculations and semaphore handling
  - — Now possible to access large data segments independent of PPAGE

- **New XGATE Module**
  - — Programmable, high performance DMA module – up to 80 MIPS RISC performance
  - — Transfers data to or from all peripherals and RAM without CPU intervention or CPU wait states
  - — Can perform simple operations on data (logical, shifts, arithmetic, bit operations)

— Enables Full CAN capability when used in conjunction with MXCAN module
— Full LIN master or slave capability when used in conjunction with the six integrated LIN SCI modules
— Can interrupt the HCS12X CPU signalling transfer completion
— Triggers from any hardware module as well as from the CPU possible

- **Non-Multiplexed External Bus**
  - — 22 address/16 data wide
  - — Support for external WAIT input or internal wait cycles to adapt MCU speed to peripheral speed requirements
  - — Upto three chip select outputs to select 16K, 2M and 4MByte address spaces
  - — Supports glueless interface to popular asynchronous RAMs and Flash devices
  - — External address space 4MByte for Data and Program space (144 pin package only)

- **System Integration Modules – including Enhanced Interrupt Controller**
  - — CRG (windowed COP watchdog, real time interrupt, clock monitor, clock generation and reset)
  - — EBI (non-multiplexed external bus interface)
  - — INT (interrupt control) with 8 levels of nested interrupt, new flexible assignment of interrupt sources to each interrupt level.

- **Five MXCAN Modules with FULL CAN capability when used in conjunction with XGATE**
  - — CAN 2.0 A, B software compatible. Five receive and three transmit buffers
  - — Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - — Four separate interrupt channels for Receive, Transmit, Error and Wake-up
  - — Low-pass filter wake-up function in STOP mode
  - — Loop-back for self test operation

NUMBER OF CANS

The number of CAN Modules (four or five) is under discussion. In case of four CAN modules all references to CAN3 should be ignored

- **Memory options**
  - — 128K, 256K, 512K and 1M Byte Flash EEPROM
  - — 2K or 4K Byte EEPROM
  - — 12K, 16K, 20K, 32K Byte RAM

- **Real Time Interrupt**
  - — Timed interrupt for task scheduling purposes or cyclic wake-up from low power modes

- **Enhanced Capture Timer**
  - — Featuring improved divide by 1 … 256 pre-scaler allowing greater resolution (e.g. down to 1 usec)
  - — 16-bit main counter with 8-bit prescaler
  - — 8 programmable input capture or output compare channels; 4 of the 8 input captures with buffer
  - — Input capture filters and buffers, three successive captures on four channels, or two captures on four channels with a capture/compare selectable on the remaining four
  - — Four 8-bit or two 16-bit pulse accumulators
  - — 16-bit modulus down-counter with 8-bit prescaler
  - — Enhanced delay counter configurations for signal filtering

- **Periodic Interrupt Timer**
  - — four 16-bit counter internal counters
    - Two independent 8-bit prescalers allowing flexible timebase settings
  - — Especially suited for operating system time ticks and accuract software timeouts

- **Analog-to-Digital Converters**
  - — One 8-channel and one 16 channel module with 10-bit resolution

— External as well as internal conversion trigger capability

• 8 PWM channels with programmable period and duty cycle (7 channels on 80 Pin Packages)
— 8-bit, 8-channel or 16-bit, 4-channel
— Separate control for each pulse width and duty cycle
— Center- or left-aligned outputs
— Programmable clock select logic with a wide range of frequencies

• Serial interfaces
— Up to six asynchronous serial communications interfaces (SCI) supporting LIN Master applications
— Three synchronous serial peripheral interfaces (SPI)
— Two IIC supporting 400kbps clock rates

• Clock generation
— Phase-locked loop clock frequency multiplier
— Self clock mode in absence of external clock
— Clock Monitor
— Low power Pierce oscillator utilizing a 0.5 to 16 MHz crystal
— or full drive Pierce 0.5MHz - 40MHz crystal oscillator reference clock

• Wake-up interrupt inputs depending on the package option
— 8-bit port H shared with SPI1, SPI2 or SCI4 and SCI5
— 2-bit port J1:0 shared with SCI2
— 1-bit Port J2 shared with chip select output
— 2-bit port J5:4 shared with IIC1 or two chip select outputs
— 2-bit port J7:6 shared with IIC0
— 8-bit port P shared with PWM or SPI1 or SPI2

• Operating frequency for ambient temperatures T_a -40°C <= T_a <= 125°C
— 80MHz equivalent to 40MHz Bus Speed for single chip mode

• Internal 3.3V-10% - 5V+10% to 2.5V Regulator

• 144-Pin LQFP or 112-Pin LQFP or 80-Pin QFP package
— I/O lines with 5V input and drive capability
— 112 Pin and 80 Pin Packages compatible with popular HCS12D and B-Family members
— 5V A/D converter inputs and 5V I/O
— 2.5V logic supply

• Development support
— Single-wire background debug™ mode (BDM)
— On-chip hardware breakpoints
— On-Chip COF (Change of flow) trace buffer

Table 1 List of MC9S12XD-Family members

Flash	RAM	EEPROM	Package	Device	XGATE	CAN	SCI	SPI	IIC	A/D	PWM	I/O
1M	32K	4K	144LQFP	9S12XDP100	yes	5	6	3	2	2/24	8	119
			112LQFP	9S12XDP100	yes	5	4	3	1	2/16	8	91
768K	32K	4K	144LQFP	9S12XDP768	yes	5	6	3	2	2/24	8	119
			112LQFP	9S12XDP768	yes	5	4	3	1	2/16	8	91
512K	20K	4K	144LQFP	9S12XDP512	yes	5	6	3	2	2/24	8	119
			112LQFP	9S12XDP512	yes	5	4	3	1	2/16	8	91
			80QFP	9S12XDT512	yes	3	2	2	1	1/8	7	59

Table 1 List of MC9S12XD-Family members

Flash	RAM	EEPROM	Package	Device	XGATE	CAN	SCI	SPI	IIC	A/D	PWM	I/O
384K	20K	4K	144LQFP	9S12XDP384	yes	5	6	3	2	2/24	8	119
			112LQFP	9S12XDP384	yes	5	4	3	1	2/16	8	91
			80QFP	9S12XDT384	yes	3	2	2	1	1/8	7	59
256K	16K	4K	144LQFP	9S12XDT256	yes	3	3	3	1	2/24	8	119
			112LQFP	9S12XDT256	yes	3	4	3	1	2/16	8	91
			80QFP	9S12XDT256	yes	3	2	2	1	1/8	7	59
128K	12K	2K	112LQFP	9S12XDG128	yes	2	3	3	1	2/16	8	91
			80QFP	9S12XDG128	yes	2	2	2	1	1/8	7	59

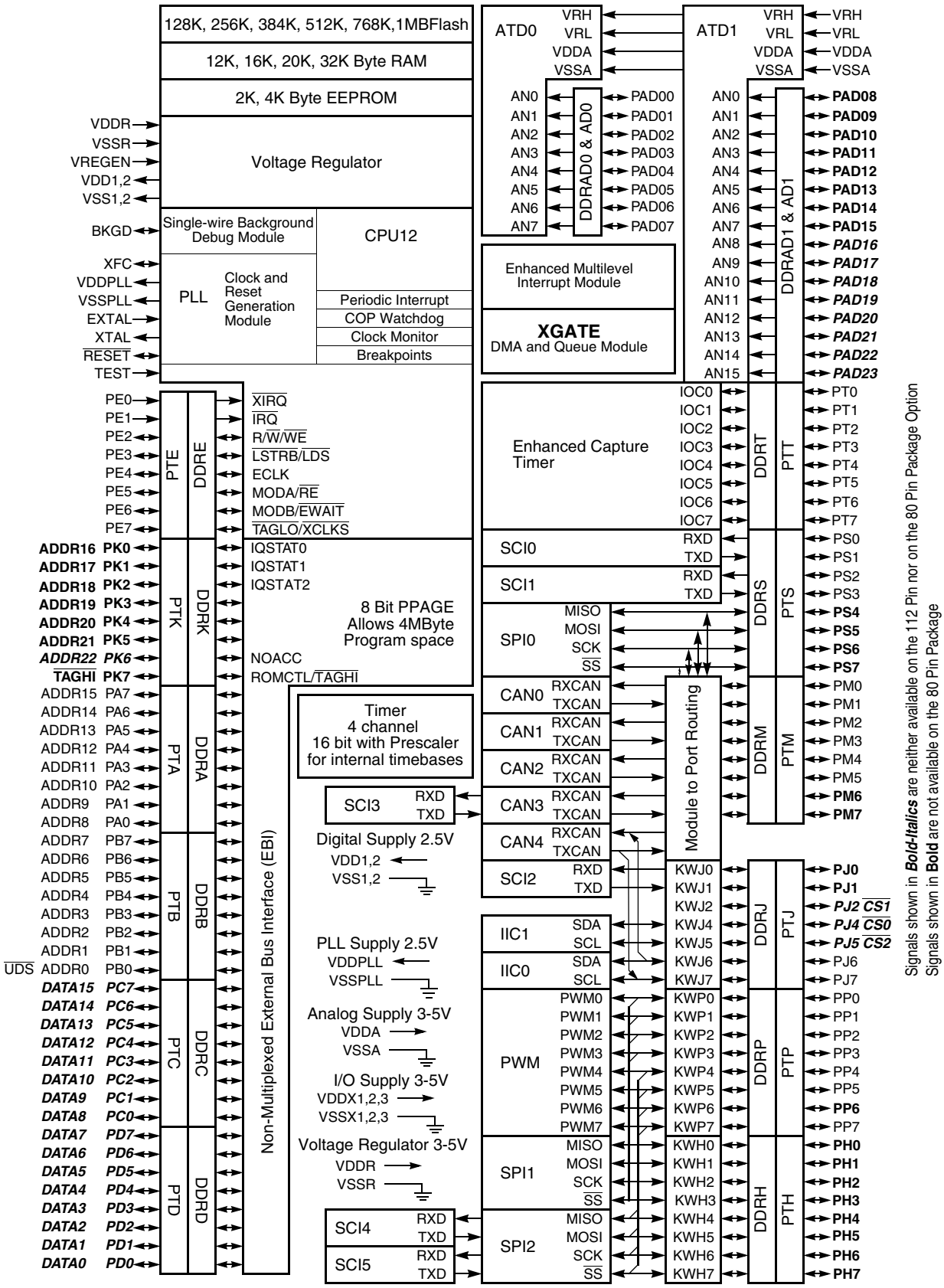
- **Pin out explanations:**
  - A/D is the number of modules/total number of A/D channels.
  - I/O is the sum of ports capable to act as digital input or output.

    144 Pin Packages:
    Port A = 8, B = 8, C=8, D=8, E = 6 + 2 input only, H = 8, J = 7, K = 8, M = 8, P = 8, S = 8, T = 8, PAD = 24
    25 inputs provide Interrupt capability (H =8, P= 8, J = 7, IRQ, XIRQ)

    112 Pin Packages:
    Port A = 8, B = 8, E = 6 + 2 input only, H = 8, J = 4, K = 7, M = 8, P = 8, S = 8, T = 8, PAD = 16
    22 inputs provide Interrupt capability (H =8, P= 8, J = 4, IRQ, XIRQ)

    80 Pin Packages:
    Port A = 8, B = 8, E = 6 + 2 input only, J = 2, M = 6, P = 7, S = 4, T = 8, PAD = 8
    11 inputs provide Interrupt capability (P= 7, J = 2, IRQ, XIRQ)

  - CAN0 can be routed under software control from PM1:0 to pins PM3:2 or PM5:4 or PJ7:6.
  - CAN4 pins are shared between IIC0 pins.
  - CAN4 can be routed under software control from PJ7:6 to pins PM5:4 or PM7:6.
  - Versions with 5 CAN modules will have CAN0, CAN1, CAN2, CAN3 and CAN4
  - Versions with 4 CAN modules will have CAN0, CAN1, CAN2 and CAN4.
  - Versions with 3 CAN modules will have CAN0, CAN1 and CAN4.
  - Versions with 2 SPI modules will have SPI0 and SPI1.
  - Versions with 3 SCI modules will have SCI0, SCI1 and SCI2.
  - Versions with 4 SCI modules will have SCI0, SCI1, SCI2 and SCI4.
  - Versions with 1 IIC module will have IIC0.
  - SPI0 can be routed to either Ports PS7:4 or PM5:2.
  - SPI1 pins are shared with PWM3:0; In 144 and 112 pin versions SPI1 can be routed under software control to PH3:0.
  - SPI2 pins are shared with PWM7:4; In 144 and 112 pin versions SPI2 can be routed under software control to PH7:4. In 80 pin packages $\overline{SS}$-signal of SPI2 is not bonded out!



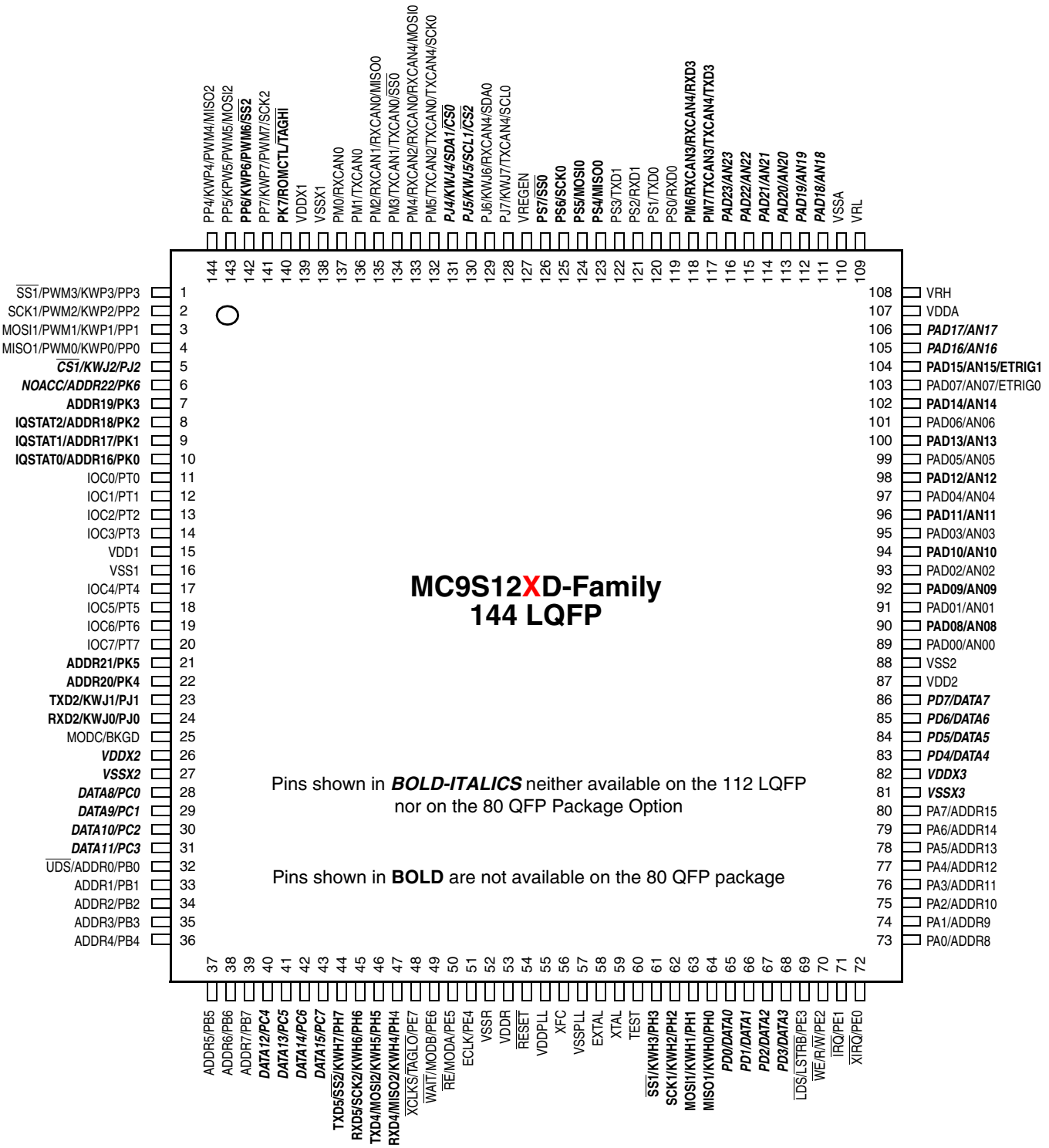


Figure 1 MC9S12XD-Family Pin assignments 144 LQFP Package

NOTE: Pin Out is subject to change!

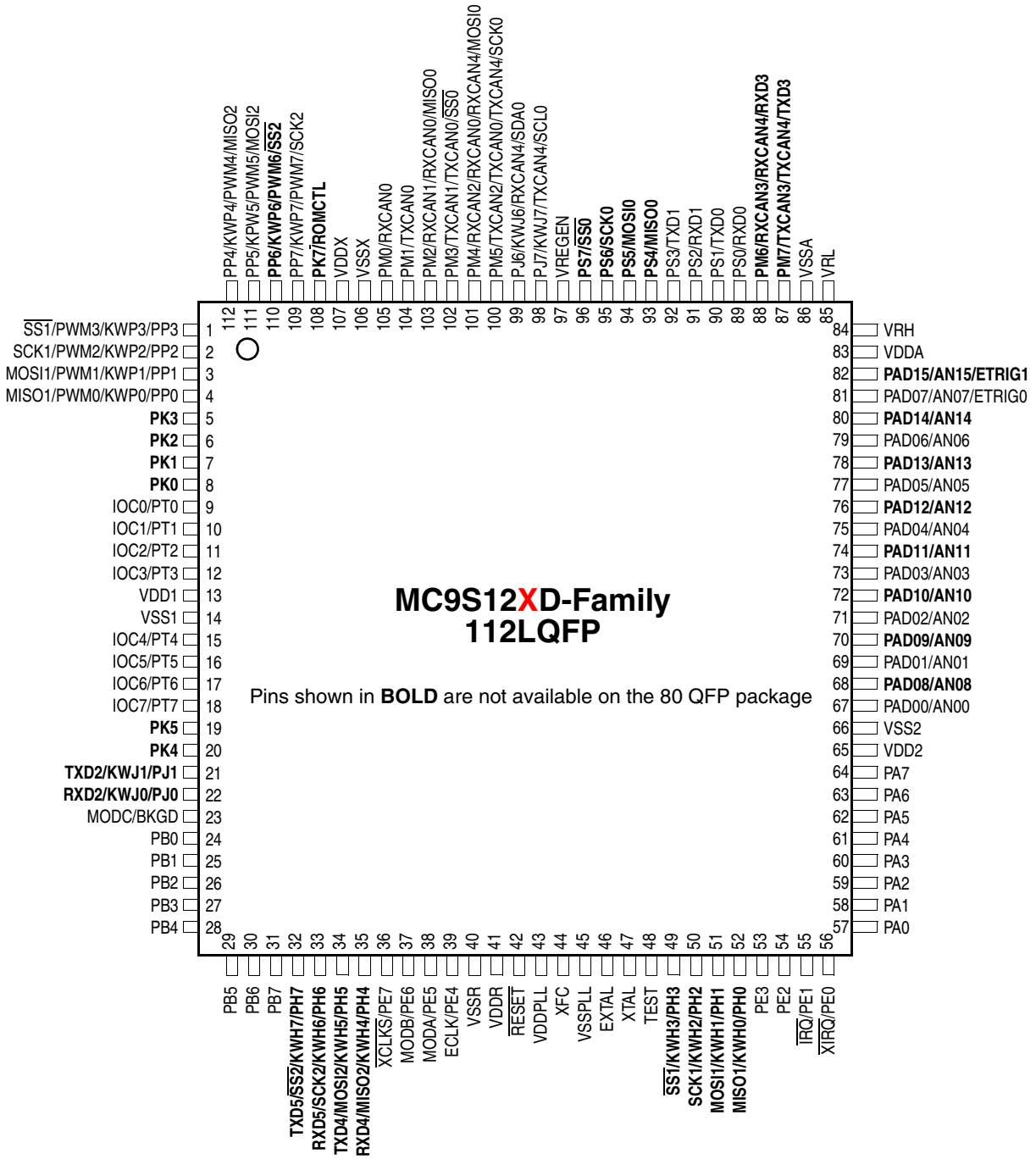


Figure 2 MC9S12XD-Family Pin assignments 112 LQFP Package

NOTE: Pin Out is subject to change!

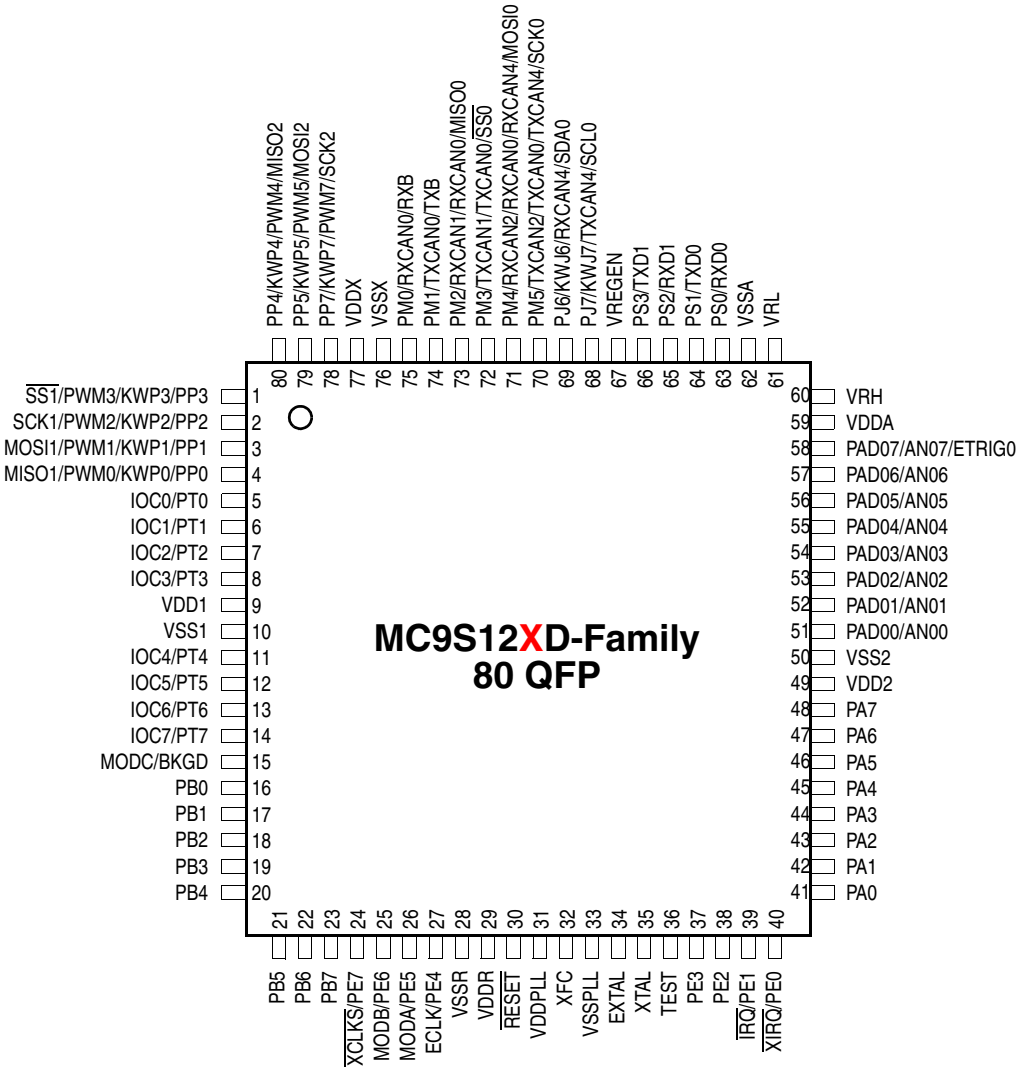


Figure 3 MC9S12XD-Family Pin assignments 80 QFP Package

NOTE: Pin Out is subject to change!

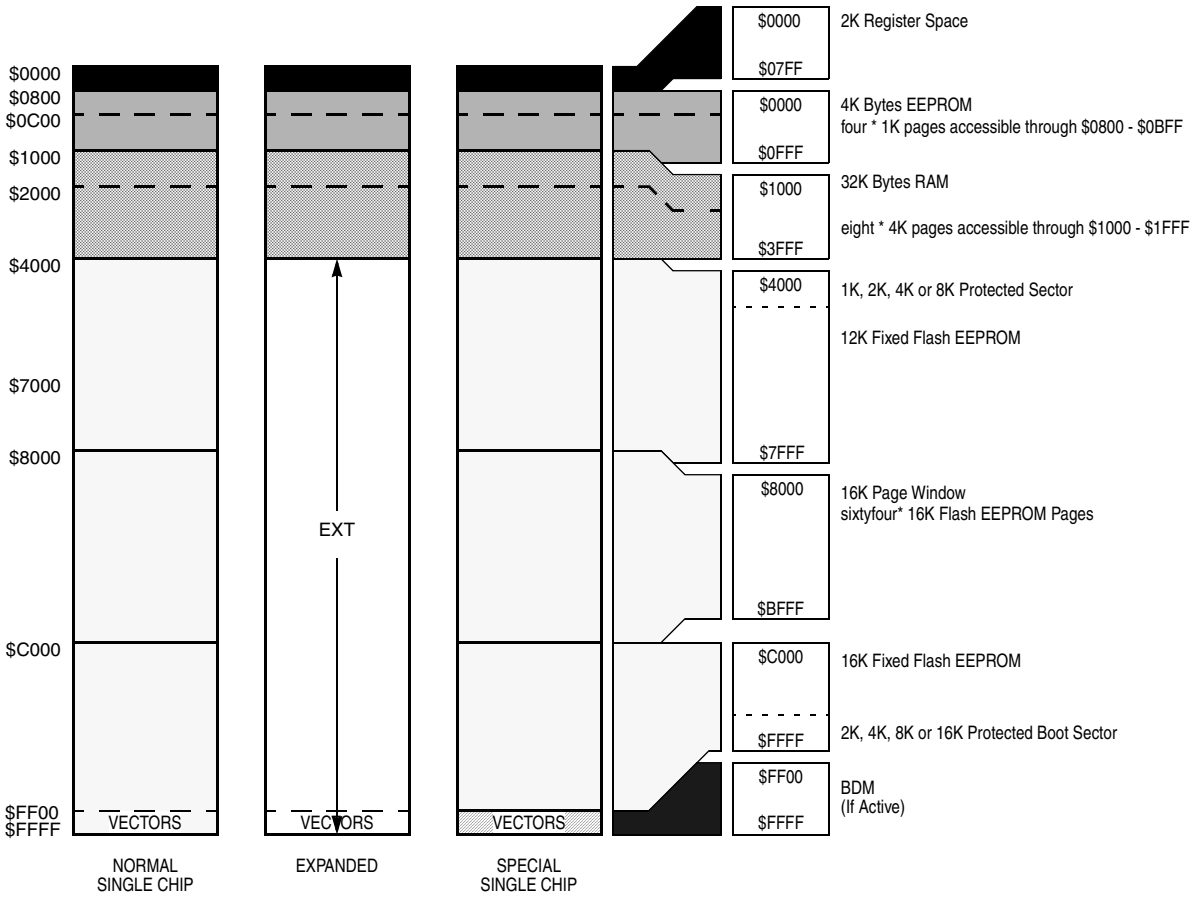


Figure 4 MC9S12XDx100 Memory Map

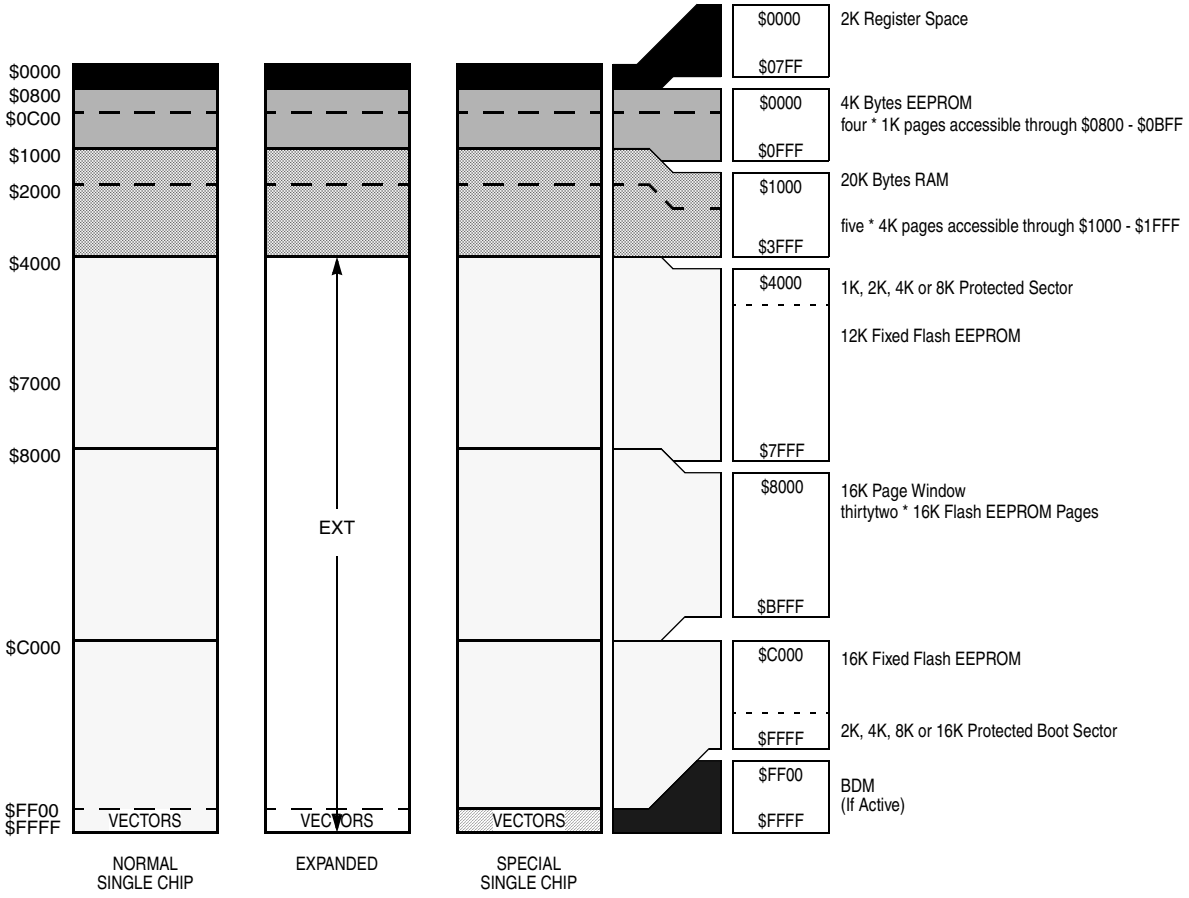


Figure 5 MC9S12XDx512 Memory Map

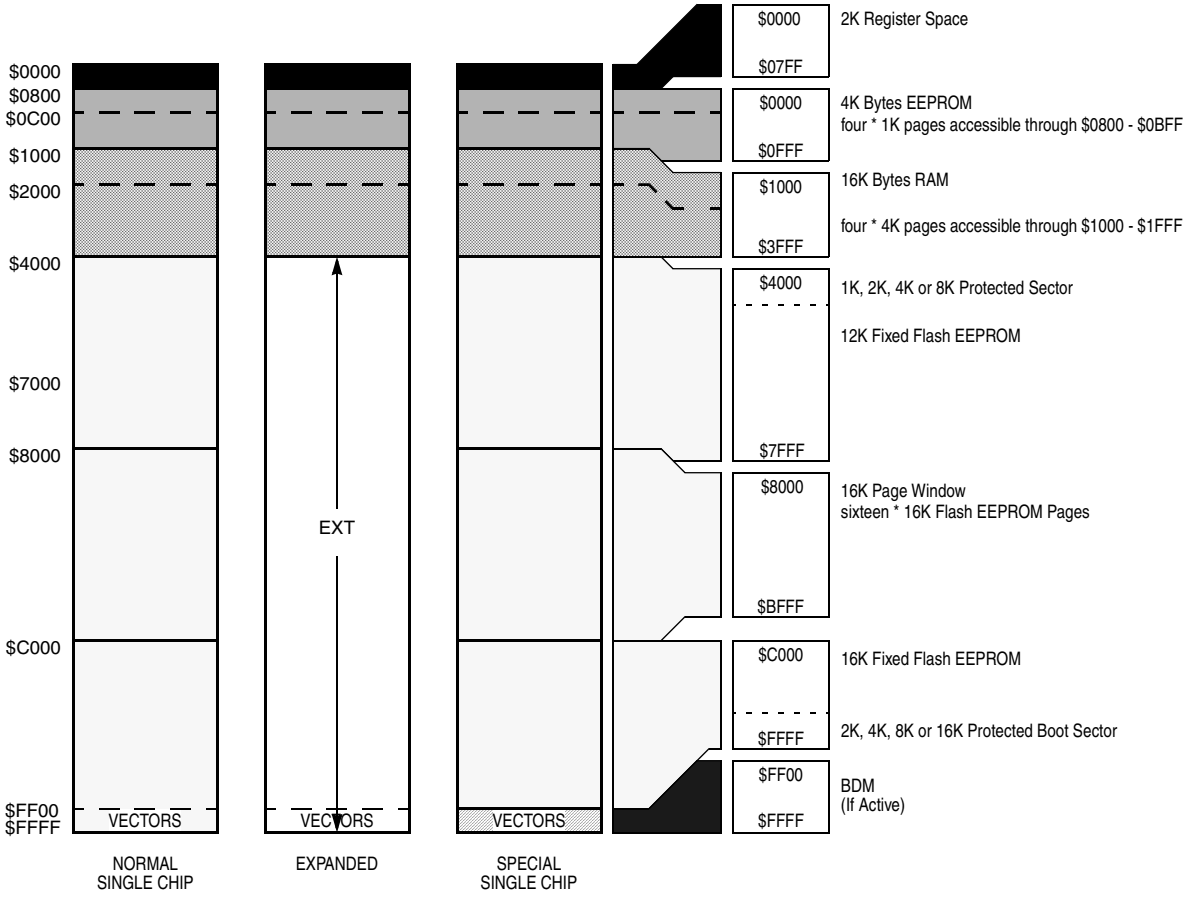


Figure 6 MC9S12XDx256 Memory Map

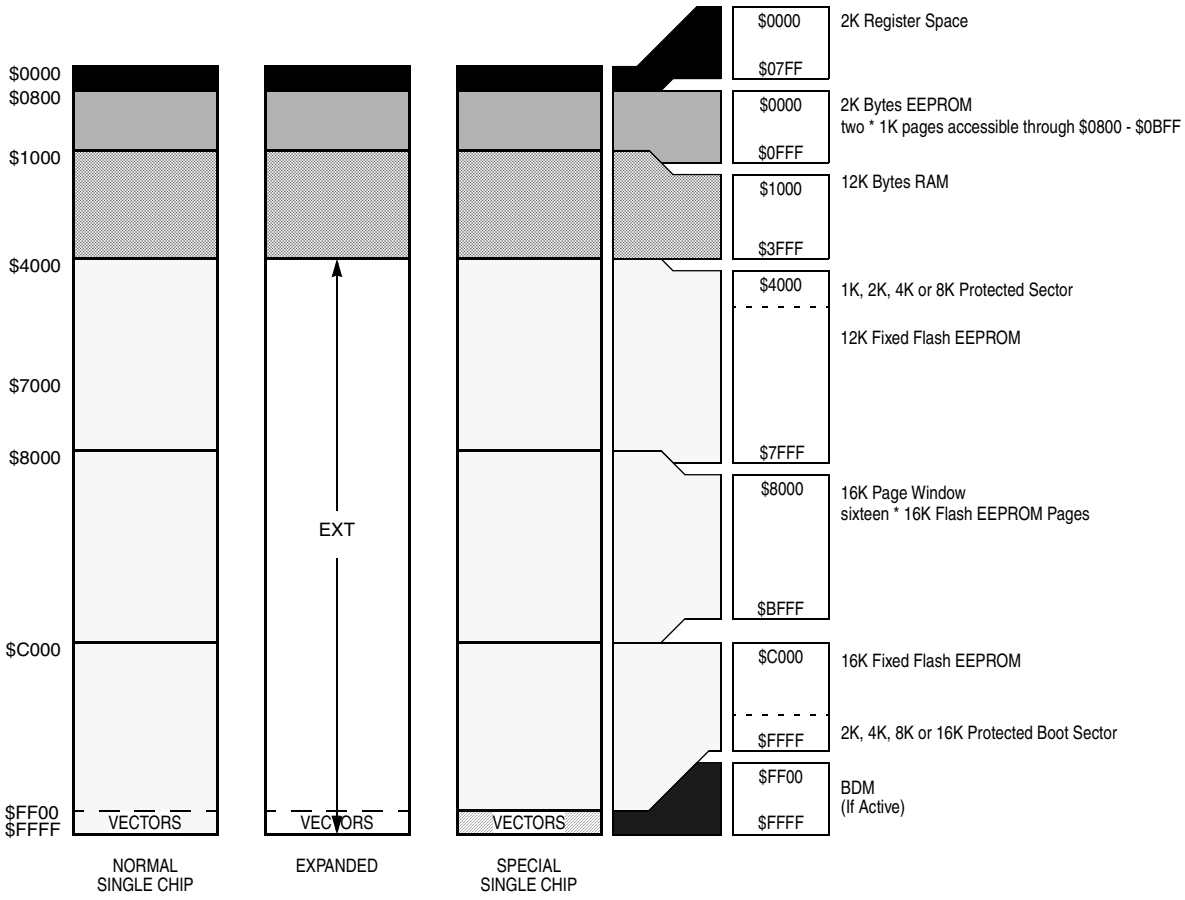
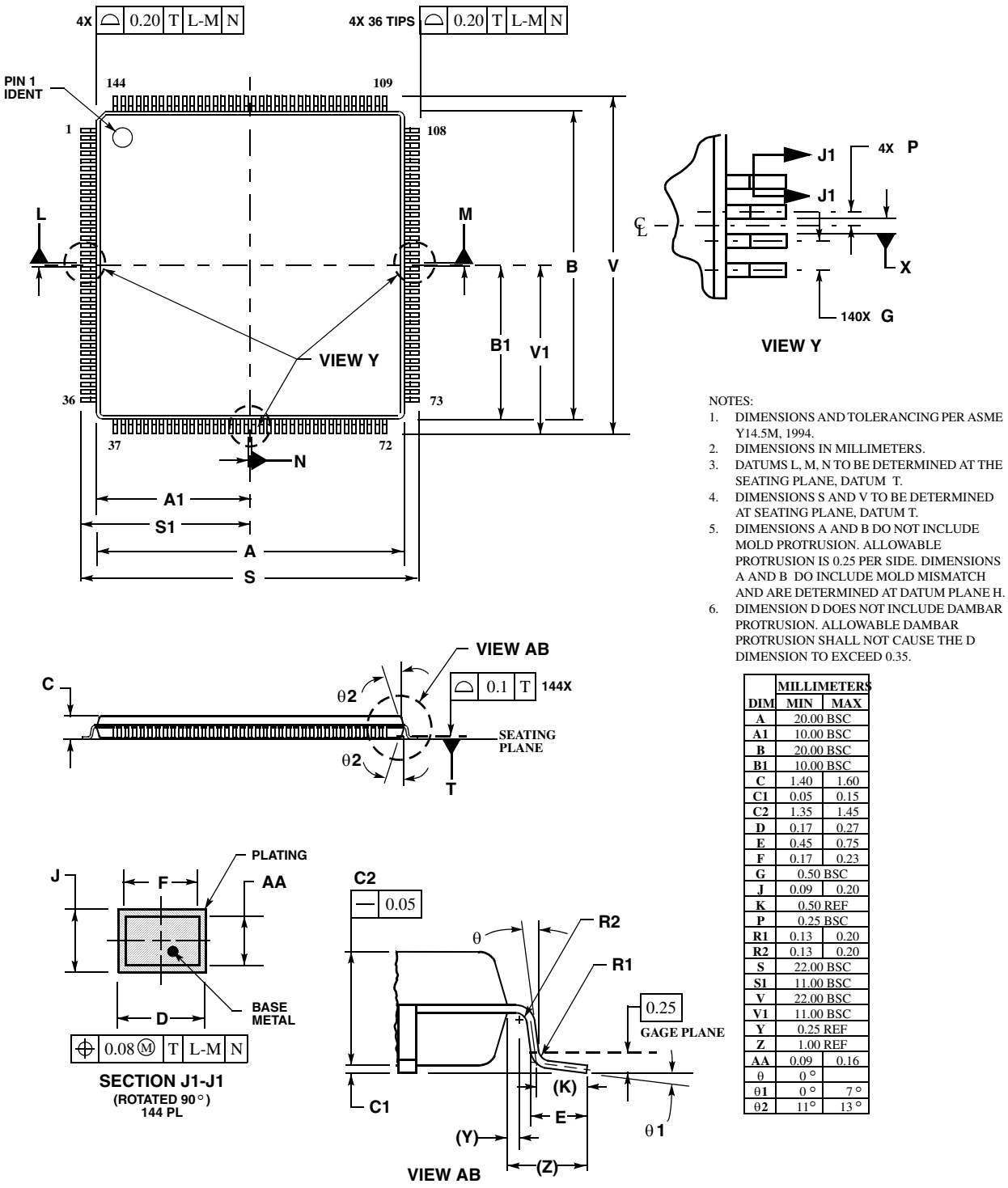
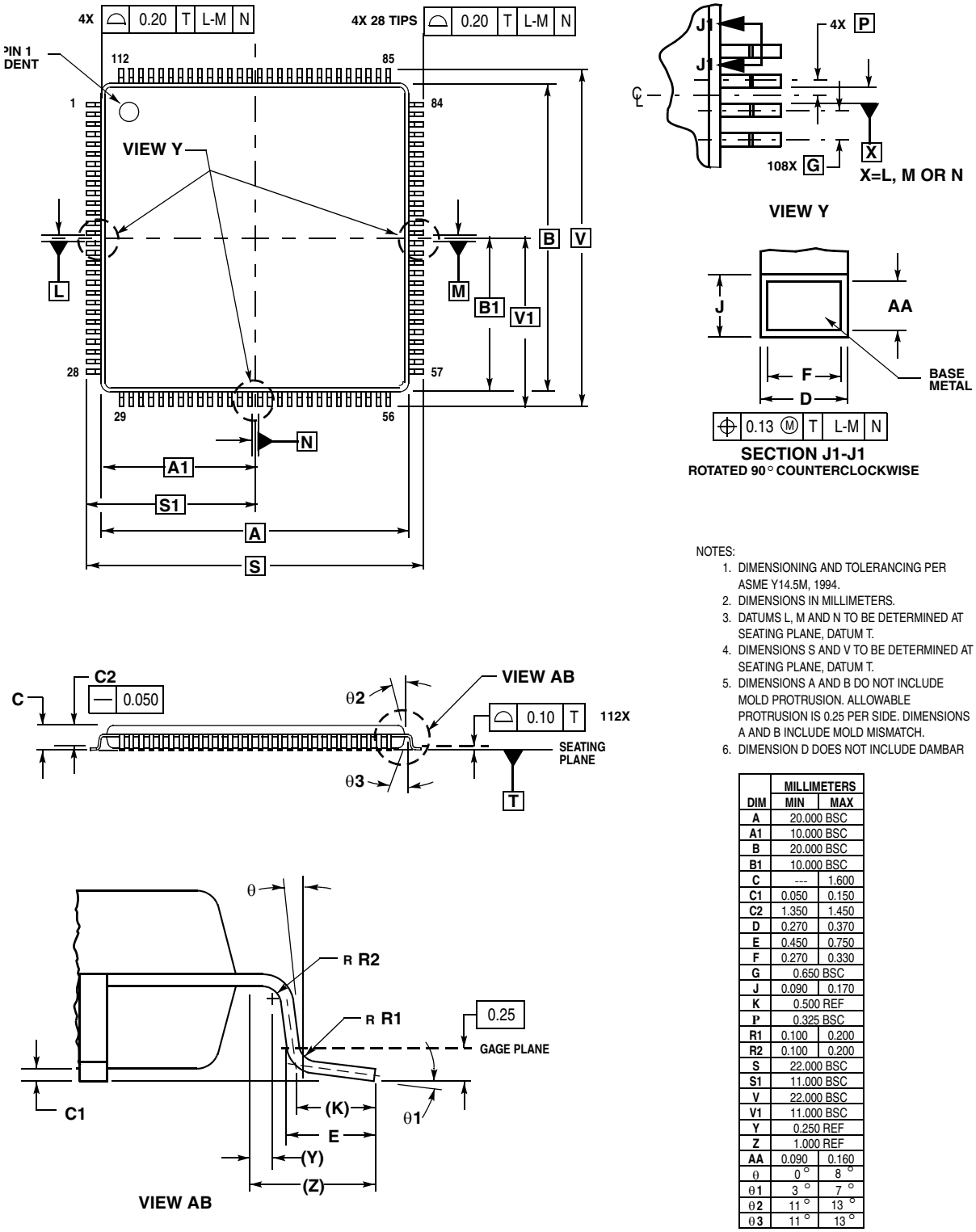


Figure 7 MC9S12XDx128 Memory Map



DIM	MILLIMETERS MIN	MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
θ	0°	
θ1	0°	7°
θ2	11°	13°

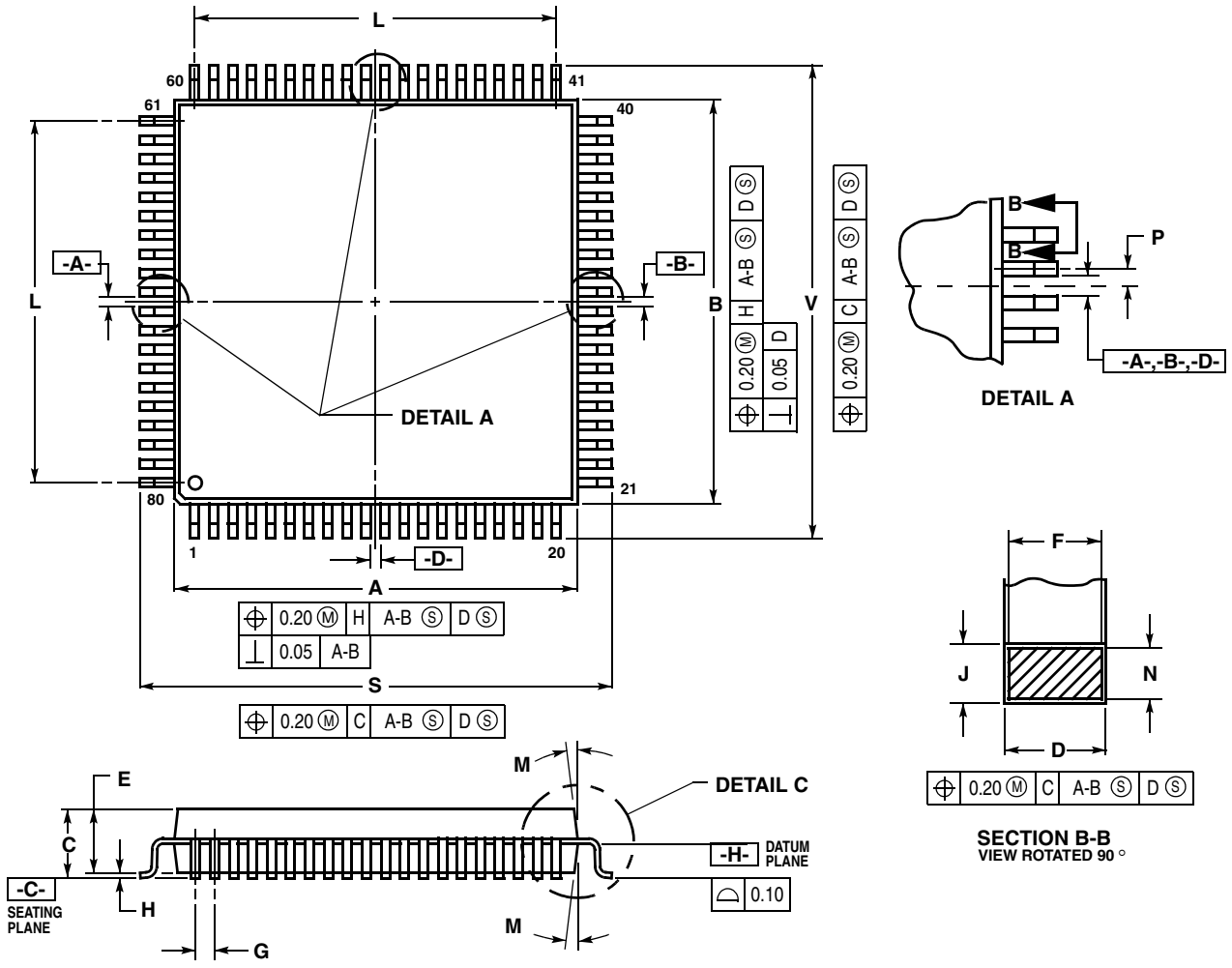
Figure 8 144-pin LQFP Mechanical Dimensions (case no. 918-03)

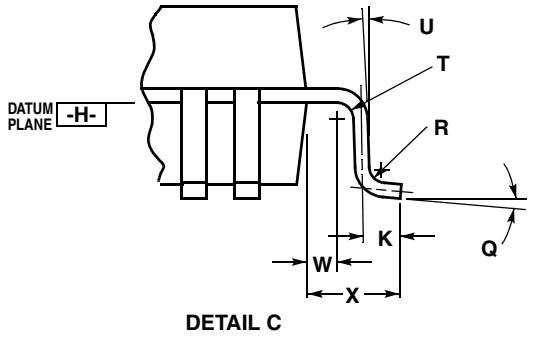


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure 9 112-pin LQFP Mechanical Dimensions (case no. 987)





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure 10 80-pin QFP Mechanical Dimensions (case no. 841B)

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For information on Freescale.s Environmental Products program, go to http://www.freescale.com/epp.