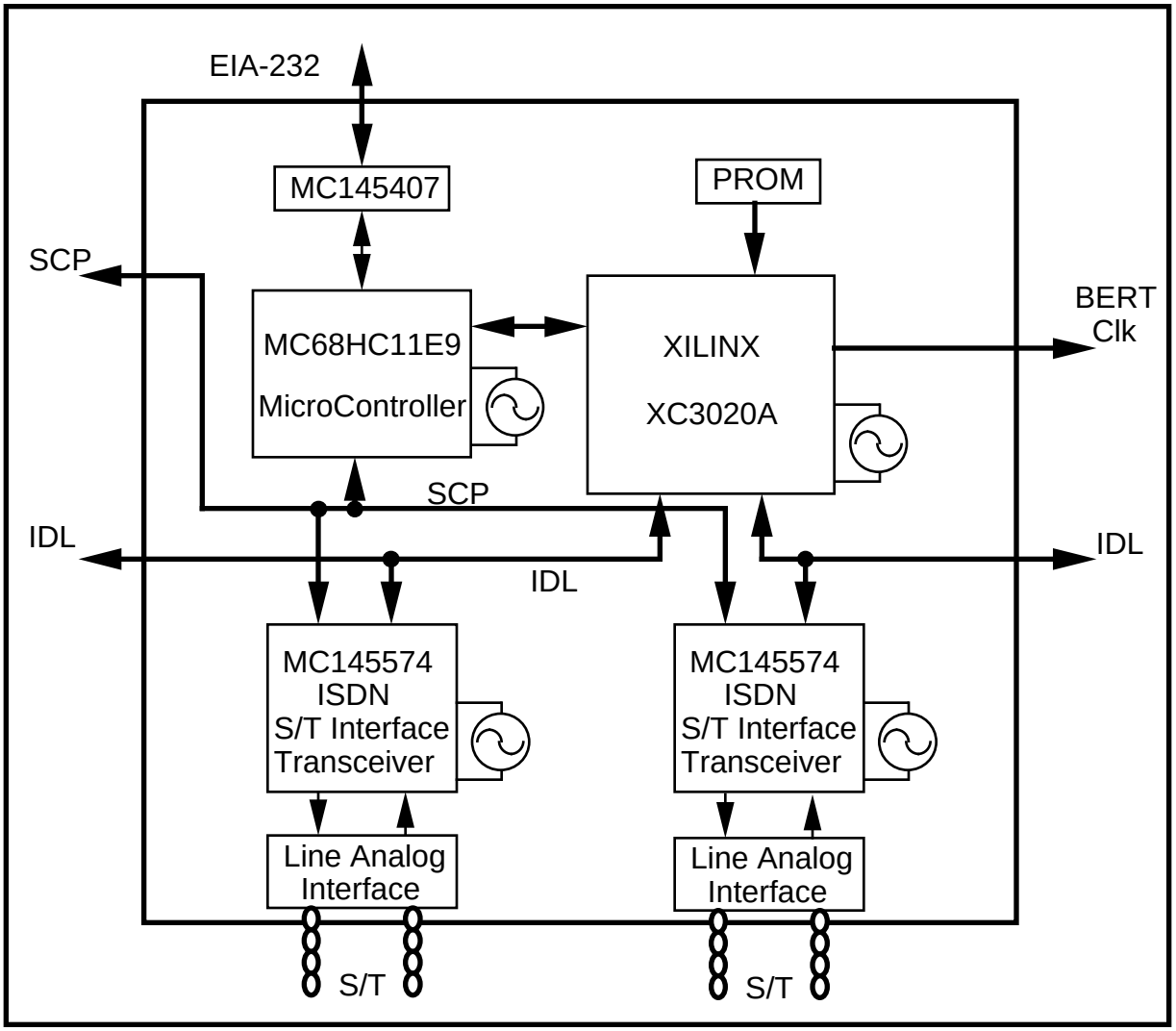
MC145574EVK

Advance Information

ISDN S/T Interface Transceiver Evaluation Kit



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1
GENERAL DESCRIPTION

1.1 ORGANIZATION OF DATA SHEET

This document is composed of four major sections. Section 1 is intended to introduce the MC145574EVK S/T-Interface Transceiver Evaluation Kit with a brief description of the evaluation board and a list of key features. Also included at the end of Section 1 is “Getting Started”, a short tutorial to help begin working with the MC145574EVK. Section 2 is a brief description of the hardware design. Section 3 contains the command set descriptions and examples. Section 4 describes the various test configurations allowed with the board.

IMPORTANT NOTE

This User’s Manual — MC145574EVK S/T-Interface Transceiver Evaluation Kit Revision 1 — corresponds with MC145574EVK Printed Circuit Demo Board Revision 2.0 with firmware version 1.0. If a discrepancy exists between this document and the MC145574 data sheet, the MC145574 data sheet should take precedence.

1.2 INTRODUCTION

The MC145574EVK S/T-Interface Transceiver Evaluation Kit provides Motorola ISDN customers a convenient and efficient vehicle for evaluation of the MC145574 ISDN S/T-Interface Transceiver. The approach taken to demonstrate the MC145574 S/T-Interface Transceiver is to provide the user with a complete set of 2 S/T-Interfaces, either programmable as TE or NT side. The MC145574EVK does not terminate any ISDN call control messages.

The kit provides the ability to interactively manipulate status registers in the MC145574 S/T-Interface Transceivers with the aid of an external terminal.

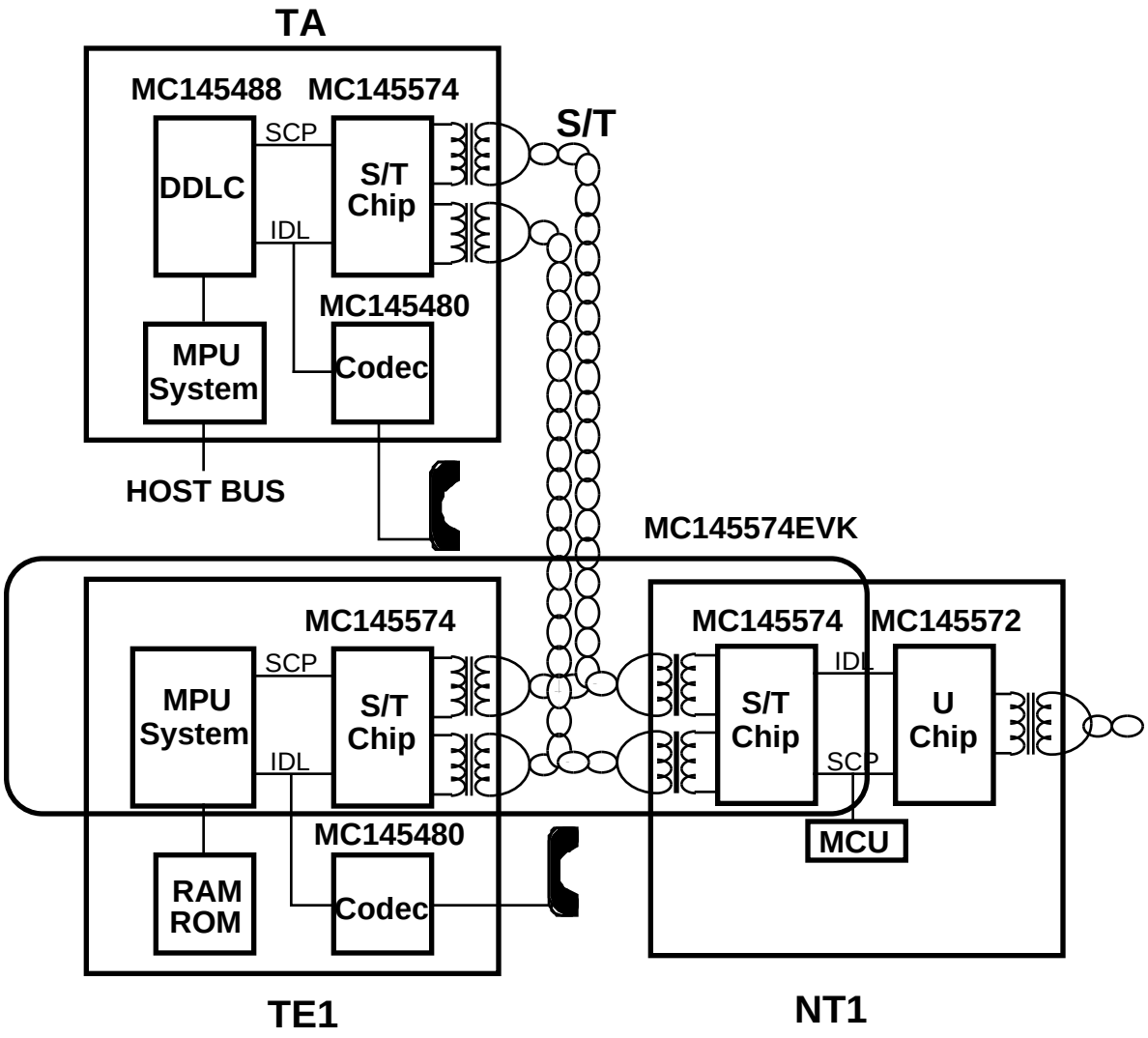


Figure 1-1. **Motorola Silicon Applications and the MC145574EVK**

1.3 FEATURES

1.3.1 GENERAL

- Provides Stand-Alone NT and TE on Single Board
- On-Board 68HC11 Microcontroller with Resident Monitor Software
- Convenient Access to Key Signals
- NT and TE Software Development Platform

1.3.2 HARDWARE

- Only +5 Volt Power Supply
- Gated Data Clocks Provided for Bit Error Rate Testing
- Can Be Used as a S/T-Interface Terminal Development Tool
- EIA-232 (V.28) Serial Port for Terminal Interface

1.3.3 SOFTWARE

- Computer Operation
- Resident Firmware Monitor for User Control of Board
- Activation & Deactivation Menus
- MC68HC11 Assembly Language Source Code Available

1.4 BLOCK DIAGRAM

Following is a basic functional block diagram for the MC145574EVK S/T-Interface Transceiver Evaluation Kit (Figure 1-2).

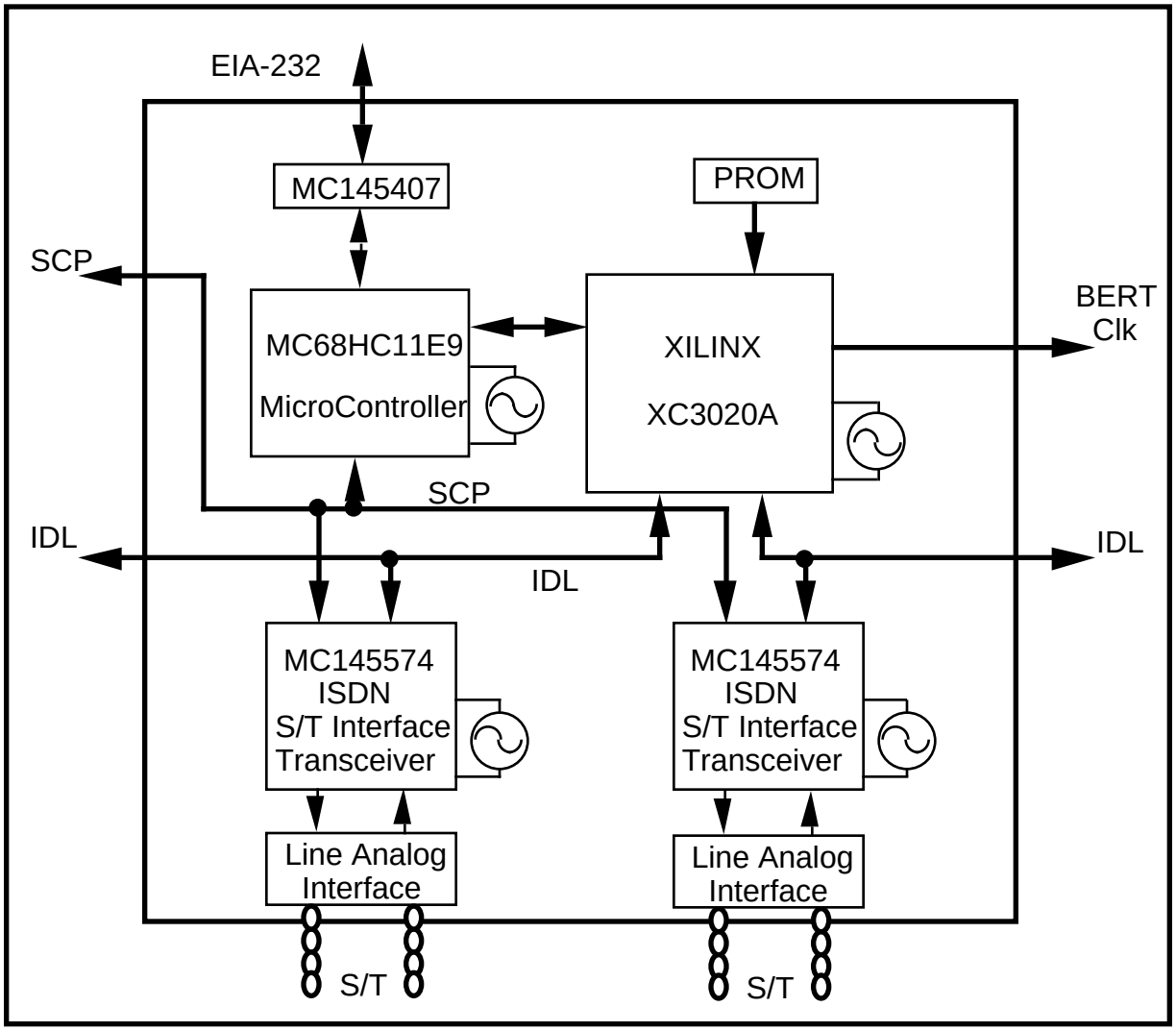


Figure 1-2. **MC145574EVK Functional Block Diagram**

1.5 GETTING STARTED

This section is provided to facilitate the user's introduction to the MC145574EVK. To maximize efficiency when working with the MC145574EVK, it is recommended that the user become familiar with the organization of this document as well as the MC145574 S/T-Interface Transceiver data sheet. To identify a starting point, power up the board and activate the S/T-Interface immediately. The only equipment needed is a 5 V, 0.5 A power supply, a two wires S/T-Interface cable and the MC145574EVK.

NOTE

The board shipped from the factory was thoroughly tested and verified to function properly prior to shipment. If you experience any problems or difficulties with the operation of the MC145574EVK, do not hesitate to call the factory or your local Motorola representative for assistance.

(1) Remove the board from its conductive environment at a static controlled station.

(2) Examine the board and its components to make certain nothing was damage during shipment of the board.

(3) Verify that the socketed ICs are seated properly.

(4) Become familiar with the layout and the various connectors. Locate the power connector. Locate the S/T-Interface RJ45 connectors, one for NT and one for TE configurations for each interface.

The DIP switches and the jumpers arrive preset from the factory (see Figure 1-3). Refer also to Jumpers in section 2.7 and DIP Switches Functions in Section 2.8. Do not change the position of any DIP switch until completely familiar with its function.

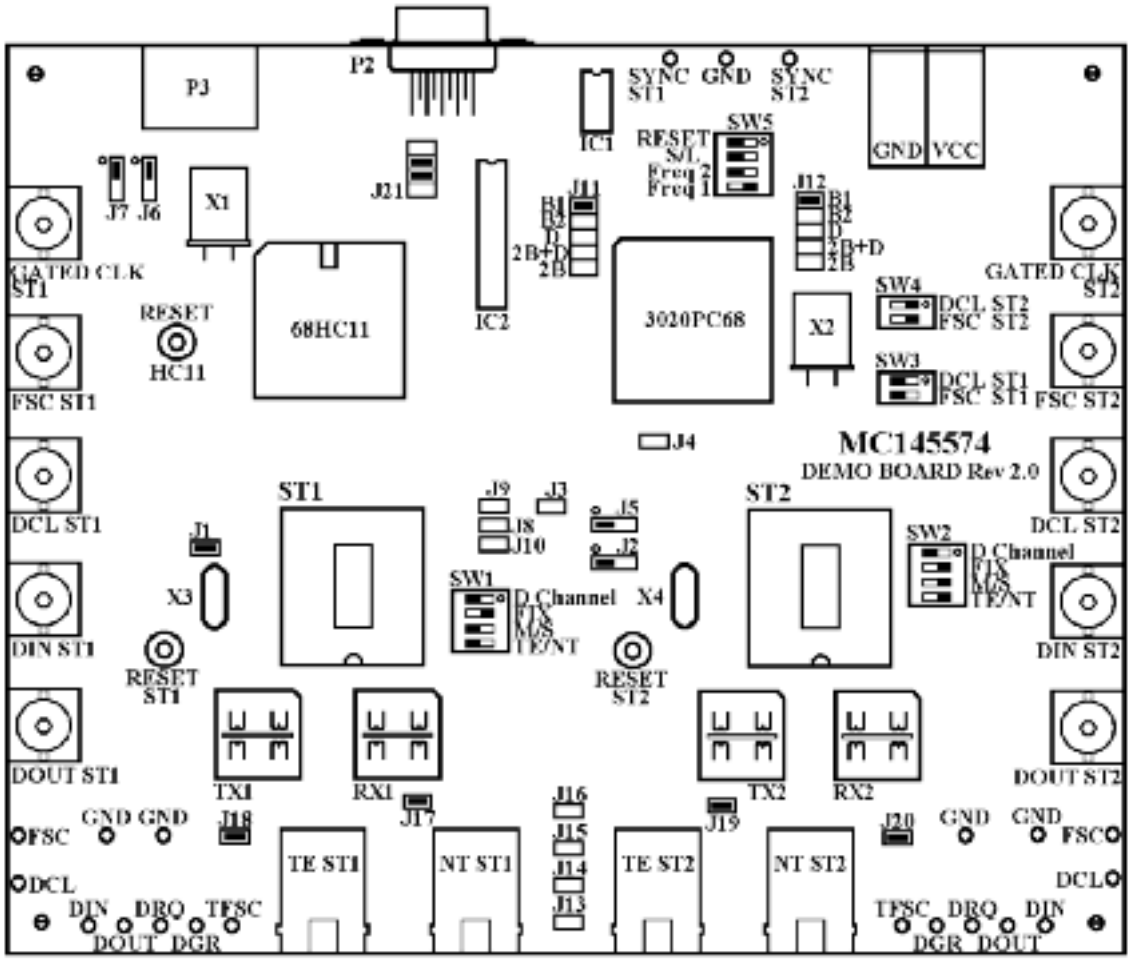


Figure 1-3. **DIP Switches and Jumper Settings to Get Started**

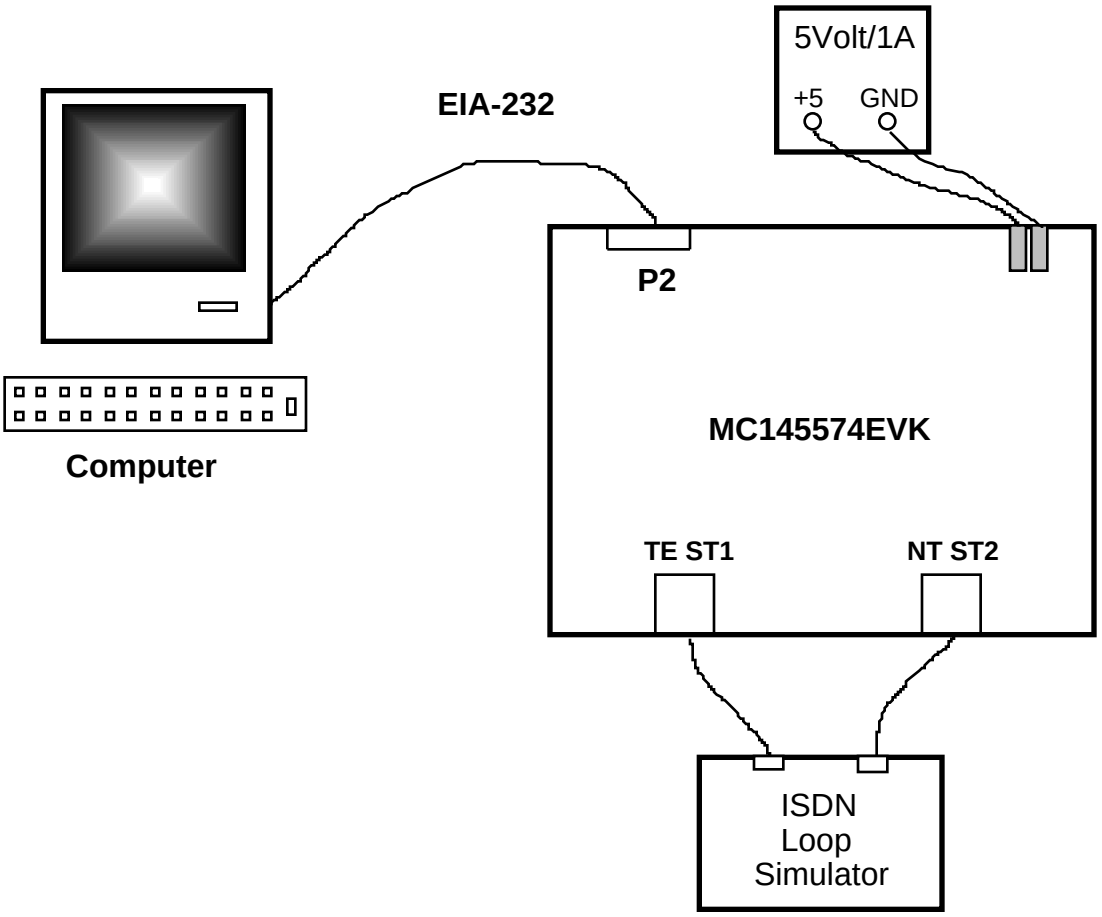


Figure 1-4. **External Connections to the MC145574EVK**

Power is now ready to be applied to the board.

(5) Connect + 5 V and ground leads to the proper power connector.

Make certain the integrity of the power supply being used has been verified to prevent any damage to the MC145574EVK.

(6) Turn the power supply on.

(7) Connect a twisted pair between the two RJ-45 connectors, TE ST1 and NT ST2 , at the bottom of the board. This is the “S/T-loop”.

(8) Depress the 3 RESET push-buttons (ST1, ST2 and HC11). These push-buttons are located adjacent to each component.

(9) Switch on the computer and start the SCP.EXE software.

(10) Connect the computer through the serial port COM1 or COM2 to the P2 connector on the board (this is a DB-9 connector). Make certain the serial port used is configured for 9600 baud, 1 stop bit and no parity. If there is no response, reverse the EIA-232 Tx and Rx signals by changing the jumpers on J21.

(11) Depress PF9 function key on the computer to perform activation on the S/T chips. See section 3 for all the other software features.

Continue reading this document to learn more about the operation of the MC145574EVK S/T-Interface Transceiver Evaluation Kit. Please call the factory for assistance with any problems encountered while “Getting Started”.

2
HARDWARE REFERENCE

NOTE

Refer to the MC145574EVK Printed Circuit Demo Board and to the MC145574 S/T-Interface Transceiver data sheet to supplement this section. Please contact the factory before committing design to PCB to be guaranteed notification of any improvements to the following circuitry. The schematic of the MC145574EVK is in Appendix A of this manual.

2.1 S/T-INTERFACE

The S/T-Interface is implemented with Motorola's single chips MC145574 S/T-Interface Transceiver (ST1 and ST2), providing ISDN Basic Rate Access capability for twisted pair loops with conformance to ANSI T1.605 and CCITT I.430. For additional specifications on designing with and the operation of the MC145574, refer to the MC145574 S/T-Interface Transceiver data sheet in addition to this document.

2.1.1 LINE INTERFACE CIRCUITRY

While the published specifications for the S/T-Interface Transformer are intended as such, it is realized that application specific parameters (i.e. primary protection) may cause some variation in transformer specifications or published line interface values. Figure 2-1 representing the Rx, and Figure 2-2 representing the Tx, show the suggested architecture of the line interface. The schematic gives the corresponding values used to interface the MC145574 to the line using the Pulse PE64998 transformer. Currently all resistor values are accurate to 1%.

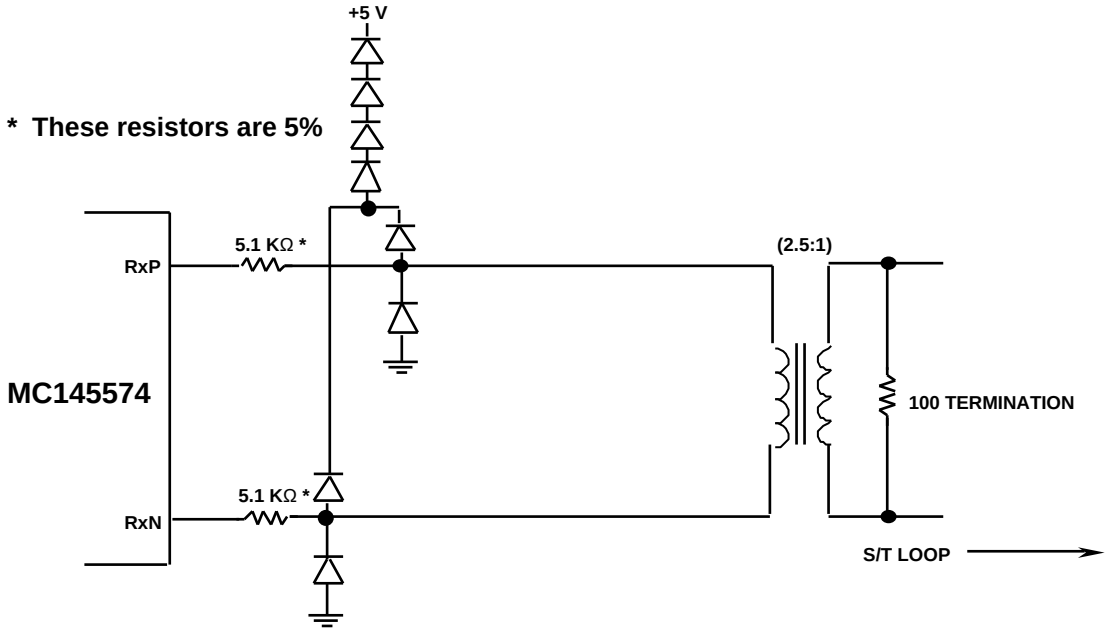


Figure 2-1. **Rx Line Interface Schematic and Component Values**

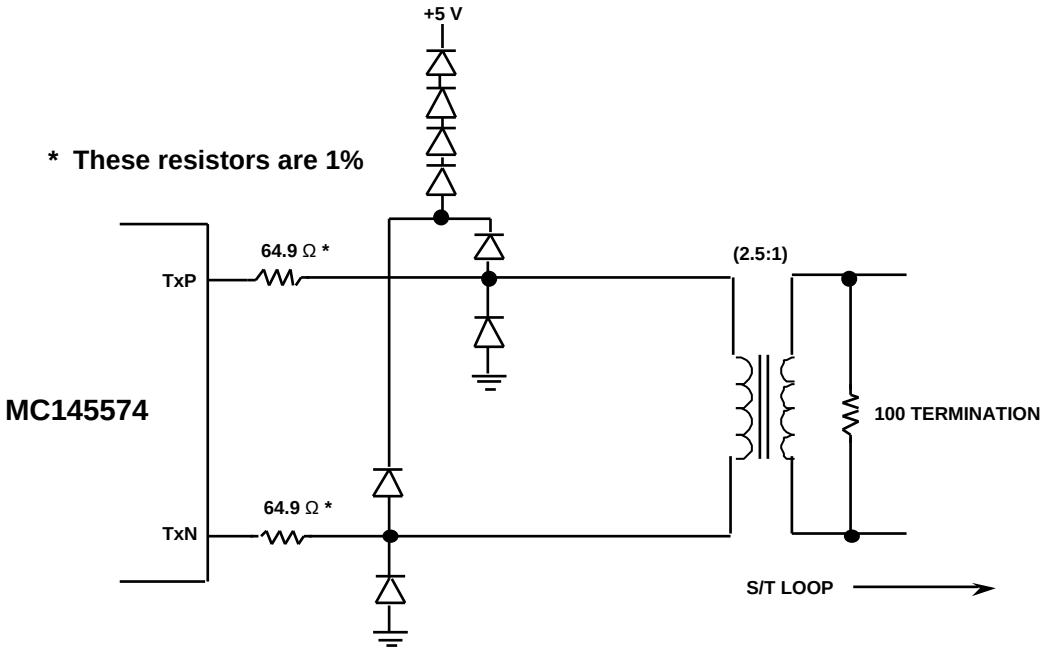


Figure 2-2. **Tx Line Interface Schematic and Component Values**

2.2 MICROCONTROLLER

The MC145574EVK is a MC68HC11E9 microcontroller-based system. Hardware RESET push-button is located on the left side near the microcontroller.

The S/T-Interfaces may be activated using a computer connected to the EIA-232 (V.28) port marked P2 at the top of the board.

The microcontroller is connected with the S/T chips through the SCP (Serial Control Port) bus. This allows the microcontroller to read and write the internal registers of each S/T chip. Some other signals are dedicated to the D channel tests.

2.3 XILINX

The XC3020 from XILINX is a Field Programmable Gate Array (FPGA). This component performs the function of a custom circuit, like a gate array, with the advantage to be programmable and over all reprogrammable easily.

The 1736DPC is a PROM which contains the program to be loaded in the XC3020. After a power up of the board, the XC3020 fetches its configuration from the PROM. So, it is able to deliver IDL clocks (until 4.096 MHz) for the S/T interfaces programmed in TE or NT slave mode. It performs also the gated clocks for both S/T interfaces and is used for D Channel Tests (see section 4) by sending data in the ST1 and ST2 D channels and generating synchronised clocks.

2.4 EIA-232 INTERFACE

The MC145574EVK provides a connector for communication between a computer and the on-board microcontroller Serial Communications Interface (SCI). The connector is industry standard DB-9 type and bring, transmit and receive data on- or off-board via Motorola's MC145407 +5 V EIA-232D Driver/Receiver.

The option is also provided to swap the Transmit and Receive pins with respect to the computer data connector. This appears in the form of a set of jumpers (J21) located near the DB-9 connector. With the jumpers populated as in Figure 2-3, the receive signal is present on pin 2 and the transmit signal on pin 3 (Rx2 - Rx2 and Tx3 - Tx3). This option is useful when the user must use a cable in which the Tx/Rx polarity at pins 2 and 3 is not known. Pin 5 of DB-9 is circuit board ground — all other pins (1, 4, 6-9) are not connected.

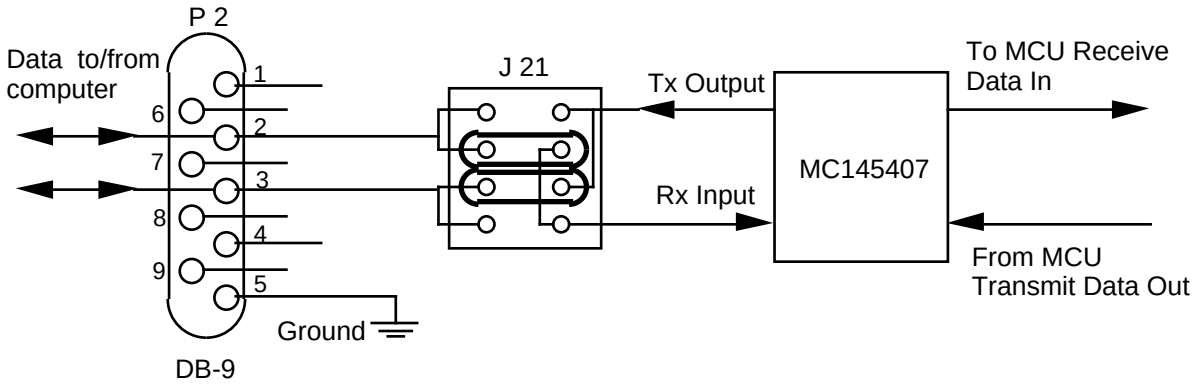


Figure 2-3 : **EIA-232 Interface Schematic**

2.5 BIT ERROR ANALYZER INTERFACE

The MC145574EVK ISDN S/T-Interface Evaluation Kit provides TTL-compatible gated clocks for the B1, B2 and D time slots to allow easy connection to a bit error rate tester. This is accomplished with the use of the XILINX XC3020. The clocks are output in an 10-bit boundary mode at the IDL clock speed. These clocks are available through coaxial plugs called GATED CLK ST1 and GATED CLK ST2.

The MC145574EVK is shipped from the factory configured so its gated clock outputs are B1 gated clocks for each S/T Interface. The 2B+D format is the IDL 10-bit frame. The gated clock signals are only available in IDL 10-bit format.

The timing diagram of this format is shown in Figures 2-4. One example of a bit error rate test set-up is explained in the following paragraph.

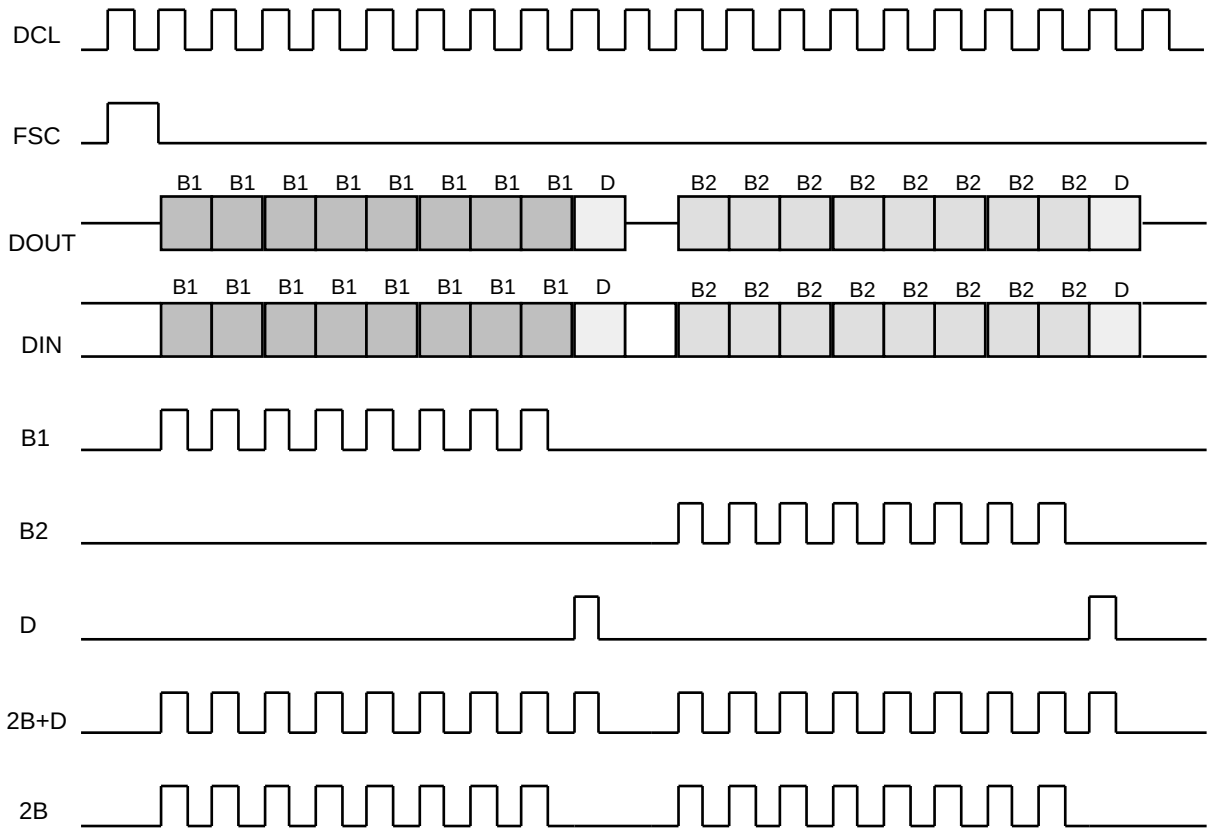


Fig 2.4 : **Gated ClocksTiming Diagram**

2.5.1 SETTING UP A BIT ERROR RATE TEST

Bit error rate testing with one bit error rate tester has been performed. The Telecommunications Techniques Corporation FIREBERD 6000 with Lab Interface Adapter has successfully been connected to the MC145574EVK. Any bit error tests that accepts TTL level signals and external data clocks up to 4.096 MHz at TTL levels may be used. The clock interface supports synchronous clocked data through the use of gated clocks running at IDL rates of 512 KHz to 4.096 MHz.

CAUTION

The MC145574EVK does not support EIA-232, RS-422, 50W or RS-485 interfaces to bit error rate testers.

To demonstrate the connection of the MC145574EVK S/T-Interface Transceiver Evaluation Kit to a bit error rate tester, detailed instructions for one test set-up follow.

EXAMPLE: Executing a 2B S/T Loop-Back at the TE side.

This example shows how to connect a bit error rate tester to the MC145574EVK. Refer to Figure 2-5 for connection details.

The data flow for this example occurs as follows: Data is input to the board by the BERT box on DIN ST2 coaxial plug . This data is then input to the ST2 configured in NT mode where it is framed, coded and transmitted over the S/T-Loop to the ST1 configured in TE mode and looped-back internal to the ST2. The data transmitted back to the ST2 over the S/T-Loop are decoded, deframed and output on DOUT ST2 coaxial plug to the BERT box where it is compared to the data originally transmitted.

(1) Make the following connections to the Bit Error Rate Tester as shown in Figure 2-5.

(2) Verify that the DIP switches and the jumpers are set as in Figure 1-3.

(3) Configure the bit error rate tester to transmit data on the rising edge of the data clock and receive data on the falling edge of the data clock.

(4) Using the software on the computer, activate the ST2 with the activation option or the PF9 key. Verifiy that the S/T-Loop is activate by using the Display Registers option or the PF10 key. If NR2 is at 9 value, the S/T-Loop is well activated. Else, reset the two S/T interfaces and try a new activation.

(5) On the Demo Board, put the jumper J12 on the 2B option.

(6) Select ST1 and use Configuration menu to activate the 2B S/T Loopback.

(7) Begin bit error rate testing.

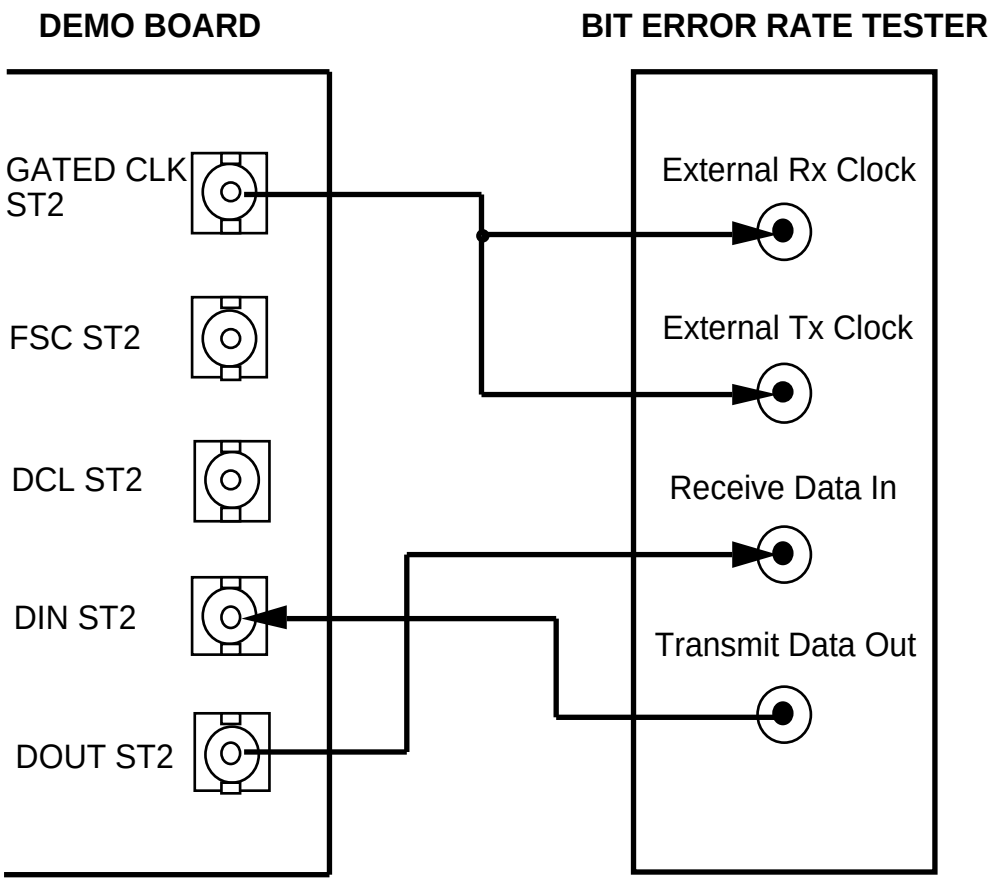


Fig 2.5 : **Gated Clocks Timing Diagram**

2.5.2 OTHER LOOPBACK TESTS

A variety of other loop-back modes may be implemented. Some modes are accessible through the Configuration menu while others require a working knowledge of the SCP registers and are accessed through the Registers menu. Refer to Figure 2-6 below and the text that follows for a description of some of these loop-backs. Refer also to the MC145574 data book loop-back section. The menu items referred to are for the NT and TE modes.

A: External Hardware IDL Loop-Back on TE Side.
Activate the loop with ST1 in TE mode and ST2 in NT mode. Use Configuration menu to enable 2B on TE side. B1, B2 and 2B loop-backs may be performed. Program J12 according to your choice.

B: IDL Loop-Back Internal to S/T-Interface Transceiver in TE mode.
Activate the loop with ST1 in TE mode and ST2 in NT mode. Use Configuration menu to enable 2B on TE side and to choose an IDL loop-back between all the 5 possibilities : B1, B2, and 2B+D (transparent or not transparent for B1 and B2). Program J11 according to your choice.

C: S/T-Interface Transceiver Loop-Back on TE side.
Activate the loop with ST1 in TE mode and ST2 in NT mode. Use Configuration menu to enable 2B on TE side and to choose an S/T loop-back between all the 5 possibilities : B1, B2, and 2B (transparent or not transparent for B1 and B2). Program J12 according to your choice.

D: External Hardware IDL Loop-Back on NT Side.
Activate the loop with ST1 in TE mode and ST2 in NT mode. Use Configuration menu to enable 2B on TE side.B1, B2 and 2B loop-backs may be performed. Program J11 according to your choice.

E: IDL Loop-Back Internal to S/T-Interface Transceiver in NT mode.
Activate the loop with ST1 in TE mode and ST2 in NT mode. Use Configuration menu to choose an IDL loop-back between all the 5 possibilities : B1, B2, and 2B+D (transparent or not transparent for B1 and B2). Program J12 according to your choice.

F: S/T-Interface Transceiver Loop-Back on NT side.
Activate the loop with ST1 in TE mode and ST2 in NT mode. Use Configuration menu to enable 2B on TE side and to choose on NT side an S/T loop-back between all the 5 possibilities : B1, B2, and 2B (transparent or not transparent for B1 and B2). Program J11 according to your choice.

NOTE

When J11 has to be programmed, gated clock comes from ST1, and when J12 has to be programmed, gated clock comes from ST2.

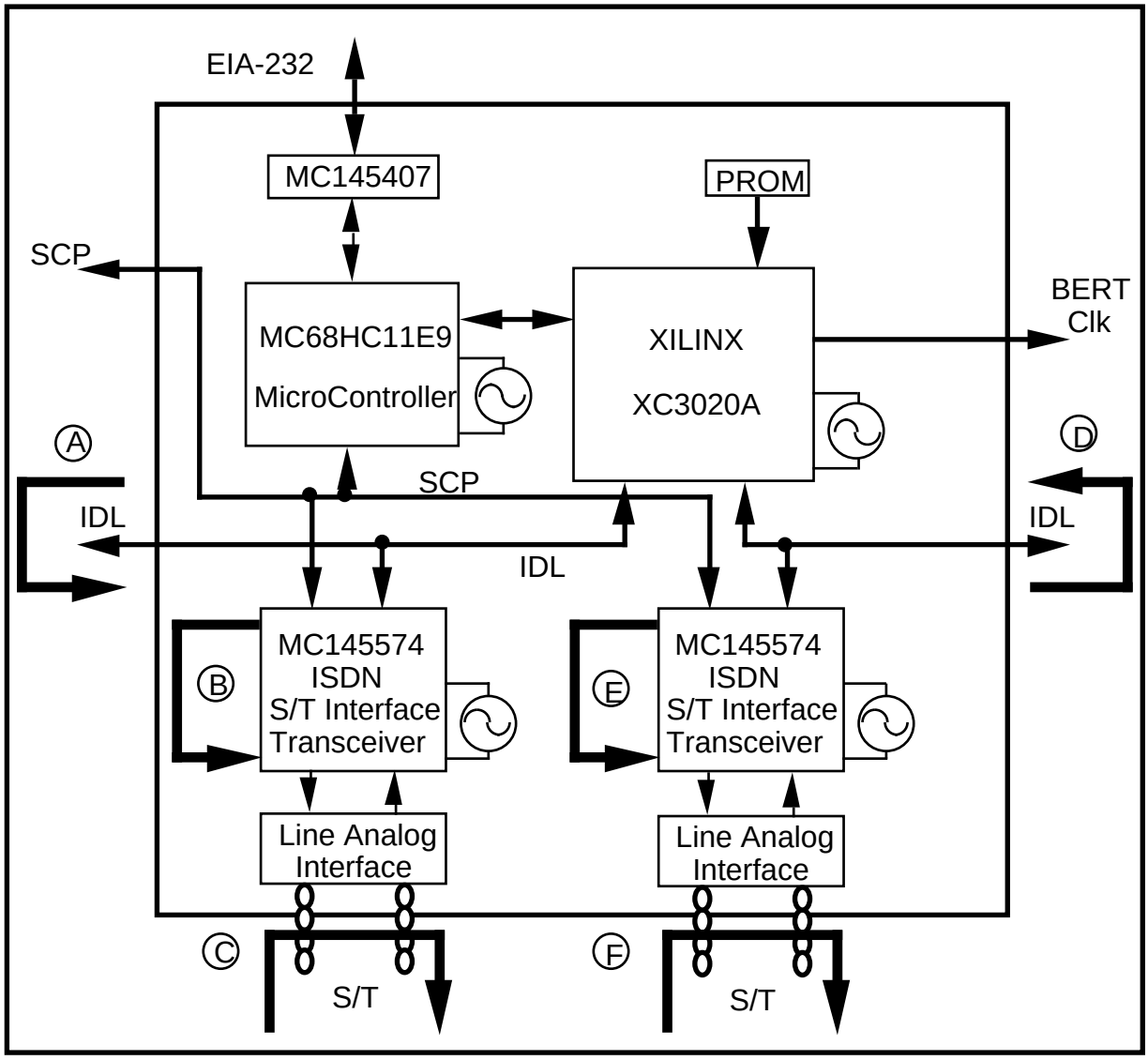


Figure 2-6 : **Loop-Back Modes for the MC145574EVK**

2.6 MC145574EVK TEST HEADERS

There are several headers on the MC145574EVK with signals of significant interest to the user.

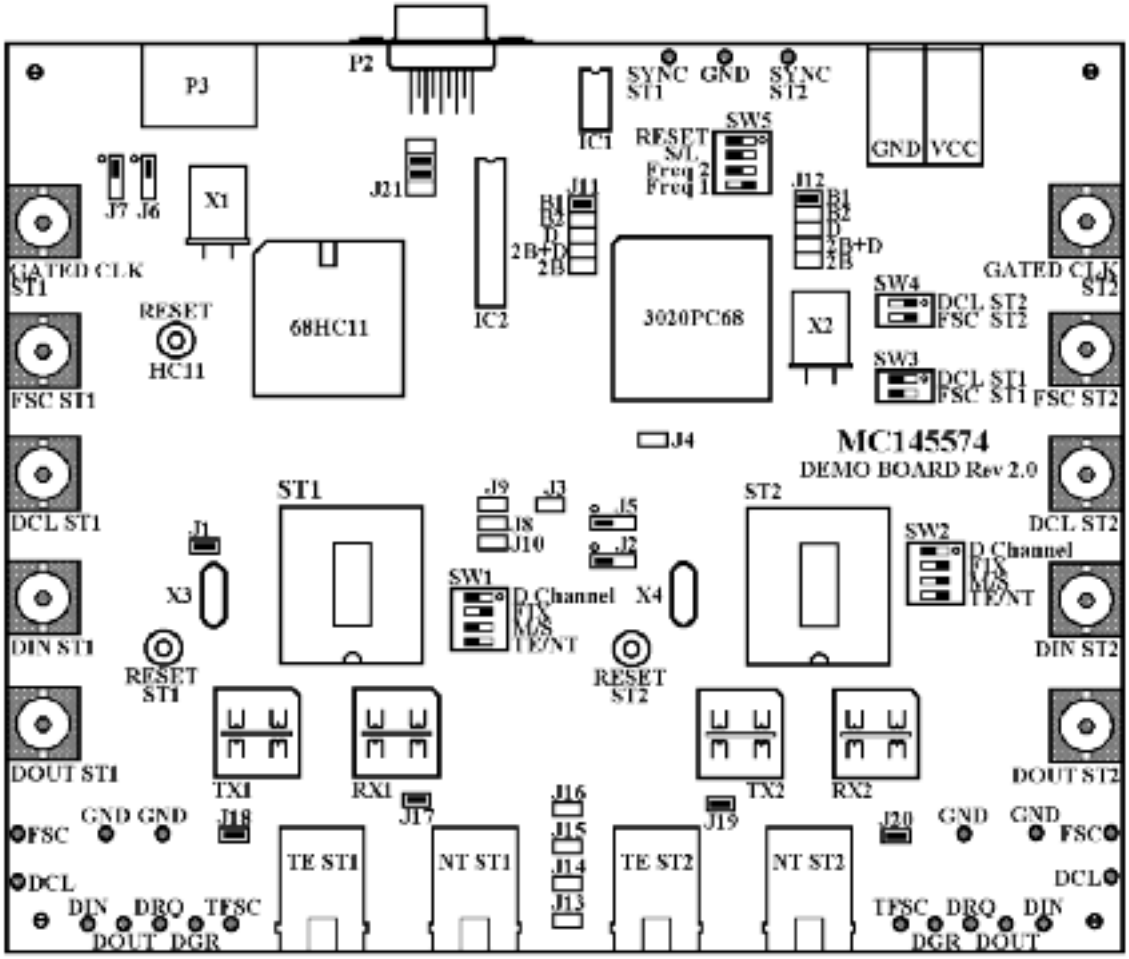


Figure 2-7 : **BNC and test points for the MC145574EVK**

These headers are splitted in 3 areas. One is for the ST1signals (bottom left of the board), one is for the ST2 signals (bottom right of the board) and the last one is for D channel dedicated signals (top of the board).

Table 1: ST1 and ST2 signals

Name of the Test Header	Type of the Test Header	Pin of the S/T Interface
FSC	BNC connector and Test point	11
DCL	BNC connector and Test point	12
DIN	BNC connector and Test point	13
DOUT	BNC connector and Test point	14
DREQUEST	Test point	9
DGRANT	Test point	8
TFSC	Test point	6
Gated Clock	BNC connector	Jumper J11 for ST1 Jumper J12 for ST2

Table 2: D channel test signals

Name of the Test Header	Type of the Test Header
SYNC ST1	Test point
SYNC ST2	Test point

These signals will be described in Section 4.

2.8 JUMPER FUNCTIONS

Table 3 : MC145574EVK Jumpers

Jumper Reference	FUNCTION
J1	ST1 5v power supply. Allows to measure the ST1 consumption
	NT Star Mode
J2	ECHO ST1 to GND if side of mark o, to DGRANT ST2 else
J3	DREQUEST ST2 to DGRANT ST1
J4	DREQUEST ST1 to VCC through a resistor
J5	ECHO ST2 to GND if side of mark o, to DGRANT ST2 else
J8	DOUT ST1 to DOUT ST2
J9	DOUT ST2 to VCC through a resitor
J10	DIN ST1 to DIN ST2
	Connector P3 for link with second board
J6 - J7	If board master : jumper to the opposite side of mark o
	If board slave : jumper to the side of mark o
J11	Gated Clock ST1
J12	Gated Clock ST2
J13 to J16	Connection of the two RJ45 connectors TE-ST1 and TE-ST2 for two TE on the S/T Loop.
J17	Default termination impedance (100 Ohms) on ST1 Transmit
J18	Default termination impedance (100 Ohms) on ST1 Receive
J19	Default termination impedance (100 Ohms) on ST2 Transmit
J20	Default termination impedance (100 Ohms) on ST2 Receive
J21	EIA-232 Interface option for Tx/Rx polarity

2.8 DIP SWITCHES FUNCTIONS

Five sets of DIP switches are provided for MC145574EVK configuration and testing. These switches are preset at the factory as shown in Figure 2-8.

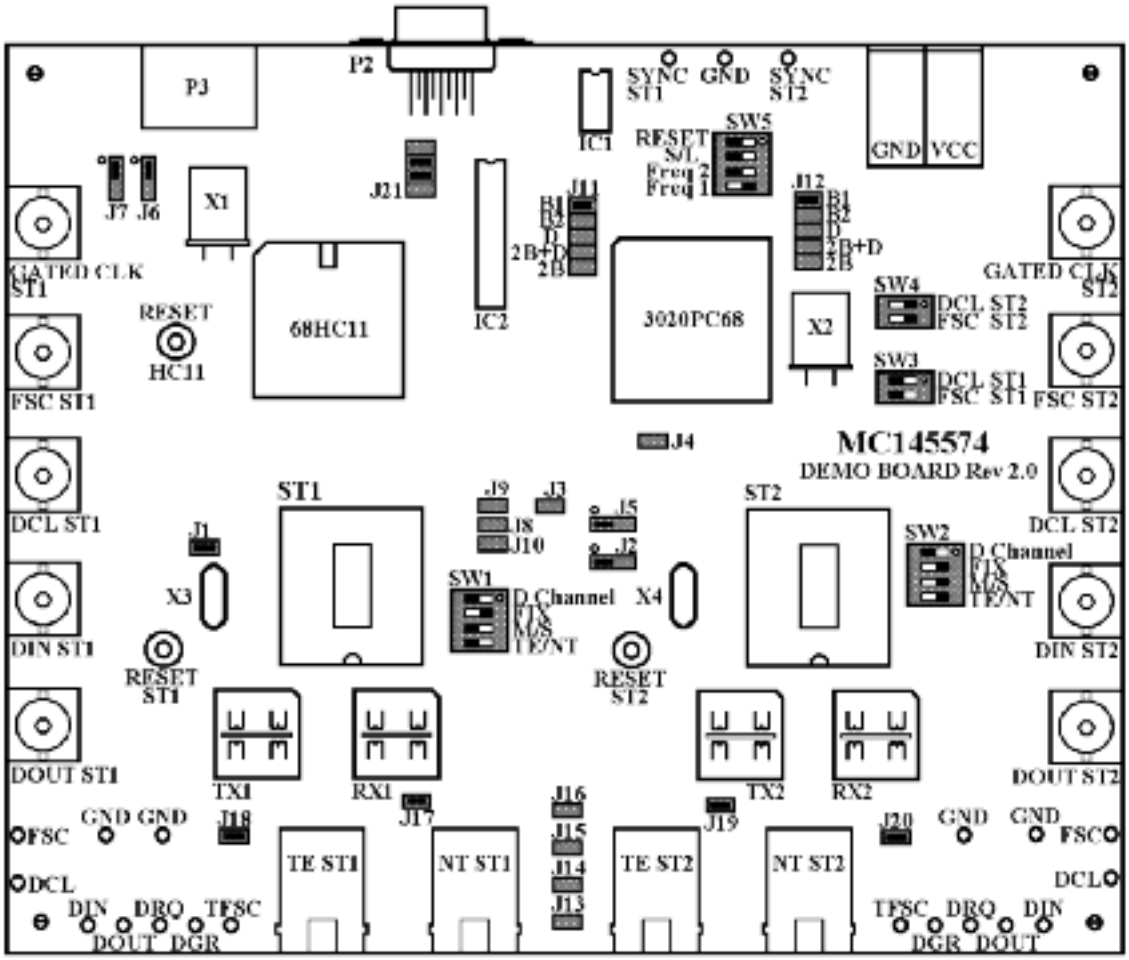


Figure 2-8 : **Jumpers and Dip Switches for the MC145574EVK**

Table 4 : MC145574EVK Dip Switches

DIP-Switch Reference	Value	FUNCTION
SW1-1	ON	For D Channel Access and NT Star Mode Tests
	OFF	
SW1-2	ON	ADAPTATIVE Mode for ST1
	OFF	FIX Mode for ST1
SW1-3	ON	SLAVE Mode for ST1
	OFF	MASTER Mode for ST1
SW1-4	ON	NT Mode for ST1
	OFF	TE Mode for ST1
SW2-1	ON	For D Channel Access and NT Star Mode Tests
	OFF	
SW2-2	ON	ADAPTATIVE Mode for ST2
	OFF	FIX Mode for ST2
SW2-3	ON	SLAVE Mode for ST2
	OFF	MASTER Mode for ST2
SW2-4	ON	NT Mode for ST2
	OFF	TE Mode for ST2
SW3-1	ON	Providing of IDL-DCL clock for ST1 in SLAVE Mode
	OFF	ST1 in MASTER Mode
SW3-2	ON	Providing of IDL-FSC clock for ST1 in SLAVE Mode
	OFF	ST1 in MASTER Mode
SW4-1	ON	Providing of IDL-DCL clock for ST2 in SLAVE Mode
	OFF	ST2 in MASTER Mode
SW4-2	ON	Providing of IDL-FSC clock for ST2 in SLAVE Mode
	OFF	ST2 in MASTER Mode

DIP-Switch	Value	FUNCTION
SW5-1	ON	RESET of the 3020PC68 logic
	OFF	
SW5-2	ON	Long Frame for IDL-FSC providing
	OFF	Short Frame for IDL-FSC providing
		IDL Clock speeds provided by the 3020PC68
SW5-3,5-4	ON-ON	4096 KHz
	OFF-ON	2048 KHz
	ON-OFF	1024 KHz
	OFF-OFF	512 KHz

2.9 POWER SUPPLY

The MC145574EVK is a + 5 V only board that pulls less than 100 mA while activated and operating in the combined NT/TE mode. It is recommended that a 5 V supply with a 200 mA minimum current capability be used (in the case the user needs to supply 2 boards).

Power supply connections are made to the terminals marked VCC and GND.

One BZX85C 1 watt zener regulator diode (5.6 V) protects the MC145574EVK from over voltage and reverse polarity conditions.

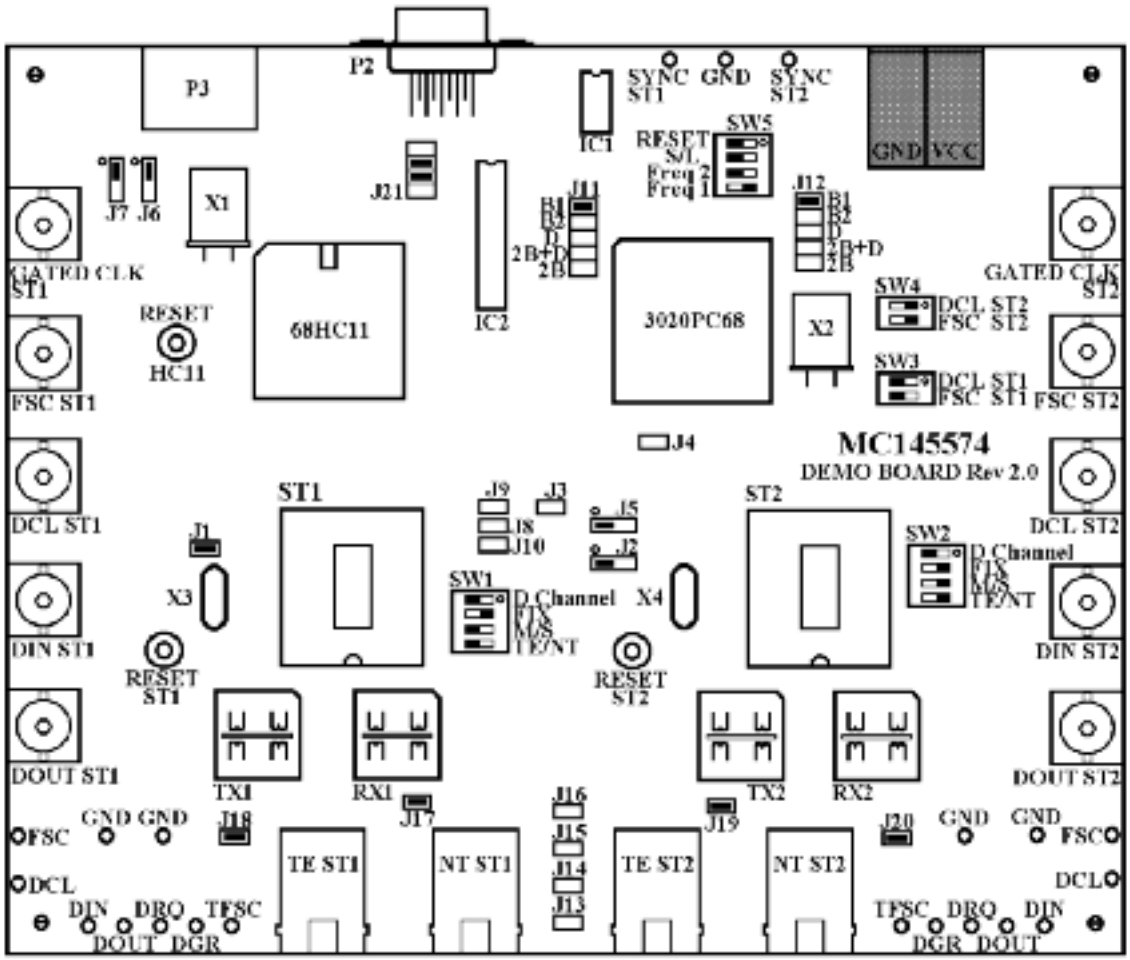


Figure 2-9. **Power Connector Pin Assignments**

3 SOFTWARE DESIGN DESCRIPTION

3.1 GENERAL DESCRIPTION

The general environment is presented below:

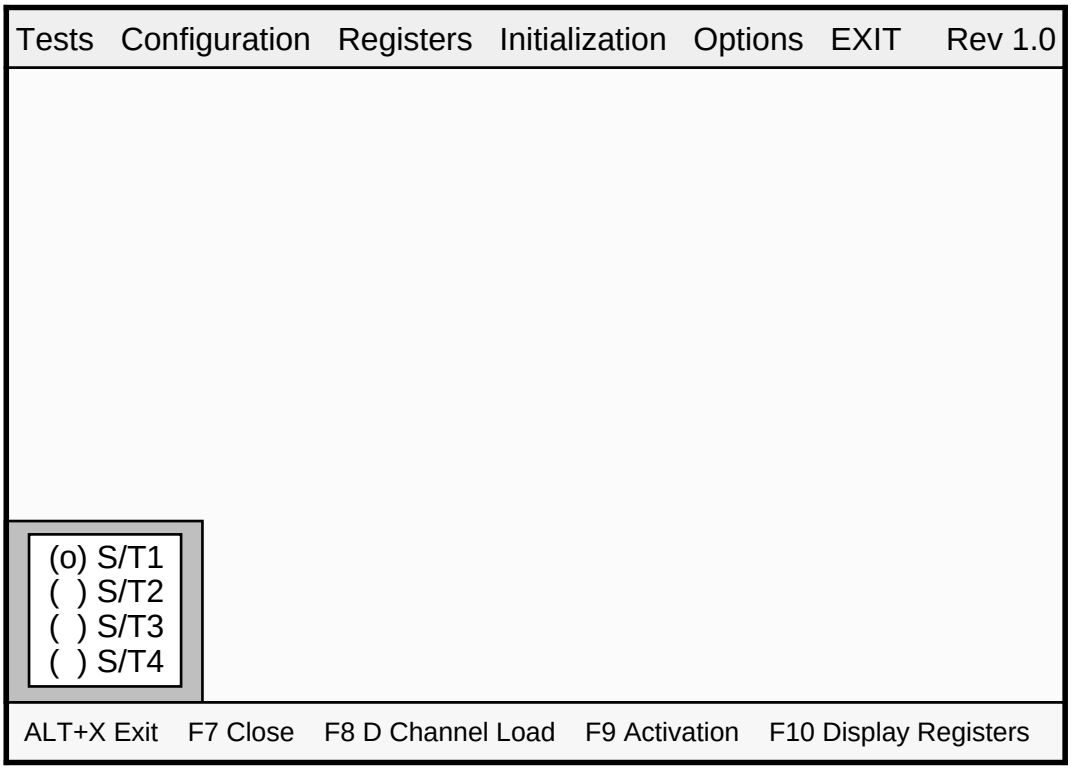


Fig 3.1 **General Menu**

There are 3 different parts in this environment:

* the general menu (top of the screen).

* the selection of the S/T interface (bottom left of the screen).

* the PF keys (bottom of the screen).

Required Hardware Environment:

* fully compatible PC.

* MS-DOS version 4.0 (minimum).

* one 3.5(High-Density floppy disk drive).

* one serial port.

* 640 Kbytes of RAM (minimum).

* mouse.

3.2 GENERAL MENU

The general menu has 6 submenus which can be selected either by the mouse or by the keys ALT + first letter of the submenu name (ex. ALT + T for Tests option).

3.2.1 EXIT

This option allows to exit of the software.

To exit, press on the OK button with the mouse or RETURN on the keyboard.

3.2.2 OPTIONS

This submenu has one option, RS232, which allows to configure the port used for the RS232 communication. Default value is COM 1.

The selection can be made with the mouse or with the arrows key.

The default values of the RS232 serial link parameters are:

* 9600 bauds.

* 1 start bit and 1 stop bit.

* 8 bits.

3.2.3 INITIALIZATION

This submenu allows to Activate, Desactivate or Reset the S/T interface selected (its number appears on the top of the window).The selection can be made with the

mouse or with the arrows key.

NOTE

The Desactivate option is not available when S/T interface is configurated in TE mode.

3.2.4 REGISTERS

This submenu allows a dialog with the registers of the S/T interfac (see MC145574 data sheet for a description of the registers).

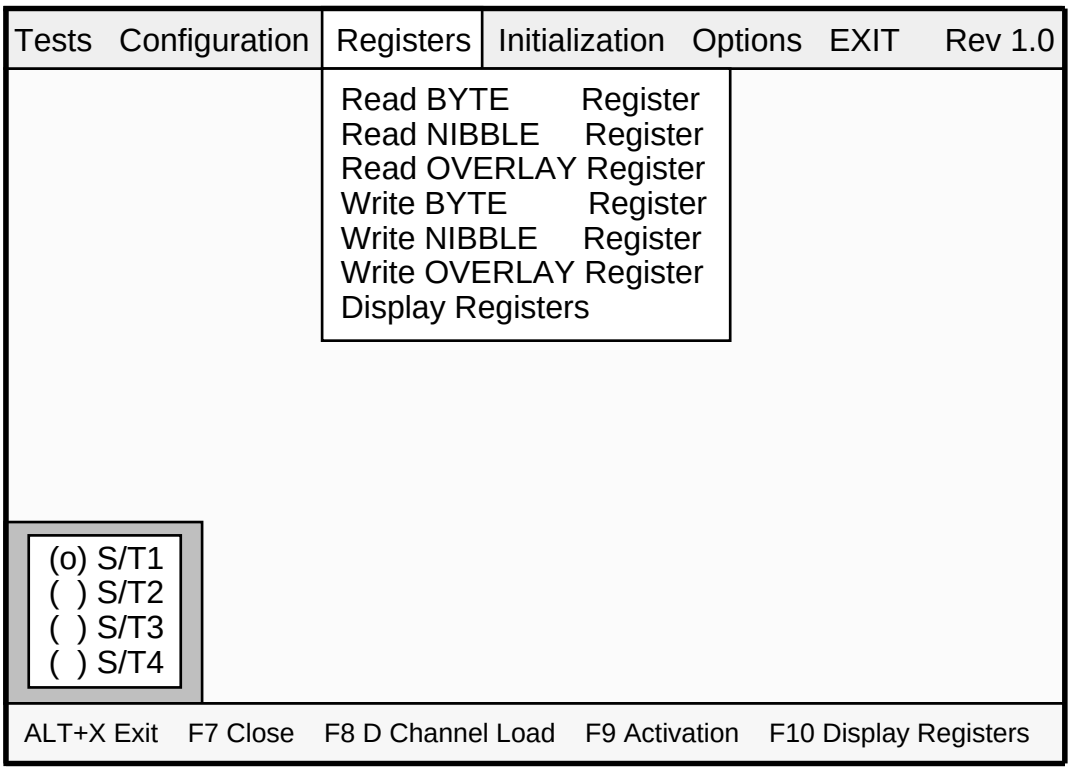


Fig 3.2 **Registers Menu**

It is possible to write and read in all these registers. Moreover, the option DISPLAY REGISTERS gives an overwiev of the registers values, the revision of the S/T interface and the D CHANNEL value loaded in the microcontroller (see 4.1 for a description of this value).

When several windows are opened, the mouse allows to select one, move and close it by pressing the left top corner (symbol [□]).

3.2.5 CONFIGURATION

This submenu allows to configure rapidly different parts of the S/T interface. These parts are:

* Loopback on the IDL Bus (the config choosen is writen in the Byte Register BR6 and the Nibble Register NR6).

* Loopback on the ST loop (the config choosen is writen in the Byte Register BR6).

* Clock Speed generated on the IDL Bus (the config choosen is writen in the Byte Registers BR7 and BR13).

* B1 and B2 enabled or ignored on the ST loop (the config choosen is writen in the Nibble Register NR5).

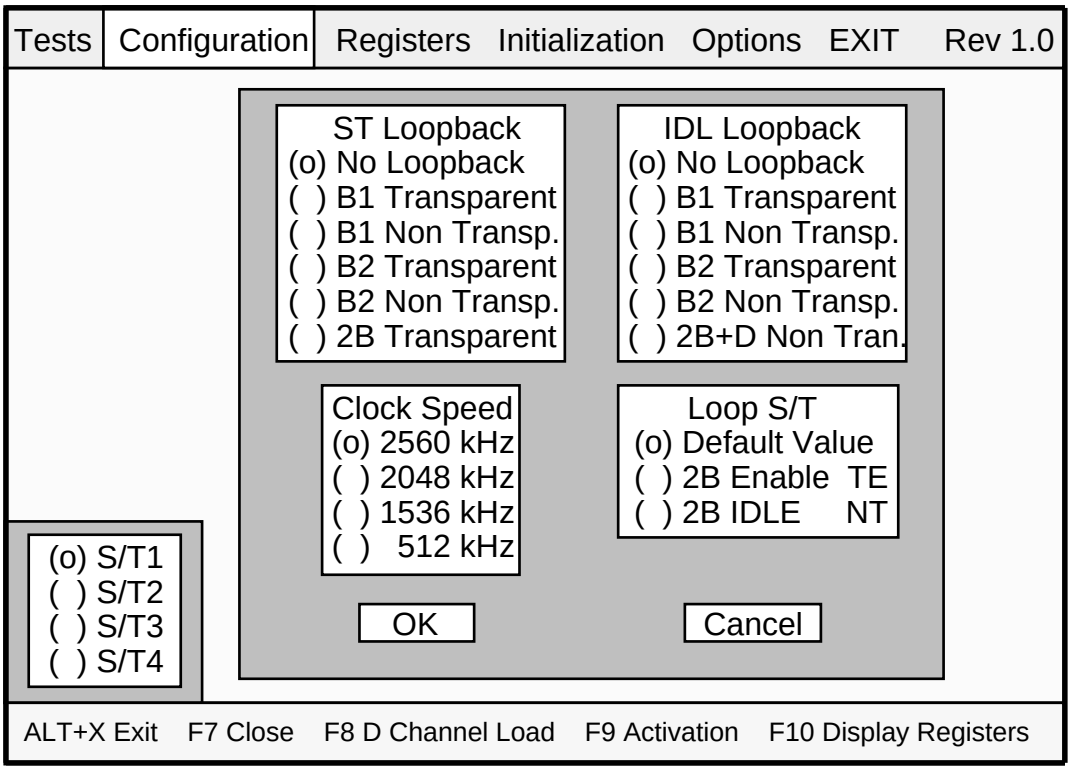


Fig 3.3 **Configuration Menu**

For more information about the registers used above, see MC145574 data sheet.

3.2.6 TESTS

The different tests implemented in the software will be described in section 4.

3.3 S/T CHIP SELECTION

4 different S/T chips can be selected. ST1 and ST2 are on the board. To access to ST3 and ST4, a second board (slave board) should be connected to the main board (master board) through the P3 connector. The microcontroller of the second board should be removed and the jumpers J6 and J7 of each board should be setup as described in section 2.8.

3.4 PF KEYS

3 accelerated keys allow to have some actions on the S/T chips selected :

* F8 to load a data for D channel tests.
* F9 to activate.
* F10 to have a display of all the registers.

F7 allows to close all the display registers windows openned.

4
TEST CONFIGURATIONS

4. TESTS MENU

The function of these different tests is to check the features of the D Channel Access.

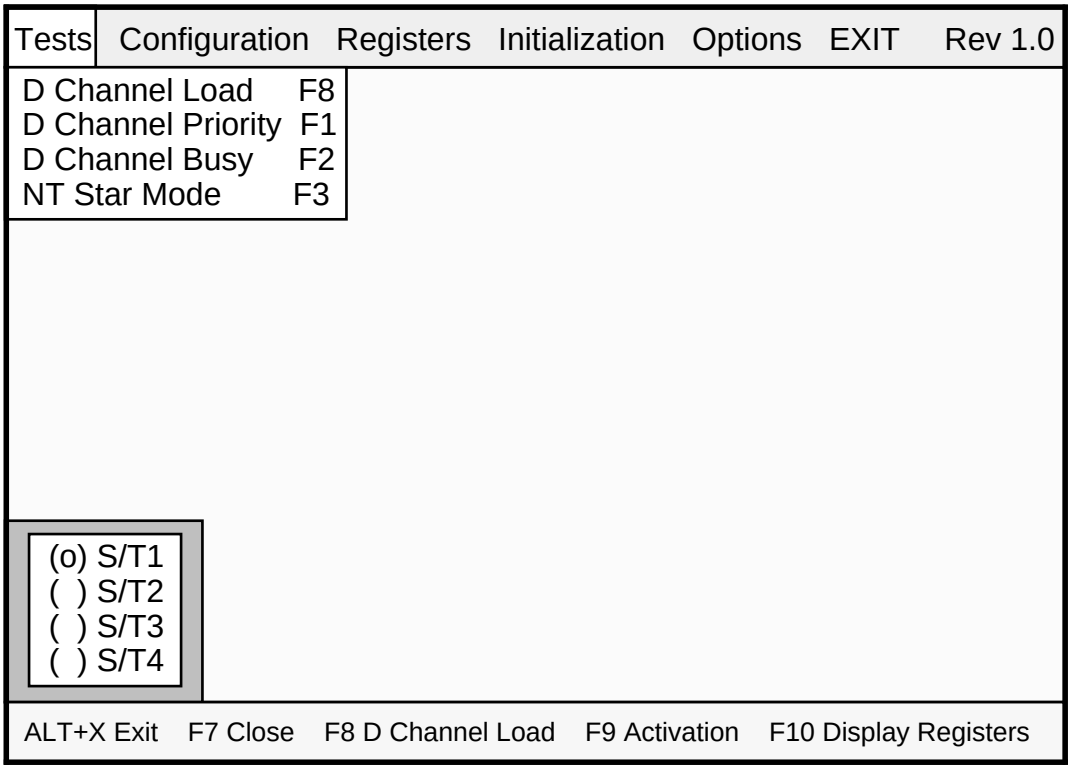


Fig 4.1 **Tests Menu**

To perform the following tests, it is necessary to have 2 boards. One will be configured as master board (with the microcontroller) and one as slave board (without the microcontroller). The link between the 2 boards is realised with a cable connected to the two P3 connectors. The jumpers J6 and J7 of each board should be setup as described in section 2.8.

4.1 D CHANNEL LOADING

This option allows to load in the microcontroller a value which will be used by the D Channel busy or NT Star Mode tests.

The value to load should be in the range 00 to FF Hexa value (default value is 00) and assigned to the S/T interfaces ST1 and ST2. The selection of the S/T interface should be done before starting the test (the selection of ST3 or ST4 will assign the value to ST1).

4.2 D CHANNEL PRIORITY

This option allows to measure the time for a S/T interface to gain access to the D channel in function of its priority class.

The ST1 and ST2 interfaces should be configured in TE mode with their loops connected. The ST3 interface should be configured in NT mode. Before starting the test, the loop between the 3 interfaces should be activated.

When the test is started, 4 possibilities appear for the ST1 and ST2 priority class configuration. When the choice is done, the microcontroller forces the ST3 to send 0 into the D channel. So, ST1 and ST2 put their DGRANT outputs to low to indicate that the D channel is busy. The microcontroller sends to ST1 and ST2 a D channel access request (DREQUEST input to high) then forces the ST3 to send 1 back into the D channel. According to their priority class, ST1 and ST2 count the number of 1 in the D channel to gain access and put their DGRANT output to high. If the priority class between ST1 and ST2 is different, the first S/T interface to gain access sends 1 into the D channel to allow to the second S/T interface to gain access to the D channel.

4.3 D CHANNEL BUSY

This option allows to create collision between two TE’s which want to gain access in the same time.

The ST1 and ST2 interfaces should be configured in TE mode with their loops connected (see figure 4.2). The ST3 interface should be configured in NT mode. Before starting the test, the loop between the 3 interfaces should be activated.

The test begins by a D channel access request (DREQUEST input to high) to ST1 and ST2 in the same time. As their DGRANT is already active (hight), this request allows to send data in the D channel. The data send are the data loaded in the microcontroller with the D Channel load test.

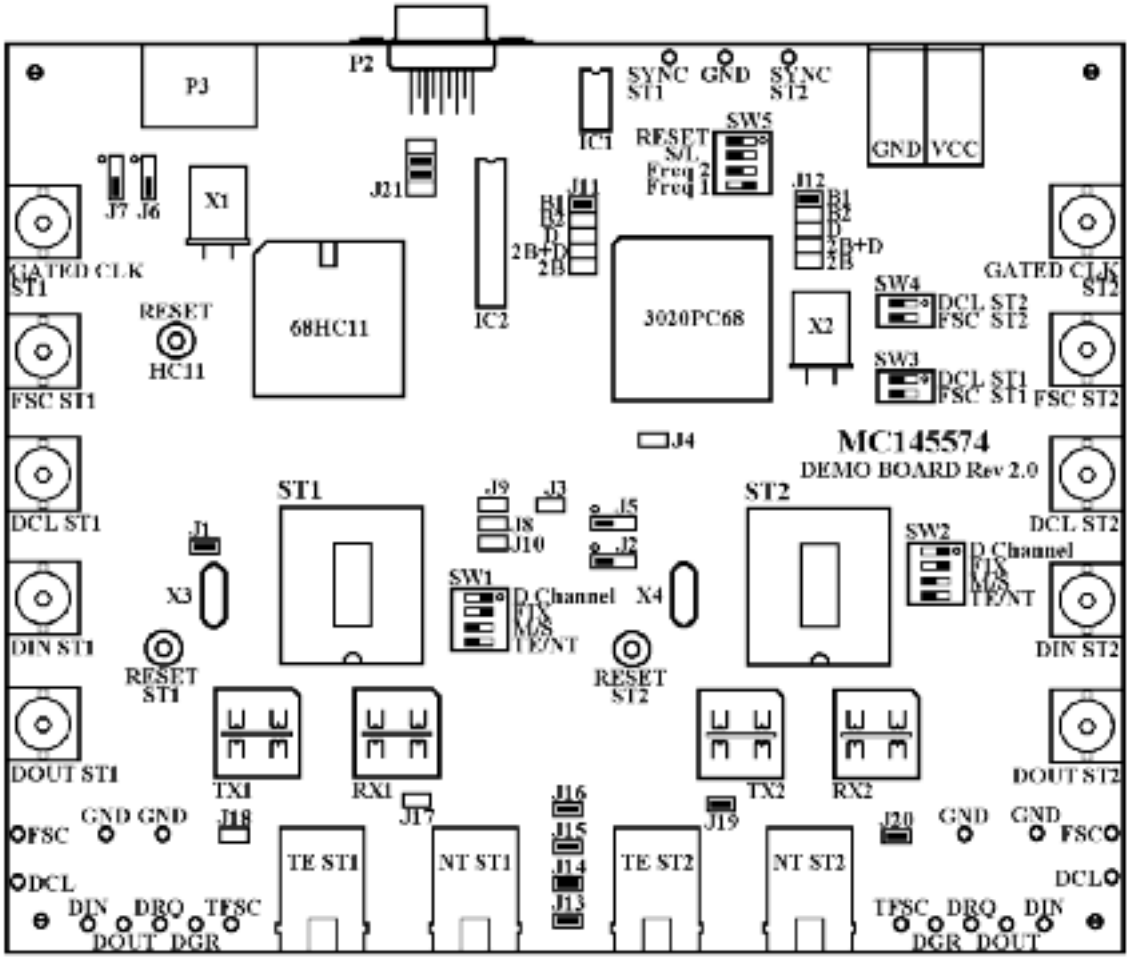


Fig 4.2 **D Channel busy test setup**

When ST1 or ST2 detects a collision, it puts immediatly its DGRANT output to low and loses the acces to the D channel. The other S/T interface continues to send its data in the D channel. The collision is detected when a 1 is sent in the D channel and come back with the value 0 in the Echo bit (see MC145574 data sheet for information on the Echo bit).

Example:

Load F5 ($11110101) in the microcontroller for ST1 and F1 ($11110001) for ST2.

Start the D Channel busy test. The micontroller sends a DREQUEST to ST1 and ST2 and begins to put data at the D channel location on the ST1 and ST2 IDL buses. The LSB (Low Significant Bit) of the values loaded in the microcontroller is the first bit sent. As the D channel of the loop is available, ST1 and ST2 transfer the D channel data from the IDL bus to the S/T loop.

The third bit sent on the S/T loop is 1 for ST1 and 0 for ST2. As the 0 value as the priority, ST1 will find a 0 in the ECHO bit so dectects the collision. ST2 will continue to send its data.

To follow the test with a scope, you can use the signals SYNC ST1 and SYNC ST2. These 2 clocks allow to repair the D datas sent on the IDL-DIN inputs when DREQUEST is high. In fact, these signals are D gated clocks provided by the 3020PC68 activated by a D Channel request.

4.4 NT STAR MODE

This option allows to create collision between two TE's which want to gain access in the same time when two NT are configured in NT Star Mode..

The ST1 and ST2 interfaces should be configured in TE mode (see figure 4.3). The ST3 and ST4 interfaces should be configured in NT Star Mode (see figure 4.4 and MC145574 data sheet). Before starting the test, the two loops between the ST1-ST3 and ST2-ST4 should be activated.

The test begins by a D channel access request (DREQUEST input to high) to ST1 and ST2 in the same time. As their DGRANT is already active (hight), this request allows to send data in the D channel. The data send are the data loaded in the microcontroller with the D Channel load test.

When ST1 or St2 detects a collision, it puts immediatly its DGRANT output to low and loses the acces to the D channel. The other S/T interface continues to send its data in the D channel. The collision is detected when a 1 is sent in the D channel and come back with the value 0 in the Echo bit (see MC145574 data sheet for information on the Echo bit).

Exemple:

Load F5 ($11110101) in the microcontroller for ST1 and FD ($11111101) for ST2.

Start the D Channel busy test. The micontroller sends a DREQUEST to ST1 and ST2 and begins to put data at the D channel location on the ST1 and ST2 IDL buses. The LSB (Low Significant Bit) of the values loaded in the microcontroller is the first bit sent. As the D channel of the loop is available, ST1 and ST2 transfer the D channel data from the IDL bus to the S/T loop.

The fourth bit sent on the S/T loop is 0 for ST1 and 1 for ST2. As the 0 value as the priority, ST2 will find a 0 in the ECHO bit so dectects the collision. ST1 will continue to send its data.

To follow the test with a scope, you can use the signals SYNC ST1 and SYNC ST2. These 2 clocks allow to repair the D datas sent on the IDL-DIN inputs when DREQUEST is high. In fact, these signals are D gated clocks provided by the 3020PC68 activated by a D Channel request.

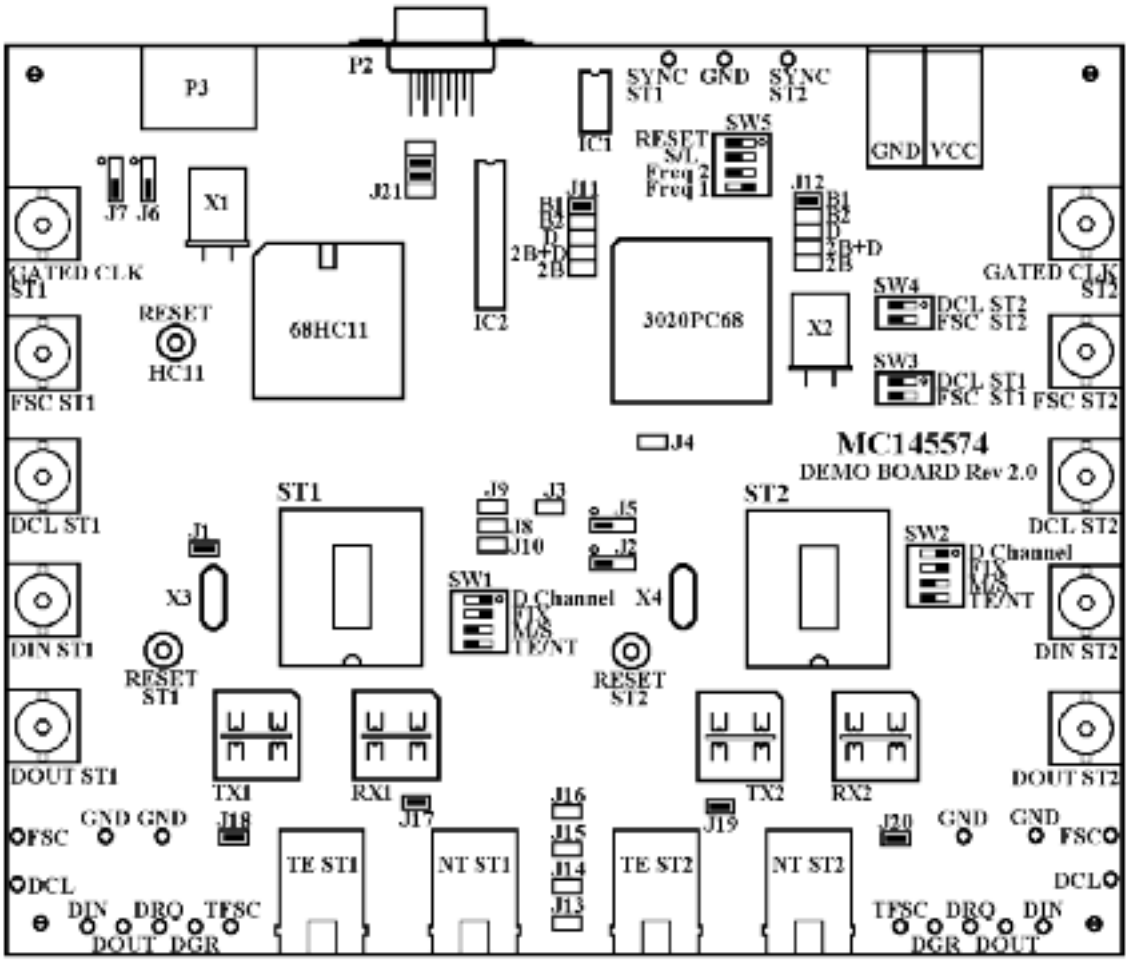


Fig 4.3 **NT Star Mode test setup for master board**

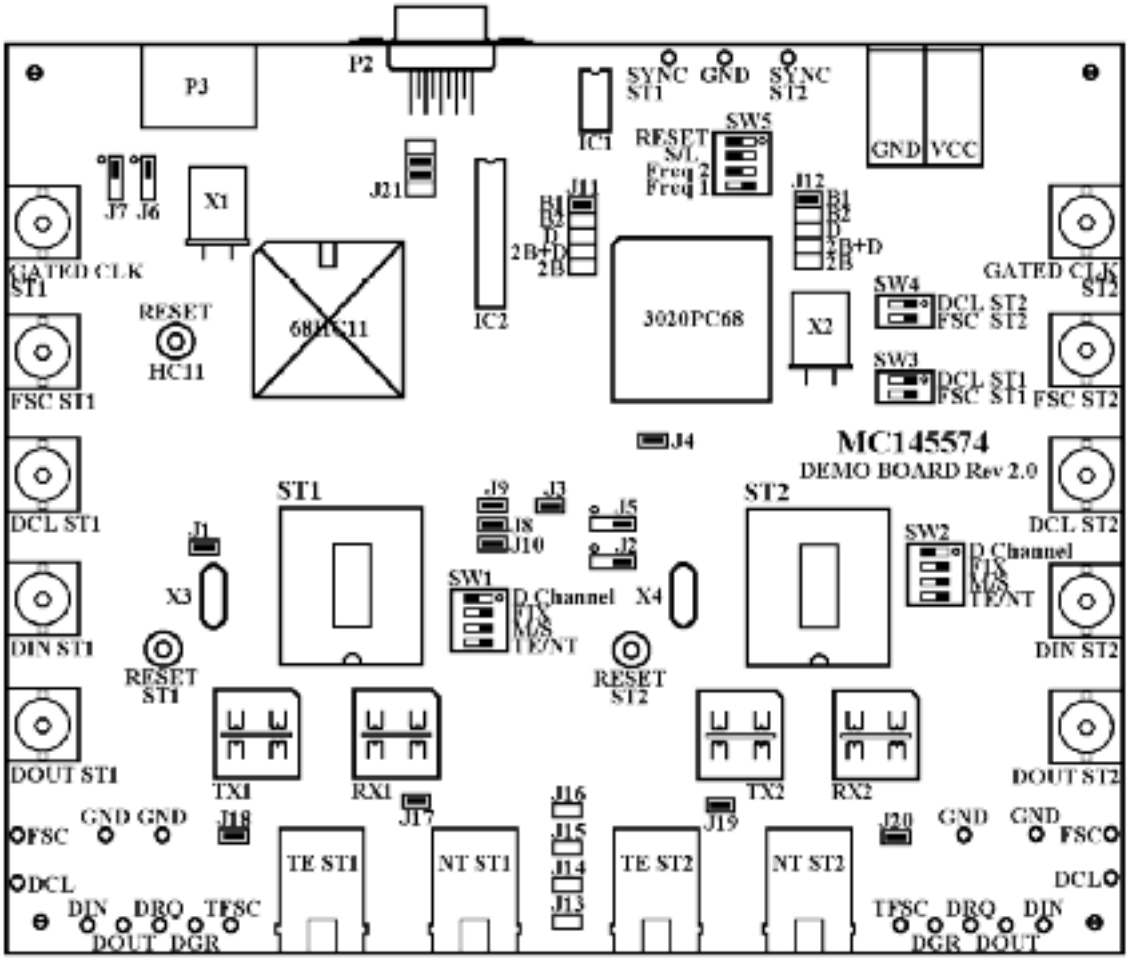
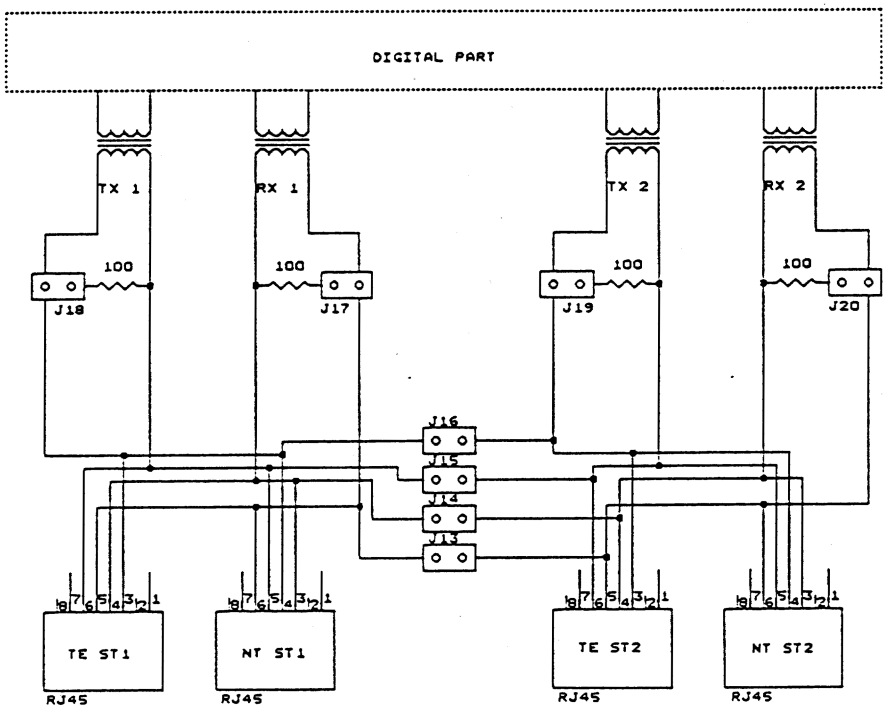


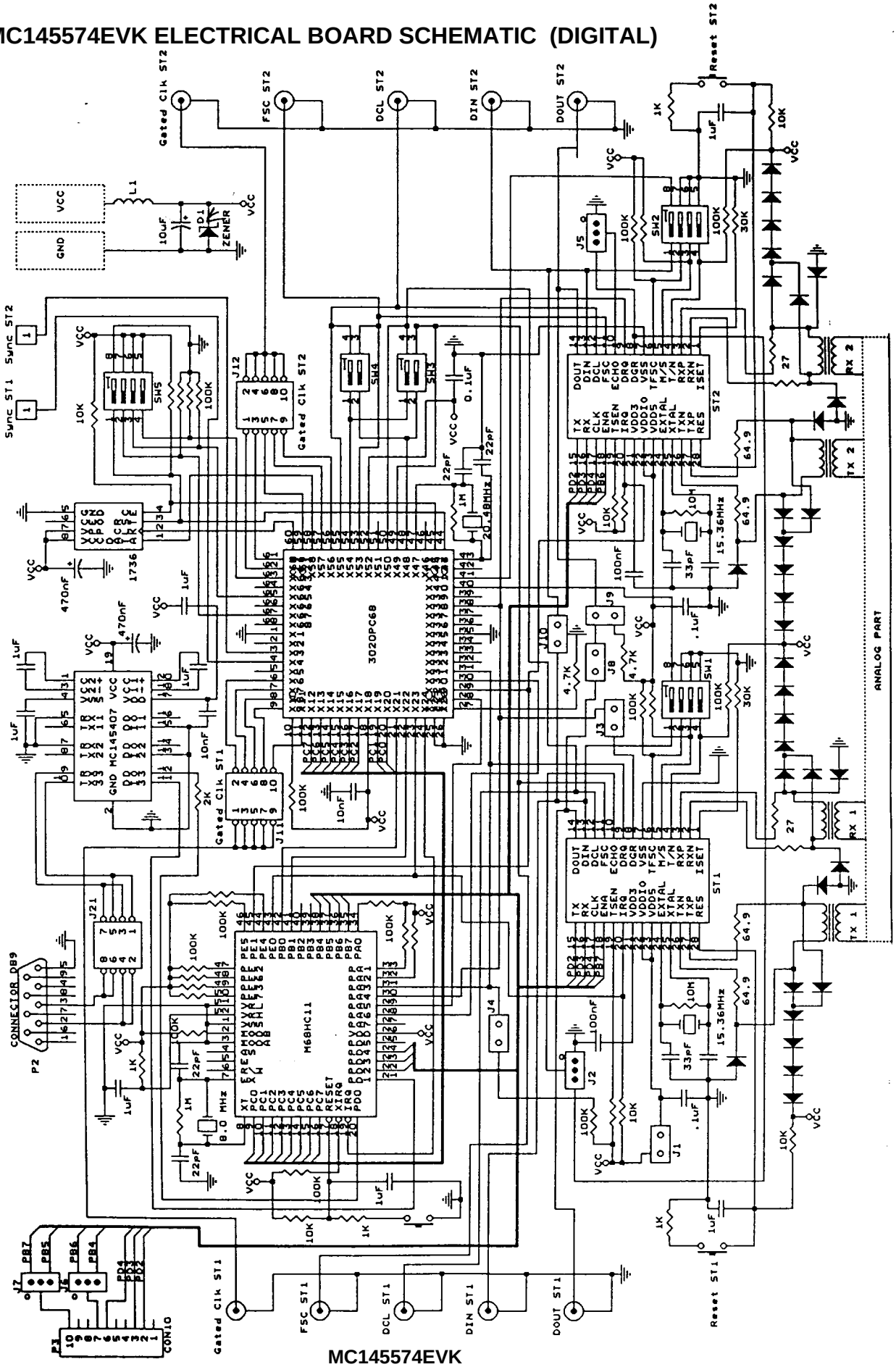
Fig 4.4 **NT Star Mode test setup for slave board**

APPENDIX A

A-1 MC145574EVK ELECTRICAL BOARD SCHEMATIC (ANALOG PART OF THE BOARD)

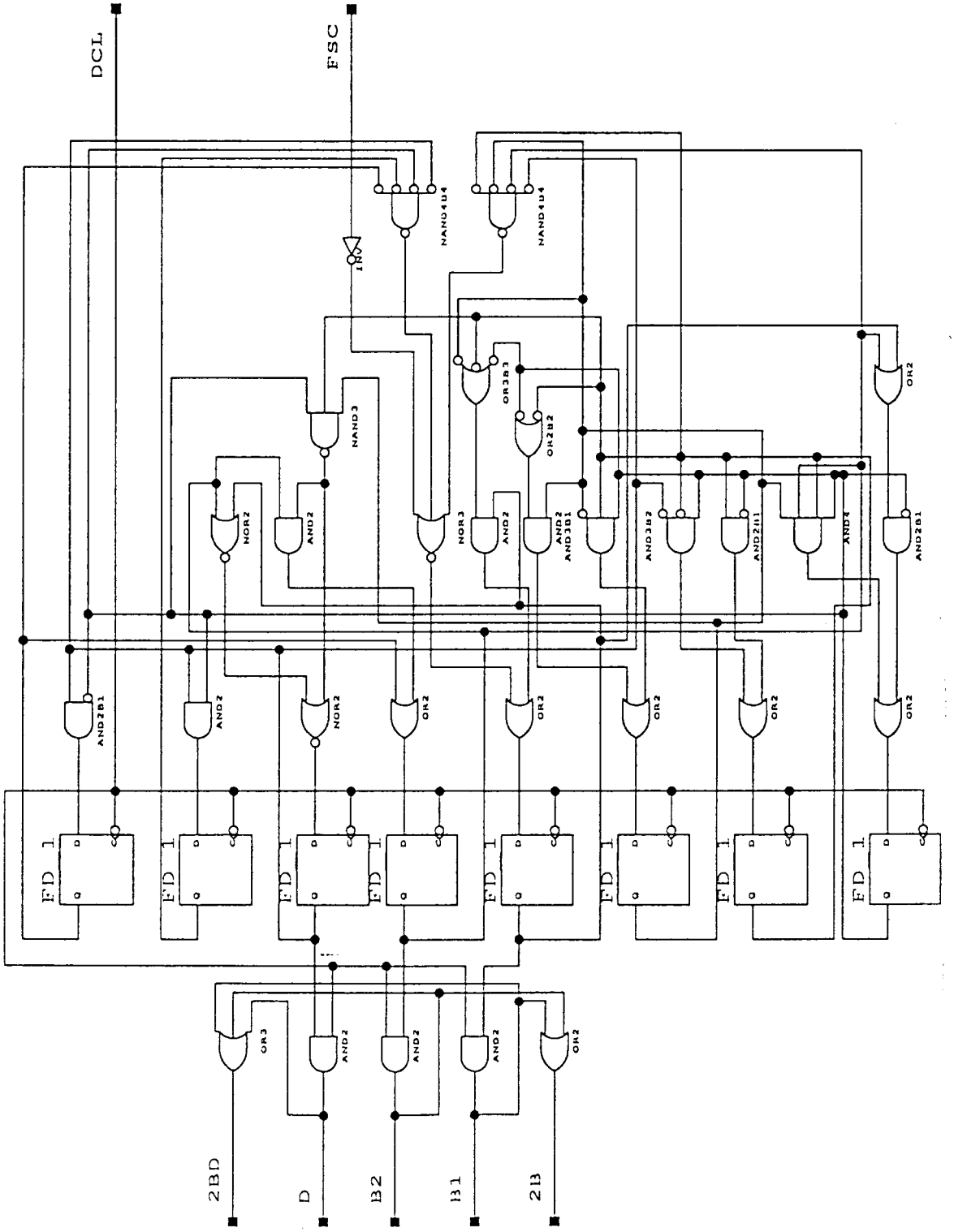


A-2 MC145574EVK ELECTRICAL BOARD SCHEMATIC (DIGITAL)

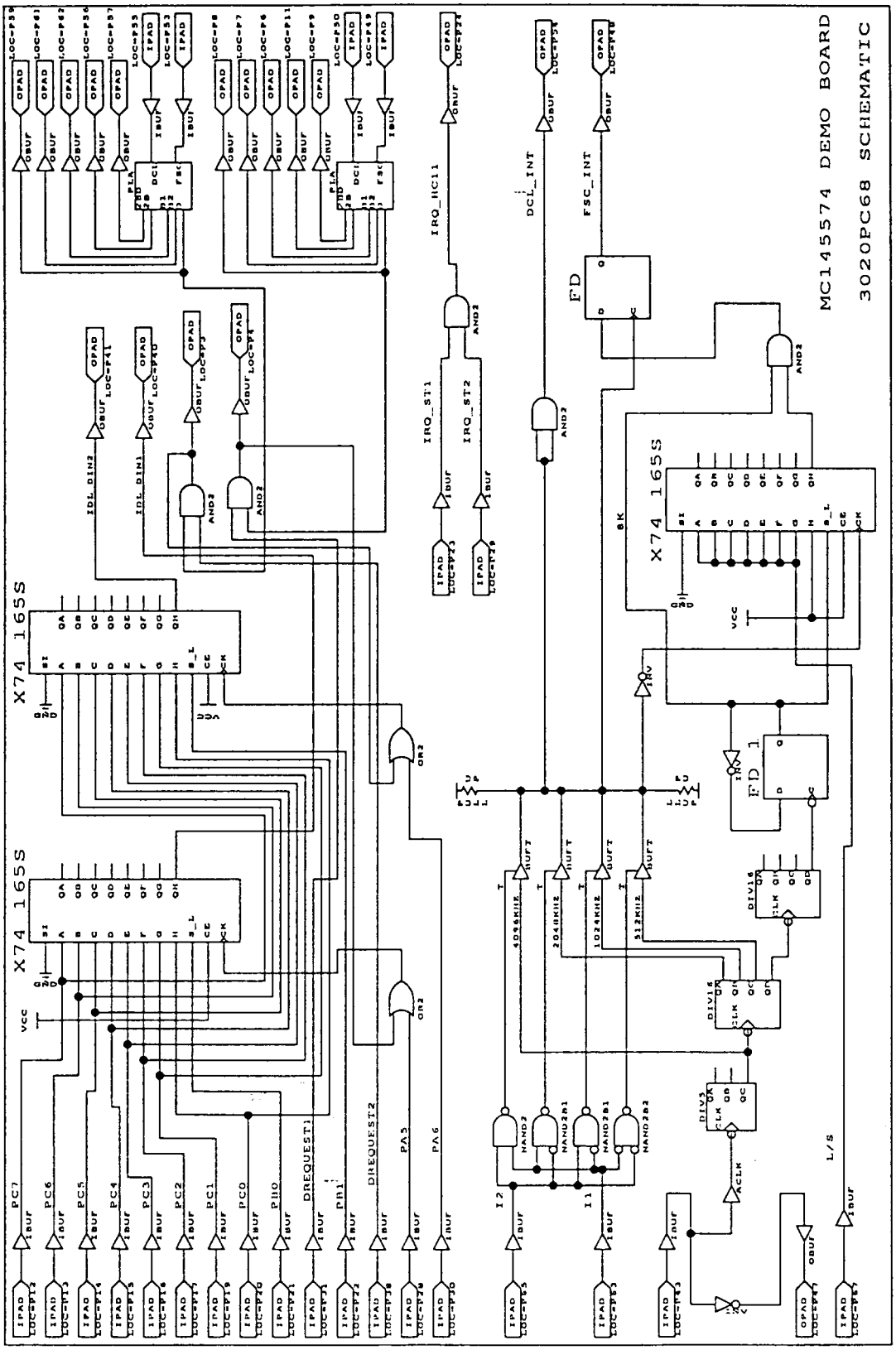


APPENDIX B

B-1 MC145574EVK XILINX (3020) PLA CONFIGURATION SCHEMATIC

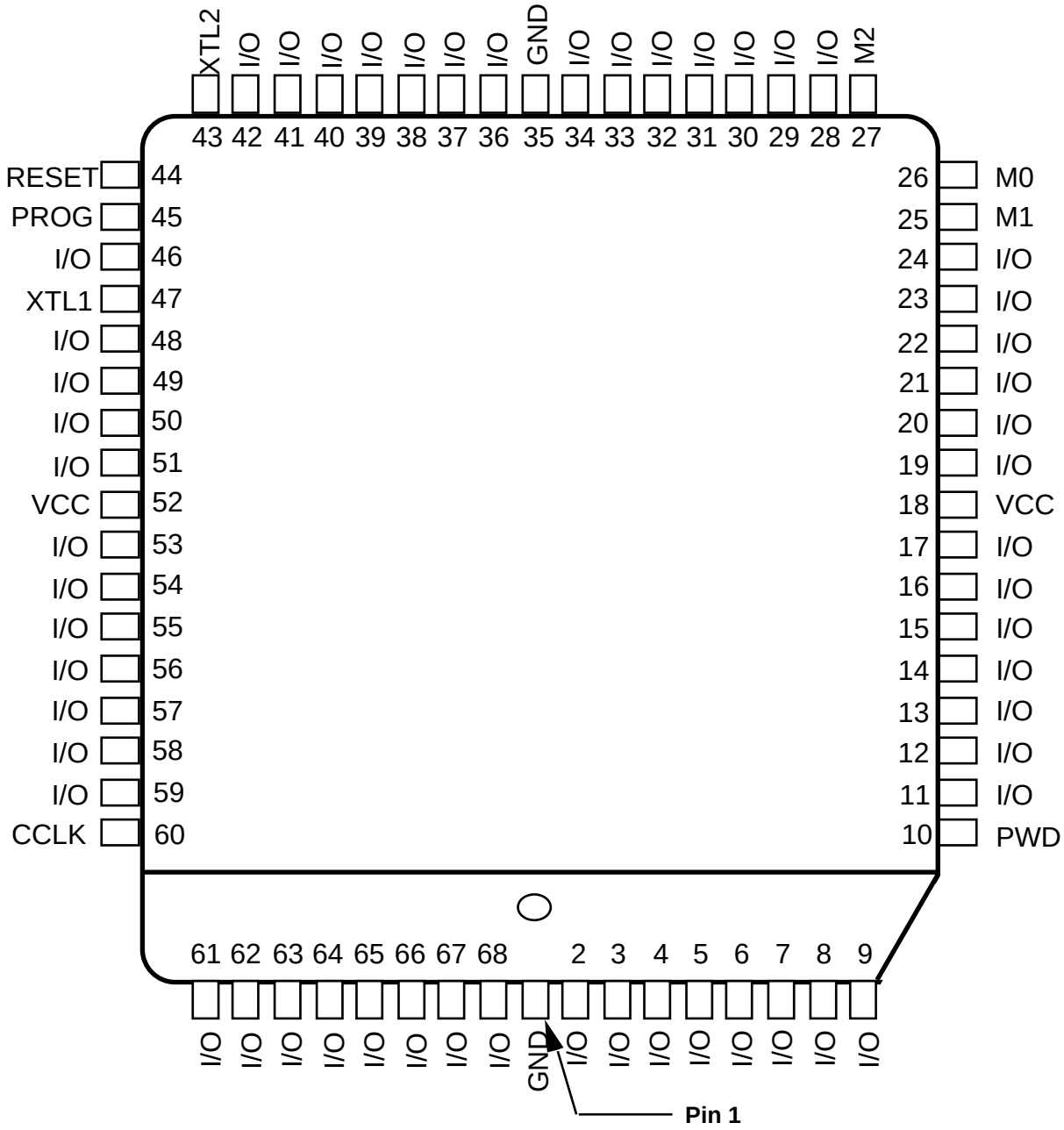


B-2 MC145574EVK XILINX (3020) GENERAL CONFIGURATION SCHEMATIC

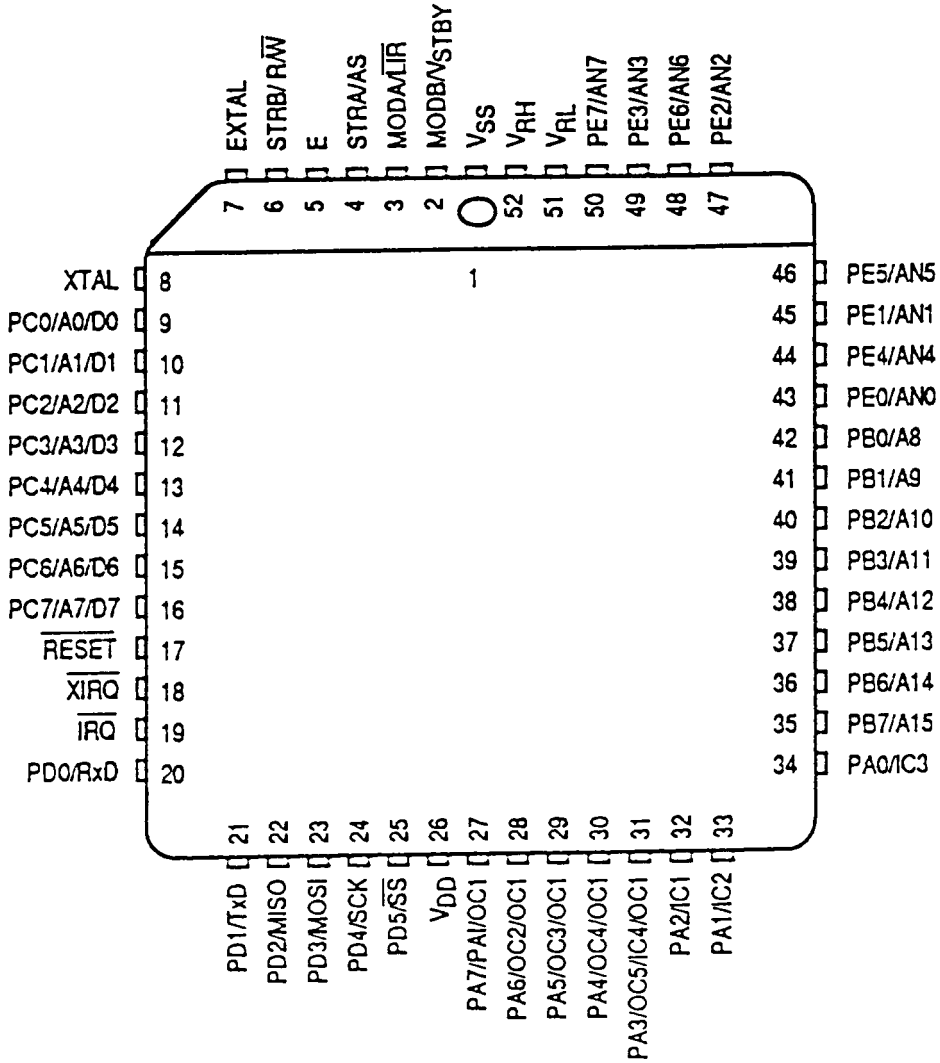


APPENDIX C

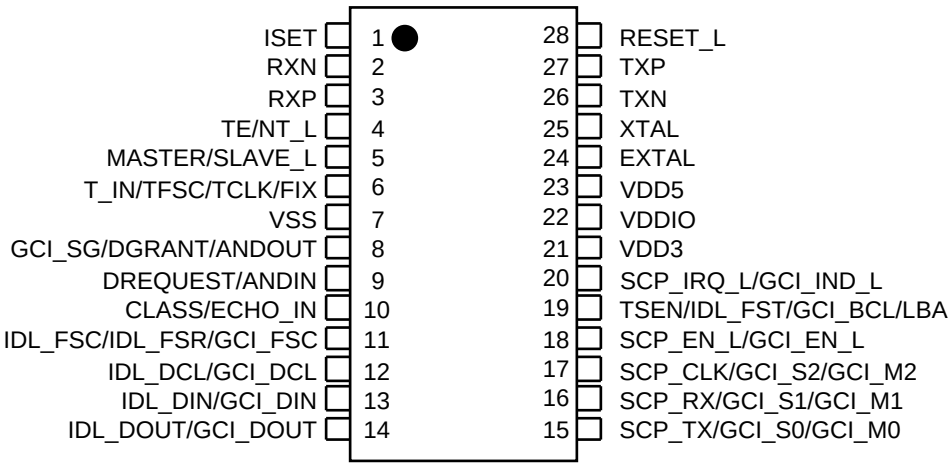
C-1 MC145574EVK XILINX (3020PC68) PINOUT



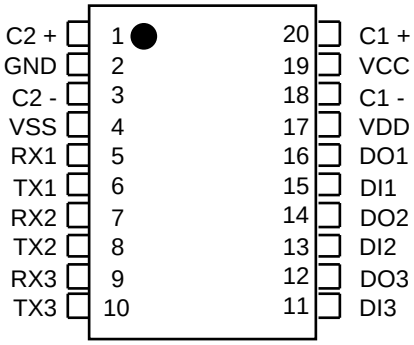
C-2 MC145574EVK MC68HC11E9 PINOUT



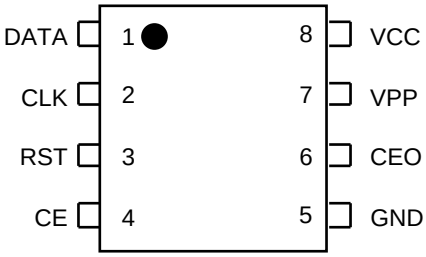
C-3 MC145574EVK MC145574DW PINOUT



C-4 MC145574EVK MC145407P PINOUT

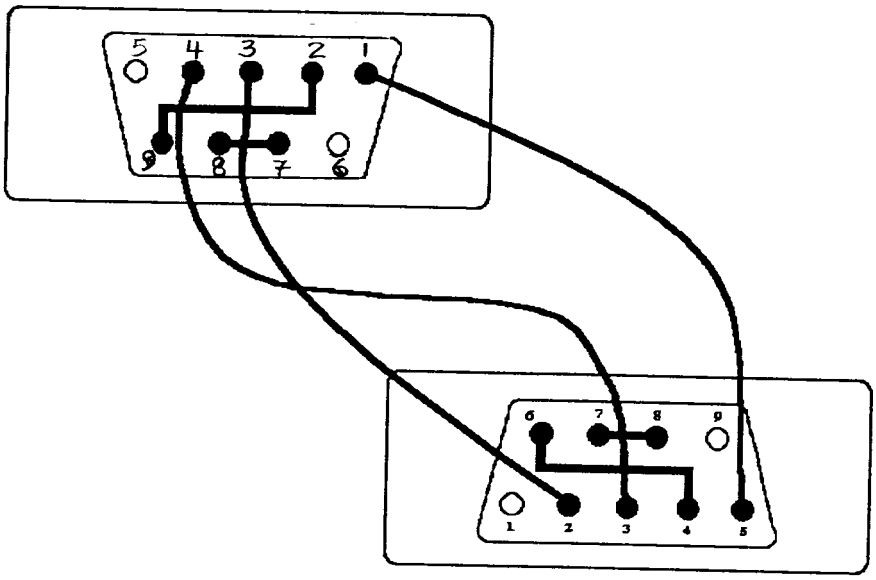


C-5 MC145574EVK PROM (1736) PINOUT



APPENDIX D

D-1 MC145574EVK RS232 CABLE



The 2 connectors are standard DB9 connectors.