

Product Preview

MC14SM5567/D

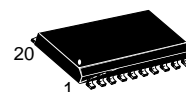
Rev. 0, 4/2002

MC14SM5567

PCM Codec-Filter

Freescale Semiconductor, Inc.

The MC14SM5567 is a per channel PCM Codec-Filter, designed to operate in both synchronous and asynchronous applications. This device performs the voice digitization and reconstruction as well as the band limiting and smoothing required for (A-Law) PCM systems.



**DW SUFFIX
SOG PACKAGE
CASE 751D**

This device has an input operational amplifier whose output is the input to the encoder section. The encoder section immediately low-pass filters the analog signal with an RC filter to eliminate very-high-frequency noise from being modulated down to the pass band by the switched capacitor filter. From the active R-C filter, the analog signal is converted to a differential signal. From this point, all analog signal processing is done differentially. This allows processing of an analog signal that is twice the amplitude allowed by a single-ended design, which reduces the significance of noise to both the inverted and non-inverted signal paths. Another advantage of this differential design is that noise injected via the power supplies is a common mode signal that is cancelled when the inverted and non-inverted signals are recombined. This dramatically improves the power supply rejection ratio.

After the differential converter, a differential switched capacitor filter band passes the analog signal from 200 Hz to 3400 Hz before the signal is digitized by the differential compressing A/D converter.

The decoder accepts PCM data and expands it using a differential D/A converter. The output of the D/A is low-pass filtered at 3400 Hz and $\sin X/X$ compensated by a differential switched capacitor filter. The signal is then filtered by an active R-C filter to eliminate the out-of-band energy of the switched capacitor filter.

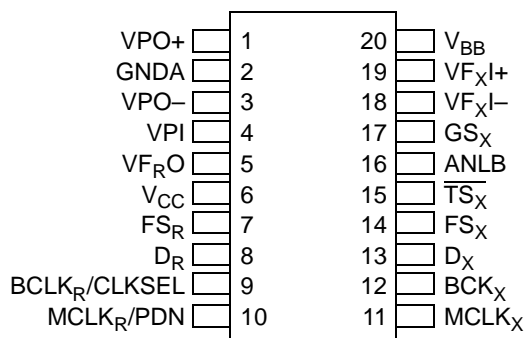
This device accepts both long- and short-frame industry standard clock formats.

- Fully Differential Analog Circuit Design for Lowest Noise
- Extended Temperature Range of -40° to 85°C
- Transmit Band-Pass and Receive Low-Pass Filters On-Chip
- Active R-C Pre-Filtering and Post-Filtering
- A-Law Companding
- On-Chip Precision Voltage Reference (2.5 V)
- Typical Power Dissipation of 40 mW, Power Down of 1.0 mW at ± 5 V
- Push-Pull Power Drivers with External Gain Adjust
- Analog Loopback
- 20-Pin SOG Package

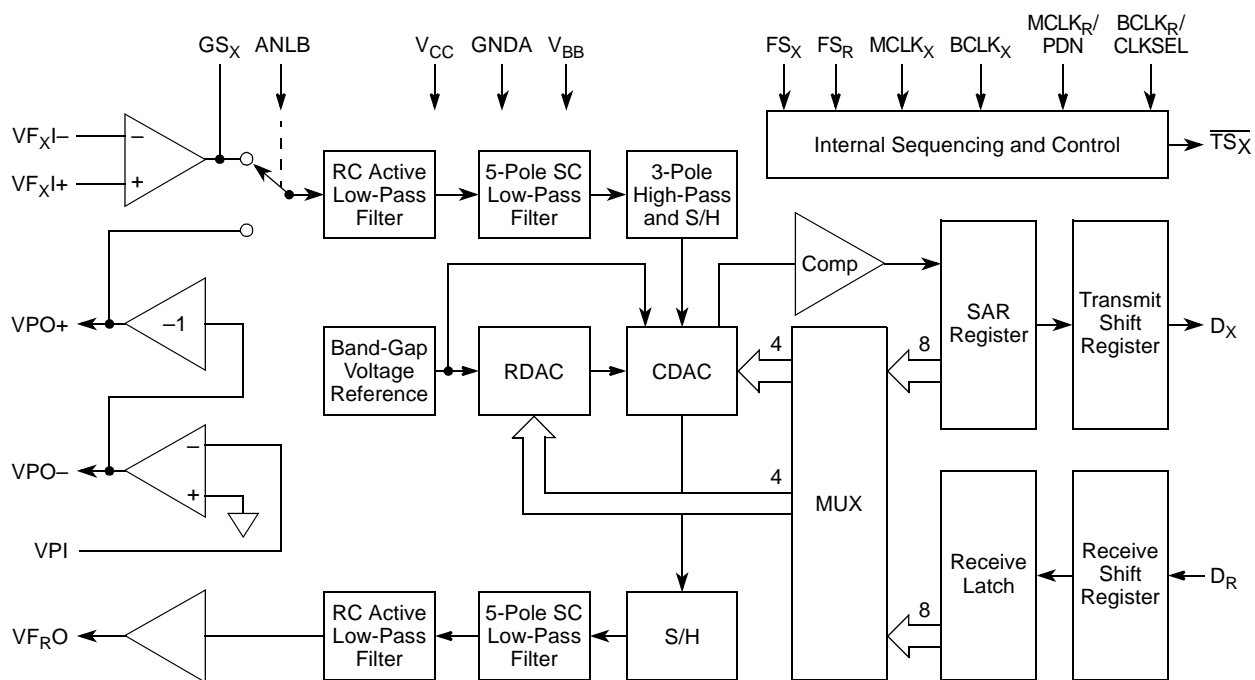


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PIN ASSIGNMENTS



FUNCTIONAL BLOCK DIAGRAM





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DEVICE DESCRIPTION

A codec-filter is used for digitizing and reconstructing the human voice. This device was developed primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from COder (for the A/D used to digitize voice) and DECoder (for the D/A used for reconstructing voice). A codec is a single device that does both the A/D and D/A conversions.

To digitize intelligible voice requires a signal-to-distortion ratio of about 30 dB over a dynamic range of about 40 dB. This can be accomplished with a linear 13-bit A/D and D/A, but will far exceed the required signal-to-distortion ratio at amplitudes greater than 40 dB below the peak amplitude. This excess performance is at the expense of data per sample. Methods of data reduction are implemented by compressing the 13-bit linear scheme to companded 8-bit schemes. There are two companding schemes used: Mu-255 Law specifically in North America, and A-Law specifically in Europe. These companding schemes are accepted world wide. These companding schemes follow a segmented or piecewise-linear curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all 16 of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits which increment. When the chord bits increment, the step bits double their voltage weighting. This results in an effective resolution of six bits (sign + chord + four step bits) across a 42 dB dynamic range (seven chords above zero, by 6 dB per chord). Table 3 shows the linear quantization levels to PCM words for the A-Law companding scheme.

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a band width of 3 kHz. This sampling requires a low-pass filter to limit the high frequency energy above 3 kHz from distorting the in-band signal. The telephone line is also subject to 50/60 Hz power line coupling, which must be attenuated from the signal by a high-pass filter before the A/D converter.

The D/A process reconstructs a staircase version of the desired in-band signal, which has spectral images of the in-band signal modulated about the sample frequency and its harmonics. These spectral images, called aliasing components, need to be attenuated to obtain the desired signal. The low-pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The MC14SM5567 PCM Codec-Filter, incorporating A-law companding, has the codec, both presampling and reconstruction filters, and a precision voltage reference on-chip, and requires no external components.



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PIN DESCRIPTION

DIGITAL

FS_R

Receive Frame Sync

This is an 8 kHz enable that must be synchronous with BCLK_R. Following a rising FS_R edge, a serial PCM word at D_R is clocked by BCLK_R into the receive data register. FS_R also initiates a decode on the previous PCM word. In the absence of FS_X, the length of the FS_R pulse is used to determine whether the I/O conforms to the Short Frame Sync or Long Frame Sync convention.

D_R

Receive Digital Data Input

BCLK_R/CLKSEL

Receive Data Clock and Master Clock Frequency Selector

If this input is a clock, it must be between 128 kHz and 4.096 MHz, and synchronous with FS_R. In synchronous applications this pin may be held at a constant level; then BCLK_X is used as the data clock for both the transmit and receive sides, and this pin selects the assumed frequency of the master clock (see Table 1).

MCLK_R/PDN

Receive Master Clock and Power-Down Control

Because of the shared DAC architecture used on this device, only one master clock is needed. Whenever FS_X is clocking, MCLK_X is used to derive all internal clocks, and the MCLK_R/PDN pin merely serves as a power-down control. If MCLK_R/PDN pin is held low or is clocked (and at least one of the frame syncs is present), the part is powered up. If this pin is held high, the part is powered down. If FS_X is absent but FS_R is still clocking, the device goes into receive half-channel mode, and MCLK_R (if clocking) generates the internal clocks.

MCLK_X

Transmit Master Clock

This clock is used to derive the internal sequencing clocks; it must be 1.536, 1.544, or 2.048 MHz.

BCLK_X

Transmit Data Clock

BCLK_X may be any frequency between 128 kHz and 4.096 MHz, but it should be synchronous with MCLK_X.

D_X

Transmit Digital Data Output

This output is controlled by FS_X and BCLK_X to output the PCM data word; otherwise this pin is in a high-impedance state.

FS_X

Transmit Frame Sync

This is an 8 kHz enable that must be synchronous with BCLK_X. A rising FS_X edge initiates the transmission of a serial PCM word, clocked by BCLK_X, out of D_X. If the FS_X pulse is high for more than eight BCLK_X periods, the D_X and TS_X outputs will remain in a low-impedance state until FS_X is brought low. The length of the FS_X pulse is used to determine whether the transmit and receive digital I/O conforms to the Short Frame Sync or to the Long Frame Sync convention.



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\overline{TS}_X

Transmit Time Slot Indicator

This is an open-drain output that goes low whenever the D_X output is in a low-impedance state (that is, during the transmit time slot when the PCM word is being output) for enabling a PCM bus driver.

ANLB

Analog Loopback Control Input

When held high, this pin causes the input of the transmit RC active filter to be disconnected from GS_X and connected to VPO+ for analog loopback testing. This pin is held low in normal operation.

ANALOG

GS_X

Gain-Setting Transmit

This output of the transmit gain-adjust operational amplifier is internally connected to the encoder section of the device. It must be used in conjunction with VF_{XI-} and VF_{XI+} to set the transmit gain for a maximum signal amplitude of 2.5 V peak. This output can drive a 600- Ω load to a 2.5-V peak.

VF_{XI-}

Voice-Frequency Transmit Input (Inverting)

This is the inverting input of the transmit gain-adjust operational amplifier.

VF_{XI+}

Voice-Frequency Transmit Input (Non-Inverting)

This is the non-inverting input of the transmit gain-adjust operational amplifier.

VF_{RO}

Voice-Frequency Receive Output

This receive analog output is capable of driving a 600- Ω load to a 2.5-V peak.

VPI

Voltage Power Input

This is the inverting input to the first receive power amplifier. Both of the receive power amplifiers can be powered down by connecting this input to V_{BB} .

VPO-

Voltage Power Output (Inverted)

This inverted output of the receive push-pull power amplifiers can drive 300 Ω to a 3.3-V peak.

VPO+

Voltage Power Output (Non-Inverted)

This non-inverted output of the receive push-pull power amplifier pair can drive 300 Ω to a 3.3-V peak.

POWER SUPPLY

GNDA

Analog Ground

This terminal is the reference level for all signals, both analog and digital, and is 0 V.



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V_{CC}
Positive Power Supply

V_{CC} is typically 5 V.

V_{BB}
Negative Power Supply

V_{BB} is typically -5 V.



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FUNCTIONAL DESCRIPTION

ANALOG INTERFACE AND SIGNAL PATH

The transmit portion of this codec-filter includes a low-noise gain setting amplifier capable of driving a 600- Ω load. Its output is fed to a three-pole anti-aliasing pre-filter. This pre-filter incorporates a two-pole Butterworth active low-pass filter, and a single passive pole. This pre-filter is followed by a single ended-to-differential converter that is clocked at 256 kHz. All subsequent analog processing utilizes fully differential circuitry. The next section is a fully-differential, five-pole switched capacitor low-pass filter with a 3.4-kHz pass band. After this filter is a three-pole switched-capacitor high-pass filter having a cutoff frequency of about 200 Hz. This high-pass stage has a transmission zero at dc that eliminates any dc coming from the analog input or from accumulated operational amplifier offsets in the preceding filter stages. The last stage of the high-pass filter is an autozeroed sample and hold amplifier.

One bandgap voltage reference generator and digital-to-analog converter (DAC) are shared by the transmit and receive sections. The autozeroed, switched-capacitor band gap reference generates precise positive and negative reference voltages that are independent of temperature and power supply voltage. A binary-weighted capacitor array (CDAC) forms the chords of the companding structure, while a resistor string (RDAC) implements the linear steps within each chord. The encode process uses the DAC, the voltage reference, and a frame-by-frame autozeroed comparator to implement a successive-approximation conversion algorithm. All of the analog circuitry involved in the data conversion—the voltage reference, RDAC, CDAC, and comparator—are implemented with a differential architecture.

The receive section includes the DAC described above, a sample and hold amplifier, a five-pole 3400-Hz switched capacitor low-pass filter with $\sin X/X$ correction, and a two-pole active smoothing filter to reduce the spectral components of the switched capacitor filter. The output of the smoothing filter is a power amplifier that is capable of driving a 600- Ω load. This device adds a pair of power amplifiers that are connected in a push-pull configuration; two external resistors set the gain of both of the complementary outputs. The output of the second amplifier may be internally connected to the input of the transmit anti-aliasing filter by bringing the ANLB pin high. The power amplifiers can drive unbalanced 300- Ω loads or a balanced 600- Ω load; they may be powered down independent of the rest of the chip by tying the VPI pin to V_{BB} .

MASTER CLOCKS

Since the codec-filter design has a single DAC architecture, only one master clock is used. In normal operation (both frame syncs clocking), the $MCLK_X$ is used as the master clock, regardless of whether the $MCLK_R/PDN$ pin is clocking or low. The same is true if the part is in transmit half-channel mode (FS_X clocking, FS_R held low). But if the codec-filter is in the receive half-channel mode, with FS_R clocking and FS_X held low, $MCLK_R$ is used for the internal master clock if it is clocking; if $MCLK_R$ is low, then $MCLK_X$ is still used for the internal master clock. Since only one of the master clocks is used at any given time, they need not be synchronous.

The master clock frequency must be 1.536, 1.544, or 2.048 MHz. The frequency that the codec-filter expects, depends on the state of the $BCLK_R/CLKSEL$ pin. The allowable options are shown in Table 1. When a level (rather than a clock) is provided for $BCLK_R/CLKSEL$, $BCLK_X$ is used as the bit clock for both transmit and receive.



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Table 1. Master Clock Frequency Determination

BCLK _R /CLKSEL	Master Clock Frequency Expected (MHz)
Clocked, 1, Open	2.048
0	1.536/1.544

FRAME SYNCs AND DIGITAL I/O

This codec-filter can accommodate both of the industry standard timing formats. The Long Frame Sync mode is used by the Motorola MC145500 family of codec-filters and the UDLT family of digital loop transceivers. The Short Frame Sync mode is compatible with the IDL (Interchip Digital Link) serial format used in the Motorola ISDN family and by other companies in their telecommunication devices. This codec-filter uses the length of the transmit frame sync (FS_X) to determine the timing format for both transmit and receive unless the part is operating in the receive half-channel mode.

In the Long Frame Sync mode, the frame sync pulses must be at least three-bit clock periods long. The D_X and \overline{TS}_X outputs are enabled by the logical ANDing of FS_X and BCLK_X; when both are high, the sign bit appears at the D_X output. The next seven rising edges of BCLK_X clock out the remaining seven bits of the PCM word. The D_X and \overline{TS}_X outputs return to a high-impedance state on the falling edge of the eighth bit clock or the falling edge of FS_X, whichever comes later. The receive PCM word is clocked into D_R on the eight falling BCLK_R edges following an FS_R rising edge.

For Short Frame Sync operation, the frame sync pulses must be one-bit clock period long. On the first BCLK_X rising edge after the falling edge of BCLK_X has latched FS_X high, the D_X and \overline{TS}_X outputs are enabled and the sign bit is presented on D_X. The next seven rising edges of BCLK_X clock out the remaining seven bits of the PCM word; on the eighth BCLK_X falling edge, the D_X and \overline{TS}_X outputs return to a high-impedance state. On the second falling BCLK_R edge following an FS_R rising edge, the receive sign bit is clocked into D_R. The next seven BCLK_R falling edges clock in the remaining seven bits of the receive PCM word.

Table 2 shows the coding format of the transmit and receive PCM words.

Table 2. PCM Data Format

Level	Sign Bits	Chord Bits	Step Bits
+ Full Scale	1	010	1010
+ Zero	1	101	0101
- Zero	0	101	0101
- Full Scale	0	010	1010

HALF-CHANNEL MODES

In addition to the normal full-duplex operating mode, this codec-filter can operate in both transmit and receive half-channel modes. Transmit half-channel mode is entered by holding FS_R low. The VF_RO output goes to analog ground but remains in a low-impedance state (to facilitate a hybrid interface); PCM data at D_R is ignored. Holding FS_X low while clocking FS_R, puts this device in the receive half-channel mode. In this state, the transmit input operational amplifier continues to operate, but the rest of the transmit circuitry is disabled; the D_X and \overline{TS}_X outputs remain in a high-impedance state. MCLK_R is used as the internal



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master clock if it is clocking. If $MCLK_R$ is not clocking, then $MCLK_X$ is used for the internal master clock, but in that case it should be synchronous with FS_R . If $BCLK_R$ is not clocking, $BCLK_X$ will be used for the receive data, just as in the full-channel operating mode. In receive half-channel mode only, the length of the FS_R pulse is used to determine whether Short Frame Sync or Long Frame Sync timing is used at D_R .

POWER-DOWN

Holding both FS_X and FS_R low causes the part to go into the power-down state. Power-down occurs approximately 2 ms after the last frame sync pulse is received. An alternative way to put this device in power-down is to hold the $MCLK_R$ /PDN pin high. When the chip is powered down, the D_X , $\overline{TS_X}$, and GS_X outputs are high impedance, the VF_{RO} , $VPO-$, and $VPO+$ operational amplifiers are biased with a trickle current so that their respective outputs remain stable at analog ground. To return the chip to the power-up state, $MCLK_R$ /PDN must be low or clocking and at least one of the frame sync pulses must be present. The D_X and $\overline{TS_X}$ outputs will remain in a high-impedance state until the second FS_X pulse after power-up.



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ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to GNDA)

Rating	Symbol	Value	Unit
DC Supply Voltage V_{CC} to V_{BB} V_{CC} to GNDA V_{BB} to GNDA		-0.5 to 13 -0.3 to 7.0 -7.0 to 0.3	V
Voltage on Any Analog Input or Output Pin		$V_{BB} - 0.3$ to $V_{CC} + 0.3$	V
Voltage on Any Digital Input or Output Pin		GNDA - 0.3 to $V_{CC} + 0.3$	V
Operating Temperature	T_A	-40 to 85	°C
Storage Temperature	T_{stg}	-85 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic level (e.g., V_{BB} , GNDA, or V_{CC}).

POWER SUPPLY ($T_A = -40^\circ$ to 85°C)

Characteristic	Min	Typ	Max	Unit
DC Supply Voltage V_{CC} V_{BB}	4.75 -4.75	5.0 -5.0	5.25 -5.25	V
Active Power Dissipation (No Load) $V_{PI} = V_{BB}$	— —	45 40	70 60	mW
Power-Down Dissipation (No Load) $V_{PI} = V_{BB}$	— —	2.0 1.0	5.0 3.0	mW

DIGITAL LEVELS ($V_{CC} = 5\text{ V} \pm 5\%$, $V_{BB} = -5\text{ V} \pm 5\%$, GNDA = 0 V, $T_A = -40^\circ$ to 85°C)

Characteristic	Symbol	Min	Max	Unit
Input Low Voltage	V_{IL}	—	0.6	V
Input High Voltage	V_{IH}	2.2	—	V
Output Low Voltage D_X or \overline{TS}_X , $I_{OL} = 3.2\text{ mA}$	V_{OL}	—	0.4	V
Output High Voltage D_X , $I_{OH} = -3.2\text{ mA}$ $I_{OH} = -1.6\text{ mA}$	V_{OH}	2.4 $V_{CC} - 0.5$	— —	V
Input Low Current $GNDA \leq V_{in} \leq V_{CC}$	I_{IL}	-10	10	μA
Input High Current $GNDA \leq V_{in} \leq V_{CC}$	I_{IH}	-10	10	μA
Output Current in High-Impedance State $GNDA \leq D_X \leq V_{CC}$	I_{OZ}	-10	10	μA



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ANALOG ELECTRICAL CHARACTERISTICS

($V_{CC} = 5\text{ V} \pm 5\%$, $V_{BB} = -5\text{ V} \pm 5\%$, V_{FXI-} Connected to GS_X , $T_A = -40^\circ$ to 85°C)

Characteristic		Min	Typ	Max	Unit
Input Current ($-2.5 \leq V_{in} \leq 2.5\text{ V}$)	V_{FXI+} , V_{FXI-}	—	± 0.05	± 0.2	μA
AC Input Impedance to GNDA (1 kHz)	V_{FXI+} , V_{FXI-}	10	20	—	$\text{M}\Omega$
Input Capacitance	V_{FXI+} , V_{FXI-}	—	—	10	pF
Input Offset Voltage of GS_X Op Amp	V_{FXI+} , V_{FXI-}	—	—	± 25	mV
Input Common Mode Voltage Range	V_{FXI+} , V_{FXI-}	-2.5	—	2.5	V
Input Common Mode Rejection Ratio	V_{FXI+} , V_{FXI-}	—	65	—	dB
Unity Gain Bandwidth of GS_X Op Amp ($R_{load} \geq 10\text{ k}\Omega$)		—	1000	—	kHz
DC Open Loop Gain of GS_X Op Amp ($R_{load} \geq 10\text{ k}\Omega$)		75	—	—	dB
Output Load Capacitance for GS_X Op Amp		0	—	100	pF
Output Voltage Range for GS_X	$R_{load} = 10\text{ k}\Omega$ to GNDA $R_{load} = 600\ \Omega$ to GNDA	-3.5 -2.8	— —	3.5 2.8	V
Output Current ($-2.8\text{ V} \leq V_{out} \leq 2.8\text{ V}$)	GS_X , V_{FO}	± 5.0	—	—	mA
Output Impedance V_{FO} (0 to 3.4 kHz)		—	1	—	Ω
Output Load Capacitance for V_{FO}		0	—	500	pF
V_{FO} Output DC Offset Voltage Referenced to GNDA		—	—	± 100	mV

Power Drivers

Input Current ($-1\text{ V} \leq V_{PI} \leq 1\text{ V}$)	V_{PI}	—	± 0.05	± 0.5	μA
Input Resistance ($-1\text{ V} \leq V_{PI} \leq 1\text{ V}$)	V_{PI}	5	10	—	$\text{M}\Omega$
Input Offset Voltage (V_{PI} Connected to V_{PO-})	V_{PI}	—	—	± 50	mV
Output Resistance, Inverted Unity Gain	V_{PO+} or V_{PO-}	—	1	—	Ω
Unity Gain Bandwidth, Open Loop	V_{PO-}	—	400	—	kHz
Load Capacitance ($\infty\ \Omega \geq R_{load} \geq 300\ \Omega$)	V_{PO+} or V_{PO-} to GNDA	0	—	1000	pF
Gain from V_{PO-} to V_{PO+} ($R_{load} = 300\ \Omega$, V_{PO+} to GNDA Level at $V_{PO-} = 1.77\text{ V}_{rms}$, +3 dBm_0)		—	-1	—	V/V
Maximum 0 dBm_0 Level for Better than $\pm 0.1\text{ dB}$ Linearity Over the Range -10 dBm_0 to +3 dBm_0 (For R_{load} between V_{PO+} and V_{PO-})	$R_{load} = 600\ \Omega$ $R_{load} = 1200\ \Omega$ $R_{load} = 10\text{ k}\Omega$	3.3 3.5 4.0	— — —	— — —	V_{rms}
Power Supply Rejection of V_{CC} or V_{BB} (V_{PO-} Connected to V_{PI})	0 to 4 kHz 4 to 50 kHz V_{PO+} or V_{PO-} to GNDA	55 35	— —	— —	dB
Differential Power Supply Rejection of V_{CC} or V_{BB} (V_{PO-} Connected to V_{PI})	V_{PO+} to V_{PO-} , 0 to 50 kHz	50	—	—	dB



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ANALOG TRANSMISSION PERFORMANCE

($V_{CC} = 5\text{ V} \pm 5\%$, $V_{BB} = -5\text{ V} \pm 5\%$, $G_{NDA} = 0\text{ V}$, $0\text{ dBm}_0 = 1.2276\text{ V}_{rms} = 4\text{ dBm} @ 600\ \Omega$, $F_{S_X} = F_{S_R} = 8\text{ kHz}$, $BCLK_X = MCLK_X = 2.048\text{ MHz}$ Synchronous Operation, $V_{F_X|}$ Connected to GS_X , $T_A = -40^\circ$ to 85°C Unless Otherwise Noted)

Characteristic	End-to-End		A/D		D/A		Unit	
	Min	Max	Min	Max	Min	Max		
Absolute Gain (0 dBm ₀ @ 1.02 kHz, $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_{BB} = -5\text{ V}$)	—	—	-0.25	-0.25	-0.25	0.25	dB	
Absolute Gain Variation with Temperature							dB	
	0 to 70°C	—	—	±0.03	—	±0.03		
	-40° to 85°C	—	—	±0.06	—	±0.06		
Absolute Gain Variation with Power Supply ($V_{CC} = 5\text{ V}$, ±5%, $V_{BB} = -5\text{ V}$, ±5%)	—	—	—	±0.02	—	±0.02	dB	
Gain vs Level Tone							dB	
(Relative to -10 dBm ₀ , 1.02 kHz)	3 to -40 dBm ₀	-0.4	0.4	-0.2	0.2	-0.2	0.2	
	-40 to -50 dBm ₀	-0.8	0.8	-0.4	0.4	-0.4	0.4	
	-50 to -55 dBm ₀	-1.6	1.6	-0.8	0.8	-0.8	0.8	
Gain vs Level Pseudo Noise CCITT G.712 (A-Law Relative to -10 dBm ₀)							dB	
	-10 to -40 dBm ₀	—	—	-0.25	0.25	-0.25	0.25	
	-40 to -50 dBm ₀	—	—	-0.30	0.30	-0.30	0.30	
	-50 to -55 dBm ₀	—	—	-0.45	0.45	-0.45	0.45	
Total Distortion With Pseudo Noise CCITT G.714							dB	
	-3 dBm ₀	27.5	—	28	—	28.5	—	
	-6 to -27 dBm ₀	35	—	35.5	—	36	—	
	-34 dBm ₀	33.1	—	33.5	—	34.2	—	
	-40 dBm ₀	28.2	—	28.5	—	30	—	
	-55 dBm ₀	13.2	—	13.5	—	15	—	
Idle Channel Noise (For End-End and A/D, Note 1) (A-Law, Psophometric Weighted)	—	-70	—	-70	—	-83	dBm _{0p}	
Frequency Response (Relative to 1.02 kHz @ 0 dBm ₀)							dB	
	15 Hz	—	-40	—	-40	-0.15	0	
	50 Hz	—	-30	—	-30	-0.15	0	
	60 Hz	—	-26	—	-26	-0.15	0	
	200 Hz	—	—	-1.0	-0.4	-0.15	0	
	300 to 3000 Hz	-0.3	0.3	-0.15	0.15	-0.15	0.15	
	3300 Hz	-0.70	0.3	-0.35	0.15	-0.35	0.15	
	3400 Hz	-1.6	0	-0.8	0	-0.8	0	
	4000 Hz	—	-28	—	-14	—	-14	
	4600 Hz	—	-60	—	-32	—	-30	
In-Band Spurious (1.02 kHz @ 0 dBm ₀ , Transmit and Receive)	300 to 3000 Hz	—	-48	—	-48	—	-48	dBm ₀
Out-of-Band Spurious at V_{FRO} (300 – 3400 Hz @ 0 dBm ₀ In)							dB	
	4600 to 7600 Hz	—	-30	—	—	—	-30	
	7600 to 8400 Hz	—	-40	—	—	—	-40	
	8400 to 100,000 Hz	—	-30	—	—	—	-30	
Idle Channel Noise Selective (8 kHz, Input = G_{NDA} , 30 Hz Bandwidth)	—	-70	—	—	—	-70	dBm ₀	
Absolute Delay (1600 Hz)	—	—	—	315	—	215	μs	
Group Delay Referenced to 1600 Hz							μs	
	500 to 600 Hz	—	—	—	220	-40	—	
	600 to 800 Hz	—	—	—	145	-40	—	
	800 to 1000 Hz	—	—	—	75	-40	—	
	1000 to 1600 Hz	—	—	—	40	-30	—	
	1600 to 2600 Hz	—	—	—	75	—	90	
	2600 to 2800 Hz	—	—	—	105	—	125	
	2800 to 3000 Hz	—	—	—	155	—	175	
Crosstalk of 1020 Hz @ 0 dBm ₀ from A/D or D/A (Note 2)	—	—	—	-75	—	-75	dB	



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ANALOG TRANSMISSION PERFORMANCE (continued)

($V_{CC} = 5\text{ V} \pm 5\%$, $V_{BB} = -5\text{ V} \pm 5\%$, $G_{NDA} = 0\text{ V}$, $0\text{ dBm} = 1.2276\text{ V}_{rms} = 4\text{ dBm}$ @ $600\ \Omega$, $FS_X = FS_R = 8\text{ kHz}$, $BCLK_X = MCLK_X = 2.048\text{ MHz}$ Synchronous Operation, VF_X - Connected to GS_X , $T_A = -40^\circ$ to 85°C Unless Otherwise Noted)

Characteristic	End-to-End		A/D		D/A		Unit
	Min	Max	Min	Max	Min	Max	
Intermodulation Distortion of Two Frequencies of Amplitudes -4 to -21 dBm0 from the Range 300 to 3400 Hz	—	-41	—	-41	—	-41	dB

NOTES:

1. Extrapolated from a 1020 Hz @ -50 dBm0 distortion measurement to correct for encoder enhancement.
2. Selectively measured while the A/D is stimulated with 2667 Hz @ -50 dBm0.

DIGITAL SWITCHING CHARACTERISTICS

($V_{CC} = 5\text{ V} \pm 5\%$, $V_{BB} = -5\text{ V} \pm 5\%$, $G_{NDA} = 0\text{ V}$, All Signals Referenced to G_{NDA} ; $T_A = -40^\circ$ to 85°C , $C_{load} = 150\text{ pF}$ Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Master Clock Frequency MCLK _X or MCLK _R	f _M	— — —	1.536 1.544 2.048	—	MHz
Minimum Pulse Width High or Low MCLK _X or MCLK _R	t _{w(M)}	100	—	—	ns
Minimum Pulse Width High or Low BCLK _X or BCLK _R	t _{w(B)}	50	—	—	ns
Minimum Pulse Width Low FS _X or FS _R	t _{w(FL)}	50	—	—	ns
Rise Time for all Digital Signals	t _r	—	—	50	ns
Fall Time for all Digital Signals	t _f	—	—	50	ns
Bit Clock Data Rate BCLK _X or BCLK _R	f _B	128	—	4096	kHz
Setup Time from BCLK _X Low to MCLK _R High	t _{su(BRM)}	50	—	—	ns
Setup Time from MCLK _X High to BCLK _X Low	t _{su(MFB)}	20	—	—	ns
Hold Time from BCLK _X (BCLK _R) Low to FS _X (FS _R) High	t _{h(BF)}	20	—	—	ns
Setup Time for FS _X (FS _R) High to BCLK _X (BCLK _R) Low for Long Frame	t _{su(FB)}	80	—	—	ns
Delay Time from BCLK _X High to D _X Data Valid	t _{d(BD)}	20	60	140	ns
Delay Time from BCLK _X High to \overline{TS}_X Low	t _{d(BTS)}	20	50	140	ns
Delay Time from the Eighth BCLK _X Low of FS _X Low to D _X Output Disabled	t _{d(ZC)}	50	70	140	ns
Delay Time to Valid Data from FS _X or BCLK _X , Whichever is Later	t _{d(ZF)}	20	60	140	ns
Setup Time from D _R Valid to BCLK _X Low	t _{su(DB)}	0	—	—	ns
Hold Time from BCLK _R Low to D _R Invalid	t _{h(BD)}	50	—	—	ns
Setup Time from FS _X (FS _R) High to BCLK _X (BCLK _R) Low in Short Frame	t _{su(F)}	50	—	—	ns
Hold Time from BCLK _X (BCLK _R) Low to FS _X (FS _R) Low in Short Frame	t _{h(F)}	50	—	—	ns
Hold Time from Second Period of BCLK _X (BCLK _R) Low to FS _X (FS _R) Low in Long Frame	t _{h(BFI)}	50	—	—	ns

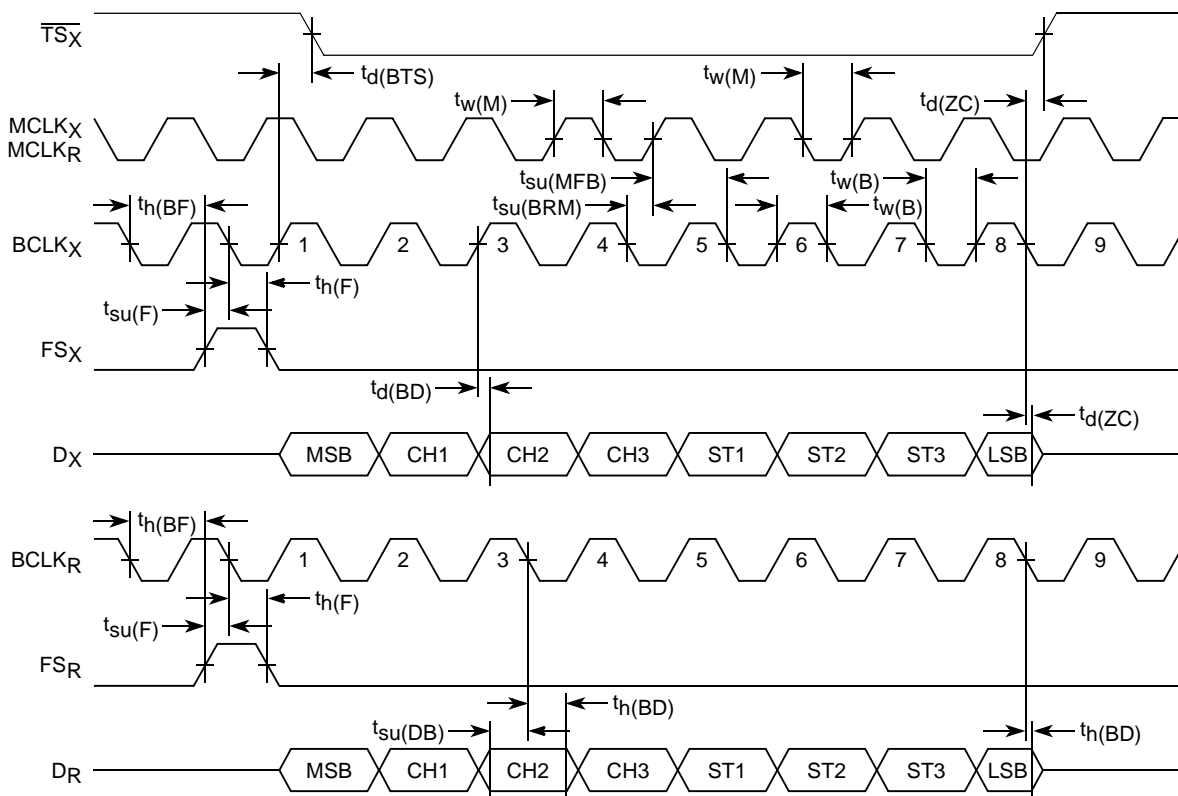


Figure 1. Short Frame Sync Timing

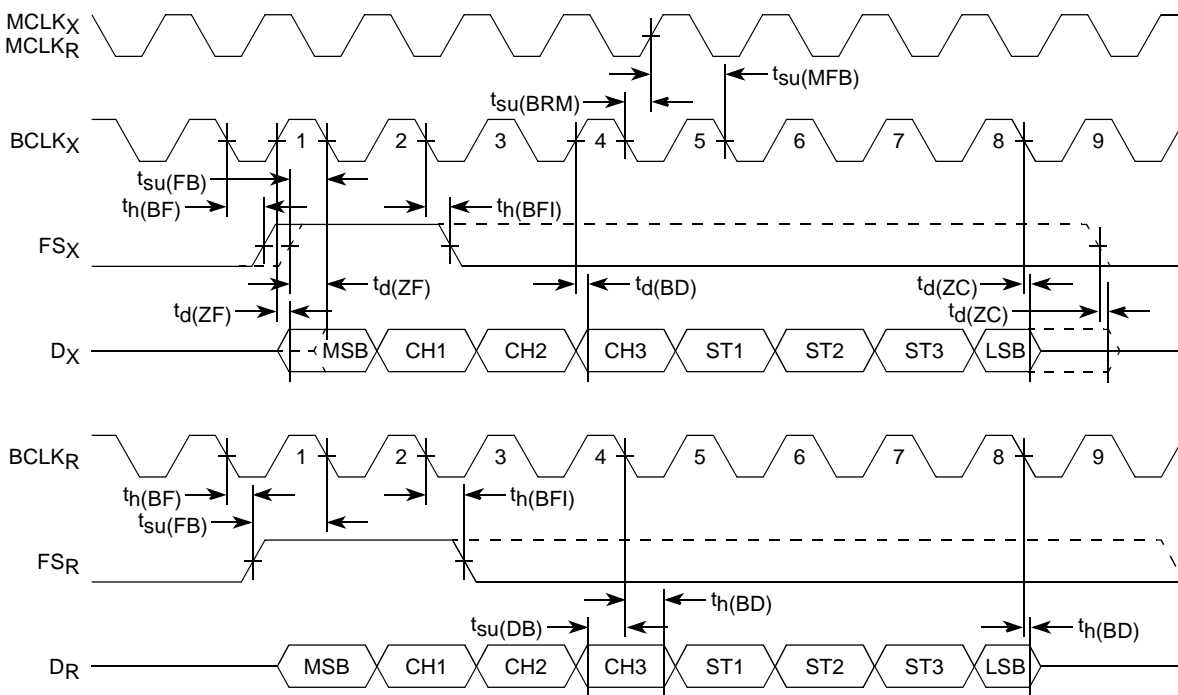


Figure 2. Long Frame Sync Timing

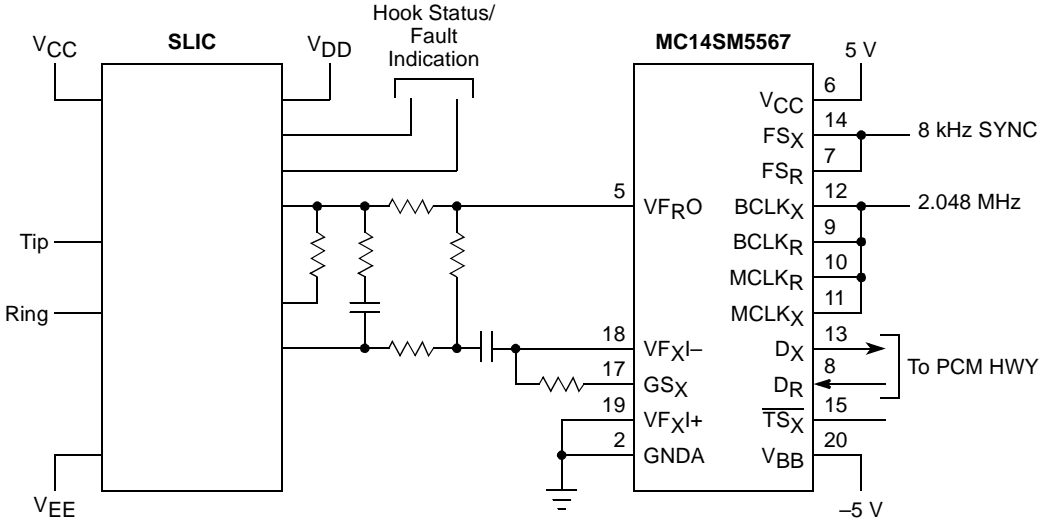


Figure 3. Single Party Channel Unit

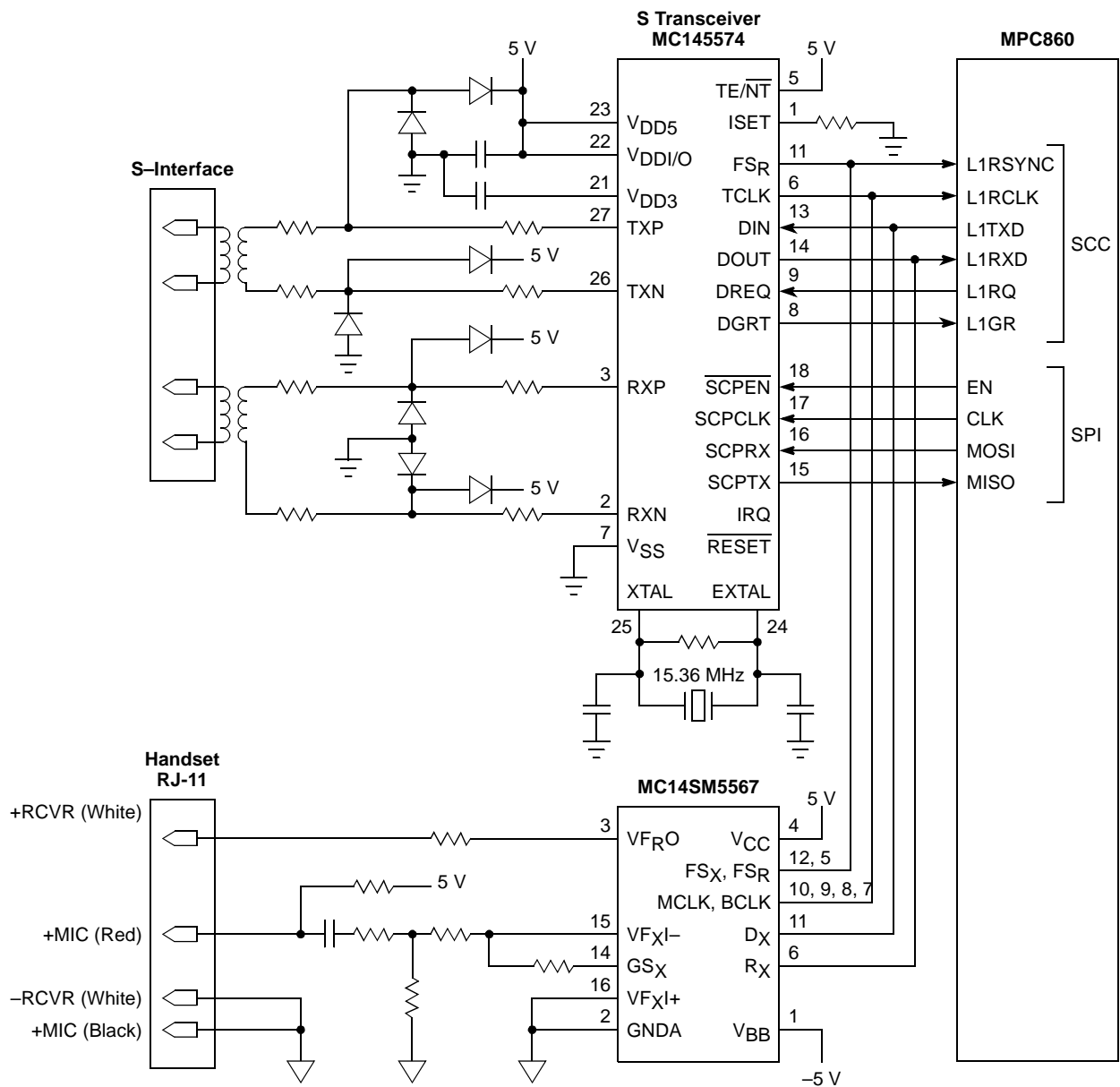


Figure 4. ISND Voice/Data Terminal



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Table 3. A-Law Encode-Decode Characteristics

Chord No.	No. of Steps	Step Size	Normalized Encode Decision Levels	Digital Code								Normalized Decode Levels
				1	2	3	4	5	6	7	8	
				Sign	Chord	Chord	Chord	Step	Step	Step	Step	
7	16	128	4096	1	0	1	0	1	0	1	0	4032
			3968	⋮								⋮
			2176	1	0	1	0	0	1	0	1	2112
6	16	64	2048	⋮								⋮
			1088	1	0	1	1	0	1	0	1	1056
			1024	⋮								⋮
5	16	32	544	1	0	0	0	0	1	0	1	528
			512	⋮								⋮
			272	1	0	0	1	0	1	0	1	264
3	16	8	256	⋮								⋮
			136	1	1	1	0	0	1	0	1	132
			128	⋮								⋮
2	16	4	68	1	1	1	1	0	1	0	1	66
			64	⋮								⋮
			2	1	1	0	1	0	1	0	1	1
1	32	2	0	⋮								⋮
			0	1	1	0	1	0	1	0	1	1

NOTES:

1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes alternate bit inversion, as specified by CCITT.



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