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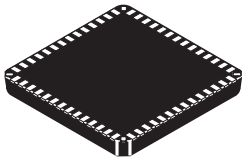
Micromotor Driver with Dual 3-Phase and Dual H-Bridge Outputs

17559

MICROMOTOR DRIVER WITH DUAL 3-PHASE AND DUAL H-BRIDGE OUTPUTS



EP SUFFIX (Pb-FREE)
98ARH99036A
56-LEAD QFN

The 17559 is a monolithic quad H-Bridge power IC ideal for portable electronic applications containing multiple brushless and brush DC-motors.

The 17559 is designed to drive motors with supplies operating from 0.9 V to 3.5 V, with independent control of each output bridge via parallel 1.8 V to 3.6 V logic-compatible I/O. Each output bridge has its own gate-drive and logic circuitry with built-in shoot-through current protection.

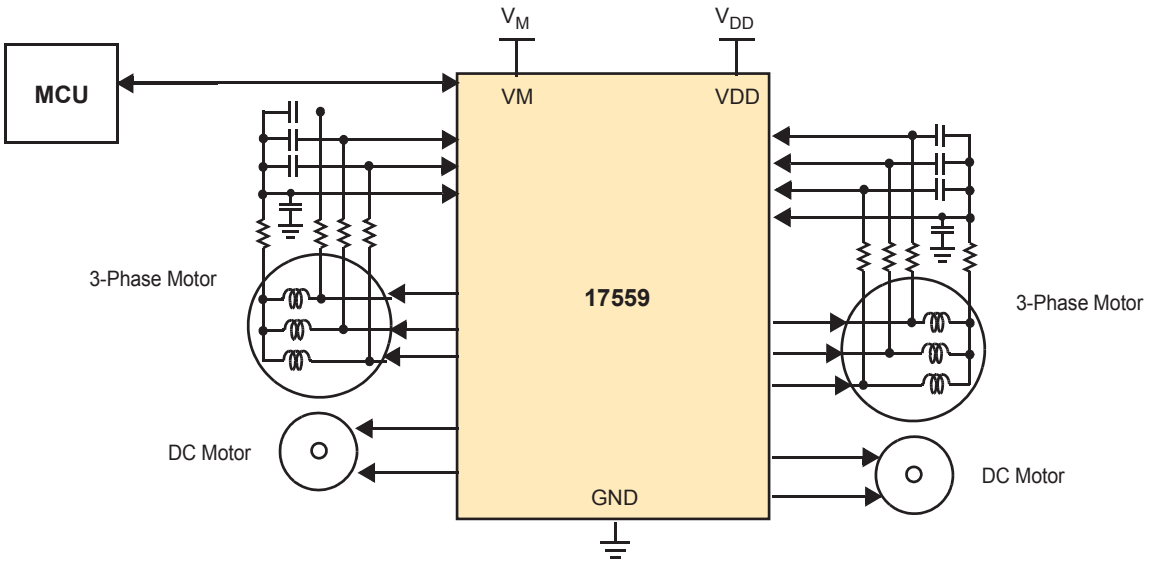
The 17559 has a low total $R_{DS(ON)}$ of 1.7 Ω max @ 25°C for each of the two 3-phase output bridges, and a low total $R_{DS(ON)}$ of 1.3 Ω max @ 25°C for each of the two H-Bridge outputs.

The 17559 can efficiently drive many types of micromotors owing to its low output resistance and high output slew rates.

Features

- Two Separate Three-Phase Motor Drivers
- Two Separate H-Bridge Motor Drivers
- Low-Voltage Detection and Shutdown Circuitry
- Pb-Free Packaging Designated by Suffix Code EP

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MPC17559EP/R2	-20°C to 65°C	56 QFN



Note Diagram represents one half of the dual application.

Figure 1. 17559 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

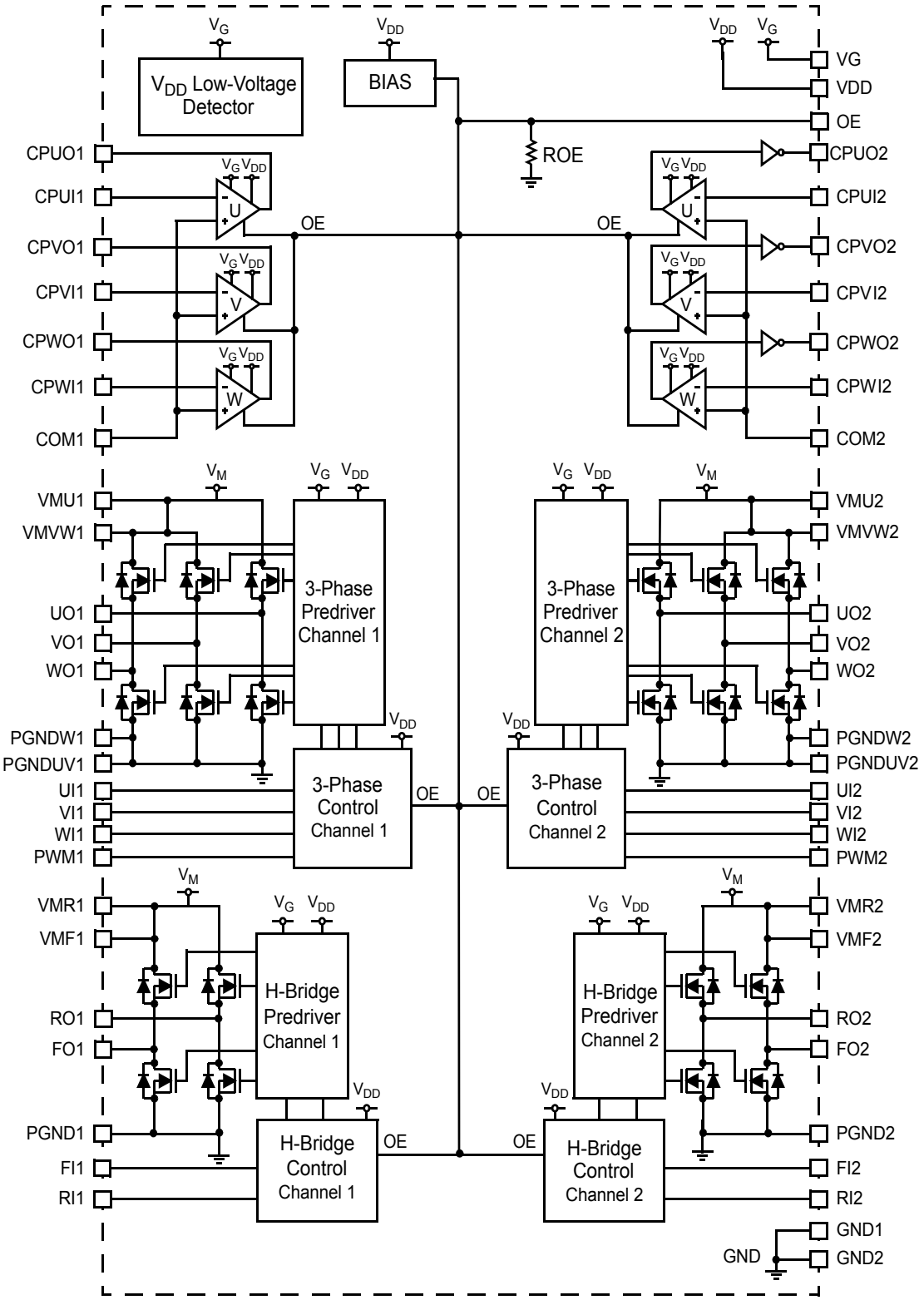


Figure 2. 17559 Simplified Internal Block Diagram

TERMINAL CONNECTIONS

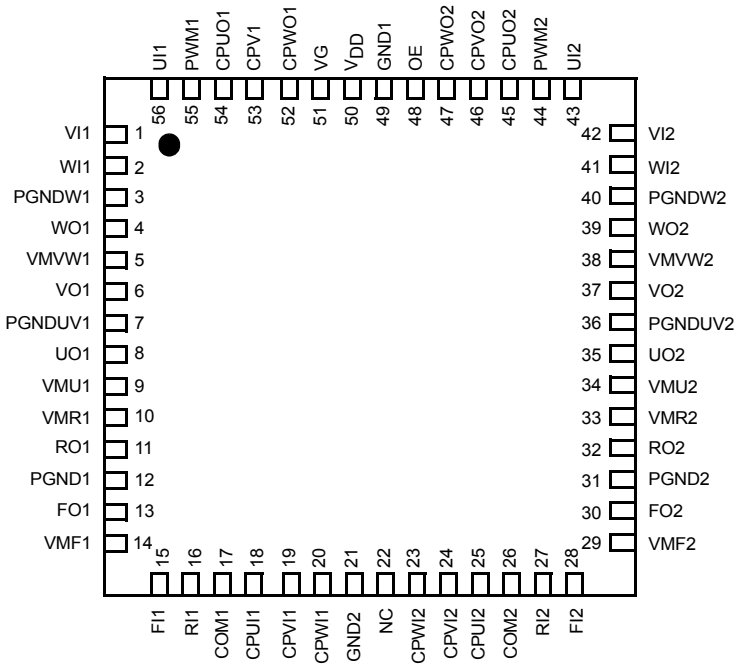


Figure 3. 17559 Terminal Connections

Table 1. 17559 Terminal Definitions

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 10.

Terminal Number	Terminal Name	Terminal Function	Formal Name	Definition
1	VI1	Input	Three-Phase Input VI1	Three-phase driver channel 1 V input terminal.
2	WI1	Input	Three-Phase Input WI1	Three-phase driver channel 1 W input terminal.
3	PGNDW1	Ground	Power Ground w1	Three-phase driver channel 1 W phase power ground terminal.
4	WO1	Output	Three-Phase Output WO1	Three-phase driver channel 1 W output terminal.
5	VMVW1	Power	Motor Driver Power Supply vw1	Three-phase driver channel 1 VW phase power supply terminal.
6	VO1	Output	Three-Phase Output VO1	Three-phase driver channel 1 phase output terminal.
7	PGNDUV1	Ground	Power Ground uv1	Three-phase driver channel 1 UV phase power ground terminal.
8	UO1	Output	Three-Phase Output UO1	Three-phase driver channel 1 U phase output terminal.
9	VMU1	Power	Motor Driver Power Supply u1	Three-phase driver channel 1 U phase power supply terminal.
10	VMR1	Power	Motor Driver Power Supply R2	H-Bridge driver channel 1 power supply terminal R.
11	RO1	Output	H-Bridge Output RO1	H-Bridge driver channel 1 reverse output terminal.
12	PGND1	Ground	Power Ground 1	H-Bridge driver channel 1 power ground terminal.
13	FO1	Output	H-Bridge Output FO1	H-Bridge driver channel 1 forward output terminal.
14	VMF1	Power	Motor Driver Power Supply F1	H-Bridge driver channel 1 power supply terminal F.
15	FI1	Input	Logic Input Control FI1	H-Bridge driver channel 1 forward input terminal.
16	RI1	Input	Logic Input Control RI1	H-Bridge driver channel 1 reverse input terminal.

Table 1. 17559 Terminal Definitions (continued)

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 10.

Terminal Number	Terminal Name	Terminal Function	Formal Name	Definition
17	COM1	Input	Forward Input UVW1	Comparator channel 1 UVW forward input terminal.
18	CPUI1	Input	Reverse Input UI1	Comparator channel 1 U reverse input terminal.
19	CPVI1	Input	Reverse Input VI1	Comparator channel 1 V reverse input terminal.
20	CPWI1	Input	Reverse Input WI1	Comparator channel 1 W reverse input terminal.
21	GND2	Ground	Ground 2	Control circuit ground terminal 2.
22	NC		No Connect	This terminal is not used.
23	CPWI2	Input	Reverse Input WI2	Comparator channel 2 W reverse input terminal.
24	CPVI2	Input	Reverse Input VI2	Comparator channel 2 V reverse input terminal.
25	CPUI2	Input	Reverse Input UI2	Comparator channel 2 U reverse input terminal.
26	COM2	Input	Forward Input UVW2	Comparator channel 2 UVW forward input terminal.
27	RI2	Input	Logic Input Control RI2	H-Bridge driver channel 2 reverse input terminal.
28	FI2	Input	Logic Input Control FI2	H-Bridge driver channel 2 forward input terminal.
29	VMF2	Power	Motor Driver Power Supply F2	H-Bridge driver channel 2 power supply terminal F.
30	FO2	Output	H-Bridge Output FO2	H-Bridge driver channel 2 forward output terminal.
31	PGND2	Ground	Power Ground 2	H-Bridge driver channel 2 power ground terminal.
32	RO2	Output	H-Bridge Output RO2	H-Bridge driver channel 2 reverse output terminal.
33	VMR2	Power	Motor Driver Power Supply R2	H-Bridge driver channel 2 power supply terminal R.
34	VMu2	Power	Motor Driver Power Suppy u2	Three-phase driver channel 2 U phase power supply terminal.
35	UO2	Output	Three-Phase Output UO2	Three-phase driver channel 2 U phase output terminal.
36	PGNDu2	Ground	Power Ground u2	Three-phase driver channel 2 UV phase power ground terminal.
37	VO2	Output	Three-Phase Output VO2	Three-phase driver channel 2 V phase output terminal.
38	VMvw2	Power	Motor Driver Power Supply vw2	Three-phase driver channel 2 VW phase power supply terminal.
39	WO2	Output	Three-Phase Output WO2	Three-phase driver channel 2 W phase output terminal.
40	PGNDw2	Ground	Power Ground w2	Three-phase driver channel 2 W phase power ground terminal.
41	WI2	Input	Three-Phase Input WI2	Three-phase driver channel 2 W input terminal.
42	VI2	Input	Three-Phase Input VI2	Three-phase driver channel 2 V input terminal.
43	UI2	Input	Three-Phase Input UI2	Three-phase driver channel 2 U input terminal.
44	PWM2	Input	PWM Input 2	Three-phase driver channel 2 PWI input terminal.
45	CPUO2	Output	Comparator Output UO2	Comparator channel 2 U output terminal.
46	CPVO2	Output	Comparator Output VO2	Comparator channel 2 V output terminal.
47	CPWO2	Output	Comparator Output WO2	Comparator channel 2 W output terminal.
48	OE	Output	Output Enable	Output enable input terminal.
49	GND1	Ground	Ground 1	Control circuit ground terminal.
50	V_{DD}	Power	Logic Supply	Control circuit power supply terminal.
51	VG		Gate Boost Voltage	Gate drive boost voltage.
52	CPWO1	Output	Comparator Output WO1	Comparator channel 1 W output terminal.
53	CPVO1	Output	Comparator Output VO1	Comparator channel 1 V output terminal.
54	CPUO1	Output	Comparator Output UO1	Comparator channel 1 U output terminal.

Table 1. 17559 Terminal Definitions (continued)

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 10.

Terminal Number	Terminal Name	Terminal Function	Formal Name	Definition
55	PWM1	Input	PWM Input 1	Three-phase driver channel 1 PWM input terminal.
56	UI1	Input	Three-Phase Input UI1	Three-phase driver channel 1 U input terminal.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Motor Supply Voltage (1)	V_M	-0.5 to 5.0	V
Logic Supply Voltage	V_{DD}	-0.5 to 4.0	V
Gate Drive Boost Voltage	V_G	V_{DD}-0.5 to 11	V
Logic Signal Input Voltage (2) Analog Signal Input Voltage (3)	V_{IL} V_{IA}	-0.5 to V_{DD}+0.5 -0.5 to V_M+0.5	V
Driver Output Current (4) DC Peak (5)	 I_O I_{OPK}	 300 600	mA
ESD Voltage Human Body Model (6) Machine Model (7)	 V_{ESD1} V_{ESD2}	 ±1000 ±200	V
Control Circuit Output Current (8)	I_{OV}	10	mA
Power Dissipation (T_A = 25°C)	P_D	1650	mW
THERMAL RATINGS			
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	-20 to 65	°C
Thermal Resistance	$R\theta_{JA}$	TBD	°C/W
Storage Temperature	T_{STG}	-65 to 150	°C
Terminal Soldering Temperature (9)	T_{SOLDER}	240	°C

Notes

1. VMu1, VMu2, VMvw1, VMvw2, VMF1, VMR1, VMF1, and VMR2 terminals.
2. OE, UI1, VI1, WI1, PWM1, UI2, VI2, WI2, PWM2, FI1, RI1, FI2, and RI2 terminals.
3. COM1, CPUI1, CPVI1, CPWI1, COM2, CPUI2, CPVI2, and CPWI2 terminals.
4. FO1, RO1, FO2, RO2, UO1, VO1, WO1, UO2, VO2, and WO2 terminals.
5. T_A = 25°C, 0.2 sec cycle, 10 ms max.
6. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
7. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
8. CPUO1, CPVO1, CPWO1, CPUO2, CPVO2, and CPWO2 terminals.
9. Soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions V_M = 1.2 V, V_{DD} = 2.4 V, $^{V}C_{RES}$ = 6.8 V, 7.0 V ≤ V_G ≤ 18 V, -20°C ≤ T_A ≤ 65°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER					
Motor Supply Voltage (10)	V_M	0.9	1.2	3.5	V
Logic Supply Voltage	V_{DD}	1.8	2.4	3.5	V
Gate Drive Boost Voltage	V_G	V_M+5.0	–	9.0	V
Standby Power Supply Current (11)					µA
Motor Supply Standby Current	I_{VMSTBY}	–	–	1.0	
Logic Supply Standby Current	$I_{VDDSTBY}$	–	–	1.0	
Gate Drive Boost Voltage	I_{VGSTBY}	–	–	1.0	
No Signal Input Supply Current (12)					µA
Logic Supply Current	I_{VDDN}	–	30	60	
Gate Drive Boost Voltage	I_{VGN}	–	75	120	
Active Supply Current (13)					
Logic Supply Current	I_{VDD}	–	50	100	µA
Gate Drive Boost Voltage	I_{VG}	–	0.54	0.65	mA
Driver Output ON Resistance (14)					Ω
Three-Phase Drivers	$R_{DS(ON)3p}$	–	1.30	1.70	
H-Bridge Drivers	$R_{DS(ON)hb}$	–	0.87	1.30	
Low-Voltage Detector Voltage					V
Circuit Disable Voltage	V_{LOon}	0.75	1.07	1.60	
Circuit Enable Voltage	V_{LOoff}	0.75	1.13	1.60	

Notes

10. VMU1, VMU2, VMVW1, VMVW2, VMF1, VMR1, VMF2, and VMR2 terminals.
11. UI1, VI1, WI1, PWM1, UI2, VI2, WI2, PWM2, FI1, RI1, FI2, and RI2 are “L” (low) or “H
12. UI1, VI1, WI1, PWM1, UI2, VI2, WI2, PWM2, FI1, RI1, FI2, and RI2 are “L” (low) or “H
13. OE = ”H” (high), f_{PWM} = 176.4 kHz, f_{UVM} = 100 Hz, f_{IN} = 88.2 kHz.
14. Summary of top and bottom when I_O = 100 mA.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_M = 1.2 V, V_{DD} = 2.4 V, $^{V}C_{RES}$ = 6.8 V, 7.0 V ≤ V_G ≤ 18 V, -20°C ≤ T_A ≤ 65°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL LOGIC					
Logic Input					
High-Level Input Voltage (15)	V_{IH}	V_{DD} x 0.7	–	–	V
Low-Level Input Voltage (15)	V_{IL}	–	–	V_{DD} x 0.3	V
High-Level Input Current (16)	I_{IH}	–	–	1.0	µA
Low-Level Input Current (15)	I_{IL}	-1.0	–	–	µA
Analog Signal Input Voltage (17)	V_{IA}	0	–	V_M	V
OE Terminal Pull-Down Resistance	R_{OE}	330	660	1000	kΩ
Comparator Input (18)					
Offset Voltage	V_{OS}	-5.0	–	5.0	mV
Input Current	I_{CP}	-1.0	–	1.0	µA
Comparator Output (19)					V
High-Level Output Voltage (20)	V_{OH}	V_{DD} x 0.85	–	–	
Low-Level Output Voltage (21)	V_{OL}	–	–	V_{DD} x 0.15	

Notes

15. OE, UI1, VI1, WI1, PWM1, UI2, VI2, WI2, PWM2, FI1, RI1, FI2, and RI2 terminals.
16. UI1, VI1, WI1, PWM1, UI2, VI2, WI2, PWM2, FI1, RI1, FI2, and RI2 terminals.
17. COM1, CPUI1, CPVI1, CPWI1, COM2, CPUI2, CPVI2, and CPWI2 terminals.
18. CPUI1, CPVI1, CPWI1, CPUI2, CPVI2, and CPWI2 terminals.
19. CPUO1, CPVO1, CPWO1, CPUO2, CPVO2, and CPWO2 terminals.
20. I_{SOURCE} = 500 µA.
21. I_{SINK} = 500 µA.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions V_M = 1.2 V, V_{DD} = 2.4 V, $^{V}C_{RES}$ = 6.8 V, 7.0 V ≤ V_G ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT					
Input Signal Frequency					
PWM1, PWM2	f_{PWM}	–	176.4	–	kHz
UI1, VI1, WI1, UI2, VI2, WI2	f_{UVW}	–	100	–	Hz
FI1, RI1, FI2, RI2	f_{IN}	–	88.2	–	kHz

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 17559 is a monolithic dual 3-phase plus dual H-Bridge multiple motor driver IC ideal for portable electronic applications containing two brushless DC motors plus two DC brush motors (or plus one bipolar step motor). The control logic translates the input signals to the gate-driver circuitry while providing cross-conduction suppression.

The drivers are designed to be PWM'ed at high frequencies for efficient and noise-free motor control. The 17559 is designed for portable audio and video applications such as camcorders, but it may be used in any application requiring highly efficient control of micromotors.Authors' Note:

FUNCTIONAL DESCRIPTION

THREE-PHASE DRIVER CHANNEL 1 INPUT (UI1, VI1, AND WI1)

The three-phase driver channel 1 input terminals (UI1, VI1, and VI1) set the driver states (UO1, VO1, and WO1) in accordance with the logic set force defined in Table 7, page 11. Typically these inputs are supplied from an MCU or a digital signal processor (DSP) to provide the phasing of the currents applied to a brushless DC motor.

THREE-PHASE DRIVER CHANNEL 1 OUTPUT (UO1, VO1, AND WO1)

The three-phase driver channel 1 output terminals (UO1, VO1, and WO1) drive a three-phase motor, as well as supply the peak currents with applied ON resistance ($R_{DS(ON)hb}$).

THREE-PHASE DRIVER CHANNEL 1 PHASE POWER GROUND (PGNDW1 AND PGNDUV1)

The three-phase driver channel 1 phase power ground terminals (PGNDw1 and PGNDuv1) are ground terminals for three-phase driver channel 1. PGNDw1 is a ground for W phase driver, and PGNDuv1 is a ground for U and V phase driver. PGNDw1 and PGNDuv1 are physically connected in the IC in order to reduce internal resistance.

THREE-PHASE DRIVER CHANNEL 1 PHASE POWER SUPPLY (VMVW1 AND VMU1)

The three-phase driver channel 1 phase power supply terminals (VMvw1 and VMu1) are power supply terminals for three-phase driver channel 1. VMvw1 is a power supply for V and W phase driver, and VMu1 is a power supply for U phase driver. VMvw1 and VMu1 are phyically connected in the IC in order to reduce internal resistance.

THREE-PHASE DRIVER CHANNEL 2 INPUT (UI2, VI2, AND WI2)

The three-phase driver channel 2 input terminals (UI2, VI2, and WI2) set the driver states (UO2, VO2, and WO2) in accordance with the logic set force in Table 7. Typically these inputs are supplied from an MCU or DSP to provide the phasing of the current applied to a brushless DC motor.

THREE-PHASE DRIVER CHANNEL 2 OUTPUT (UO2, VO2, AND WO2)

The three-phase driver channel 2 output terminals (UO2, VO2, and WO2) drive a three-phase motor, as well as supply the peak currents with applied ON resistance ($R_{DS(ON)hb}$).

THREE-PHASE DRIVER CHANNEL 2 PHASE POWER GROUND (PGNDW2 AND PGNDUV2)

The three-phase driver channel 2 phase power ground terminals (PGNDw2 and PGNDuv2) are ground terminals for three-phase driver channel 2. PGNDw2 is a ground for W phase driver, and PGNDuv2 is a ground for U and V phase driver. PGNDw2 and PGNDuv2 are physically connected in the IC in order to reduce internal resistance.

THREE-PHASE DRIVER CHANNEL 2 PHASE POWER SUPPLY (VMVW2 AND VMU2)

The three-phase driver channel 2 phase power supply terminals (VMvw2 and VMu2) are power supply terminals for three-hase driver channel 2. VMvw2 is a power supply for V and W phase driver, and VMu2 is a power supply for U phase driver. VMvw2 and VMu2 are phyically connected in the IC in order to reduce internal resistance.

LOGIC INPUT (OE, FI1, RI1, FI2, AND RI2)

These logic input terminals control each H-Bridge output. OE = 1 is an output enable for each H-Bridge control and for each three-phase comparator (refer to Table 6, page 11).

H-BRIDGE OUTPUTS (RO1, FO1, RO2, AND FO2)

These terminals provide connection to the outputs of each internal H-Bridge (see Figure 1, 17559 Simplified Application Diagram, page 1).

POWER SUPPLY (VMR1, VMF1, VMR2, AND VMF2)

These VM terminals carry the main power supply voltage and current into the H-Bridge power section of the 17559. The supply voltage then becomes controlled and/or modulated by the IC as it delivers the power to the loads attached between the output terminals. All VM terminals are connected internally for VMR1 and VMF1, and VMR2 and

VMF2, but they must be connected together on the printed circuit board.

SUPPLY VOLTAGE (VDD)

The V_{DD} terminal carries the logic supply voltage and current into the logic sections of the 17559. The V_{DD} has an undervoltage threshold. If the supply voltage drops between the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input terminals.

GROUND (GND1 AND GND2)

The GND1 and GND2 are main ground terminals for internal logic. They are connected internally.

POWER INPUT (PWM)

The pulse width modulation input provides a single input terminal to accomplish PWM modulation of the output pairs in accordance with the states of input conditions described in Table 7.

LOGIC COMMAND REGISTERS

Table 5. Operating Function

OE	Bias Circuit	H Bridge Driver	3 Phase Driver	Comparator
L	Stop	Output “L”	Output “L”	1*
H	Operation	Operation	Operation	Operation

L = Low.
H = High.
*1: CPUO1, CPVO1, CPWO1 Output = L, CPUO2, CPVO2, CPWO2 Output = H.

Table 6. H-Bridge Driver

Input			Output	
OE	FIn	RIn	FOn	ROn
L	X	X	L	L
H	L	L	L	L
H	L	H	L	H
H	H	L	H	L
H	H	H	L	L

L = Low.
H = High.
X = Don’t care.
Z = High impedance.

Table 7. Three-Phase Driver

Input				Output		
OE	UIn	VIn	WIn	UOn	VOn	WOn
L	X	X	X	L	L	L
H	L	L	L	L	L	L
H	L	L	H	Z	L	PWM
H	L	H	L	L	PWM	Z

Table 7. Three-Phase Driver

H	L	H	H	L	Z	PWM
H	H	L	L	PWM	Z	L
H	H	L	H	PWM	L	Z
H	H	H	L	Z	PWM	L
H	H	H	H	L	L	L

L = Low.
H = High.
X = Don't care.
Z = High impedance.
PWM = Duty pulse same as PWM terminal input.

TYPICAL APPLICATIONS

INTRODUCTION

Figure 4 shows a typical application for the 17559.

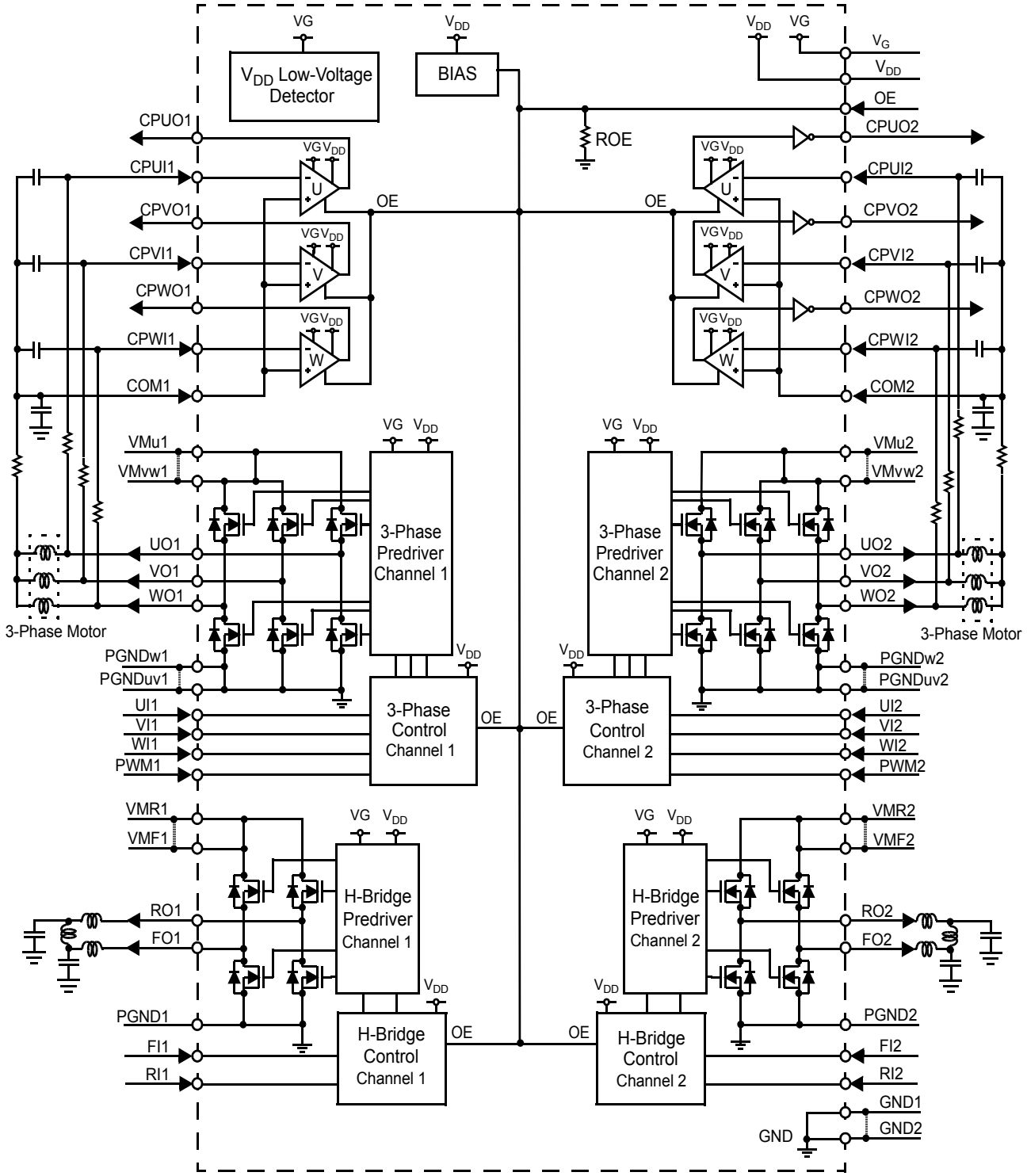


Figure 4. 17559 Typical Application Diagram

CEMF SNUBBING TECHNIQUES

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients by placing a capacitor or zener at the motor supply voltage terminal (VM).

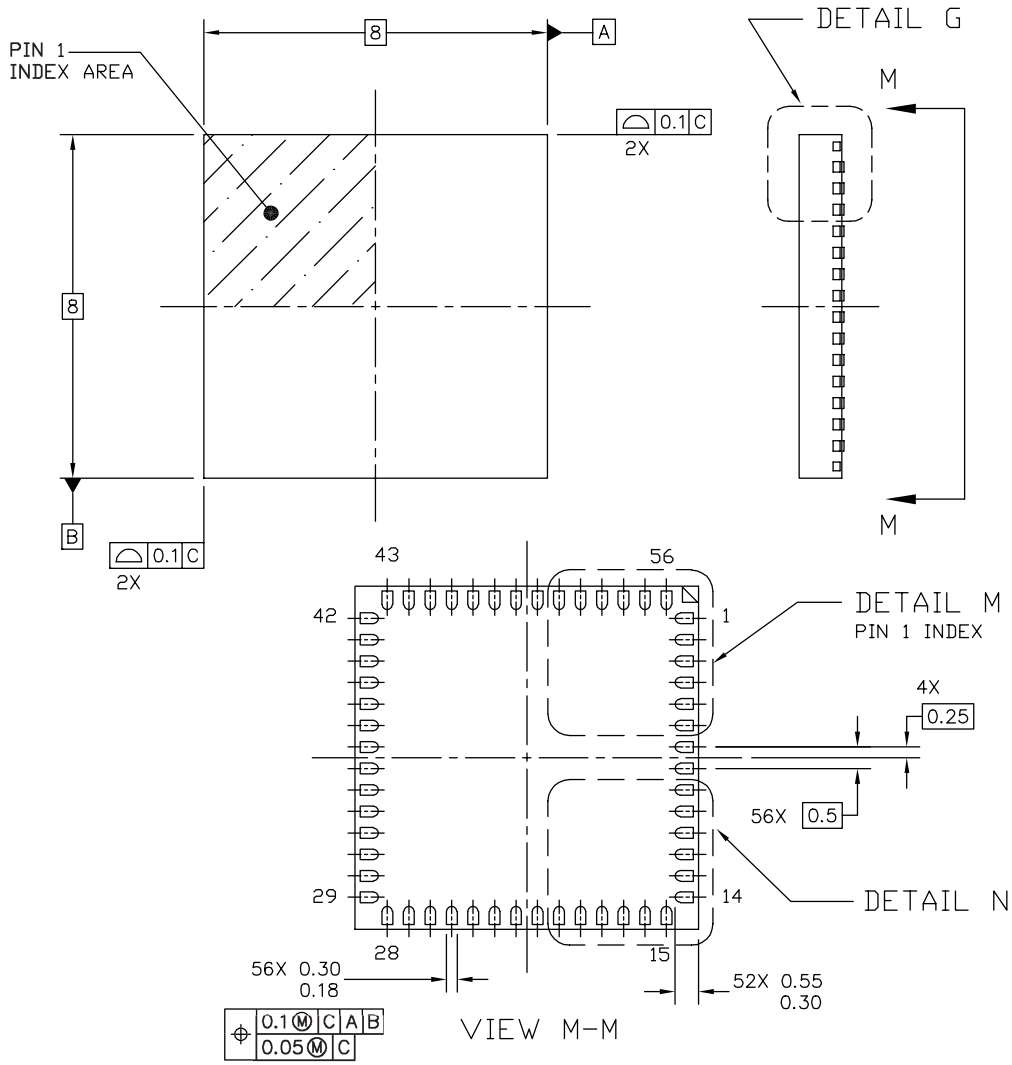
PCB LAYOUT

When designing the printed circuit board (PCB), connect sufficient capacitance between power supply and ground terminals to ensure proper filtering against transients. For all high-current paths, use wide copper traces and the shortest possible distances.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a “keyword” search using the 98ARH99036A listed.



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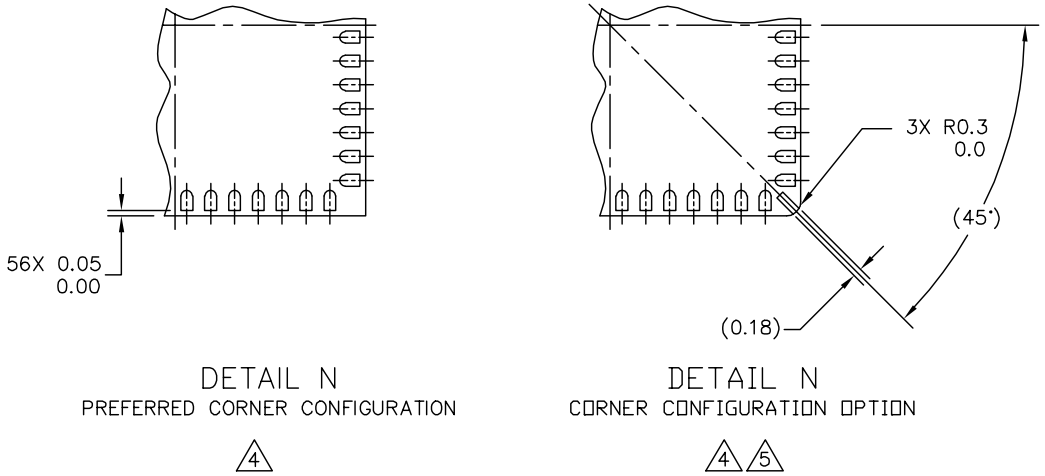
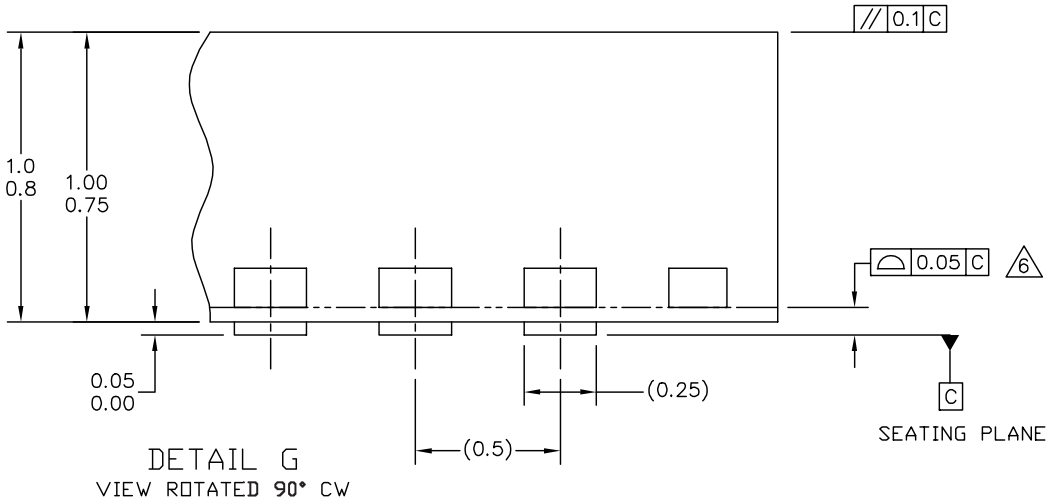
	CASE NUMBER: 1312-02	04 JUL 2005
	STANDARD: NON-JEDEC	

EP SUFFIX
56-LEAD QFN
PLASTIC PACKAGE
98ARH99036A
ISSUE B

17559





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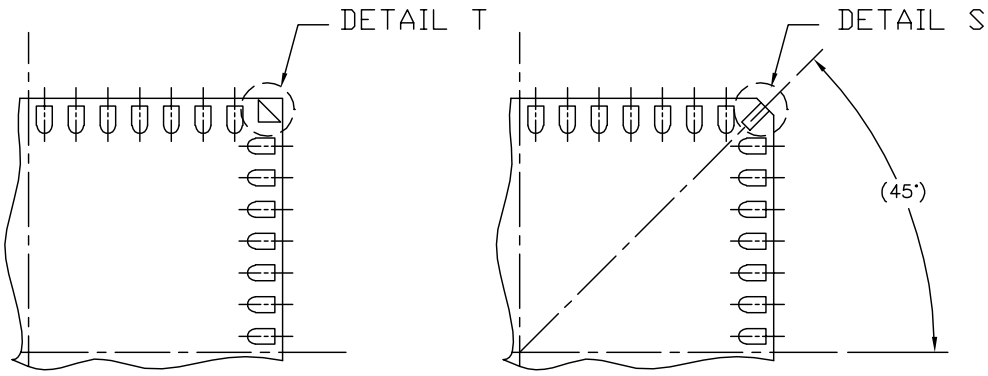
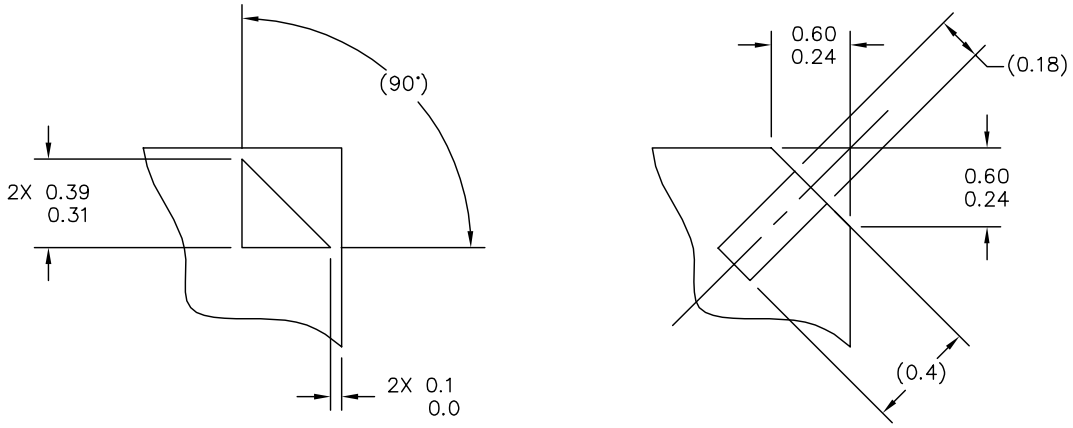
EP SUFFIX
56-LEAD QFN
PLASTIC PACKAGE
98ARH99036A
ISSUE B

17559



DETAIL M
PREFERRED PIN 1 BACKSIDE IDENTIFIER

DETAIL M
PIN 1 BACKSIDE IDENTIFIER OPTION



DETAIL T
PREFERRED PIN 1 BACKSIDE IDENTIFIER

DETAIL S
PIN 1 BACKSIDE IDENTIFIER OPTION

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	CASE NUMBER: 1312-02	04 JUL 2005
	STANDARD: NON-JEDEC	

EP SUFFIX
56-LEAD QFN
PLASTIC PACKAGE
98ARH99036A
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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
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