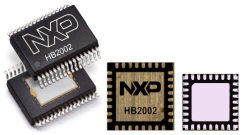


MC33HB2002

10 A H-bridge, SPI programmable brushed DC motor driver

Rev. 3.0 — 18 October 2019 Data sheet: advance information

1 General description

The MC33HB2002 is a SMARTMOS monolithic H-Bridge Power IC, enhanced with SPI configurability and diagnostic capabilities. It is designed primarily for DC motor or servo motor control applications within the specified current and voltage limits.

The MC33HB2002 is similar to the MC33HB2000 device with higher overtemperature setting and the use of current foldback for current limiting to extend fault operation range.

The MC33HB2002 is able to control inductive loads with peak currents greater than 10 A. The nominal continuous average load current is 3.0 A. A current mirror output provides an analog feedback signal proportional to the load current.

This part is designed to specifically address the ISO 26262 safety requirements. It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 1 qualified.

2 Simplified application diagram

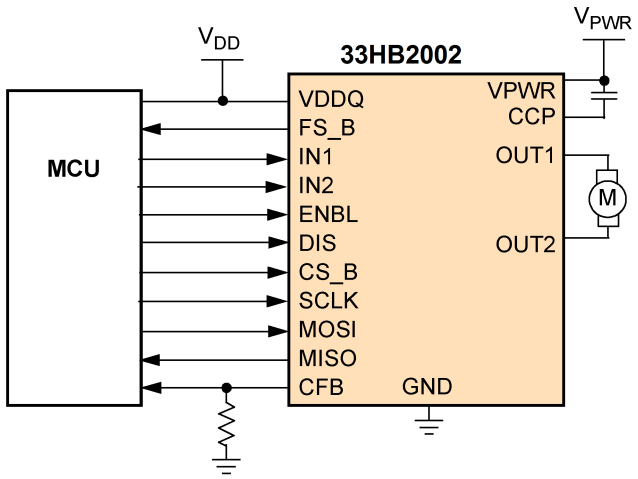


Figure 1. Simplified application diagram

3 Features and benefits

- Advanced diagnostic reporting via a serial peripheral interface (SPI): charge pump undervoltage, overvoltage, and undervoltage on VPWR, short to ground and short to VPWR for each output, open load, temperature warning and overtemperature shutdown
- Thermal management: Excellent thermal resistance of <1.0 °C/W between junction and case (exposed pad)

- Eight selectable slew rates via the SPI: 0.25 V/µs to more than 16 V/µs for EMI and thermal performance optimization
- Four selectable current limits via the SPI: 5.4/7.0/8.8/10.7 A covering a wide range of applications
- Extended high temperature operating range with current foldback while limiting the current
- Three package sizes available in SOIC, PQFN and HVQFN to meet footprint and application requirement
- Can be operated without SPI with default slew rate of 2.0 V/µs and a 7.0 A current limit threshold
- Highly accurate real-time current feedback through a current mirror output signal with less than 5.0 % error
- Drives inductive loads in a full H-bridge or Half-bridge configuration
- Overvoltage protection places the load in high-side recirculation (braking) mode with notification in H-bridge mode
- Wide operating range: 5.0 V to 28 V operation
- Low $R_{DS(on)}$ integrated MOSFETs: Maximum of 235 mΩ (T_J = 150 °C) for each MOSFET
- Internal protection for overtemperature, undervoltage, and short-circuit by signaling the error condition and disabling the outputs
- I/O pins can withstand up to 36 V
- AEC-Q100 grade 1 qualified

4 Applications

- Electronic throttle control
- Exhaust gas recirculation control (EGR)
- Turbo, swirl and whirl and waste flap control
- Electric pumps, motor control and auxiliaries

5 Ordering information

This section describes the part numbers available to be purchased along with their differences.

Table 1. Orderable parts

Part number [1]	Operating temperature	Package
PC33HB2002EK [2]	T_A = –40 °C to 125 °C T_J = –40 °C to 150 °C	32-pin SOICW exposed pad
PC33HB2002FK		32-pin PQFN exposed pad
PC33HB2002ES		28-pin HVQFN exposed pad

[1] To order parts in tape and reel, add the R2 suffix to the part number.
[2] The SOIC package is still under consideration.

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com and perform a part number search.

6 Internal block diagram

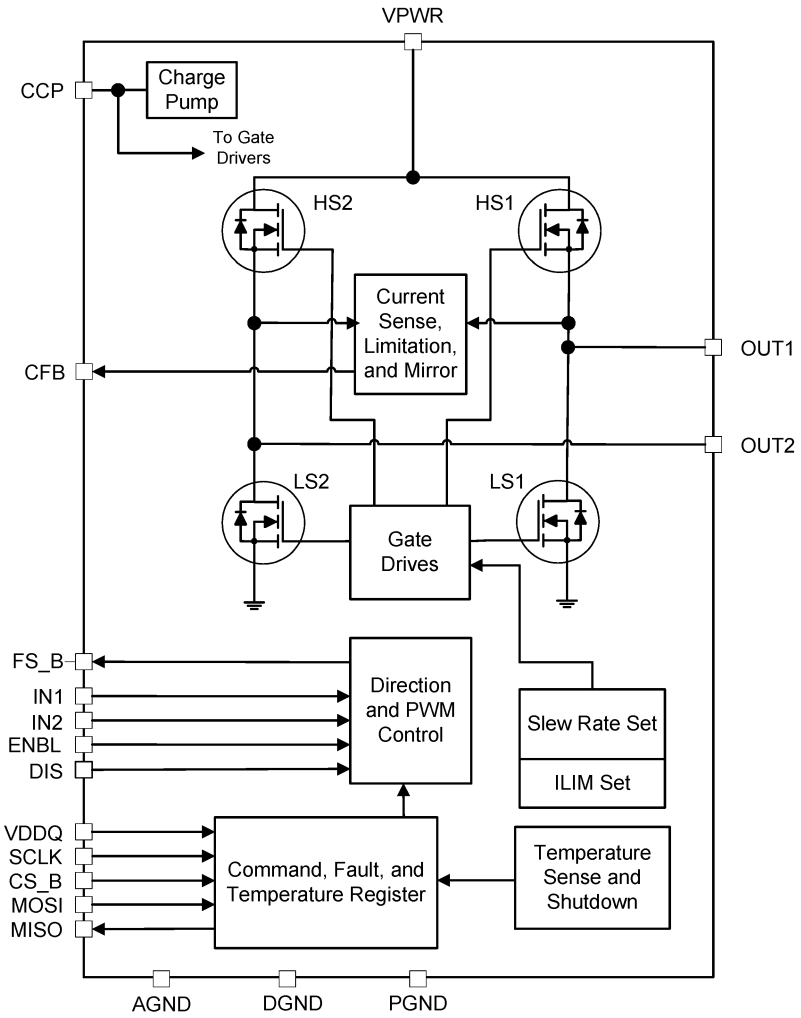


Figure 2. Internal block diagram

7 Pinning information

7.1 Pinning

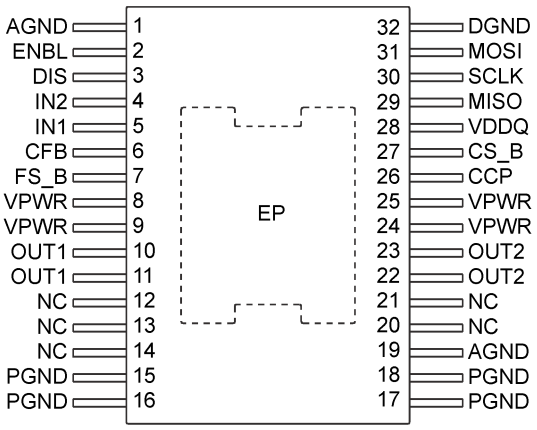


Figure 3. Pin configuration for 32-pin SOICW

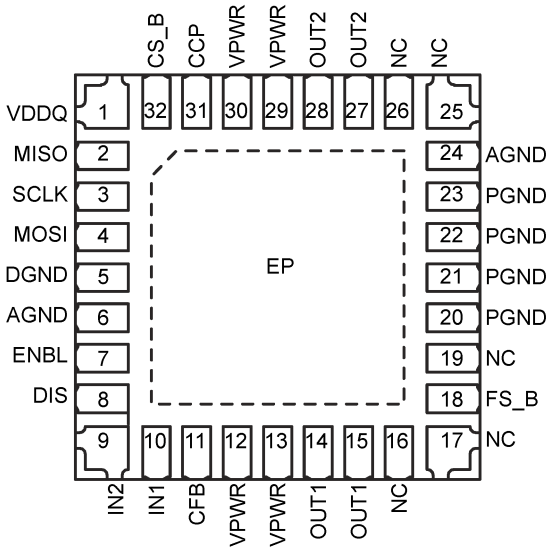


Figure 4. Pin configuration for 32-pin PQFN

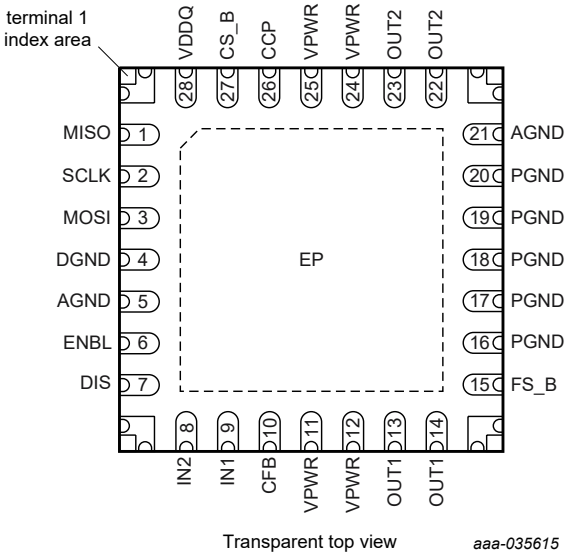


Figure 5. Pin configuration for 28-pin HVQFN

7.2 Pin description

For functional description of each pin see Section 7.3 "Functional pin description".

Table 2. Pin description

Symbol	32-pin SOICW	32-pin PQFN	28-pin HVQFN	Pin function	Definition
AGND	1, 19	6, 24	5, 21	GND	Ground for analog[1]
ENBL	2	7	6	D_In	When ENBL is logic HIGH, the H-bridge is operational. When ENBL is logic LOW, the H-bridge outputs are tri-stated and placed in Sleep mode.
DIS	3	8	7	D_In	When DIS is logic HIGH, both OUT1 and OUT2 are tri-stated
IN2	4	9	8	D_In	Logic input control of OUT2
IN1	5	10	9	D_In	Logic input control of OUT1
CFB	6	11	10	A_Out	The load current feedback output provides ground referenced 0.25 % of the high-side output current.
FS_B	7	18	15	D_Out	Open drain active LOW status flag output
VPWR	8, 9, 24, 25	12, 13, 29, 30	11, 12, 24, 25	Supply	These pins must be connected together physically as close as possible and directly soldered down to a wide, thick, low resistance supply plane on the PCB.
OUT1	10, 11	14, 15	13, 14	A_Out	Source of HS1 and drain of LS1
NC	12, 13, 14, 20, 21	16, 17, 19, 25, 26	—	NC	No connection to die or substrate
PGND	15, 16, 17, 18	20, 21, 22, 23	16, 17, 18, 19, 20	GND	Power ground for OUT1 and OUT2[1]
OUT2	22, 23	27, 28	22, 23	A_Out	Source of HS2 and drain of LS2

Symbol	32-pin SOICW	32-pin PQFN	28-pin HVQFN	Pin function	Definition
CCP	26	31	26	A_Out	External reservoir capacitor connection for the internal charge pump; connected to VPWR
CS_B	27	32	27	D_In	SPI control chip select bar input pin
VDDQ	28	1	28	Supply	Logic level bias
MISO	29	2	1	D_Out	Provides digital data from HB2002 to the MCU
SCLK	30	3	2	D_In	SPI control clock input pin
MOSI	31	4	3	D_In	SPI control data input pin from MCU
DGND	32	5	4	GND	Ground for logic[1]
EP	EP	EP	EP	GND	Thermal exposed pad – connected to substrate[1]

[1] All PGND, AGND, DGND and EP pins must be connected together with very low-impedance on the PCB.

7.3 Functional pin description

7.3.1 Logic bias input (VDDQ)

VDDQ supplies a level shifted bias voltage for the logic level outputs designed to be read by the microprocessor/microcontroller. This pin applies the logic supply voltage to MISO making the output logic levels compliant to logic systems from 3.3 V to 5.0 V. See Section 10.3 "VDDQ digital output supply voltage" for more details.

7.3.2 Supply voltage (VPWR)

VPWR is the power supply input for the H-bridge. The input voltage range with full performance is from 5.0 V to 28 V. In either case, the maximum allowable transient voltage during the event such as load dump is 40 V. Exceeding this limit could result in an avalanche breakdown, as discussed in Section 11.3 "Output avalanche protection". A Zener clamp and/or an appropriately valued capacitor are common methods of limiting the transient. This pin must be externally protected against application of a reverse voltage through an external inverted N-channel MOSFET, diode or switched relay.

7.3.3 Outputs (OUT1 and OUT2)

The OUT1 and OUT2 outputs drive the bi-directional DC motor. Each output has two internal N-channel MOSFETs connected in a Half-bridge configuration between VPWR and ground. Only one internal MOSFET is ON at one time for each output. The turn ON/OFF slew times are determined by the selected SPI slew time register contents.

7.3.4 Inputs (IN1 and IN2)

The IN1 and IN2 inputs determine the direction of current flow in the H-Bridge by directing the PWM input to one of the low-side MOSFETs (see Table 21). When a change in the current direction is commanded via the microprocessor/microcontroller, the PWM switches from one low-side MOSFET to the other without shoot-through current in the H-Bridge. Both MOSFETs cannot be turned ON simultaneously in the same Half-bridge.

7.3.5 Enable inputs (ENBL)

The ENBL pin at logic [0] disables all four of the output drivers (outputs tri-stated) and the part goes into Sleep mode. The ENBL pin at logic [1] enables the part functionality.

7.3.6 Disable inputs (DIS)

The DIS pin at logic [1] disables all four of the output drivers (outputs tri-stated) and the part goes into Standby mode. However, it does not put the part in Sleep mode. The DIS pin is at logic [0] does not inhibit the output.

7.3.7 Current recopy (CFB)

High-side FETs have a current recopy feature through an internal current-mirror which supplies 1/400th of the load current. The current recopy has better than 5.0 % accuracy for load currents between 2.0 A and 10 A. An external resistor may be connected to the CFB pin (R_{CFB}), which sets current to voltage gain. The circuit operates properly in the presence of high-frequency noise. An external capacitor is used to provide filtering. Tie to GND through a resistor if not used.

$$V_{CFB} = \frac{I_{OUT}}{400} \times R_{CFB}$$

7.3.8 Charge pump capacitor (CCP)

This pin is the charge pump output pin for connecting the external charge pump reservoir capacitor. A typical value is 100 nF. The capacitor must be connected from the CCP pin to the VPWR pin. The part does not operate properly without the external reservoir capacitor.

7.3.9 Serial peripheral interface (SPI)

The MC33HB2002 has a serial peripheral interface consisting of Chip Select (CS_B), Serial Clock (SCLK), Master IN Slave Out (MISO), and Master Out Slave In (MOSI). This device is configured as a SPI slave and is daisy-chainable (single CS_B for multiple SPI slaves). See Section 9.6 "16-bit SPI interface" for detailed information on the SPI.

7.3.9.1 Serial clock (SCLK)

The SCLK input is the clock signal input for synchronization of serial data transfer. This pin has TTL/CMOS level compatible input voltages, which allows proper operation with microprocessors using a 3.3 V to 5.0 V supply. When CS_B is asserted low, the MOSI data reads on the SCLK falling edge and the MISO data is updated on the SCLK rising edge.

7.3.9.2 Serial data output (MISO)

The MISO is the SPI data out pin. When CS_B is asserted (low), the MSB is the first bit of the word transmitted on MISO and the LSB is the last bit of the word transmitted on MISO. After all 16 bits of the fault register are transmitted, the MISO output sequentially transmits the digital data received on the MOSI pin. This allows the microprocessor to distinguish a shorted MOSI pin condition. The MISO output continues to transmit the

input data from the MOSI input until CS_B eventually transitions from a logic [0] to a logic [1]. The MISO output pin is in a high-impedance condition unless CS_B is low. When active, the output is “rail to rail”, depending on the voltage at the VDDQ pin.

7.3.9.3 Serial data input (MOSI)

The MOSI input takes data from the microprocessor while CS_B is asserted (low). The MSB is the first bit of each word received on MOSI and the LSB is the last bit of each word received on MOSI. The MC33HB2002 serially wraps around the MOSI input bits to the MISO output after the MISO output transmits its fault flag bits. This pin has TTL/CMOS level compatible input voltages, allowing proper operation with microprocessors using a 3.3 V to 5.0 V supply.

7.3.9.4 Chip select (CS_B)

The CS_B input selects this device for serial transfers. The SPI applies the contents of the I/O register when CS_B rises. When CS_B falls, the I/O register is loaded with the contents of the previously addressed register. This pin has TTL/CMOS level compatible input voltages, which allows proper operation with microprocessors using a 3.3 V to 5.0 V supply.

7.3.10 Status fault (FS_B)

This pin is the device fault status output which signals the MCU of any fault. The fault status pin goes low to report system status according to the bits selected in the Fault Status Mask register as explained in Table 15. This output is active LOW open drain structure, which requires a pull-up resistor to VDD. For more details on this pin, see Table 21.

8 General product characteristics

8.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min.	Max.	Unit
SUPPLY				
V_{PWR}	Supply voltage (VPWR)	−0.3	40	V
V_{DDQ}	Logic bias input (VDDQ)	−0.3	36	V
V_{AGND}	Analog ground (AGND)	−0.3	0.3	V
V_{DGND}	Digital ground (DGND)	−0.3	0.3	V
V_{PGND}	Power ground (PGND)	−0.3	0.3	V
CHARGE PUMP				
V_{CCP}	Charge pump (CCP) voltage	−0.3	V_{PWR} + 12	V
DIGITAL I/O				
V_{IN1}	Input 1 (IN1) voltage	−0.3	36	V
V_{IN2}	Input 2 (IN2) voltage	−0.3	36	V
V_{DIS}	Disable (DIS) voltage	−0.3	36	V

Symbol	Description (Rating)	Min.	Max.	Unit
V_{ENBL}	Enable (ENBL) voltage	−0.3	36	V
V_{FS_B}	Status flag (FS_B) voltage	−0.3	36	V
SPI				
V_{MISO}	Serial data output (MISO) voltage	–0.3	V_{DDQ} + 0.3	V
V_{MOSI}	Serial data input (MOSI) voltage	–0.3	36	V
V_{CSB}	Chip select (CS_B) voltage	–0.3	36	V
V_{SCLK}	Serial clock (SCLK)	–0.3	36	V
OUTPUTS				
V_{OUTX}	OUT1 and OUT2 voltage	−0.3	V_{PWR} + 2.0	V
V_{CFB}	Current recopy (CFB)	−0.3	30	V
CURRENTS				
I_{POUTX}	OUTx peak current Transient current (< 5.0 ms) $T_J \leq 150$ °C	—	16	A
I_{CLAMP}	Digital pin current in clamping mode ENBL, DIS, MOSI, CS_B, SCLK, IN1, IN2	−3.0	3.0	mA
ESD PROTECTION				
	ESD Voltage [1] [2] Human Body Model (HBM)			
V_{ESD_A1}	Local pins, all pins except VPWR, OUT1, OUT2	—	±2000	V
V_{ESD_G1}	Global pins: VPWR, OUT1, OUT2	—	±4000	
	Charge Device Model (CDM)			
V_{ESD_A2}	All pins	—	±500	
V_{ESD_C2}	Corners pins	—	±750	
V_{ESD_C2}	Machine Model			
	All pins	—	±200	

[1] Human body model: AEC-Q100
[2] Charged Device model and Machine model: AEC-Q100 Rev H

8.2 Thermal characteristics

Table 4. Thermal ratings

Symbol	Description (Rating)	Min.	Max.	Unit
THERMAL RATINGS				
T_J	Operational junction temperature Continuous Transient	 −40 −40	 150 195	°C
T_A	Operational ambient temperature [1]	−40	125	°C
T_{STG}	Storage temperature	−65	150	°C
T_{PPRT}	Peak package reflow temperature during reflow [2] [3]	—	260	°C
MC33HB2002EK THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS				
$R_{\Theta JA}$	Junction to ambient natural convection – single layer board (1s) [4] [5]	—	75.7	°C/W
$R_{\Theta JA}$	Junction to ambient natural convection – four layer board (2s2p) [4] [5]	—	23.9	°C/W
$R_{\Theta JB}$	Junction to board [6]	—	7.1	°C/W
$R_{\Theta JCBOTTOM}$	Junction to case (bottom) [7]	—	0.66	°C/W

Symbol	Description (Rating)		Min.	Max.	Unit
Ψ_{JT}	Junction to package top – natural convection	[8]	—	2.97	°C/W
MC33HB2002ES THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS					
$R_{\Theta JA}$	Junction to ambient natural convection – single layer board (1s)	[4] [5]	—	88.5	°C/W
$R_{\Theta JA}$	Junction to ambient natural convection – four layer board (2s2p)	[4] [5]	—	31.3	°C/W
$R_{\Theta JB}$	Junction to board	[6]	—	11.3	°C/W
$R_{\Theta JCBOTTOM}$	Junction to case (bottom)	[7]	—	0.39	°C/W
Ψ_{JT}	Junction to package top – natural convection	[8]	—	1.45	°C/W
MC33HB2002FK THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS					
$R_{\Theta JA}$	Junction to ambient natural convection – single layer board (1s)	[4] [5]	—	63.4	°C/W
$R_{\Theta JA}$	Junction to ambient natural convection – four layer board (2s2p)	[4] [5]	—	21.55	°C/W
$R_{\Theta JB}$	Junction to board	[6]	—	6.41	°C/W
$R_{\Theta JCBOTTOM}$	Junction to case (bottom)	[7]	—	0.61	°C/W
Ψ_{JT}	Junction to package top – natural convection	[8]	—	2.6	°C/W

[1] The circuit specification describes IC operation within the parametric operating range defined in the electrical characteristic table.
[2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
[3] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to nxp.com, search by part number. Remove prefixes/suffixes and enter the core ID to view all orderable parts (for MC33xxxD enter 33xxx), and review parametrics.
[4] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[5] Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
[6] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[7] Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
[8] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters (Ψ) are not available, the thermal characterization parameter is written as Psi-JT.

8.3 Operating conditions

This section describes the operating conditions of the device. Conditions apply to the following data, unless otherwise noted.

Table 5. Nominal operation

Within the range of functionality, all functionalities have to be guaranteed. All voltages refer to GND. Currents are positive into and negative out of the specified pin. T_J = −40 °C to 150 °C, unless otherwise specified.

Symbol	Description (Rating)	Min.	Max.	Unit
SUPPLY VOLTAGE				
V_{PWR}	Functional operating supply voltage range—VPWR	5.0	28	V
SPI				
f_{SPI}	SPI frequency range	0.5	10	MHz

Table 6. Supply current consumption

V_{PWR} = 5.0 V to 28 V, T_J = −40 °C to 150 °C, unless otherwise specified.

Symbol	Description (Rating)		Min.	Max.	Unit
VPWR SUPPLY CURRENT CONSUMPTIONS					
I_{VPWR}	Operating mode—V_{PWR}	[1]	—	20	mA
$I_{VPWR(SLEEP)}$	Sleep mode, measured at V_{PWR} = 12 V	[2]	—	50	µA

Symbol	Description (Rating)	Min.	Max.	Unit
LEAKAGE CURRENTS FOR THE FUNCTIONS CONNECTED TO VPWR				
$I_{OUTLEAK}$	Output leakage current, outputs off, VPWR = 28 V V_{OUTx} = VPWR V_{OUTx} = GND	 — −60	 100 —	µA

[1] ENBL = Logic [1], I_{OUT} = 0 A
[2] ENBL = Logic[0], DIS = Logic[1] and I_{OUT} = 0 A

8.3.1 Reverse battery

To protect against a reverse battery condition, a dedicated device to block reverse current must be populated in the application, as shown in Figure 22 (with a diode).

Some applications require operation at very low battery voltages (start-stop applications), and many systems have multiple H-bridges in parallel, which require high current reverse battery protection with very low voltage drops during the operation. In such applications, an external, reverse-polarity, FET may be used instead of the reverse protection diode, to lower the voltage drop from battery to VPWR pins. The CCP pin can be used to bias the gate of an N-channel FET, provided the bias current requirement is less than 20 µA. In Figure 23, the NPN transistor is used for fast response of the N-Channel FET during turn-off.

8.3.2 Digital I/Os characteristics

Table 7. Digital I/Os characteristics

V_{PWR} = 5.0 V to 28 V, T_J = −40 °C to 150 °C, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
DIGITAL INPUTS				
V_{IH_X}	Input high-voltage	2.0	—	V
V_{IL_X}	Input low-voltage	—	0.8	V
V_{HYS_X}	Input voltage threshold hysteresis	100	—	mV
R_{PD_X}	Input pull-down resistance—MOSI, SCLK, ENBL, IN1, IN2	40	175	kΩ
R_{PU_X}	DIS, CS_B Input pull-up resistance to 5.0 V	40	175	kΩ
C_{IN}	Input capacitance	—	12	pF
DIGITAL OUTPUTS				
V_{OH_X}	MISO output high-voltage, with −1.0 mA	0.8 × V_{DDQ}	—	V
V_{OL_X}	MISO output low-voltage, with 1.0 mA	—	0.4	V
I_{MISO_LK}	MISO tri-state leakage current	−10	10	µA
$V_{OL\_FS\_B}$	FS_B low-voltage, with 1.0 mA	—	0.4	V
$R_{PU\_FS\_B}$	FS_B output pull-up resistance to 5.0 V	100	500	kΩ

9 General IC functional description and application information

9.1 Introduction

The MC33HB2002 is a programmable H-bridge, power integrated circuit (IC) designed to drive DC motors or bi-directional solenoid controlled actuators, such as throttle control or exhaust gas recirculation actuators. It is particularly well suited for the harsh environment

found in automotive power train systems. The MC33HB2002 is designed to specifically address the ISO 26262 safety standard requirements. The key characteristic of this versatile driver is configurability. The selectable slew rate permits the customer to choose the slew rate needed for performance and noise suppression. The Serial Peripheral Interface (SPI) allows the system microprocessor to clear the fault register, select a programmable current limit, and select the slew rate.

The MC33HB2002 is designed to drive a bi-directional DC motor using pulse-width modulation (PWM) for speed and torque control. A current mirror output provides an analog feedback signal proportional to the load current. SPI diagnostic reporting includes, open load, short-to-battery, short-to-ground, die temperature range, overvoltage, and undervoltage.

9.2 Features

- Advanced diagnostic reporting via the serial peripheral interface (SPI)
  - Charge pump undervoltage
  - Overvoltage and undervoltage on VPWR
  - Short to ground as well as short to VPWR for each output
  - Open load
  - Temperature warning
  - Overtemperature shutdown
- Excellent thermal resistance of <1.0 °C/W between junction and case (exposed pad)
- Eight selectable slew rates via the SPI from 0.25 V/µs to more than 16 V/µs, giving the user flexibility to perform trade-offs between low EMI and better thermal performance
- Active current limiting with four selectable current limits via the SPI: 5.4/7.0/8.8/10.7 A covering a wide range of applications
- Can be operated without SPI with default slew rate of 2.0 V/µs and a 7.0 A current limit threshold. See Figure 22 for operation without SPI.
- Efficient thermal management scheme by reducing conduction losses to ensure continuous operation and availability of the part under hash operating conditions
- Accurate real-time current feedback through a current mirror output signal with less than 5.0 % error
- Configurable for full H-bridge or Half-bridge operation through the SPI
- Overvoltage protection places the load in high-side recirculation (braking) mode and signal the error condition in H-bridge mode
- Wide operating range: 5.0 V to 28 V operation
- Internal protection for short-circuit, overtemperature, and undervoltage by signaling the error condition and disabling the outputs
- I/O pins can withstand up to 36 V

9.3 Functional block diagram

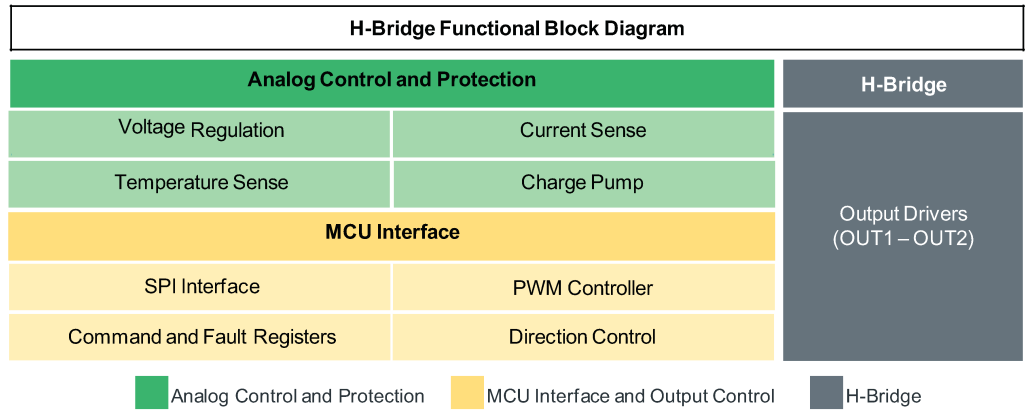


Figure 6. Functional block diagram

9.4 Functional description

9.4.1 H-bridge output drivers (OUT1 and OUT2)

The MC33HB2002 power IC provides the means to efficiently drive a DC motor in both forward and reverse shaft rotation via a monolithic H-bridge comprising low $R_{DS(on)}$ N-channel MOSFETs and integrated control circuitry. The switching action of the H-bridge can be pulse-width modulated to obtain both torque and speed control, with slew rates selectable from 0.25 V/µs to 16 V/µs in eight steps, giving the user flexibility to perform trade offs between meeting the EMI requirements and minimize switching losses. The outputs comprise four power MOSFETs configured as a standard H-bridge, controlled by the IN1 and IN2 inputs.

9.4.2 Analog control, protection, and diagnostics

The MC33HB2002 has integrated voltage regulators supplying the logic and protection functions internally. This reduces the requirements for external supplies and insures the device is safely controlled at all times when battery voltage is applied. An integrated charge pump provides the required bias levels to insure the output MOSFETs turn fully ON when commanded. Each MOSFET provides feedback to the protection circuitry by way of a current sensor. Each sense signal is compared with programmable overcurrent levels and produces an immediate shutdown in case of a high current short-circuit. The high-side current sense is also used for producing a current limiting PWM to reduce overload conditions as determined by the programmable limits. The high-side current sense is available to the MCU as an analog current proportional to the load current.

Each MOSFET has overtemperature protection circuitry disabling the device. A thermal warning sets a flag in the SPI register when the device is approaching a protection limit. A thermal management scheme decreases the conduction losses by dropping the current to half the value of selected limit threshold when $T_J > OT_W$.

The MC33HB2002 consists of advanced diagnostics and protection features such as open load detection, overvoltage sense and protection, undervoltage protection, or charge pump undervoltage detection.

9.4.3 MCU interface and output control

The SPI and control logic signals are compatible with both 5.0 V and 3.3 V logic systems. The SPI provides an easy to configure interface for the MCU through programmable control of output slew rates, current limits, enabling/disabling of outputs, SPI equivalent of inputs (VIN1 and VIN2), and mode of operation (H-bridge/half-bridge). The status register makes detailed diagnostics available for protective and warning functions. The output drivers are controlled by the input signals ENBL, DIS, IN1, and IN2 using the parallel inputs and VIN1, VIN2, as well as EN using the SPI control.

9.5 Modes of operation

9.5.1 Description

The operating modes are:

- **Sleep mode**
  All MC33HB2002 functions are disabled. The current consumption does not exceed the sleep-state current specification.
- **Standby mode**
  All MC33HB2002 logic are fully operational with the outputs in a high-impedance state.
- **Normal mode**
  All MC33HB2002 functions are fully operational. Any detected faults transition the device to Fault mode.
- **Fault mode**
  Certain of functions are forced off and FS_B signal is latched to logic [0] indicating a fault.

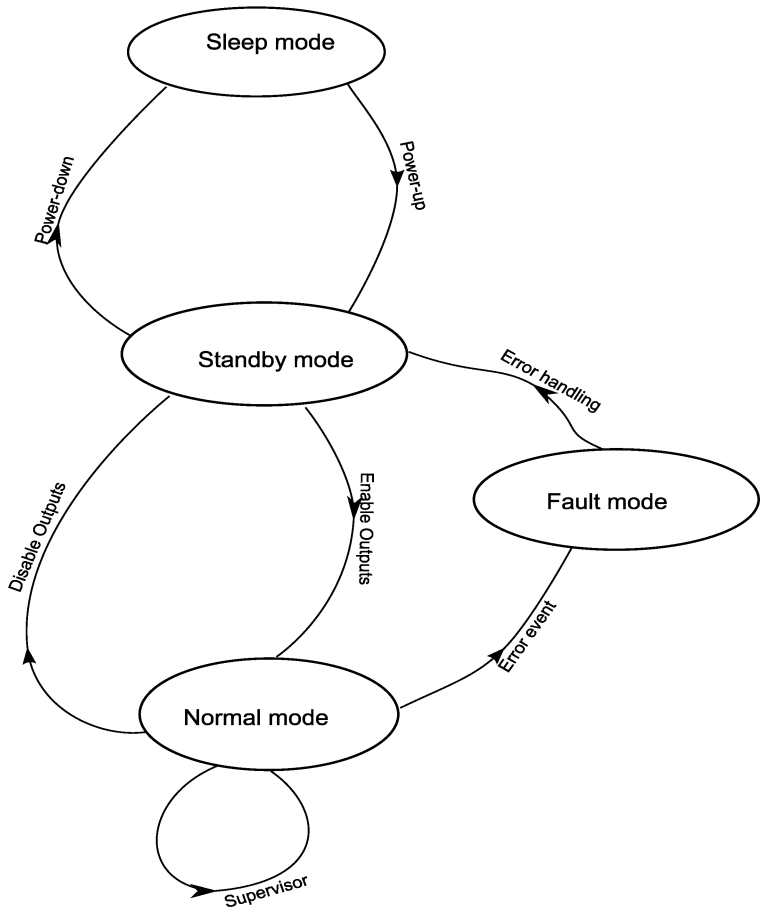


Figure 7. Operating mode state diagram

The MC33HB2002 wakes up by EN going to a logic high state. If a valid wake-up event occurs while the V_{PWR} voltage level is above the specified threshold, the regulators power-up sequence is initiated as illustrated in Figure 8.

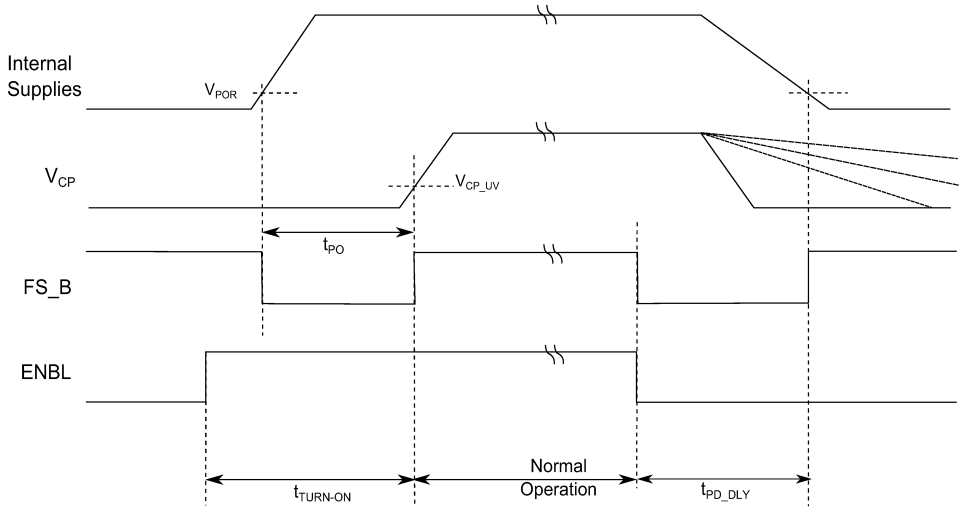


Figure 8. Regulators power-up and power-down sequences

On Power-up, Fault Status (FS_B) activates after the internal supplies reach their operating threshold. All regulators acquire their steady-state by the turn-on delay time ($t_{TURN-ON}$). On power-up, FS_B is active for at least t_{PO}, and then deactivates after V_{CP} is greater than the undervoltage threshold (V_{CP_UV}) and all faults are clear. When ENBL transitions to logic LOW, the outputs turn off (high-impedance state) and FS_B goes low. Power-down starts t_{PD_DLY} after ENBL goes low. DIS must also be low for FS_B to deactivate. On Power-down, FS_B is activated until the internal supplies are disabled.

9.5.2 Electrical characteristics

Table 8. Electrical characteristics

V_{PWR} = 5.0 V to 28 V, T_J = −40 °C to 150 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit
Wake-up					
$t_{TURN-ON}$	Turn-on delay time. Time from ENBL going high to FS_B returning high [1]	—	—	1.0	ms
t_{PO}	Turn-on Status time. Minimum pulse width on FS_B during power up	1.0	—	2.0	µs
t_{PD_DLY}	Turn-off delay time. ENBL going low until FS_B is allowed to go high	8.0	—	11	µs

[1] ENBL is a digital input and has the characteristics defined in Table 7.

9.6 16-bit SPI interface

9.6.1 Description

The Serial Peripheral Interface (SPI) has the following features:

- Full duplex, 4-wire synchronous communication
- Slave mode operation only
- Fixed SCLK polarity and phase requirements
- Fixed 16-bit command word
- SCLK operation up to 10 MHz

The SPI communication works as follows:

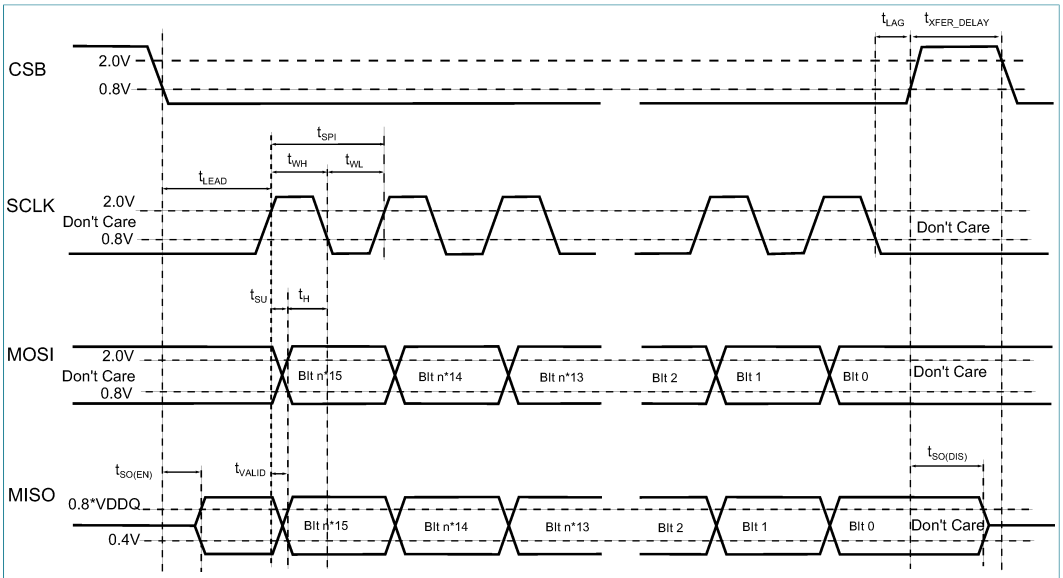


Figure 9. SPI dynamic diagram

SPI communication is “MSB first” and is composed of 16 SCLK cycles. The MOSI data is read on SCLK falling edge and the MISO data is updated on SCLK rising edge. The daisy-chain feature passes data in excess of 16 bits to the next device in line. If the number of clock pulses within CS_B low is not more than 0 and an integer multiple of 16, the current SPI communication is ignored and a framing error is recorded in the status register. Both the serial input and the serial output data are valid on the SCLK falling edge, and transitions on the rising edge of SCLK.

The content reported by the MC33HB2002 is the previous selected register address at the time CS_B goes low. On the first SPI communication after enable goes high, the first register sent on the MISO line is the status register. When addressing a READ register, the content bits are ignored. See Table 9 for detail on timing parameters.

Note:

It is recommended to use good programming practices incorporating writes to SPI registers, immediately verified by reads to the registers. This ensures a reliable communication between MCU and the device. MCU is responsible for detecting any malfunction in the communication that may come up due to hardware or software failure.

9.6.2 Electrical characteristics

Table 9. Electrical characteristics

V_{DDQ} = 3.13 V to 5.25 V, T_J = −40 °C to 150 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit
SPI INTERFACE TIMING					
f_{SPI}	Recommended frequency of SPI operation, $t_{SPI} = 1/f_{SPI}$	0.5	—	10	MHz
t_{LEAD}	Falling edge of CS_B to rising edge of SCLK (required setup time)	30	—	—	ns
t_{LAG}	Falling edge of SCLK to rising edge of CS_B (required setup time)	30	—	—	ns
t_{XFER_DELAY}	No data time between SPI commands	300	—	—	ns
t_{WH}	High time of SCLK	45	$t_{SPI}/2$	—	ns
t_{WL}	Low time of SCLK	45	$t_{SPI}/2$	—	ns
t_{SU}	SCLK rising edge to MOSI (required setup time)	15	—	—	ns
$t_{SO(EN)}$	Time from falling edge of CS_B to MISO low-impedance	—	—	30	ns
$t_{SO(DIS)}$	Time from rising edge of CS_B to MISO high-impedance	—	—	30	ns
t_{VALID}	Time from falling edge of SCLK to MISO data valid, V_{DDQ} = 5.0 V, 1.0 V ≤ MISO ≤ 4.0 V, CL = 50 pF	—	—	30	ns
t_{VALID}	Time from falling edge of SCLK to MISO data valid, V_{DDQ} = 3.3 V, 0.66 V ≤ MISO ≤ 2.64 V, CL = 50 pF	—	—	45	ns
t_H	Data hold time	30	—	—	ns

9.6.3 SPI fault reporting

The MC33HB2002 has an advanced SPI fault reporting and error detection feature. The fault status register latches a fault at the time a fault is detected.

9.6.3.1 Clearing the fault status

The fault status is cleared when the fault is no longer present and one of three events occurs, this is referred to as “clr_flt” throughout this document.

Table 10. Timing parameters for clearing fault status

Symbol	Characteristic	Min.	Typ.	Max.	Unit
t_{DIS_MIN}	The falling edge of a logic signal on DIS clears non-active faults. Minimum pulse width to ensure the faults are cleared.	—	—	1.0	µs
t_{ENBL_MIN}	The rising edge of a logic signal on ENBL clears non-active faults. Minimum pulse width to ensure the faults are cleared.	—	—	1.0	µs
	A write to the status register selectively clears fault status with a ‘1’ in this bit location.				

9.6.3.2 SPI framing error detection

A SPI Framing error is recorded if either of the following two conditions are met:

- The number of clock pulses within CS_B low is not more than 0 and an integer multiple of 16
- Register 00 is addressed for a Write operation

9.6.4 SPI mapping

Bit 15 is 1 for a Write operation and 0 for a Read operation. A write to the status register selectively clears the fault status with a '1' in this bit location, unless the fault is still present.

Table 11. SPI register selection

14	13	Register
0	0	Device Identification (Reserved)
0	1	Status
1	0	Fault Status Mask
1	1	Configuration and Control

Table 12. Device identification (Reserved)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	1	RV3	RV2	RV1	RV0

RV0-RV3 reserved bits. Bit 4 is the device identifier.

Table 13. Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	—	—	—	FRM	CP_U	UV	OV	SCP2	SCP1	SCG2	SCG1	OL	OC	TW	OT
Read [1]	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Write	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X

[1] The default value for all bits (bit 0 to bit 11) in status register is 0 if no fault is detected in the device.

Table 14. Status bits description

Bit	Bit name	Description
15	—	—
14	—	—
13	—	—
12	—	—
11	FRM	SPI framing error
10	CP_U	Charge pump undervoltage
9	UV	VPWR undervoltage
8	OV	VPWR overvoltage
7	SCP2	Short-circuit to power output 2
6	SCP1	Short-circuit to power output 1
5	SCG2	Short-circuit to ground output 2

Bit	Bit name	Description
4	SCG1	Short-circuit to ground output 1
3	OL	Open load
2	OC	Overcurrent - current limit has been activated
1	TW	Thermal warning
0	OT	Overtemperature shutdown

Table 15. Fault status mask

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	—	—	**DOV**	**FRM**	**CP_U**	**UV**	**OV**	**SCP2**	**SCP1**	**SCG2**	**SCG1**	**OL**	**OC**	**TW**	**OT**
Read [1]	0	1	0	0	0	1	1	0	1	1	1	1	0	0	0	1
Write	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X

[1] The SPI bits in “Read” section show the default values.

The mask bits are in the same order as the Status bits. A '1' causes the FS_B to become active when this fault is active.

Bit 12 (DOV - Disable overvoltage) configures the response to an overvoltage condition:

- 1 = Disable overvoltage protection (OV bit is warning only)
- 0 = Enable overvoltage protection in Full Bridge mode

Table 16. Configuration and control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	—	—	—	**CL**	**TM**	**AL**	**ILM1**	**ILM0**	**SR2**	**SR1**	**SR0**	**EN**	**MODE**	**INPUT**	**VIN2**	**VIN1**
Read [1]	0	1	1	0	1	1	0	1	1	0	0	1	1	0	0	0
Write	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X

[1] The SPI bits in “Read” section show the default values.

Table 17. Configuration and control bits description

Bit	Bit name	Description
15	—	—
14	—	—
13	—	—
12	CL	Check for open load (in Full Bridge Standby mode) • 1 = Enabled on transition from Standby to Normal mode. Execute test in Standby on transition to 1 • 0 = Disable test
11	TM	Thermal Management mode • 1 = Enable current limiting with t_B= 32 µs at the selected current limit threshold (ILIM) and derate to ILIM/2 when in OT_W state • 0 = Disable switching of current limit threshold from ILIM to ILIM/2. The current limit threshold is set to ILIM/2 from the beginning which scales up and down according to selected ILIM setting.

Bit	Bit name	Description
10	AL	Active Current Limit mode • 1 = Enable active current limit when overcurrent ILIM threshold has been exceeded • 0 = Disable active current limit. Exceeding overcurrent ILIM threshold set OC flag but does not control outputs
9	ILIM1	ILIM Bit 1
8	ILIM0	ILIM Bit 0
7	SR2	Slew Rate Bit 2
6	SR1	Slew Rate Bit 1
5	SR0	Slew Rate Bit 0
4	EN	Disable Outputs • 1 = ENABLE output control when ENBL pin is high and DIS pin is low • 0 = DISABLE output control and tri-state outputs
3	MODE	Input Control mode[1] • 1 = H-bridge control mode • 0 = Half-bridge control mode
2	INPUT	Active INPUT Control mode • 1 = SPI control of outputs by way of VIN1 and VIN2, IN1 pin and IN2 pin are disabled • 0 = Parallel control of outputs by way of IN1 pin and IN2 pin, VIN1 and VIN2 are disabled
1	VIN2	Virtual Input 2 (SPI equivalent of IN2) • 1 = ON equivalent to IN2 pin at logic high in parallel mode • 0 = OFF equivalent to IN2 pin at logic low in parallel mode
0	VIN1	Virtual Input 1 (SPI equivalent of IN1) • 1 = ON equivalent to IN1 pin at logic high in parallel mode • 0 = OFF equivalent to IN1 pin at logic low in parallel mode

[1] When MODE=0 (Half-bridge mode): Active Current Limit mode is disabled, OV is a warning only, SC acts independent on each output, open load is disabled.

9.7 Protection and supervision

The MC33HB2002 includes supervision features which enable advanced diagnostics by monitoring the V_{PWR} undervoltage, V_{PWR} overvoltage and die temperature.

9.7.1 V_{PWR} undervoltage detection

9.7.1.1 Description

When VPWR is less than V_{PWR_FUV} longer than t_{VPWR} all output transistors turn off and remain off until VPWR increases above the V_{PWR_FUV} threshold by V_{PWR_UVHYS}. While ramping up the voltage on VPWR, when VPWR increases to a voltage greater than V_{PWR_FUV} + V_{PWR_UVHYS} for at least t_{VPWR}, the MC33HB2002 starts unrestricted operation.

9.7.1.2 Electrical characteristics

Table 18. V_{PWR_UV} electrical characterization

T_J = −40 °C to 150 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{PWR} UNDERVOLTAGE					
V_{PWR_FUV}	Undervoltage threshold to disable outputs (falling edge)	3.55	—	4.0	V
V_{PWR_UVHYS}	Undervoltage hysteresis	250	—	450	mV
t_{VPWR}	Undervoltage detection filter time	—	—	10	µs
V_{PWR_POR}	Power On Reset with VPWR falling	2.3	—	3.1	V

9.7.2 V_{PWR} overvoltage detection

If VPWR voltage is higher than $OV_{\_HSD}$ threshold longer than t_{OV_HSD}, the OV status bit is set and the device is in an overvoltage condition. When the device is in an overvoltage condition and is also in H-bridge mode (MODE bit =1), both OUT1 and OUT2 low-side switches controlling the load is turned off and both OUT1 and OUT2 high-side switches are turned on to drain the energy in the load.

When VPWR voltage drops by more than $OV_{\_HYS}$ below the $OV_{\_HSD}$ threshold, the outputs are restored to operation without an overvoltage condition. The OV status bit is not reset until clr_flt conditions are satisfied.

9.7.2.1 Electrical characteristics

Table 19. V_{PWR_OV} electrical characterization

T_J = −40 °C to 150 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit
OVERVOLTAGE DETECTION					
$V_{PWR\_OV\_HSD}$	Overvoltage detection threshold	33	35	37	V
$V_{PWR\_OV\_HYS}$	Overvoltage detection hysteresis	2.3	2.45	2.5	V
t_{OV_HSD}	Overvoltage detection filter time [1]	—	—	3.0	µs

[1] Measured in H-bridge mode, 1.0 A resistive load, SR = 000, measured from FS_B low to both $V_{OUT} \geq 10\ \% V_{PWR}$

9.7.3 Die temperature

9.7.3.1 Description

The MC33HB2002 has temperature sensors near the center of each power device.

The threshold of the overtemperature warning (OT_W) is approximately 175 °C on any power device. Temperature warning condition is defined as exceeding OT_W. When a temperature warning occurs, outputs are not shutdown. However, the SPI status bit shows the actual status at accessing time. This is a non-latching condition and the status clears when the temperature falls below the hysteresis threshold. Further action is taken on temperature warning as described in Section 9.6.4 "SPI mapping" and Section 10.4.1.4 "Active current limit regulation".

When the temperature is above the overtemperature threshold (OT) for the defined filter time (t_{OT}), the driver latches off, the SPI OT fault bit is set. This is a latching fault and

requires performing clr_flt, as described in Section 9.6.3.1 "Clearing the fault status", after the temperature reduces T_{HYS} below the threshold.

9.7.3.2 Electrical characteristics

Table 20. OT electrical characterization

V_{PWR} = 5.0 V to 28 V, unless otherwise specified.

Symbol	Characteristic		Min.	Typ.	Max.	Unit
OVERTEMPERATURE/TEMPERATURE WARNING						
OT_W	Overtemperature warning detection threshold	[1]	165	175	185	°C
OT	Overtemperature shutdown threshold	[1]	175	187.5	200	°C
T_{HYS}	Overtemperature hysteresis	[1]	—	12	—	°C
t_{OT}	Temperature warning detection filter time		—	—	11	µs

[1] Guaranteed by characterization.

9.7.4 Truth table

The following truth table summarizes the output response to input states. The tri-state conditions and the status flag are reset using DIS, ENBL, or SPI. The truth table uses the following notations: L = LOW, H = HIGH, X = HIGH or LOW, Xb is inverse of X, and Z = High-impedance.

Table 21. Truth table

Device state	Input conditions				Status	Outputs	
	ENBL	DIS[1]	IN1[2]	IN2[2]	FS_B[3]	OUT1	OUT2
HALF-BRIDGE CONTROL MODE							
Forward	H	L	H	L	H	H	L
Reverse	H	L	L	H	H	L	H
Freewheeling Low	H	L	L	L	H	L	L
Freewheeling High	H	L	H	H	H	H	H
IN1 Disconnected	H	L	Z	X	H	L	X
IN2 Disconnected	H	L	X	Z	H	X	L
H-BRIDGE CONTROL MODE							
Forward	H	L	H	H	H	H	L
Reverse	H	L	L	H	H	L	H
Freewheel High	H	L	X	L	H	H	H
IN1 Disconnected – Reverse	H	L	Z	X	H	Xb	H
IN2 Disconnected – Freewheel High	H	L	X	Z	H	H	H
PROTECTION							
Disable (DIS)	H	H	X	X	L	Z	Z
DIS Disconnected	H	Z	X	X	L	Z	Z
Undervoltage Lockout[4]	H	X	X	X	L	Z	Z
Overvoltage[5]	H	X	X	X	L	H	H
Overtemperature[6]	H	X	X	X	L	Z	Z
Short-circuit[7]	H	X	X	X	L	Z	Z
Sleep mode ENBL	L	X	X	X	H	Z	Z
ENBL Disconnected	Z	X	X	X	H	Z	Z

[1] SPI bit EN=1 AND DIS=L for table entry DIS=L
[2] When the SPI bit INPUT = 1, the SPI bit VIN1 behaves the same as IN1 and SPI bit VIN2 behaves the same as IN2.
[3] Default response for FS_B, SPI programming may change the default behavior.
[4] In the event of an undervoltage condition, the outputs tri-state and status flag is SET logic LOW. Upon undervoltage recovery the outputs are restored to their original operating condition, FS_B remains low until clr_flt clears the status register.
[5] In the event of an overvoltage condition, the outputs go to freewheeling high configuration, independent of the input signals, and the status flag is latched to a logic LOW. Upon overvoltage recovery, the outputs are restored to following the input signals but FS_B remains low until clr_flt clears the status register. In Half-bridge mode an overvoltage event does not change the output state.
[6] When a short-circuit or overtemperature condition is detected, the power outputs are tri-state latched-OFF, independent of the input signals, and the status flag is latched to a logic LOW. To reset from this condition requires the toggling of either DIS, ENBL, or V_{PWR} or flt_clr from the SPI.
[7] When in H-bridge control mode, short-circuit controls both OUT1 and OUT2. However, in Half-bridge mode, short-circuit only controls the output which detects the short-circuit.

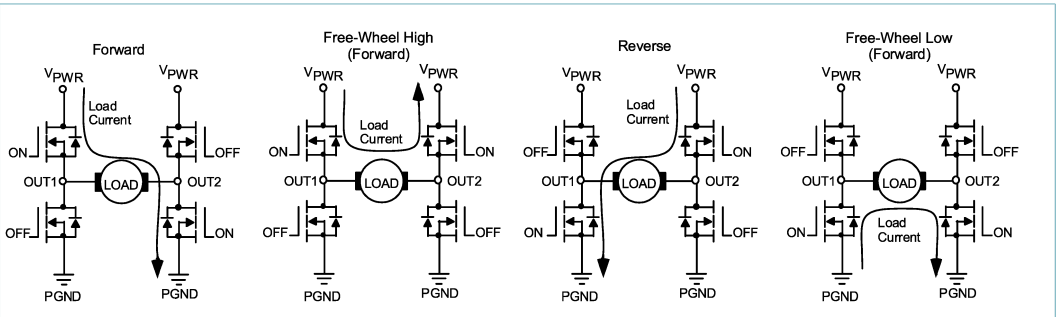


Figure 10. Output operating configurations

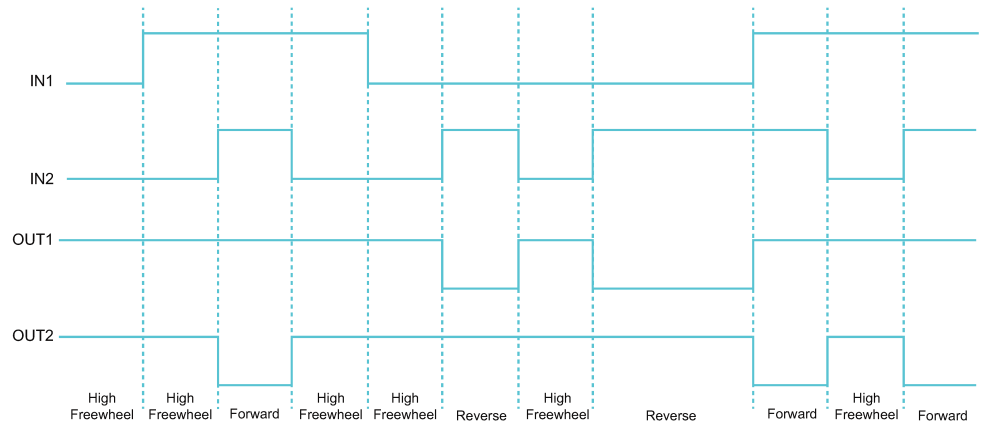


Figure 11. H-bridge operation with ENBL = 1 and DIS = 0

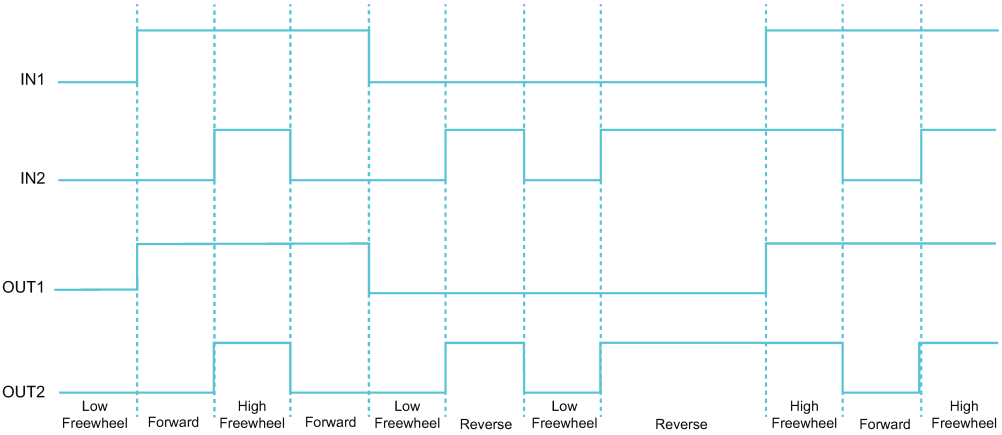


Figure 12. Half-bridge operation with ENBL = 1 and DIS = 0

9.8 Error handling

Table 22. Error handling

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
SUPERVISION				
Overtemperature shutdown	Normal mode	See Table 21	Write Clear Fault SPI bit OT	Latching fault requires clr_flt
Die temperature warning	All except Sleep mode	SPI flag only (TW)	Non-latching auto clears when condition clears	Non-latching fault clears when condition clears
Overcurrent	Normal mode	SPI flag only (OC)	Write Clear Fault SPI bit OC	Latching fault requires clr_flt
Open load	Transition to Normal mode or request from MCU	SPI flag only (OL)	Write Clear Fault SPI bit OL	Information only, no restart required

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
Short-circuit to Ground Output 1	Normal mode	See Table 21	Write Clear Fault SPI bit SCG1	Latching fault requires clr_flt
Short-circuit to Ground Output 2	Normal mode	See Table 21	Write Clear Fault SPI bit SCG2	Latching fault requires clr_flt
Short-circuit to VPWR Output 1	Normal mode	See Table 21	Write Clear Fault SPI bit SCP1	Latching fault requires clr_flt
Short-circuit to VPWR Output 2	Normal mode	See Table 21	Write Clear Fault SPI bit SCP2	Latching fault requires clr_flt
VPWR Overvoltage	All except Sleep mode	See Table 21	Write Clear Fault SPI bit OV	Non-latching fault clears when condition clears
VPWR Undervoltage	All except Sleep mode	See Table 21	Write Clear Fault SPI bit UV	Non-latching fault clears when condition clears
CP Undervoltage	All except Sleep mode	SPI flag only (CP_UV). No action, except if micro requests a shutdown	Non-latching fault clears when condition clears	Non-latching fault clears when condition clears
SPI failure	All except Sleep mode	SPI flag only (FRM)	Write Clear Fault SPI bit FRM	A valid SPI communication

10 Functional block description

10.1 Oscillator

A single clock module is used for all systems and filter timing.

10.1.1 Frequency modulation

The clock is frequency modulated to spread the oscillator's energy over a wide frequency band. This spreading decreases the peak electromagnetic radiation level and improves electromagnetic compatibility (EMC) performance.

Table 23. Frequency electrical characteristics

V_{PWR} = 5.0 V to 28 V, T_J = −40 °C to 150 °C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Oscillator					
f_{OSC}	Oscillator frequency	8.277	9.3	10.323	MHz

10.2 Charge pump

10.2.1 Description

The charge pump generates a voltage of 9.5 V nominal/12 V maximum above the V_{PWR} supply. The maximum external load which can be connected to the CCP pin is 20 µA. The charge pump requires an external 20 V capacitor for energy storage and to cover

transients. A SPI flag error is reported when $V_{CP} \leq V_{CP\_UV}$. The charge pump frequency is modulated by means of the spread spectrum modulation of the main clock.

Table 24. Charge pump electrical characteristics

V_{PWR} = 5.0 V to 28 V, T_J = −40 °C to 150 °C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Charge pump					
C_{CP}	Charge pump external capacitor [1]	—	100	—	nF
V_{CP}	Charge pump voltage referenced to V_{PWR} [2]	V_{CP_UV}	9.5	12	V
V_{CP}	Charge pump voltage referenced to V_{PWR} [3]	6.0	—	$(2 \times V_{PWR}) - 1.0$	V
I_{CP}	Charge pump current capability	1.0	—		mA
V_{CP_UV}	Charge pump undervoltage threshold	7.45	8.0	8.7	V
$t_{CP\_UV\_F}$	Charge pump undervoltage detection filter time	—	18.0	—	µs
f_{CP}	Charge pump frequency	—	9.3	—	MHz

[1] A 20 V X7R capacitor with at least ≤ ±20 % tolerance is recommended.
[2] With 1.0 mA loading on the charge pump and 8.0 V ≤ V_{PWR} < 28.0 V
[3] With 1.0 mA loading on the charge pump and 5.0 V ≤ V_{PWR} < 8.0 V

10.3 VDDQ digital output supply voltage

10.3.1 Description

The VDDQ pin supplies the digital output buffer (MISO) of the MC33HB2002, either at 5.0 V or 3.3 V, by connecting externally to the system MCU supply:

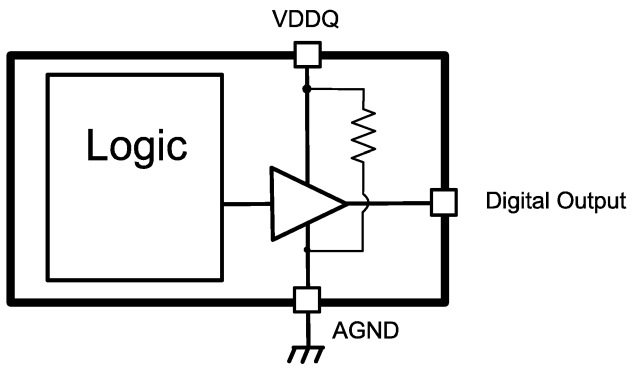


Figure 13. Digital output buffer supply

This pin has a pull-down resistor to ensure the input is low in the event it is left open. If this pin is shorted to ground or left open, the SPI MISO reports 0000h.

Table 25. VDDQ electrical characterizations

V_{DDQ} = 3.13 V to 5.25 V, T_J = −40 °C to 150 °C, unless otherwise specified.

Symbol	Characteristic	Min.	Typ.	Max.	Unit
R_{DOWN_VDDQ}	VDDQ pull-down resistor	55	100	260	kΩ

10.4 H-bridge and Half-bridge operation

10.4.1 Description

The H-bridge output control is defined by the SPI bit.

Half-bridge control

- In parallel mode, the physical inputs IN1 and IN2 control the OUT1 and OUT2 respectively
- In SPI mode, VIN1 and VIN2 control the Half-bridge outputs similar to physical inputs

H-bridge control

- In parallel mode, the physical input IN1 controls direction and IN2 controls PWM
- In SPI mode, VIN1 and VIN2 control the H-Bridge outputs similar to physical inputs

This device provides active recirculation through the opposing FET of each Half-bridge. Embedded protections avoid cross conduction. In Half-bridge mode, active current limit, overvoltage protection, and open load detection features are disabled. For overvoltage, there is OV warning only. Moreover, unlike H-bridge control mode, the short-circuit protection acts independently on each output.

A more detailed explanation of output characteristic with respect to inputs in H-bridge as well as Half-bridge mode is explained in Section 9.7.4 "Truth table". The differences in fault priorities between the two modes is described in section Section 10.4.1.1 "H-bridge and Half-bridge fault priority".

10.4.1.1 H-bridge and Half-bridge fault priority

The following tables specify which fault control dominates output control if two or more are present at one time. Note that for these tables ENBL and DIS are defined as the signal condition which disables the output. EN is the SPI control bit setting which disables the outputs.

Table 26. H-Bridge mode fault priority

	OT	OC	SCG1	SCG2	SCP1	SCP2	OV	UV	ENBL	DIS
OC	OT									
SCG1	SC	SC								
SCG2	SC	SC	SC							
SCP1	OT	SC	SC	SC						
SCP2	OT	SC	SC	SC	SC					
OV	OT	OV	SC	SC	OV	OV				
UV	UV	UV	UV	UV	UV	UV	UV			
ENBL	ENBL	ENBL	ENBL	ENBL	ENBL	ENBL	ENBL	ENBL		
DIS	DIS	DIS	DIS	DIS	DIS	DIS	OV	DIS	ENBL	
EN	EN	EN	EN	EN	EN	EN	OV	UV	ENBL	DIS

Table 27. Half-bridge mode fault priority

	OT	SCG1	SCG2	SCP1	SCP2	UV	ENBL	DIS
SCG1	OT							
SCG2	OT	SC1 AND 2						
SCP1	OT	SC1	SC1 AND 2					
SCP2	OT	SC1 AND 2	SC2	SC1 AND 2				
UV	UV	UV	UV	UV	UV			
ENBL	ENBL	ENBL	ENBL	ENBL	ENBL	ENBL		
DIS	DIS	DIS	DIS	DIS	DIS	DIS	ENBL	
EN	EN	EN	EN	EN	EN	UV	ENBL	DIS

Table 28. Fault priority description

Name	Description
OT	Overtemperature
OC	Overcurrent
SC	Short-circuit
SCGx	Short to ground
SCPx	Short to power (VPWR)
OV	Overvoltage
UV	Undervoltage

10.4.1.2 Current recopy

High-side FETs have current recopy feature. Current recopy has less than 5 % error referred to the load, for currents between 2.0 A and 10 A. Current recopy is a ratio of 1/400 of the current through the FET. This recopy current is made available on the CFB pin.

10.4.1.3 Slew rate selection

The slew rate is selectable by SPI bits from 0.25 V/µs to 16 V/µs. There is a bypass setting which switches the outputs as fast as possible.

10.4.1.4 Active current limit regulation

Figure 14 presents the simplified current regulation loop.

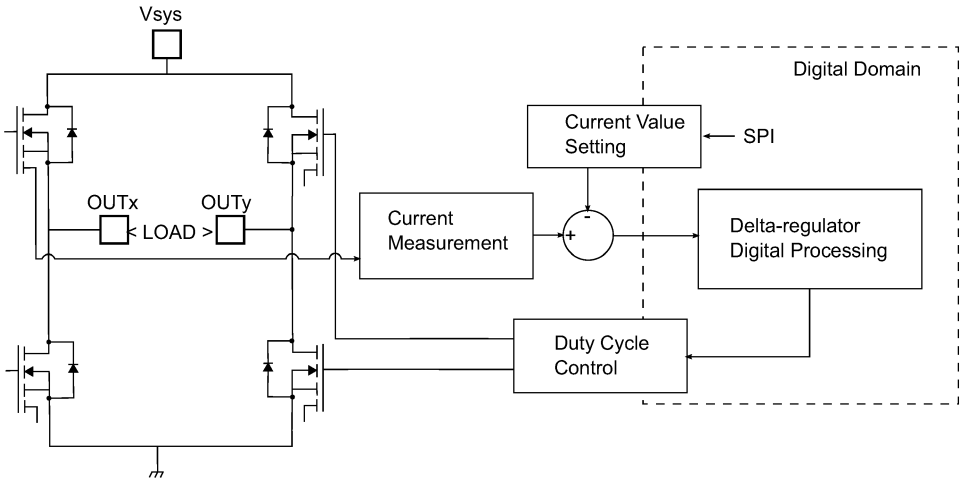


Figure 14. Simplified current regulated loop for I_{LIM}

The active current limit threshold is selectable by the SPI in four steps from 5.4 A to 10.7 A. The active current limit is initiated, and the OC SPI fault status bit is set when the current exceeds the threshold set by the current limit comparator.

A blanking time (t_B, 32 µs) is set from the time the current limit is exceeded. If a short-circuit shutdown is not triggered before the blanking time has expired, the H-bridge switches to high-side recirculation mode for *2 * t_A*. t_A is determined by the time it takes for the current to decay below the current limit threshold after switching to recirculation mode.

After *2 * t_A*, the control of the gates releases, restoring the output to the configuration set by the inputs. If the average output FET temperature exceeds the die temperature warning threshold (OT_W), the current limit threshold is set to 50 % of of its original value selected via SPI and output keeps switching with t_B set at 32 µs with t_A as explained above and in Figure 15. The temperature dependent blanking time does not change during the blanking interval. Input control does not cause the output to switch ON while current is greater than I_{LIM}. Input control commanding the output to switch OFF immediately switches OFF the output and resets the I_{LIM} circuit.

Note:

Short-circuit is ignored when $T_J > OT_W$ for an interval of $t_B + 2*t_A$ while current limit threshold transitions to 50 % of its set value as shown in Figure 15. Although, short-circuit is ignored for this small time interval, overtemperature protection will still be able to protect the FETs in this time interval if excessive heating happens due to a short-circuit event or high temperature transients.

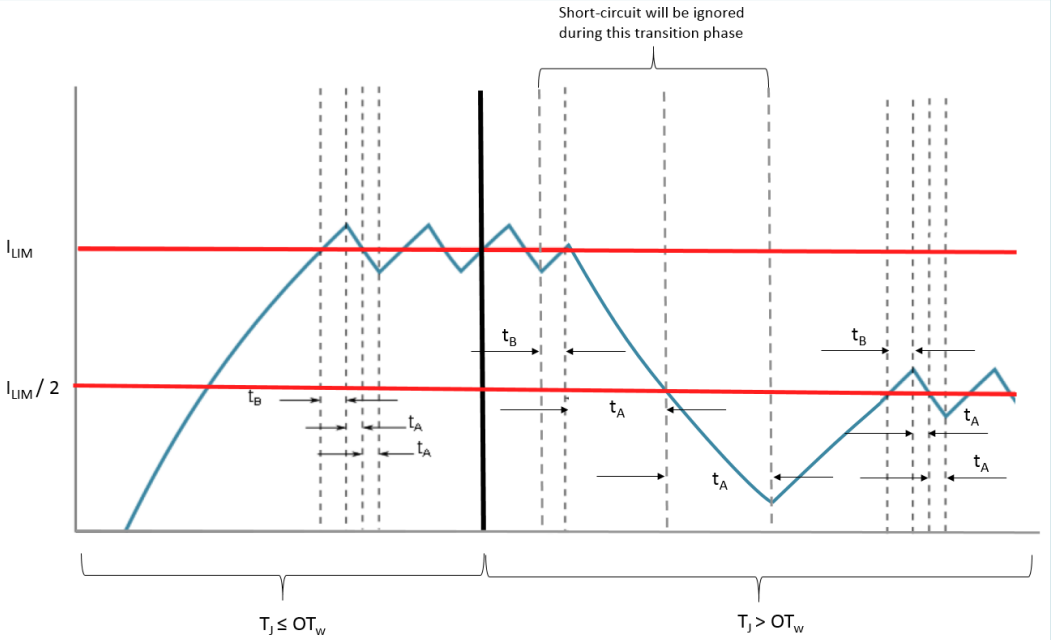


Figure 15. ILIM timing and thermal response

10.4.1.5 Open load detection in standby mode

This diagnostic only operates when the device is in Standby mode (both outputs in a high-impedance state) and is configured for full H-bridge mode. It is designed for applications having less than 50 nF from OUT1 and OUT2 to GND, a load inductance less than 15 mH, and an equivalent resistance of 600 Ω (typical) as a target for open load detection.

The diagnostic can activate in one of two ways:

1. The device is transitioning from STBY mode to Normal mode and the CL bit is high.
2. The device is in STBY mode and receives a command changing the CL bit setting from low to high.

When the open load check is performed, if there is current in an inductive load at the start of the test, the results may not be valid.

The diagnostic is activated in two stages:

1. The circuit turns on both low-side output FETs, to discharge any residual charge on the output capacitance. During this stage, the short-circuit detection for OUT1 or OUT2 is functional and provides normal short-circuit protection and diagnostics.
2. In second stage, the circuit turns off the OUT1 low-side FET and applies an internal pull-up of 1.0 mA on OUT1 while maintaining the OUT2 low-side driver on. If the voltage on OUT1 is greater than the open load threshold after the defined filter time, an open load fault is recorded. See Figure 16 for more details. The OUT1 and OUT2 are restored to the commanded configuration after the test results are latched into the fault buffer.

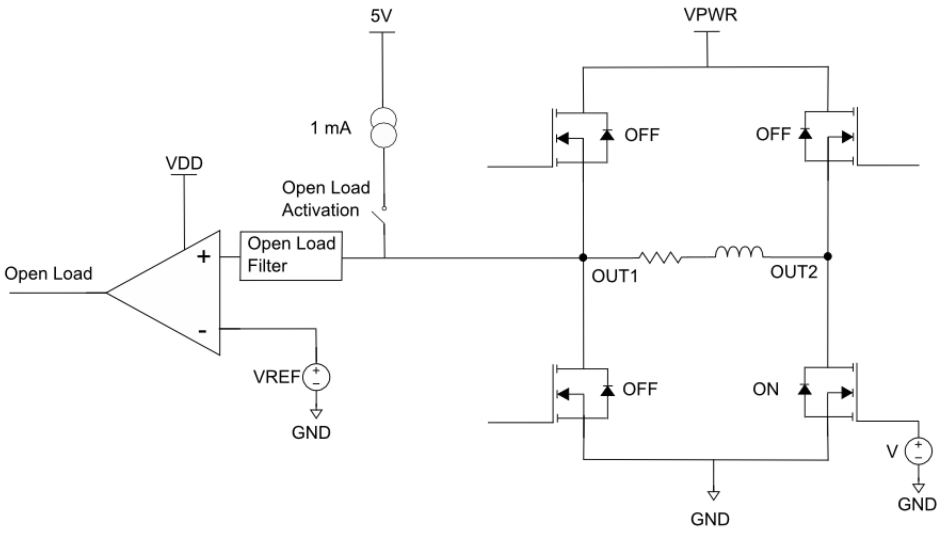


Figure 16. Open load detection circuit

10.4.1.6 Open load detection in active mode

Open load detection in Active mode is active when the output is configured for full H-Bridge mode and an output is being switched. Open load in Active mode is detected when the OUT1 and OUT2 voltages do not exhibit overshoot greater than the V_{OLATH} (threshold) over V_{PWR} between the time the low-side is commanded OFF and the low-side FET is turned back on during an output PWM cycle, as shown in Figure 17 and Figure 18. On the other hand, an open load is not detected if the energy stored in the inductor is high enough to cause an overshoot greater than the V_{OLATH} (threshold) over V_{PWR} caused by the fly-back current flowing through the body diode, as shown in anti-shoot through phase of Figure 17.

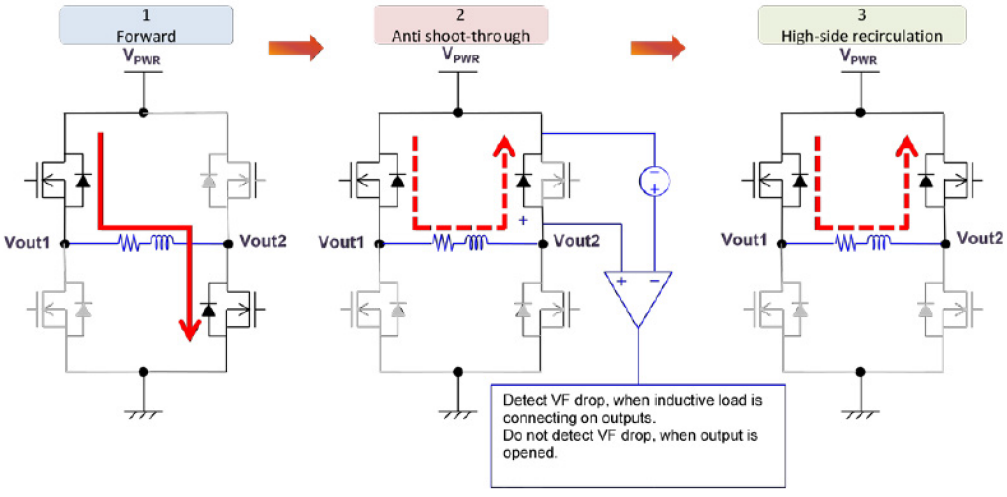


Figure 17. Open load detection circuit for active mode

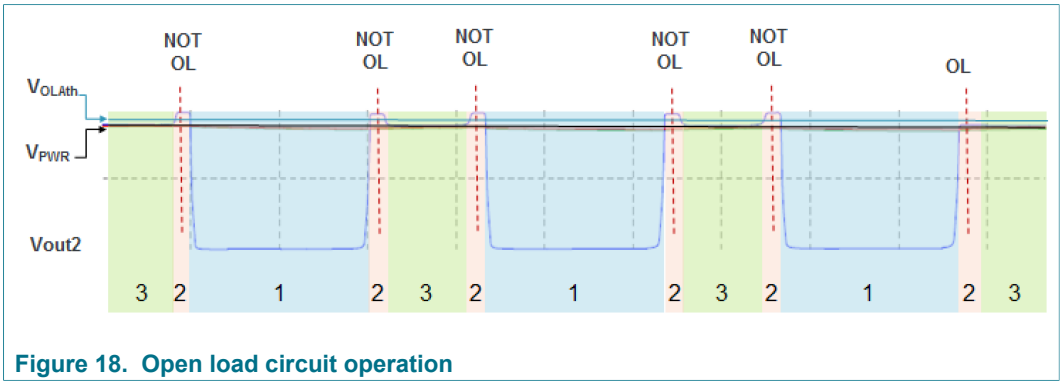


Figure 18. Open load circuit operation

During normal operation, the result of the open load detection window is held until the end of the next detection window. Open load detected in the active mode is a dynamic status which is only cleared by detecting the load is not open or leaving Normal mode.

10.4.1.7 Short-circuit detection

The short-circuit detection circuit monitors both high-side and low-side FETs continuously. When the current is above the short-circuit threshold (SC) for the defined filter time (t_{SC}), the driver is switched off, and the SPI fault bit is set. The driver can be restored to normal operation by clearing the fault status by performing clr_flt, as described in Section 9.6.3.1 "Clearing the fault status".

10.4.2 Electrical characteristics

Table 29. H-bridge electrical characterization

V_{PWR} = 5.0 V to 28 V, T_J = −40 °C to 150 °C, unless otherwise specified.

Symbol	Parameter		Min.	Typ.	Max.	Unit
OUTPUT						
$R_{DS(ON\_LSD)}$	LSDx on-state resistance, I_{LDS} = 3.0 A, T_J = 150 °C	[1]	—	—	235	mΩ
$R_{DS(ON\_LSD)}$	LSDx on-state resistance, I_{LDS} = 3.0 A, T_J = −40 °C	[1] [2]	—	—	125	mΩ
$R_{DS(ON\_HSD)}$	HSDx on-state resistance, I_{LDS} = 3.0 A, T_J = 150 °C	[1]	—	—	235	mΩ
$R_{DS(ON\_HSD)}$	HSDx on-state resistance, I_{LDS} = 3.0 A, T_J = −40 °C	[1] [2]	—	—	125	mΩ
V_F	Output MOSFET body diode forward voltage drop with I_{LDS} = 3.0 A		—	—	2.0	V
t_{DON} t_{DOFF}	OUTx turn-on and turn-off delay times Digital signal to 10 % or 90 % I_{LOAD} = 1.0 A, V_{PWR} = 14 V, SR = “000”, resistive load		—	—	3.0	µs
$t_{DDISABLE}$	OUTx disable delay time		—	—	3.0	µs
$t_{RDISABLE\_1}$	OUTx disable recovery delay time Open load detection disabled, DIS recovery after 1.0 µs high or ENBL recovery after 5.0 µs low, SR = “000”, resistive load < 400 Ω		—	—	8.0	µs
$t_{RDISABLE\_2}$	OUTx disable recovery delay time Open load detection enabled, DIS recovery after 1.0 µs high or ENBL recovery after 5.0 µs low, SR = “000”, resistive load < 400 Ω		—	—	128	µs

Symbol	Parameter	Min.	Typ.	Max.	Unit
SR	OUTx rising and falling slew rate, from 10 % to 90 % of V_{PWR}, measured with 1.0 A resistive load at VPWR = 14 V				
	SPI SR = 000	—	bypass	—	V/µs
	SPI SR = 001	11.2	16	20.8	
	SPI SR = 010	5.6	8.0	10.4	
	SPI SR = 011	2.8	4.0	5.2	
	SPI SR = 100 (default)	1.4	2.0	2.6	
	SPI SR = 101	0.7	1.0	1.3	
	SPI SR = 110	0.35	0.5	0.65	
	SPI SR = 111	0.15	0.25	0.35	
CURRENT SENSE					
I_{RATIO}	Current recopy ratio (per 1.0 A of load current)				
	I_{LOAD} < 2.0 A	—	2.5	—	mA
	2.0 A ≤ I_{LOAD} < 10 A	—	2.5	—	
I_{ERROR}	Load current error, I_{LOAD} < 2.0 A	−0.100	—	0.100	A
I_{ERROR}	Load current error, 2.0 A ≤ I_{LOAD} < 10 A	−5.0	—	5.0	%
dI/dt	Load current slew rate	0.5	—	—	A/µs
FAULT DETECTION AND CURRENT LIMIT REGULATION					
I_{LIM}	Current limit threshold current (T_J ≤ OT_W)				
	SPI ILIM = 00	4.0	5.4	6.8	A
	SPI ILIM = 01 (default)	6.0	7.0	8.0	
	SPI ILIM = 10	7.3	8.8	10.3	
	SPI ILIM = 11	9.0	10.7	12.5	
$I_{LIM}/2$	Current limit threshold current (T_J > OT_W) [3]				
	SPI ILIM = 00	—	2.7	—	A
	SPI ILIM = 01 (default)	—	3.5	—	
	SPI ILIM = 10	—	4.4	—	
	SPI ILIM = 11	—	5.4	—	
t_B	Blanking time (T_J ≤ OT_W) and (T_J > OT_W)	—	32	—	µs
SHORT-CIRCUIT SHUTDOWN (T_J ≤ OT_W)					
I_{SC_LS}	Low-side short-circuit detection threshold current	I_{LIM} + 3.0	—	I_{LIM} + 8.0	A
I_{SC_HS}	High-side short-circuit detection threshold current	I_{LIM} + 4.0	—	I_{LIM} + 9.0	A
t_{SC}	Short-circuit detection filter time (T_J ≤ OT_W) and (T_J > OT_W)	5.0	—	10	µs
SHORT-CIRCUIT SHUTDOWN (T_J > OT_W)					
$I_{SC\_LS}/2$	Low-side short-circuit detection threshold current [3]	$I_{LIM}/2$ + 1.5	—	$I_{LIM}/2$ + 4.0	A
$I_{SC\_HS}/2$	High-side short-circuit detection threshold current [3]	$I_{LIM}/2$ + 2.0	—	$I_{LIM}/2$ + 4.5	A
OPEN LOAD DETECTION					
V_{OP}	Open load detection voltage threshold	0.6	—	0.8	V
I_{OL}	Out1 pull-up current	0.8	—	1.3	mA
t_{OP_LSD}	Open load detection filter time	93	—	118	µs
V_{OLATH}	Open load active mode threshold V_{OLA} = V_{OUTx} − V_{PWR}	160	—	360	mV

[1] In an application, $R_{DS(on)}$ depends on charge pump loading and timing limitations, including slew rate and duty cycle. These factors determine the enhancement level of the device's integrated high-side FETs during switching.
[2] Guaranteed by characterization
[3] Guaranteed by design

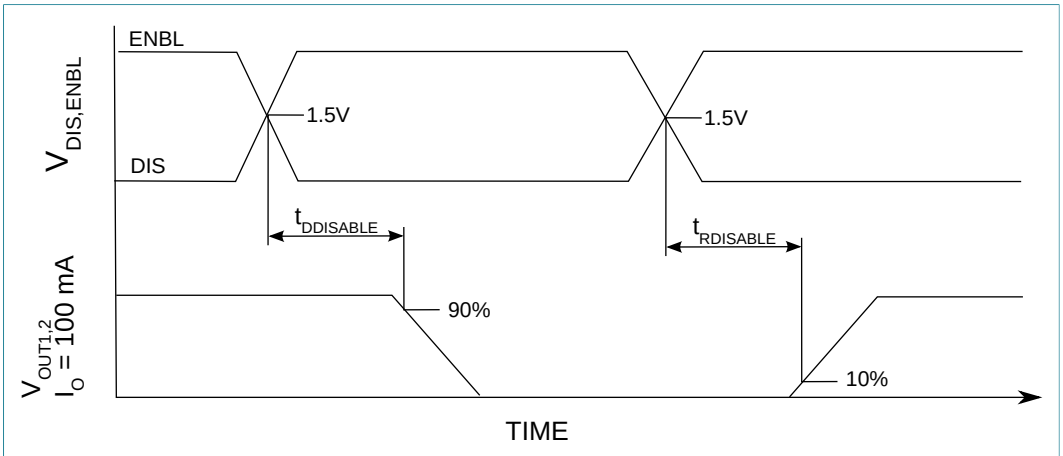


Figure 19. Disable delay timing

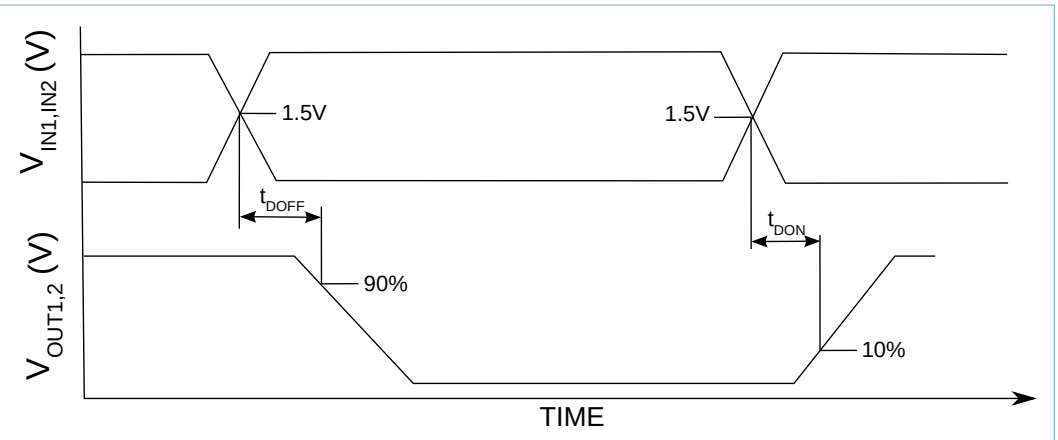


Figure 20. Output delay timing

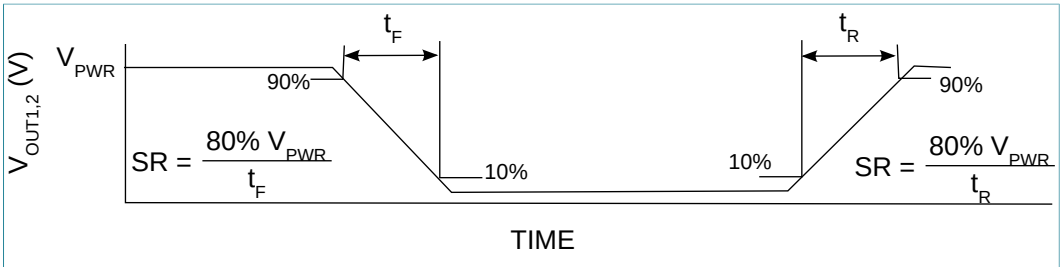


Figure 21. Slew rate

11 Applications

11.1 Introduction

The MC33HB2002 is a programmable and configurable H-bridge, power integrated circuit (IC) designed to drive DC motors or bi-directional solenoid controlled actuators, such as throttle control or exhaust gas recirculation actuators, with continuous average current of

3.0 A and peaks over 10.0 A. Figure 22 shows a typical simplified minimum application schematic without SPI interface to MCU and reverse battery protection through a diode. Figure 23 shows a typical simplified application diagram with reverse battery protection using an external N-channel FET driven by the CCP pin. This is useful for low battery voltage applications where diode drops could be significant. See Section 8.3.1 "Reverse battery" for details on reverse battery protection.

The value of C1 is determined based on the maximum current in the load, and the maximum system voltage. C1 should be able to absorb this energy without exceeding 40 V, otherwise a clamp is required, as explained in Section 11.3 "Output avalanche protection". If ENBL is high and the part is in H-bridge mode, the OV protection protects against this condition.

11.2 Application diagram

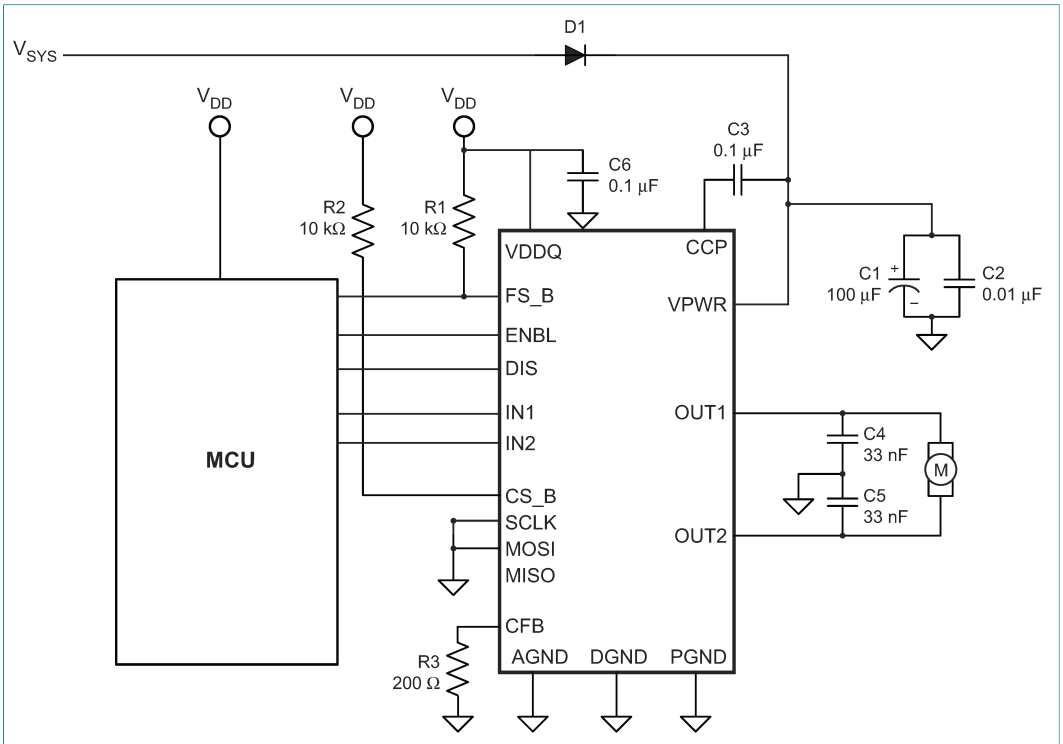


Figure 22. Simplified minimum application schematic (Reverse battery protection using a diode and operation without SPI)

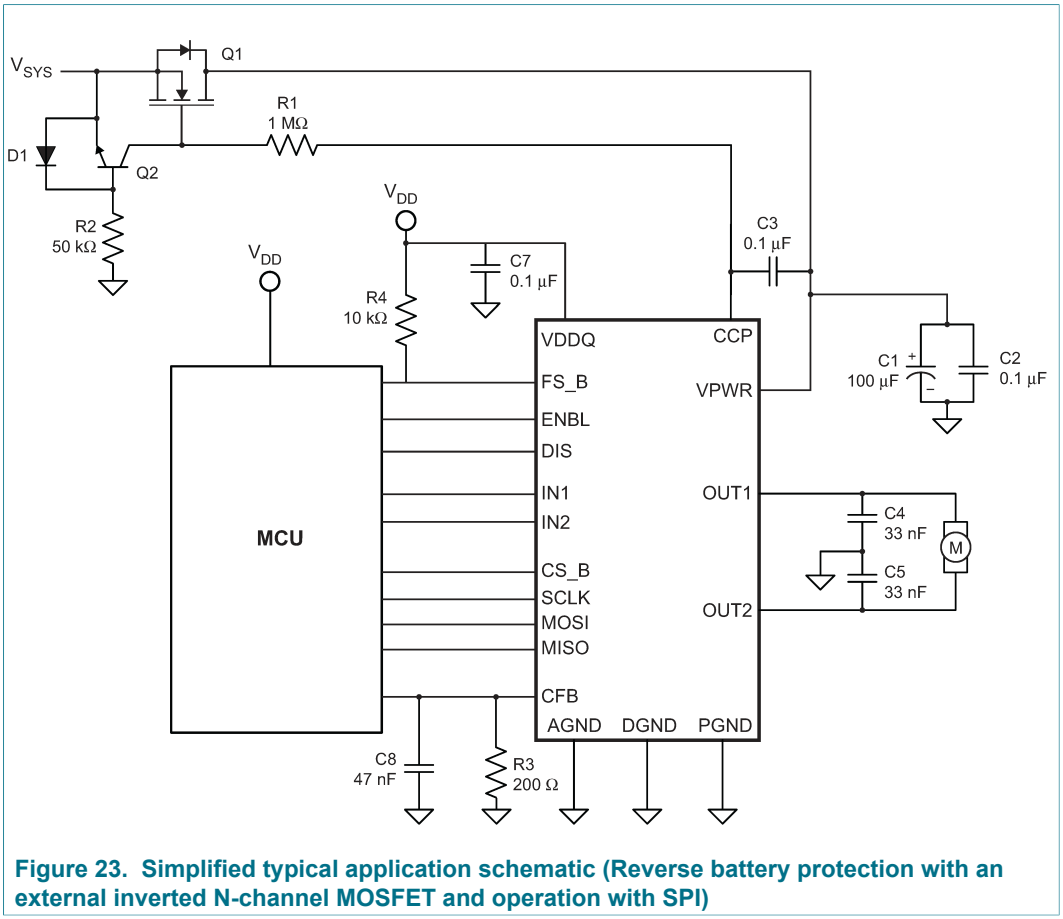


Figure 23. Simplified typical application schematic (Reverse battery protection with an external inverted N-channel MOSFET and operation with SPI)

11.3 Output avalanche protection

The MC33HB2002 has in-built overvoltage protection, preventing output avalanche breakdown when configured for operation in H-bridge mode (default operation mode) by setting the bit MODE (bit number 3) to 1 in the Configuration and Control SPI register. As long as the part is enabled, the entire energy in the inductor is dissipated in the high-side recirculation loop, as explained in Section 9.7.2 "VPWR overvoltage detection". However, when the DOV bit (bit number 12) is set to 1, which disables the overvoltage protection and only gives an overvoltage warning, or while operating the part in Half-Bridge mode by setting the bit MODE (bit number 3) to 0 in the Configuration and Control SPI register, it is important to implement output avalanche protection, as shown in Figure 24. If VPWR were to become an open circuit, the outputs would likely tri-state simultaneously due to the disable logic. This could result in an unclamped inductive discharge.

The VPWR input to the MC33HB2002 should not exceed 40 V during this transient condition, to prevent electrical overstress of the output drivers. This can be accomplished with a zener clamp or MOV, and/or an appropriately valued input capacitor with sufficiently low ESR as shown in Figure 24. If ENBL is at logic [1] and the part is in H-bridge mode, this problem is mitigated by internal overvoltage protection.

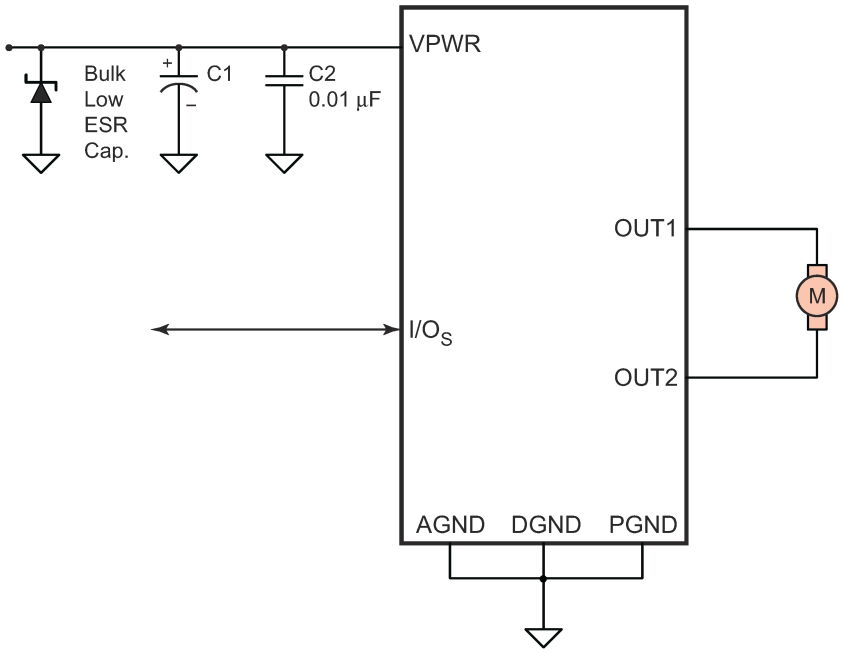


Figure 24. Output avalanche protection

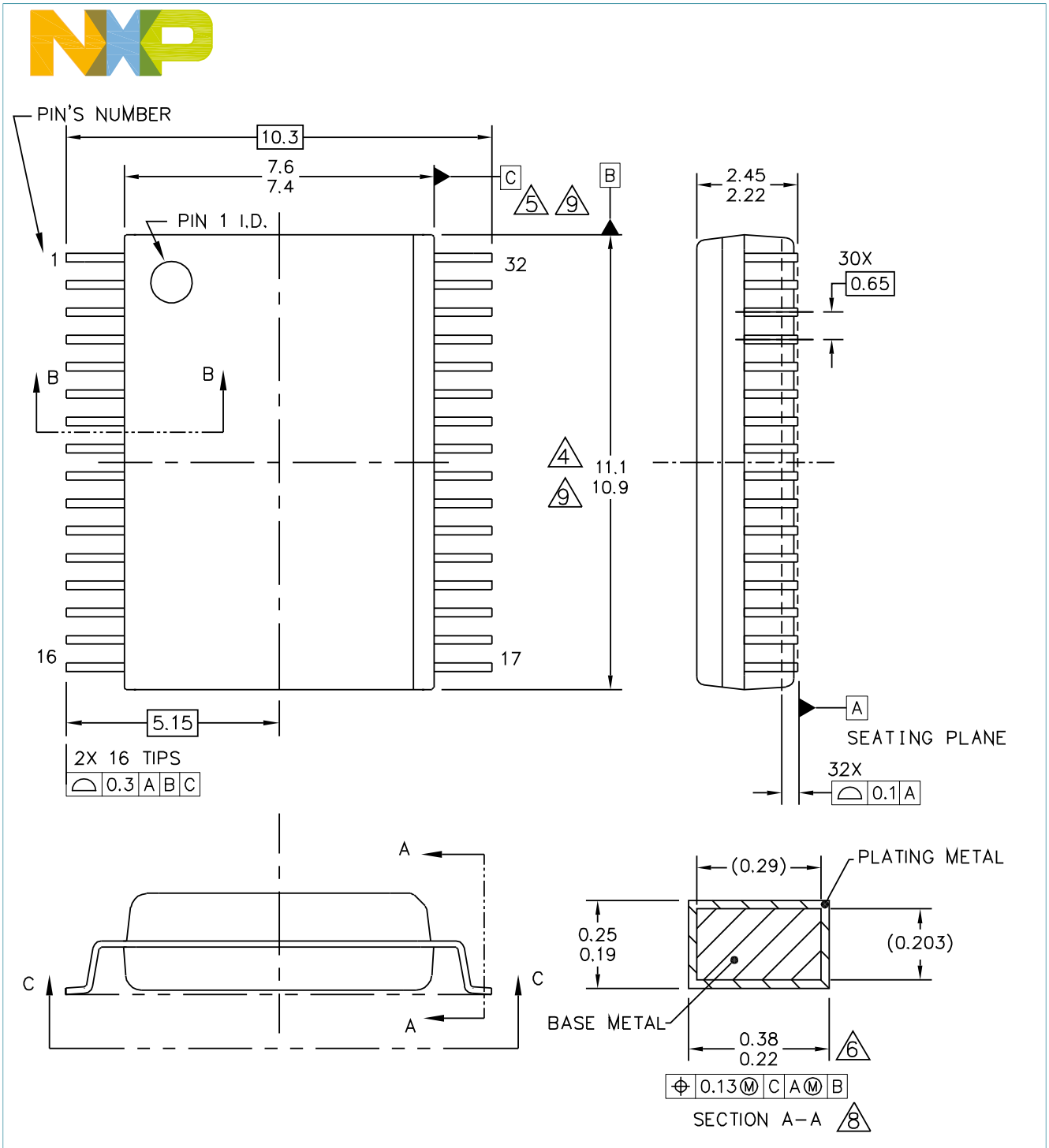
12 Packaging

12.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 30. Package outline

Package	Suffix	Package outline drawing number
32-pin SOICW-EP	EK	98ARL10543D
32-pin PQFN	FK	98ARL10579D
28-pin HVQFN	ES	98ASA00993D



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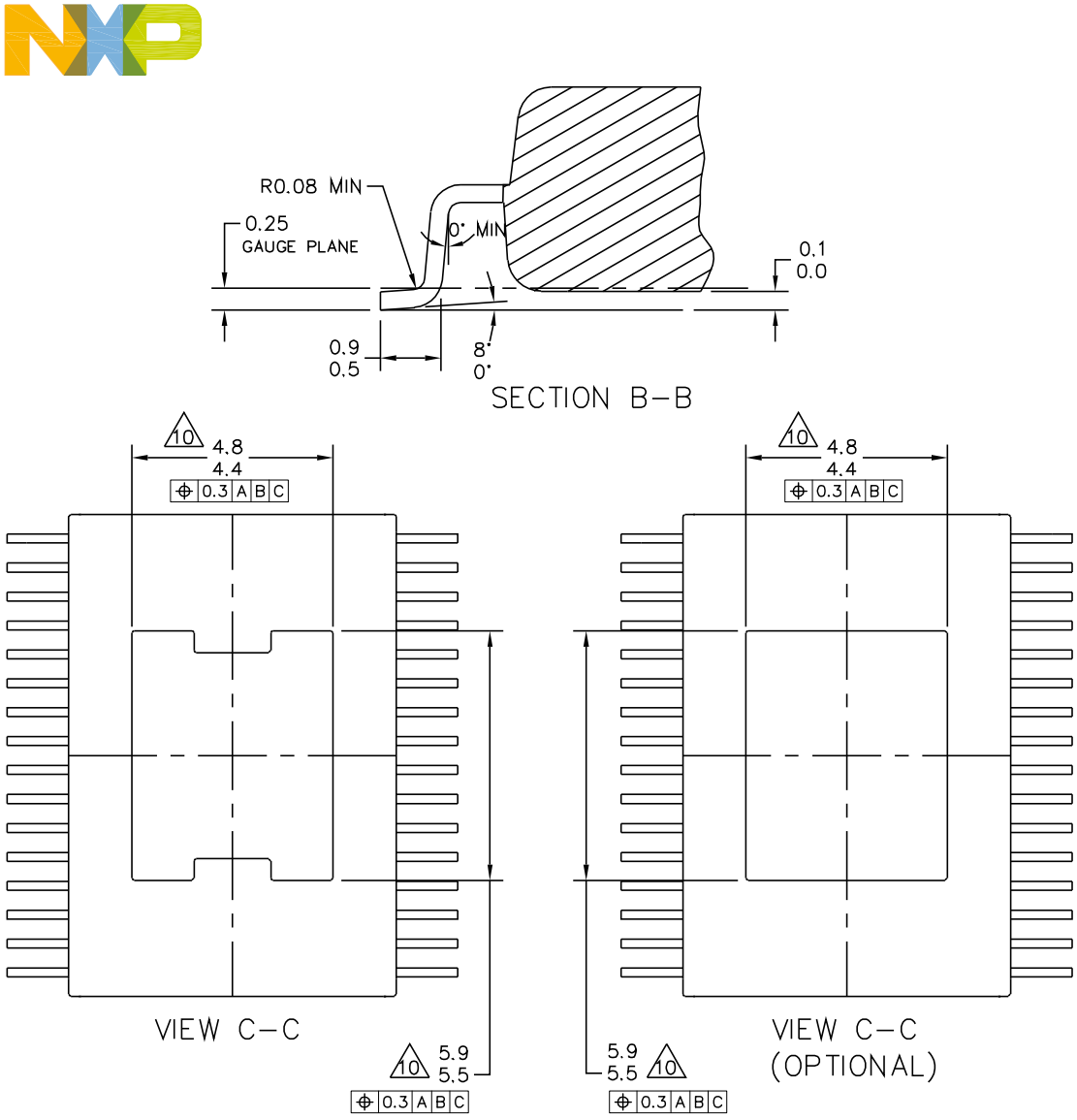
TITLE: 32LD SOIC W/B, 0.65 PITCH 5.7 X 4.6 EXPOSED PAD CASE OUTLINE	DOCUMENT NO: 98ARL10543D	REV: F
	STANDARD: NON-JEDEC	
	SOT1746-1	01 FEB 2016



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	STANDARD: NON-JEDEC	
	SOT1746-1	01 FEB 2016

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSIONS RANGES DEFINE THE PRIMARY KEEP–OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.9mm FROM MAXIMUM EXPOSED PAD SIZE

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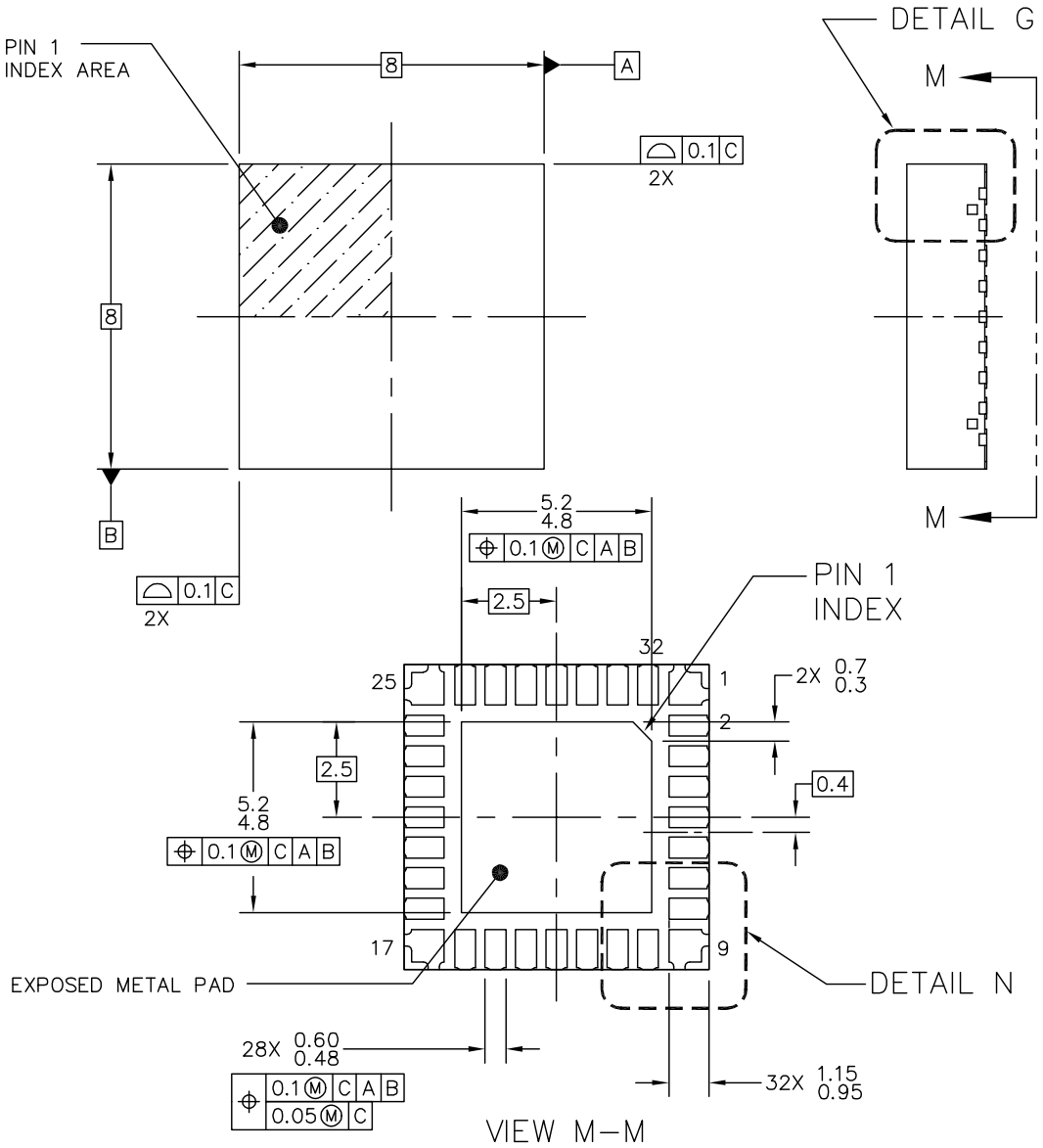
	STANDARD: NON–JEDEC	
	SOT1746–1	01 FEB 2016



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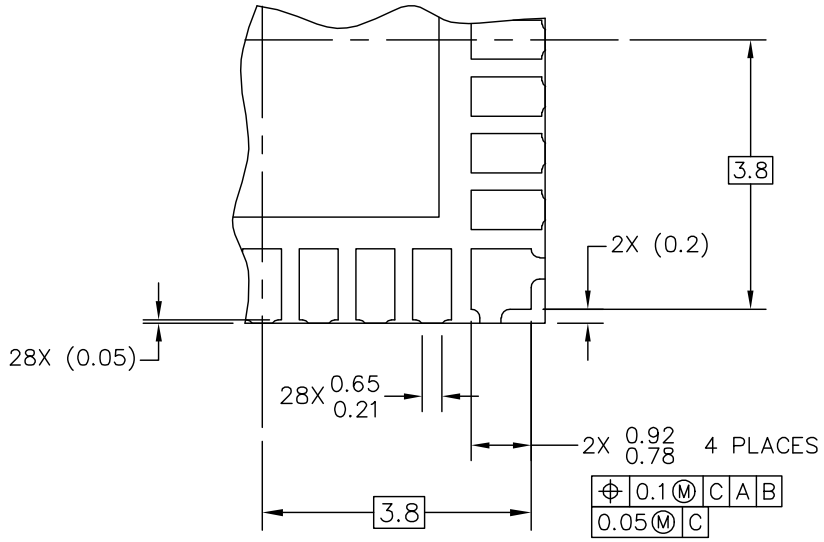
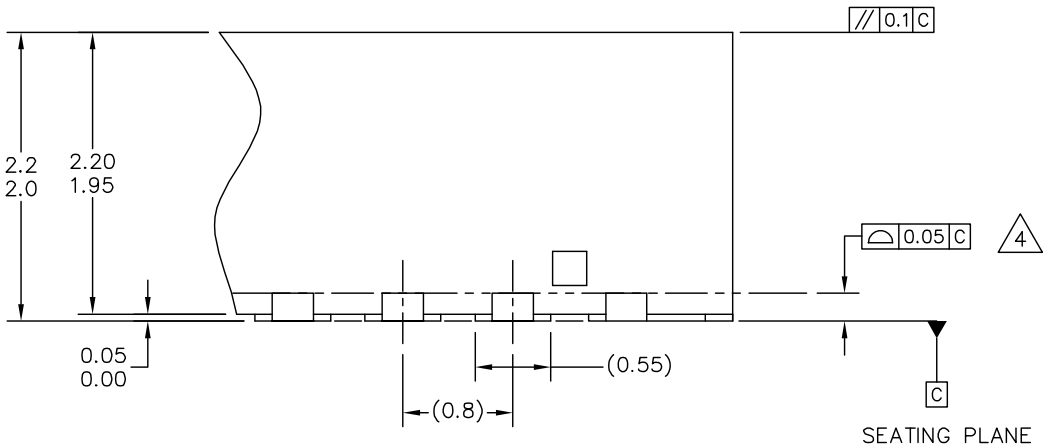
TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN), 32 TERMINAL, 0.8 PITCH(8X8X2.1)	DOCUMENT NO: 98ARL10579D	REV: C
	CASE NUMBER: 1536–04	31 OCT 2006
	STANDARD: JEDEC MO–251A ADDB–1	



DETAIL N
CORNER CONFIGURATION



DETAIL G
VIEW ROTATED 90° CW

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	CASE NUMBER: 1536–04	31 OCT 2006
	STANDARD: JEDEC MO–251A ADDB–1	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: F–PQFP–N.
4. COPLANARITY APPLIES TO LEADS AND CORNER LEADS.
5. MINIMUM METAL GAP SHOULD BE 0.25MM.

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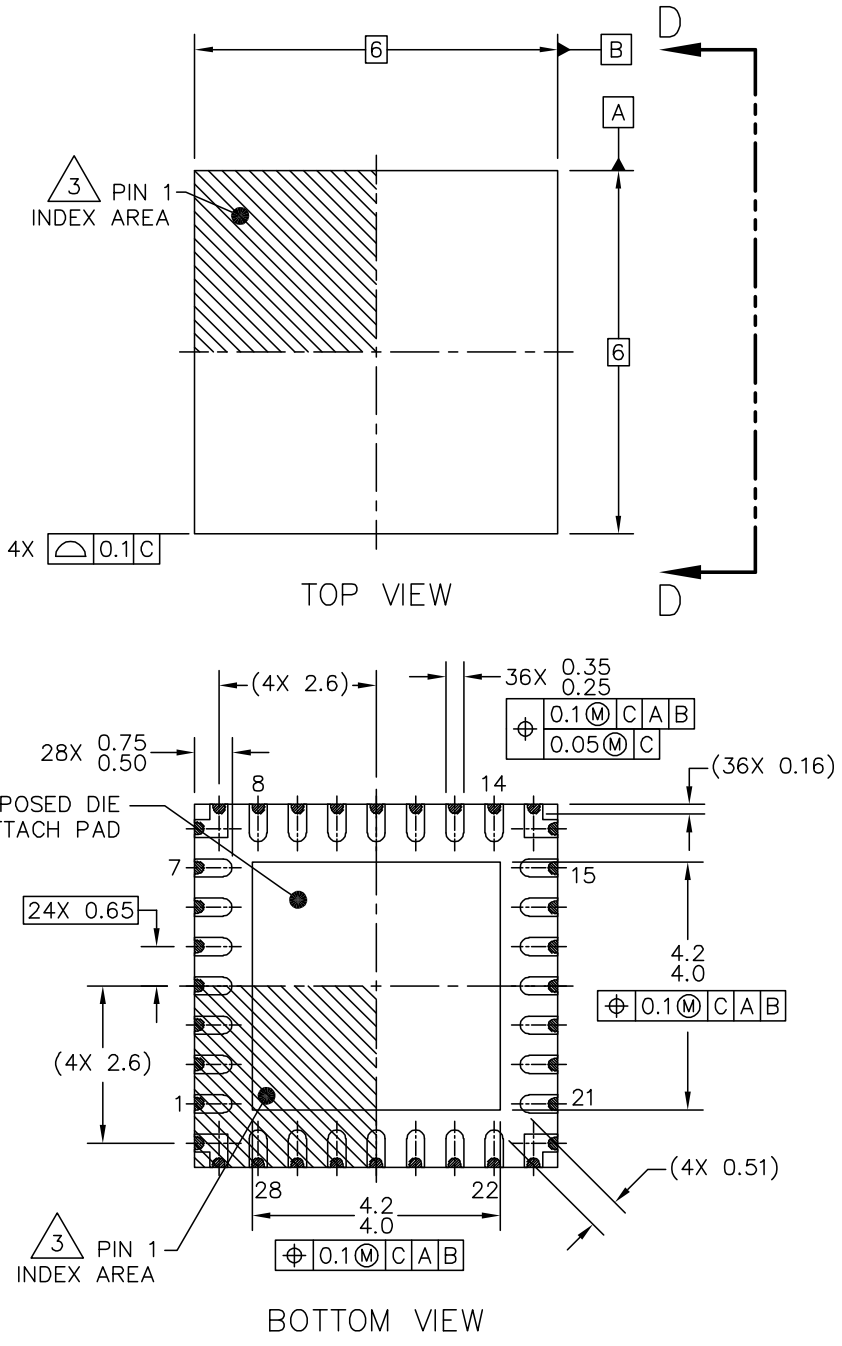
	CASE NUMBER: 1536–04	31 OCT 2006
	STANDARD: JEDEC MO–251A ADDB–1	

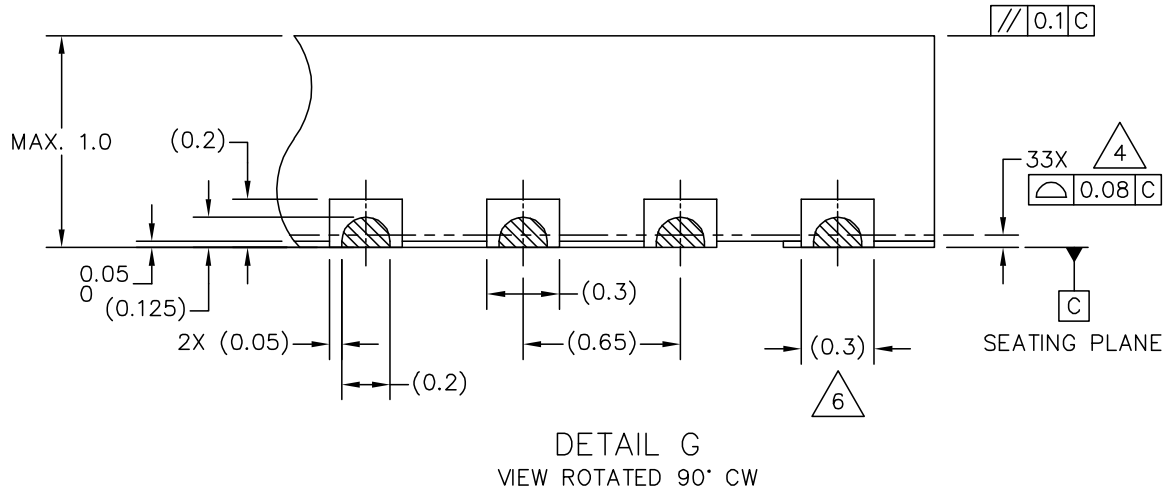
H–PQFN–28 I/O 0.125 DIMPLE WETTABLE FLANK
6 X 6 X 0.85 PKG, 0.65 PITCH

SOT788–3(DD)



H–PQFN–28 I/O 0.125 DIMPLE WETTABLE FLANK
6 X 6 X 0.85 PKG, 0.65 PITCH

SOT788–3(DD)



DETAIL G
VIEW ROTATED 90° CW

H–PQFN–28 I/O 0.125 DIMPLE WETTABLE FLANK
6 X 6 X 0.85 PKG, 0.65 PITCH

SOT788–3(DD)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE, SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP SHOULD BE 0.25 MM.
6. ANCHORING PADS.

13 Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MC33HB2002 v.3.0	20191018	Data sheet: advance information	—	MC33HB2002 v.2.0
Modifications	• Section 1 and Section 3: added AEC-Q100 grade 1 qualified • Section 7.1: updated Figure 5 • Table 4: added max value for T_{PPRT} • Table 4: updated thermal resistance and package dissipation ratings for MC33HB2002ES • Section 12.1: updated package outline drawing (98ASA00993D)			
MC33HB2002 v.2.0	20180604	Data sheet: advance information	—	MC33HB2002 v.1.0
Modifications	• Updated MC33HB2002ES thermal resistance and package dissipation ratings in Table 4			
MC33HB2002 v.1.0	20171009	Data sheet: product preview	—	—

14 Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
[short] Data sheet: product preview	Development	This document contains certain information on a product under development. NXP reserves the right to change or discontinue this product without notice.
[short] Data sheet: advance information	Qualification	This document contains information on a new product. Specifications and information herein are subject to change without notice.
[short] Data sheet: technical data	Production	This document contains the product specification. NXP Semiconductors reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Tables

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Date of release: 18 October 2019
Document identifier: MC33HB2002