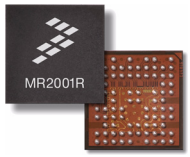
Document Number: MC33MR2001R
Rev. 5.0, 9/2016

76-77 GHz RF receiver front-end for W-band radar applications

MR2001R

ADVANCED DRIVER ASSISTANCE SYSTEM



VK SUFFIX (PB-FREE)
98ASA00540D
6.0 X 6.0 X 0.95 RCPBGA

The MR2001 is an expandable three package solution for automotive radar modules. The chipset consists of a VCO (voltage controlled oscillator), a two-channel Tx transmitter, and a three-channel Rx receiver. The MR2001R is a high performance, highly integrated, three-channel, receiver (RX) ideally suited for automotive radar applications. In conjunction with the MR2001V, a four-channel voltage controlled oscillator, and an MR2001T, a two-channel transmitter, it provides an expandable three package solution for automotive radar modules.

The chips are connected together via the LO signal around 38 GHz. The individual control of each chip is realized by SPI. The main controller and modulation master is a single microprocessor (MCU) with integrated high-speed analog to digital converters (ADC) and appropriate signal processing capability such as fast fourier transforms.

The front-end solution is specifically architected to be controlled by NXP's Qorivva MPC5775 MCU. Especially the baseband functionality (high-pass filters, variable gain amplifiers, anti-aliasing filters) on the receiver chips has been designed to work with the MPC5775 MCU.

Features

- Scalable to 4 TX channels and 12 RX channels
- Advanced packaging technology
- High performance supports fast modulation with simultaneous active channels
- Excellent spatial resolution and detection accuracy
- Local oscillator at 38 GHz to lower the distribution loss and reduce impact on antenna pattern
- Best phase noise < -75 dBc/Hz at 100 kHz offset
- Low power consumption of 2.5 W for the total transceiver
- Integrated system level calibration when combined with Qorivva MPC577xK MCU
- Compatible with all leading MCUs
- Optimized for the NXP Qorivva MPC577xK MCU
- Scalable approach to support SRR, MRR and LRR applications
- Reduced number of external components due to higher integration level
- Baseband integration on receiver suitable to work with the MPC577xK Qorivva MCU
- Bi-phase modulator on the transmitter chip

Applications

- Automotive proximity radar
- LRR, MRR and SRR
- ADAS
- Industrial surveillance and security systems

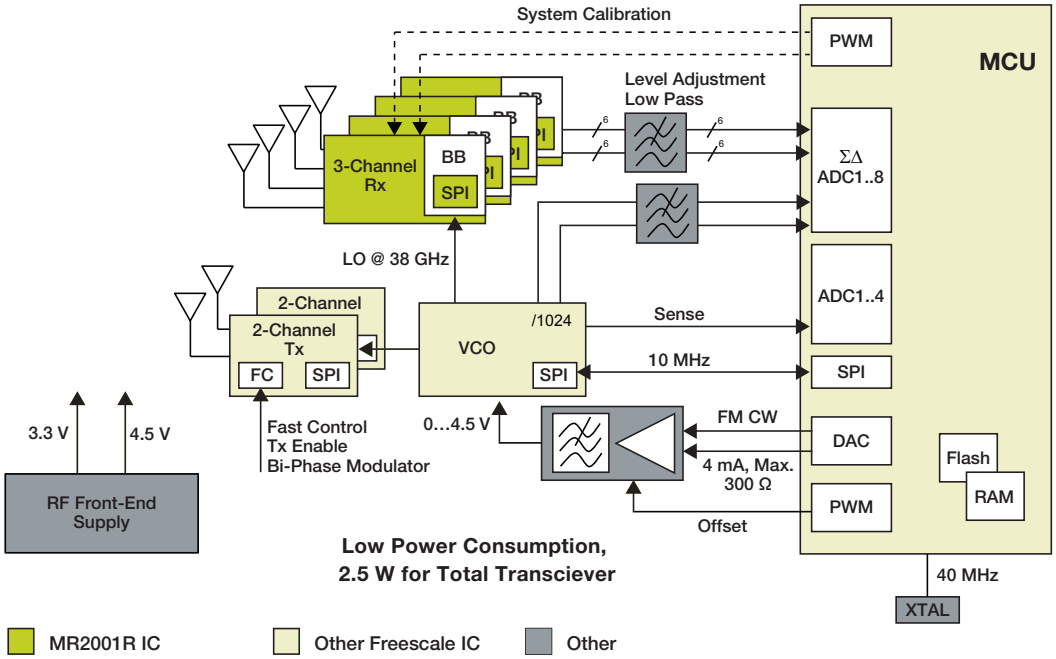


Figure 1. MR2001R simplified application diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table of Contents

1 Orderable parts

Table 1. Orderable part variations

Part number	Temperature (temp)	Package	Notes
MC33MR2001RVK	-40 °C to 125 °C	6.0 x 6.0 mm RCP (10 x 11 array) 0.5 mm pitch	(1) (2)

Notes

1. To order parts in tape & reel, add R2 to the suffix of the part number.
2. The device is packaged inside a 6.0 mm x 6.0 mm RCP with 10 x 11 solder balls. The pitch of the solder balls is 0.5 mm.

2 Internal block diagram

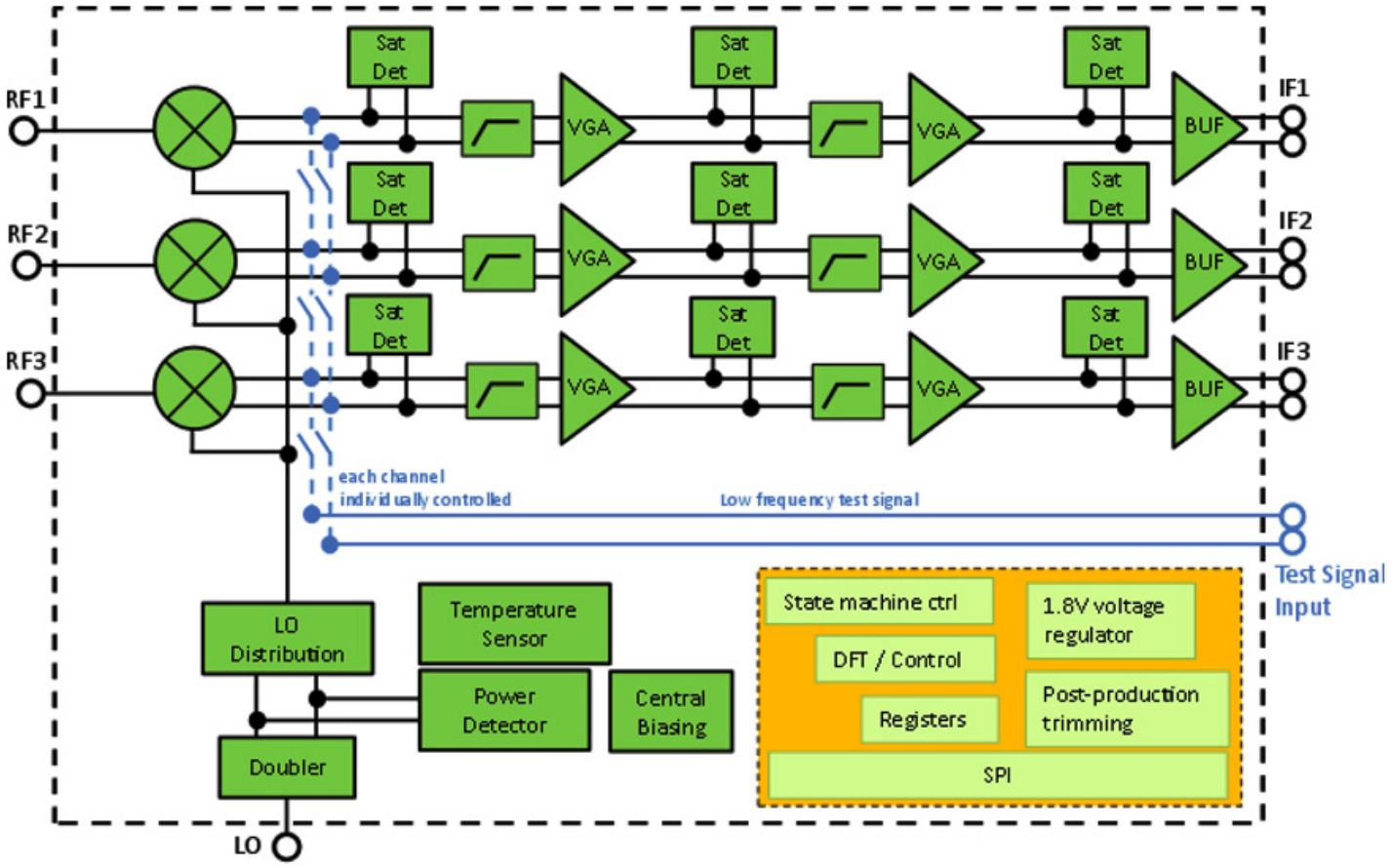


Figure 2. MR2001R three-channel receiver block diagram

3 Pin connections

3.1 Pinout diagram

The layout and arrangement of the signal pads are shown in Figure 3.

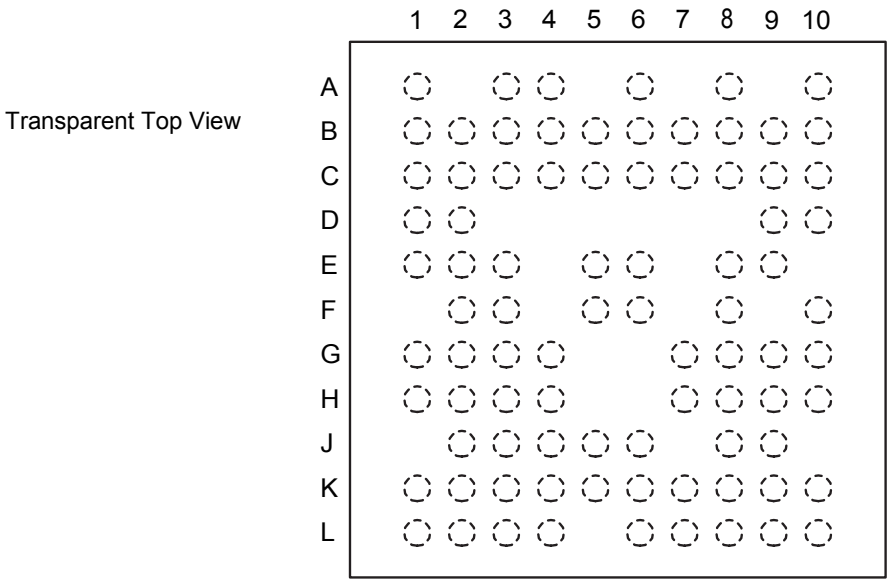


Figure 3. Pinout (ball) diagram

3.2 Pin definitions (ball)

A functional description of each pin for the MR2001R can be found in Table 2. Equivalent I/O schematics is found in Table 3

Table 2. MR2001R pin definitions

Ball location	Pin name	Pin function	Pin type	Level	Description
A1, A10, D1, D2, E8, F5, F6, F8, G4, G7, G8, G9, G10, H4, H7, K7, L1, L2, L3, L7, L8, L9, L10	GND [4]	DC Ground	Power	0.0 V	
A3	MOSI	SPI MOSI (master out, slave in)	Digital Input	0 to 3.3 V	
A4	RSETB	Digital hard reset signal	Digital Input	0 to 3.3 V	
A6	IF1	Differential IF output channel 1	Analog Output	0 to 3.3 V	
A8	IF3x	Differential IF output channel 3	Analog Output	0 to 3.3 V	
B1	SEB	SPI enable (chip enable)	Digital Input	0 to 3.3 V	
B2	SCLK	SPI serial clock	Digital Input	0 to 3.3 V	
B3	MISO	SPI MISO (master in, slave out)	Digital Output	0 to 3.3 V	
B4	SCANB	Digital scan test	Digital Input	0 to 3.3 V	
B5	IF2	Differential IF output channel 2	Analog Output	0 to 3.3 V	

Table 2. MR2001R pin definitions (continued)

Ball location	Pin name	Pin function	Pin type	Level	Description
B6	IF2x	Differential IF output channel 2	Analog Output	0 to 3.3 V	
B7	IF1x	Differential IF output channel 1	Analog Output	0 to 3.3 V	
B8	IF3	Differential IF output channel 3	Analog Output	0 to 3.3 V	
B9	TIN	IQ or differential test signal inputs	Analog Input Analog Input	0 to 3.3 V	
B10	TINx	IQ or differential test signal inputs	Analog Input	0 to 3.3 V	
C1, C2	VCC3 (3)	3.3 V Power Supply	Power	3.3 V	
C6	VCC2 (3)	3.3 V Power Supply	Power	3.3 V	
C8	VCC1 (3)	3.3 V Power Supply	Power	3.3 V	
D9	SENS	Sensor output (temperature and power peak detector)	Analog output	0 to 3.3 V	
D10	RP	Bandgap reference resistor (positive temperature slope)	Analog Input	0 to 3.3 V	See Table 6
E1, E2, E3, F3, G1, G2, G3, H1, H2, H3, H8, H9, H10, J3, J4, J5, J6, J8, K1, K2, K3, K4, K6, K8, K9, K10, L4, L6	GND1 (4)	RF Ground	Power	0.0 V	
E5	ADR1	Chip key Bit [1]	Digital Input	0 to 3.3 V	
E6	ADR0	Chip key bit [0]	Digital Input	0 to 3.3 V	
E9	SD	Saturation detector output	Analog output	0 to 3.3 V	
F2	RX2	77 GHz RX input channel 2	RF Input	0.0 V	
F10	RN	Bandgap reference resistor (negative temperature slope)	Analog Input	0 to 3.3 V	See Table 6
J2	RX1	77 GHz RX input channel 1	RF Input	0.0 V	
J9	RX3	77 GHz RX input channel 3	RF Input	0.0 V	
K5	LO	38 GHz LO input	RF Input	0.0 V	

Notes

3. VCC1, VCC2, VCC3 are only connected via the on-chip metal layers. It is mandatory for each supply domain to be connected to the common power supply.
4. GND and GND1 are connected together in the package via the interconnection layer. GND1 is mandatory to be connected, to realize a suitable RF PCB to package transition.

3.3 Equivalent schematics

Table 3. Equivalent I/O schematics for pin descriptions

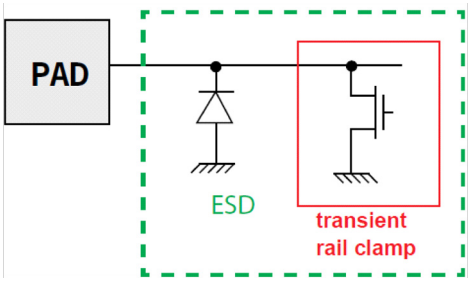
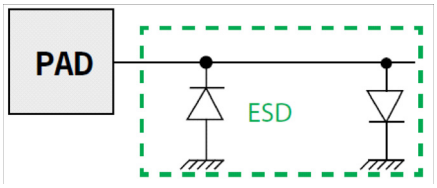
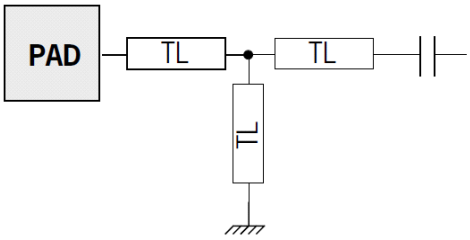
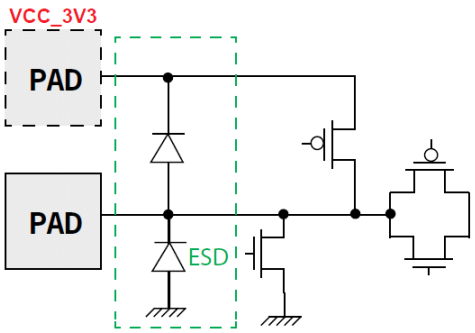
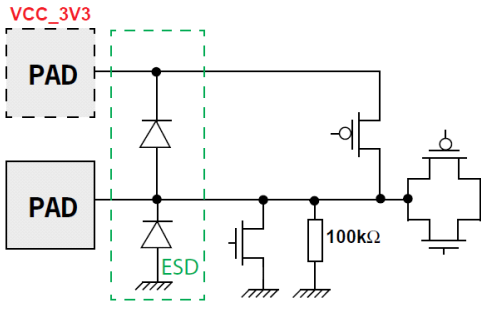
Ball location	Pin function	Equivalent I/O schematic
C1, C2, C6, C8	3.3V Power Supply	
E1, E2, E3, F3, G1, G2, G3, H1, H2, H3, H8, H9, H10, J3, J4, J5, J6, J8, K1, K2, K3, K4, K6, K8, K9, K10, L4, L6	RF Ground	
A1, A10, D1, D2, E8, F5, F6, F8, G4, G7, G8, G9, G10, H4, H7, K7, L1, L2, L3, L7, L8, L9, L10	DC Ground	
K5,	38 GHz LO input	
J3	77 GHz RX input channel 1	
F3	77 GHz RX input channel 2	
J9	77 GHz RX input channel 3	
B3	SPI MISO (master in, slave out)	
A3	SPI MOSI (master out, slave in)	
B2	SPI serial clock	

Table 3. Equivalent I/O schematics for pin descriptions

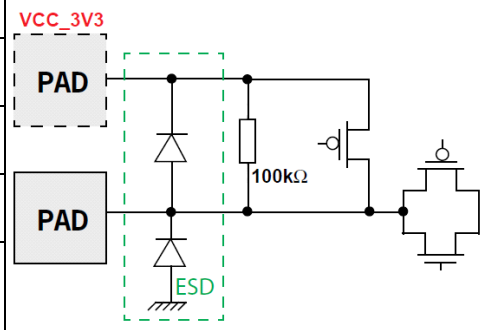
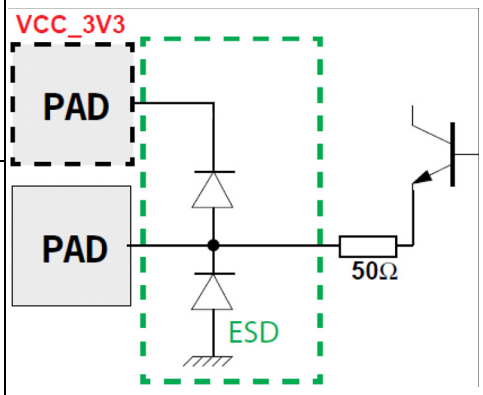
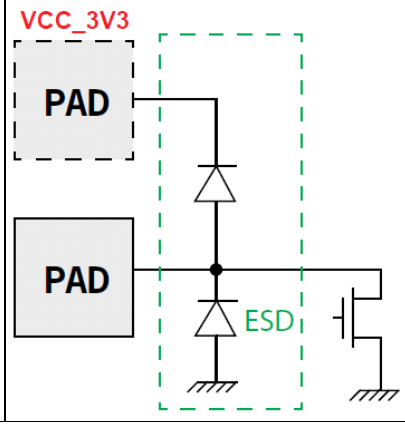
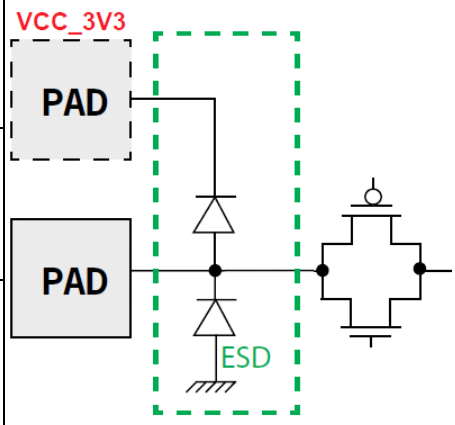
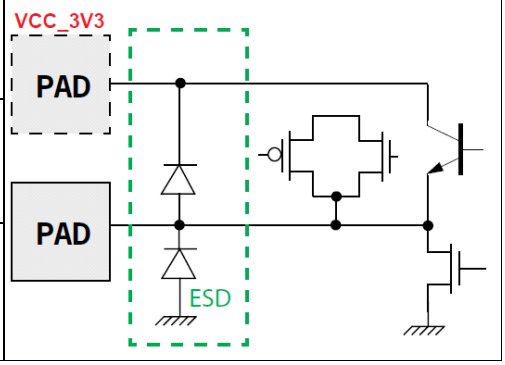
Ball location	Pin function	Equivalent I/O schematic
A4	Digital hard reset signal	
B1	SPI enable (chip enable)	
E5	Chip key Bit [1]	
E6	Chip key bit [0]	
B4	Digital scan test	
F10	Bandgap reference resistor (negative temperature slope)	
D10	Bandgap reference resistor (positive temperature slope)	
E9	Saturation detector output	

Table 3. Equivalent I/O schematics for pin descriptions

Ball location	Pin function	Equivalent I/O schematic
D9	Sensor output (temperature and power peak detector)	
B9	IQ or differential test signal inputs	
B10	IQ or differential test signal inputs	
A8, B8	Differential IF output channel 3	
B5, B6	Differential IF output channel 2	
A6, B7	Differential IF output channel 1	

4 General product characteristics

4.1 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Min.	Max.	Unit	Notes
V_{STATIC_MAX}	Supply Voltage (static)	-0.30	3.63	V	
V_{DYN_MAX}	Supply Voltage (dynamic) • allowed < 10% of product total lifetime	-0.30	4.00	V	
V_{DIG_MAX}	Digital Supply Voltage (static, dynamic)	-0.30	3.63	V	
V_{IN_MAX}	Voltage Applied to All Used I/O Pins	-0.30	3.63	V	
ESD					
ESD_HBM	ESD for Human Body Model (HBM) Digital I/O, Analog, RF	-2000	2000	V	
ESD_MM	ESD for Machine Model (MM)	-200	200	V	
R1	HBM Circuit Description I	–	±1500	W	
C	HBM Circuit Description II	–	±100	pF	
	ESD for human body model (HBM) digital I/O	-1000	1000	V	
	ESD HBM, RF I/O	-100	100	V	

4.2 General operating conditions

Table 5. General operation conditions

Temp = -40 °C to +125 °C, f_{OUT} = 76 to 77 GHz, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
dpack	Package Thickness (mounted condition)	–	950	1200	µm	
Temp	Ambient Package Temperature	-40	27	125	°C	
LU	Latch Up (LU) for DC and Bias Pads • Pulsed current injection method	-100	–	+100	mA	
Pitch	BGA Pitch	–	500	–	µm	
dchip	Chip Thickness	113	—	143	µm	
St_temp	Storage Temperature	-55	—	150	°C	
I_{PAD_MAX}	Pad withstanding	—	—	150	mA	
Number of pulses per pad						
	Positive pulses (HBM)	—	—	1		
	Negative Pulses (HBM)	—	—	1		
	Interval of Pulses	—	—	1	s	

5 General IC function description and application information

5.1 Introduction

NXP provides a total system solution with next-generation embedded radar-based products that include the Qorivva MPC577xK MCU and 77 GHz packaged radar front-end chipset for both low- and high-end radar modules. This pairing delivers a complete embedded radar system for automotive designs. Our total solution advances automotive safety by enabling vehicles to sense potential crash situations. This radar solution provides long- and mid-range functionality, allowing automotive systems to monitor the environment around the vehicle to help prevent crashes.

A typical radar module consists of a transmit solution (Tx), VCO and three-channel receiver IC (Rx), along with an MCU. The chips are connected via the local oscillator signal, around 38 GHz. The individual control of each chip is implemented by a serial peripheral interface (SPI) bus. The main controller and modulation master is a single MCU with integrated high-speed analog-to-digital converters (ADCs) and appropriate signal processing capability, such as fast Fourier transforms (FFTs).

5.1.1 Features

- 76 GHz to 77 GHz RX input and 38 GHz to 38.5 GHz LO input
- Supply voltage 3.3 V ±5.0%
- Supply current typ. 240 mA
- Power dissipation typ. 0.8 W
- Baseband suitable for Qorivva MPC577xK MCU (5.0 MHz)
- On-chip baseband test concept
- Linearity > -5.0 dBm
- Conversion gain 23 dB to 60 dB at 4.0 MHz
- SSB noise figure typical 14 dB
- Saturation detectors
- Tri-state IF outputs

5.2 Electrical characteristics

5.2.1 Receiver Rx

Table 6. Interface levels

Temp = -40 °C to +125 °C, f_{OUT} = 76 to 77 GHz, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{CC}	Supply Voltage • Nominal supply ±5% variation	3.135	3.3	3.465	V	
I_{CC}	Supply Current (all channels on)	175	242	288	mA	
I_{CC0}	Supply Current S0 (chip de-activated)	–	19	30	mA	
P_{ON}	Power Consumption (on)	–	0.8	1.0	W	
Frequency and # of channels						
n_Rx	Number of Channels	–	–	3.0	–	
F_{REQ_RF}	RF Range	76	76.5	77	GHz	
F_{REQ_LO}	LO Range	38	38.25	38.5	GHz	
Thermal parameters						
R_{TH}	Thermal Resistance	–	15	22	°C/W	

Table 6. Interface levels

Temp = -40 °C to +125 °C, f_{OUT} = 76 to 77 GHz, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Control						
SPI	SPI Functionality - 10 MHz clock required		Yes			
RF, LO return loss						
G_LO	LO-port Return Loss (50 Ω)	10	–	–	dB	
G_RF	RF-port Return Loss (50 Ω)	10	–	–	dB	(5)
LO input power						
P_LO	LO Input Power - single-ended configuration	-11	–	0.0	dBm	
BB parameters						
IF_BW	IF Bandwidth - output DC coupled, information only	0.0	–	5.0	MHz	
IF_COUP	IF Coupling		DC		–	
f_{HP}	High-pass (HP) Filter Edge Frequency (-6.0 dB)	240	300	360	kHz	
s_{HP}	Slope Below f_HP	–	40	–	dB/decade	
LP_order	Low Pass Filter (LP) Order - center freq. at approx. 8.0 MHz - information only	–	1.0	–	–	
LP_freq	Low Pass Filter (LP) Edge Frequency - 1.0 dB attenuation at 5.0 MHz, LP 1st order	5.0	–	–	MHz	
Conversion gain						
CG_{MAX}	Max. Conversion Gain at f = 4.0 MHz - 22 dB 1st VGA, 16 dB 2nd VGA	50	57	61	dB	
CG_{MIN}	Min. Conversion Gain at f = 4.0 MHz - 10 dB 1st VGA, -2.0 dB 2nd VGA	20	26.5	32	dB	
CG_{STEP}	Conversion Gain Step-size (VGA settings)	4.5	5.5	6.5	dB	
CG_VS_FREQ	Conversion Gain Max. Difference (76 GHz to 77 GHz range) • 27 °C and 125 °C • -40 °C	 0.0 0.0	 – –	 1.5 2.0	dB	
CG_RIPPLE	Conversion Gain Frequency Slope - not measured in production in the frequency range from 76 GHz to 77 GHz, only smooth transition allowed	–	–	0.2	dB/ 100 MHz	
IF_LOAD_R	IF Load Impedance (single-ended) - IF output is differential and DC coupled, RaceRunner has 6.0 kΩ input impedance. AC coupling of load is required. Support of 200, 500 Ω controllable via the SPI.	200	–	–	W	
IF_LOAD_C	IF Load Capacity (single-ended) - parasitic cap due to PCB	–	–	30	pF	
AM_REJ	LO AM Noise Rejection Modulation Index = 10%, f = 200 k up to 5.0 M, 200 k steps GA1 = tbd, VGA 2 = tbd - Suppression = PIF - PAM, LO	40	–	–	dB	
PH_CH2CH	Phase Variation From Channel-to-Channel - cannot be verified by NXP measurements, will be measured in system and guaranteed by design.	–	–	3.0	degree	
CG_CH2CH	Conversion Gain Variation From Channel-to-Channel - cannot be verified by NXP measurements, will be measured in system and guaranteed by design	–	–	1.0	dB	
ICG_CH2CH	Initial Conversion Gain Variation From Channel-to-Channel - static variation of gain; std. condition	–	–	2.0	dB	

Notes

5. Referenced after matching structure on board; see Figure 24.

Table 6. Interface levels

Temp = -40 °C to +125 °C, f_{OUT} = 76 to 77 GHz, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Spurious						
PRES_38G	LO/RF (38 GHz) Residual Power at RF Input	–	–	-45	dBm	
PRES_76G	LO/RF (76 GHz) Residual Power at RF Input	–	-18	-10	dBm	
Linearity						
P-1DB_AT 10KHZ	Input referred 1 dB compression point at CG = min, at f = 10 kHz	-5.0	–	–	dBm	
P-1dB_AT 4MHz	Input referred 1 dB compression point at CG = min, at f = 4.0 MHz	-28	–	–	dBm	
P-1dB_AT 4MHz	Input referred 1 dB compression point at G = max, at f = 4.0 MHz	-54	–	–	dBm	
Intermodulation (multiple of 10 kHz are generally ignored)						
Set-up definition for specs RX35A to RX35F, f_{LO} = 38.25 GHz (-10 dBm)						
f1 = 2 x f_{LO} + 10 kHz (-10 dBm)						
f2 = 2 x f_{LO} + 100 kHz (-36 dBm)						
f3 = 2 x f_{LO} + 125 kHz (-36 dBm)						
VGA1 = 16 dB						
VGA2 = 10 dB						
IM_LOW_1	PIF at 100 kHz - max. (PIF mixing products) excluded are separately specified intermodulation products	40	–	–	dB	
IM_LOW_2	PIF at 125 kHz - max. (PIF mixing products) excluded are separately specified intermodulation products	40	–	–	dB	
IM_LOW_2	PIF at 100 kHz - PIF at 90 kHz and PIF at 125 kHz - PIF at 115 kHz	30	–	–	dB	
IM_LOW_3	PIF at 100 kHz - PIF at 110 kHz and PIF at 125 kHz - PIF at 135 kHz	30	–	–	dB	
IM_LOW_4	PIF at 100 kHz - PIF at 80 kHz and PIF at 125 kHz - PIF at 105 kHz	30	–	–	dB	
IM_LOW_5	PIF at 100 kHz - PIF at 120 kHz and PIF at 125 kHz - PIF at 145 kHz	30	–	–	dB	
Intermodulation (multiple of 10 kHz are generally ignored)						
Set-up definition for specs RX37A to RX37F, f_{LO} = 38.25 GHz (-10 dBm)						
f1 = 2 x f_{LO} + 10 kHz (-10 dBm)						
f2 = 2 x f_{LO} + 1.0 MHz (-66 dBm)						
f3 = 2 x f_{LO} + 1.1 MHz (-66 dBm)						
VGA1 = 16 dB						
VGA2 = 16 dB						
IM_HIGH_1	PIF at 1.0 MHz - max. (PIF mixing products) excluded are separately specified intermodulation products	55	–	–	dB	
IM_HIGH_2	PIF at 1.1 MHz - max. (PIF mixing products) excluded are separately specified intermodulation products	55	–	–	dB	
IM_HIGH_2	PIF at 1.0 MHz - PIF at (1.0 MHz - 10 kHz) and PIF at 1.1 MHz - PIF at (1.1 MHz - 10 kHz)	30	–	–	dB	
IM_HIGH_3	PIF at 1.0 MHz - PIF at (1.0 MHz + 10 kHz) and PIF at 1.0 MHz - PIF at (1.1 MHz + 10 kHz)	30	–	–	dB	
IM_HIGH_4	PIF at 1.0 MHz - PIF at (1.0 MHz - 20 kHz) and PIF at 1.0 MHz - PIF at (1.1 MHz - 20 kHz)	30	–	–	dB	
IM_HIGH_5	PIF at 1.0 MHz - PIF at (1.0 MHz + 20 kHz) and PIF at 1.0 MHz - PIF at (1.1 MHz + 20 kHz)	30	–	–	dB	
OIP3	Coupled Output Intermodulation	4.0	–	–	dBV	

Table 6. Interface levels

Temp = -40 °C to +125 °C, f_{OUT} = 76 to 77 GHz, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Noise figure						
NFSSB_50K	Single-side Band Noise Figure at 50 kHz - max. gain	–	–	42	dB	
NFSSB_200K	Single-side Band Noise Figure at 200 kHz - max. gain	–	–	24	dB	
NFSSB_1M	Single-side Band Noise Figure at 1.0 MHz - max. gain	–	–	16	dB	
NFSSB_5M	Single-side Band Noise Figure at 5.0 MHz - max. gain	–	–	16	dB	
Isolation						
IF_ISO	Channel-to-Channel IF Isolation	30	–	–	dB	
Peak detector						
$V_{DET\_RX\_RANGE}$	Peak Detector Output Voltage Range - two sequential readings required	0.0	–	V_{CC}	V	
V_{DET_RX}	Peak Detector Threshold Voltage - two sequential readings required. V_Det_Rx > min. value guarantees functionality of Rx • at -40 ° • at 27 °C • at 125 °C	 400 350 250	 – – –	 – – –	mV	
Control						
RX_CH_DIS	Ch. enable/disable functionality (each ch. individually) if all ch. are disabled additionally the doubler is disabled - IF output must show high-impedance if ch. disabled	via SPI				
SEN_IMP_DIS	Sensor, IF high output impedance at disabled condition (LO peak detector, temp. sensor, overflow signal detector) - If corresponding sensor is disabled the output should show high-impedance	Yes				
OVERLOAD	Overload indicator - located after mixer core, and after 1st and 2nd gain stage, dedicated pin. And external resistor of 365 Ω to V_{CC} is required	Yes				
R_{SAT}	Overload Detected Output Load	361	365	370	W	
V_{LOW}	Overload Detected Voltage Level	0.0	–	0.8	V	
V_{HIGH}	Overload Not Detected Voltage Level	2.0	–	3.3	V	
$t_{OVERLOAD}$	Overload Signal Indicating Compression Detection Time	–	–	4.0	ns	
P_MIXER_SAT	Input Referred Saturation Detector Threshold at CG = min at f = 10 kHz	–	-3.0	–	dBm	
V_{VGA1_SAT}	1st VGA Stage Output Saturation Level (stage directly after mixer core)	–	400	–	mVpk	
P_CGMIN_SAT	Input Referred Saturation Detector Threshold at CG = min at f = 4.0 MHz	–	–	-15	dBm	
V_{VGA2_SAT}	2nd VGA Stage Output Saturation Level	–	350	–	mVpk	
P_CGMAX_SAT	Input Referred Saturation Detector Threshold at CG = max at f = 4.0 MHz	–	–	-40	dBm	
RX_TEST	RX On-chip Test Concept: test signal applied after mixer, and measured on IF output Baseband test signal can be applied on each individual channel, and measured on the corresponding IF output. Concept controlled via SPI.	Yes				
SENSE	Multiplexed sensor pin	power detector, diff. temp sensor				

Table 6. Interface levels

Temp = -40 °C to +125 °C, f_{OUT} = 76 to 77 GHz, and V_{CC3P3} = 3.3 V ±5.0%, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Sensor output						
S_IMP_DIS	Sensor High Output Impedance (temp. sensor) - If the corresponding sensor is disabled, the output should show high-impedance		Yes			
R_{S_LOAD}	Sensor Load Resistance - to ground (temp, peak detector)	90	100	110	kΩ	
C_{S_LOAD}	Sensor Load Capacity - to ground (temp, peak detector)	–	–	30	pF	
Temperature sensor						
T_SLOPE	Temperature Sensor Sensitivity - two sequential readings required	–	0.55	–	mV/K	
T_SLOPE_VAR	Temperature Sensor Tolerance - deviation from mean slope (T_slope) over-temperature, max. precision at high temp requested	-5.0	0.0	5.0	K	
V_{T_RANGE}	Temperature Sensor Output Voltage Range - max. value achieved at 150 °C	0.4	–	3.0	V	
Rx test signal						
TS_CONF	Test Signal Configuration - balanced for BB test		2 x signals, single-ended, DC-coupled			
$T_{S\_FREQUENCY}$	Test Signal Input Frequency Range	0.0	–	5.0	MHz	
V_{TS_LEVEL}	Test Signal Input Level	–	1.0	–	V	
External resistors for biasing						
R_P	External Resistor 1 - E96, ±1.0%, TK = ±100 ppm/K, SMD, 0402 or smaller, 50 µA current	–	2.15	–	kΩ	
R_N	External resistor 2 - E96, ±1.0%, TK = ±100 ppm/K, SMD, 0402 or smaller, 50 µA current	–	14.7	–	kΩ	
Start-up time						
t_S	Start-up time - S0 to S1 time to guarantee specifications	–	–	50	µs	

6 Functional block requirements and behaviors

NXP millimeter wave and radar products enable advanced, high-performance, multi-channel systems for use in automotive radar, automotive advanced driver assistance systems (ADAS), automotive safety systems and other high-performance communication infrastructure and industrial systems.

The MR2001 is a high-performance 77 GHz radar transceiver chipset scalable for multi-channel operation enabling a single radar platform with electronic beam steering and wide field of view to support long-range radar (LRR), mid-range radar (MRR) and short-range radar (SRR) applications. This new radar chipset consists of a VCO (MR2001VC), a two-channel Tx transmitter (MR2001TX) and a three-channel Rx receiver (MR2001RX). This 77 GHz radar transceiver chipset is compatible with all leading MCUs, including the Qorivva MPC577xK MCU.

The MR2001 radar chipset is designed to support fast modulation with simultaneous active channels, enabling excellent spatial resolution and detection accuracy across a wide field of view. It supports a large variety of chirps in open loop VCO radar system architectures and consumes minimal power. An integrated BB filter and VGA saves on the total bill of materials. The MR2001 radar chipset uses advanced packaging technology to ensure the highest performance and minimum signal interference on the printed circuit board (PCB).

6.1 SPI communication

6.1.1 SPI interface

SPI read and write are illustrated in Figure 4 and Figure 5. Figure 6 shows the SPI read/write operation to ASCAN.

a[5:0] is the SPI address to be written, as shown in the memory map.

d[7:2] is the data that is written to, or read from this address.Bit [1:0] are reserved.

rwb is the read write bit. Read is done when rwb is ‘1’, write is done when rwb is ‘0’.

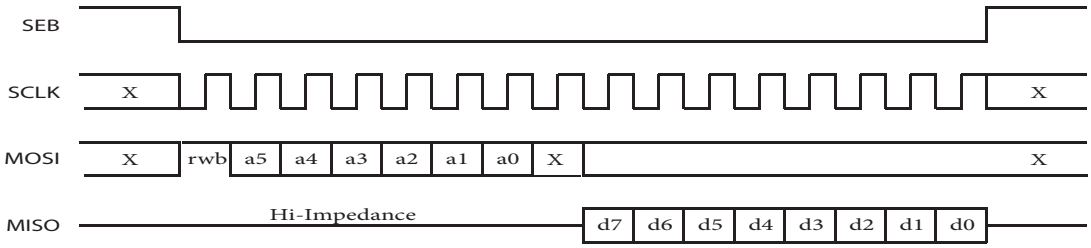


Figure 4. SPI read from internal registers

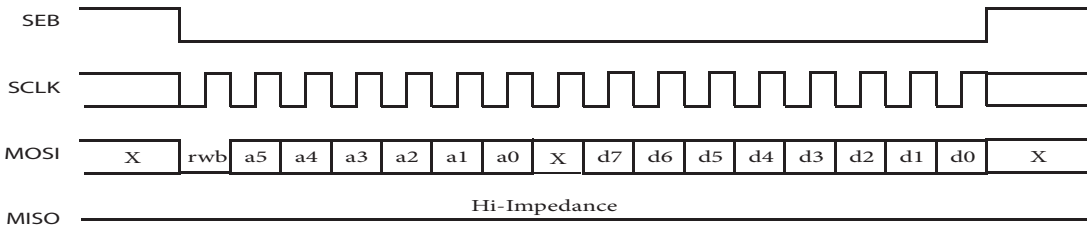


Figure 5. SPI write to internal registers

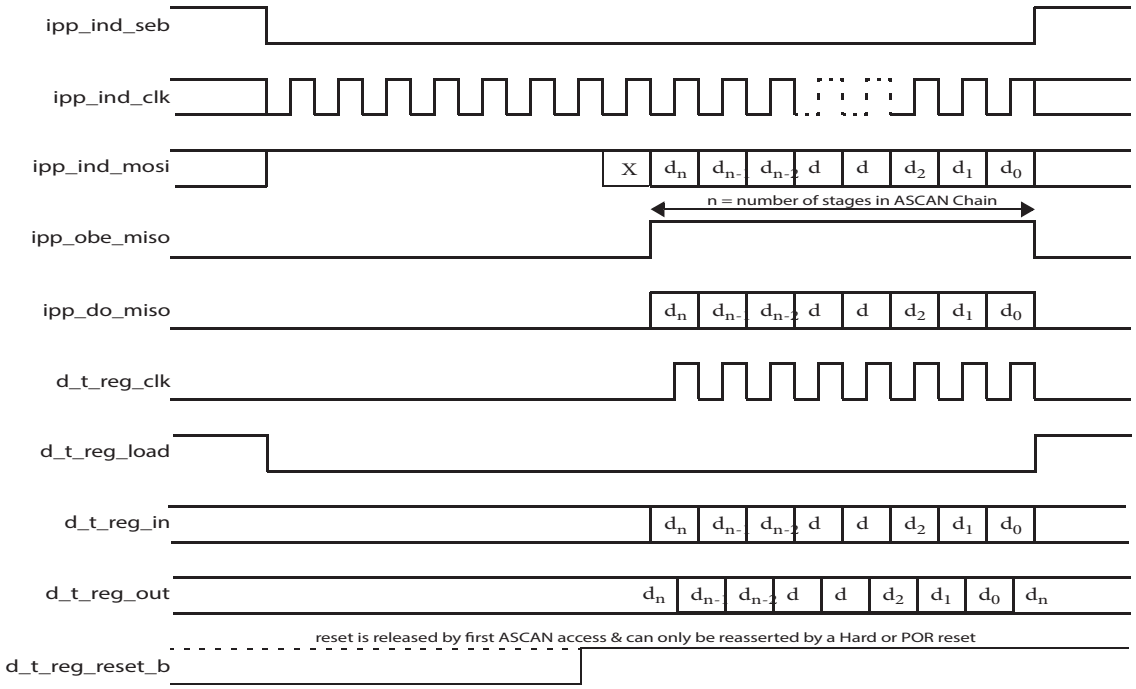


Figure 6. SPI write/read to ASCAN

6.1.2 Timing

SPI timings are described in Table 7 and illustrated in Figure 7. The SPI timing diagram, with the temperature and supply voltage conditions described in this document, and a maximum load capacitance, CL = 20 pF.

Table 7. SPI timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes [6]
t_{SCLK}	SCLK Cycle Time - SCLK pin	100	–	–	ns	(1)
t_{CSC}	SEB to SCLK Delay - SEB, SCLK pin	90	–	–	ns	(2)
t_{ASC}	After SCLK Delay - SCLK, SEB pin	2.5	–	–	ns	(3)
t_{SDC}	SCLK Duty Cycle - SCLK pin	0.9* (t_{SCLK}/2)	–	1.1* (t_{SCLK}/2)	ns	(4) [7]
t_{SUI}	Data Setup Time for Inputs - MOSI, SCLK pin	40	–	–	ns	(5)
t_{HI}	Data Hold Time for Inputs - MOSI, SCLK pin	40	–	–	ns	(6)
t_{SUO}	Data Valid (after SCLK edge) - MISO, SCLK pin	–	–	50	ns	(7)
t_{HO}	Data Hold Time for Outputs - MISO, SCLK pin	50	–	–	ns	(8)
H_{ZSEB}	High-impedance to SEB - MOSI, SEB pin	0.0	–	–	ns	(9)

Notes

6. The numbers under the Notes heading refer to the corresponding numbers in Figure 7.
7. For the maximum clock speed of 10 MHz

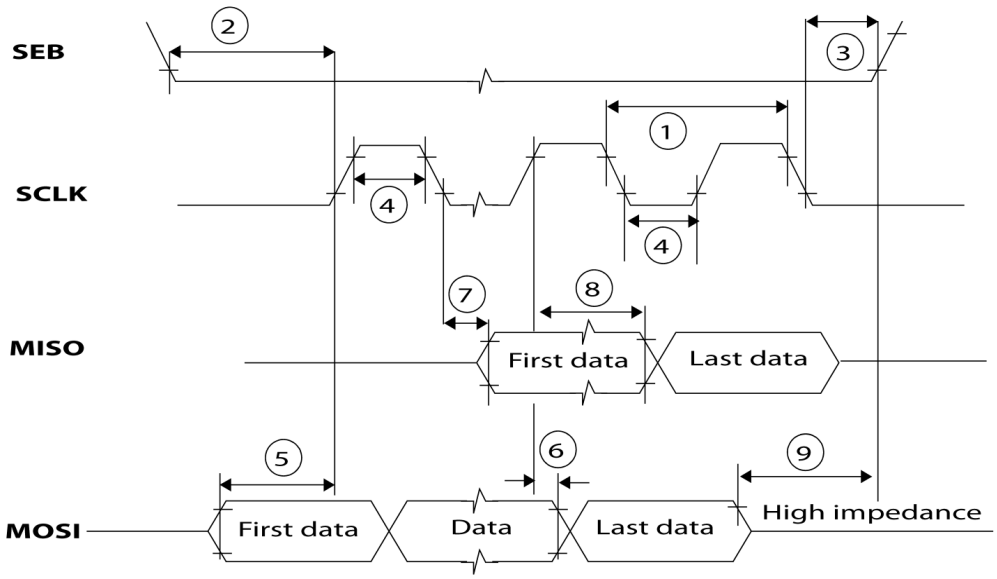


Figure 7. Typical SPI timing chart

6.2 External address solder balls ADR0 and ADR1

To minimize the effort on hardware wiring of signals, the MR2001R is using a combination of hardware and software coded addressing of each individual chip. Due to this procedure the hardware SEB (chip select) signal usage can be minimized.

If the software addressing is not longer sufficient (e.g. more than 4 RX chips) than a combination of SEB and software addressing is recommended.

Depending on the chip up to two external solder balls (address bit) are available (ADR0, ADR1). A connection to VCC represents a logical "1" and a connection to GND represents a logical "0", respectively. By default the logical "1" is already activated by a connection on the Die. If the corresponding pin is not connected to GND (used ball, not soldered ball), then this represents a logical "1".

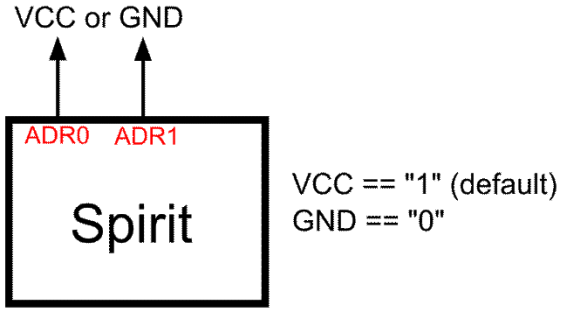


Figure 8. External connection of address pins ADR0 and ADR1 to define the identification key of the chip

6.3 System partitioning

Using the "software" addressing scheme of Spirit chips, any system up to max. one VCO, two transmitter (TX) and 4 receiver (RX) chips are supported.

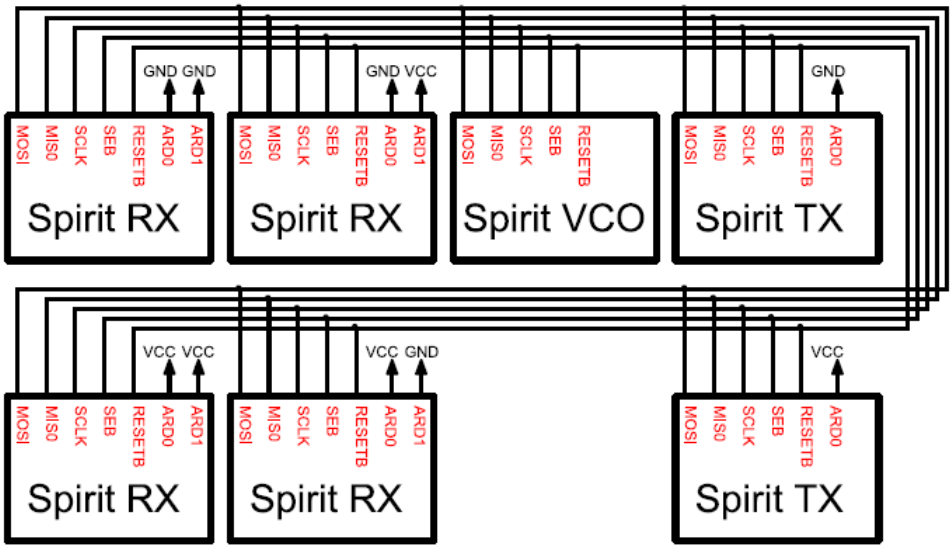


Figure 9. Chip partitioning using only software addressing of individual chips

If a system requires more than 4 Rx chips and/or 2 Tx chips and/or 1 VCO chip. Table 10 shows a proposed way to address the chips with a combination of the SEB (chip select) signal and "software" addressing.

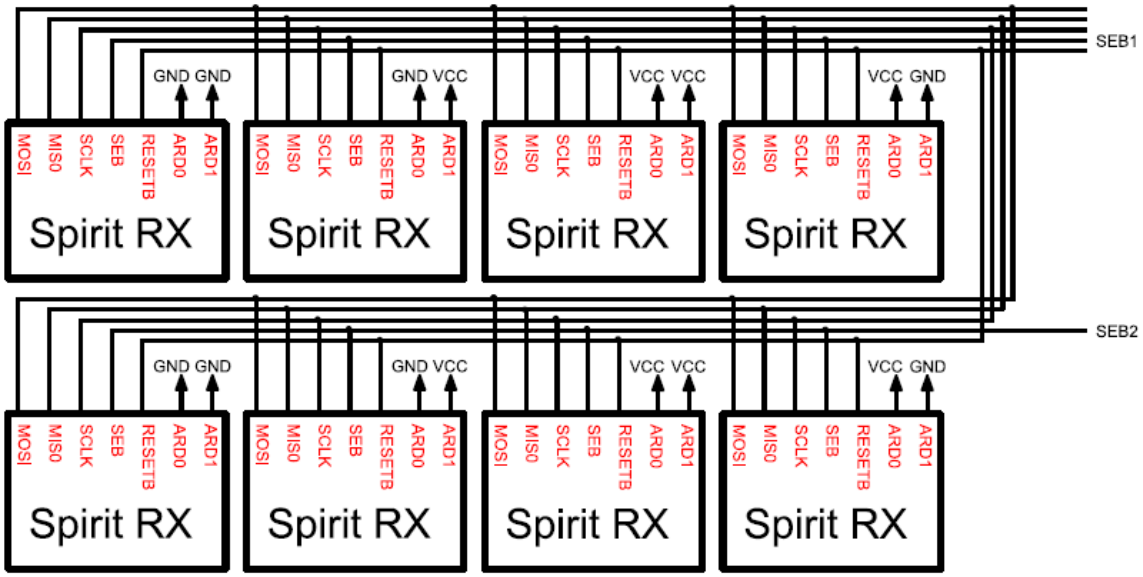


Figure 10. Typical Rx chip partitioning for more than four receivers. individual SEB Signals for more than four Rx chips are required

6.4 Identification key

The Identification key is used to address the correct chip via SPI and it is composed of four up to six internal (on the chip hard wired) bits and up to two external bits defined by the voltage level applied to the ADR0 and ADR1 solder balls.

Table 8. Identification key

Chip	Internal bits	ADR0	ADR1	Chip key
RX1	1010	0	0	101000
RX2	1010	1	0	101001
RX3	1010	0	1	101010
RX4	1010	1	1	101011
TX1	01110	0	-	011100
TX2	01110	1	-	011101
VCO	101100	-	-	101100

If more individual chips must be addressed then the chip select (SEB) signal must be used.

6.5 Access protocol

6.5.1 Write access

Write access to the device is done as follows:

Table 9. Write access

SPI_WRITE(add0, RX1 key)	access to RX1 is activated
SPI_WRITE(add1, data1)	write data1 to the RX1 register at address 1
SPI_WRITE(add0, VCO key)	access to VCO is activated
SPI_WRITE(add3, data3)	write data3 to the VCO register at address 3

6.5.2 Read access

Read access to the device is done as follows:

Table 10. Read access

SPI_WRITE(add0, RX1 key)	access to RX1 is activated
SPI_READ(add1, data1)	read data1 to the RX1 register at address 1
SPI_WRITE(add0, VCO key)	access to VCO is activated
SPI_READ(add3, data3)	read data3 to the VCO register at address 3

7 Memory map

7.1 Generic memory map

All three MR2001R chips share the same general memory map which simplifies the programming and minimizes the error due to changes in varying register addresses.

Table 11. Generic memory map

Addr	Register	Type	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	KEY	R/W	0x00	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0	RESERVED	RESERVED
0x01	FSM0	R/W	0x04	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S0_F	RESERVED	RESERVED
0x02	FSM1	R/W	0x00	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S1_F	RESERVED	RESERVED
0x03	EN	R/W	0x00	EN_5	EN_4	EN_3	EN_2	EN_1	EN_0	RESERVED	RESERVED
0x04	CTRL0	R/W	0x00	CTRL0_5	CTRL0_4	CTRL0_3	CTRL0_2	CTRL0_1	CTRL0_0	RESERVED	RESERVED
0x05	CTRL1	R/W	0x00	CTRL1_5	CTRL1_4	CTRL1_3	CTRL1_2	CTRL1_1	CTRL1_0	RESERVED	RESERVED
0x06	CTRL2	R/W	0x00	CTRL2_5	CTRL2_4	CTRL2_3	CTRL2_2	CTRL2_1	CTRL2_0	RESERVED	RESERVED
0x07	CTRL3	R/W	0x00	CTRL3_5	CTRL3_4	CTRL3_3	CTRL3_2	CTRL3_1	CTRL3_0	RESERVED	RESERVED
0x08	SNSOUT	R/W	0x00	SNSOUT_5	SNSOUT_4	SNSOUT_3	SNSOUT_2	SNSOUT_1	SNSOUT_0	RESERVED	RESERVED
0x09	TST	R/W	0x00	TST_5	TST_4	TST_3	TST_2	TST_1	TST_0	RESERVED	RESERVED

As an example, the register 0x03 describes the control enable/disable functionality. The level of control/enable can be different for each individual chip. Details can be found in the register map of each chip.

7.2 RX memory map

Table 12. RX memory map

Addr	Register	Type	Reset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	KEY	R/W	0x00	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0	RESERVED	RESERVED
0x01	FSM0	R/W	0x04	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S0_F	RESERVED	RESERVED
0x02	FSM1	R/W	0x00	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S1_F	RESERVED	RESERVED
0x03	EN	R/W	0x00	CH3	CH2	CH1	NOT_USED	DB_IN	RESERVED	RESERVED	RESERVED
0x04	CTRL0	R/W	0x00	NOT_USED	VGA1_1	VGA1_0	VGA2_2	VGA2_1	VGA2_0	RESERVED	RESERVED
0x05	CTRL1	R/W	0x00	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	RESERVED	RESERVED
0x06	CTRL2	R/W	0x00	IF_SEL	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	RESERVED	RESERVED
0x07	CTRL3	R/W	0x00	SD_CH3	SD_CH2	SD_CH1	NOT_USED	NOT_USED	NOT_USED	RESERVED	RESERVED
0x08	SNSOUT	R/W	0x00	TMP_EN	TMP_SEL	PD_EN	PD_SEL0	TMP_TYP	SNS_RSET	RESERVED	RESERVED
0x09	TST	R/W	0x00	T_IF3	T_IF2	T_IF1	T_BBCH3	T_BBCH2	T_BBCH1	RESERVED	RESERVED

7.2.1 0x00 RX key register

Address	0x00					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0	RESERVED	RESERVED
Reset	0	0	0	0	0	0	N/A	N/A

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[7:2]	KEY	Device Identification Key

7.2.2 0x01 RX S0 state machine register (disabled)

Address	0x01					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S0_F	RESERVED	RESERVED
Reset	0	0	0	0	0	1	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	S0_F	State machine register. When S0_F is set to 1 the state machine is changing from S1 (enable) to S0 (disable)
[7:3]	NOT_USED	Unused bits

7.2.3 0x02 RX S1 state machine register (enabled)

Address	0x02					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	S1_F	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	S1_F	State machine register. When S1_F is set to 1 the state machine is changing from S0 (disable) to S1 (enable)
[7:3]	NOT_USED	Unused bits

7.2.4 0x03 RX channel enable/disable and RF test bits

Address	0x03					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	CH3	CH2	CH1	NOT_USED	DB_IN	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	RESERVED	RESERVED
[3]	DB_IN	Enable LO doubler input stable (can be used to minimize load pulling due to enable/disable of the complete RX chip)
[4]	NOT_USED	Unused bits
[5]	CH1	Enable RX channel1
[6]	CH2	Enable RX channel2
[7]	CH3	Enable RX channel3

7.2.5 0x04 RX VGA control bits

Address	0x04					Access: User read write		
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	VGA1_1	VGA1_0	VGA2_2	VGA2_1	VGA2_0	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

The receiver contains on-chip high-pass filter (STC) and two variable gain stages. VGA1_x bits are addressing the 1st VGA stage (directly after the mixer core, 20 dB high-pass filter is in front of VGA1). VGA2_x bits are addressing the 2nd VGA stage (20 dB high-pass filter is in front of VGA2).

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[4:2]	VGA2_x	Gain settings of 2nd stage VGA [VGA2_2, VGA2_1, VGA2_0] 000 == -8.0 dB 001 == -2.0 dB 010 == 4.0 dB 011 == 10 dB 100 == 16 dB 101 == 22 dB 110 == 28 dB 111 == 28 dB (unused combination of bits)
[6:5]	VGA1_x	Gain settings of 1st stage VGA [VGA1_1, VGA1_0] 00 == 4.0 dB 01 == 10 B 10 == 16 dB 11 == 22 dB
[7]	NOT_USED	unused bit

Typically the max. gain (suitable for combination with the NXP RaceRunner MCU) is VGA1 = 22 dB and VGA2 = 16 dB or VGA1 = 16 dB and VGA2 = 22 dB. The second combination slightly increases the noise figure of the receiver by approx. 0.5 dB.

7.2.6 0x05 RX general control bits

Address	0x05					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[7:2]	NOT_USED	Unused bits

7.2.7 0x06 RX IF load impedance settings

Address	0x06					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	IF_SEL	NOT_USED	NOT_USED	NOT_USED	NOT_USED	NOT_USED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[6:2]	NOT_USED	Unused bits
[7]	IF_SEL	IF load drive capability selection 0 == min. 200 Ω single-ended load supported. 1 == min. 500 Ω single-ended load supported (slightly lower power consumption of the receiver)

7.2.8 0x07 RX saturation detector enable settings

Address	0x07					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	SD_CH3	SD_CH2	SD_CH1	NOT_USED	NOT_USED	NOT_USED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[4:2]	NOT_USED	Unused bits
[5]	SD_CH1	Enable saturation detectors of the receiver channel 1
[6]	SD_CH2	Enable saturation detectors of the receiver channel 2
[7]	SD_CH3	Enable saturation detectors of the receiver channel 3

Each receiver channel contains in total three saturation detectors (after the mixer core, after 1st VGA stage, and after 2nd VGA stage). The outputs of the saturation detectors from each channel are hardwired together; a separate activation/de-activation of the saturation detectors in one receiver branch is not possible. All saturation detectors can be activated simultaneously.

7.2.9 0x08 RX sensor settings

Address	0x08					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	TMP_EN	TMP_SEL	LOPD_EN	LOPD_SEL	TMP_TYP	SNS_RSET	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	SNS_RSET	Sensor reset (discharge of on-chip capacitance)
[3]	TMP_TYP	Activate temperature sensor 1: Temperature sensor activated
[4]	LOPD_SEL	LO power detector (after on-chip LO double) branch selection 0 : Select signal branch 1: Select reference branch
[5]	LOPD_EN	Enable LO power detector
[6]	TMP_SEL	Temperature sensor output selection 0 : diode row 1 1: diode row 2
[7]	TMP_EN	Enable temperature sensor

Only the temperature sensor or the LO peak detector can be enabled at a time. The temperature sensor is using a reference (diode row = 0) and a signal branch (diode row = 1) only the absolute difference between these two voltages gives a voltage with is proportional to temperature, and peak voltage level. Example for the temperature sensor activation is as follows.

SPI_WRITE(0x00, RX key)	access to RX is activated
SPI_WRITE(0x08, 04h)	Activate sensor reset SNS_RSET (discharge on-chip capacitance)
SPI_WRITE(0x08, 88h)	Enable temperature sensor at diode row 0
<measure V1>	Measure voltage V1 at sense output
SPI_WRITE(0x08, 04h)	Activate sensor reset SNS_RSET (discharge on-chip capacitance)
SPI_WRITE(0x08, C8h)	Enable temperature sensor at diode row 1
<measure V2>	Measure voltage V2 at sense output

|V1-V2| gives a voltage which is proportional to the on-chip temperature. SNS_RSET (sensor reset) activation discharges an on-chip capacitance to pull down the output to GND. The activation maybe required between each change of the sensor branch to speed up communication. Similar scheme must be used to read out values of the peak detector.

7.2.10 0x09 RX on-chip test capability

7.2.10.1 0x09 baseband on-chip test capability

Address	0x09					Access: user read write		
Bit	7	6	5	4	3	2	1	0
R/W	T_IF3	T_IF2	T_IF1	T_BBCH3	T_BBCH2	T_BBCH1	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Field	R/W	Description
[1:0]	RESERVED	Reserved bits
[2]	T_BBCH1	External test signal (differential external signals at TIN/TINx required) routed to baseband chain of channel 1 (Input of 1st. stage high pass filter of VGA1). 0 : switch open 1 : switch closed
[3]	T_BBCH2	External test signal (differential external signals at TIN/TINx required) routed to baseband chain of channel 2 (Input of 1st. stage high pass filter of VGA1). 0 : switch open 1 : switch closed
[4]	T_BBCH3	External test signal (differential external signals at TIN/TINx required) routed to baseband chain of channel 3 (Input of 1st. stage high pass filter of VGA1). 0 : switch open 1 : switch closed
[5]	T_IF1	External test signal (differential external signals at TIN/TINx required) routed to IF output of channel 1. 0 : switch open 1 : switch closed
[6]	T_IF2	External test signal (differential external signals at TIN/TINx required) routed to IF output of channel 2. 0 : switch open 1 : switch closed
[7]	T_IF3	External test signal (differential external signals at TIN/TINx required) routed to IF output of channel 3. 0 : switch open 1 : switch closed

Register 0x09 controls the baseband chain on-chip test feature. A differential external signal (DC up to 5.0 MHz) must be applied to the test signal inputs (TIN/TINx).

Some test modes can be selected to route TIN/TINX to the baseband output or baseband input. Controls are done through the RXTST register. Since the TIN/TINx inputs are shared with the RF test mode (and then externally AC coupled), it means the internal nodes are floating, especially when T_IFx = 1. It is recommended then to enable the RFTST bit to 1 to bias the TIN/TINx inputs.

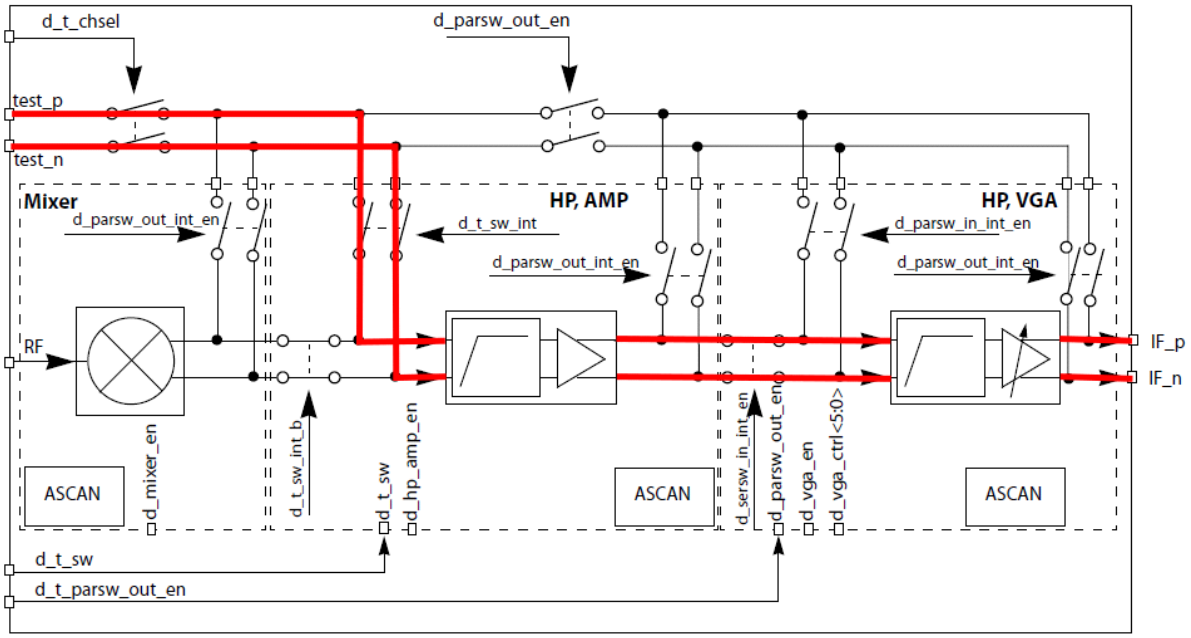


Figure 11. Signal path of the test signal for the control bits T_BBCH1, T_BBCH2 and T_BBCH3. The test signal is shown in red

7.3 State machine

The MR2001 chipset contains a digital controller which provides a simplified enable/disable control of the key analog blocks. The state machine has only two states S0 and S1. S0 corresponds to the OFF (disabled) mode and S1 corresponds to the ON (enabled) mode, respectively.

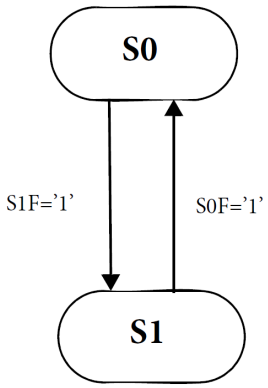


Figure 12. MR2001R state machine with the two states S0 and S1

The signals, block controlled by the state machine are listed in the following table.

Internal signal names	Chip	State machine S1 (register 0x02 set to 0x04)	State machine S0 (register 0x01 set to 0x04)
d_out8	Rx	Mixer channel 1 enabled	Mixer channel 1 disabled
d_out8	Rx	HP filter and VGA1 channel 1 enabled	HP filter and VGA1 channel 1 disabled
d_out8	Rx	HP filter and VGA2 channel 1 enabled	HP filter and VGA2 channel 1 disabled
d_out10	Rx	Mixer channel 2 enabled	Mixer channel 2 disabled
d_out10	Rx	HP filter and VGA1 channel 2 enabled	HP filter and VGA1 channel 2 disabled
d_out10	Rx	HP filter and VGA2 channel 2 enabled	HP filter and VGA2 channel 2 disabled
d_out12	Rx	Mixer channel 3 enabled	Mixer channel 3 disabled
d_out12	Rx	HP filter and VGA1 channel 3 enabled	HP filter and VGA1 channel 3 disabled
d_out12	Rx	HP filter and VGA2 channel 3 enabled	HP filter and VGA2 channel 3 disabled
d_out23	Rx	IF saturation detector channel 1 enabled	IF saturation detector channel 1 disabled
d_out32	Rx	LO doubler enabled	LO doubler disabled
d_out36	Rx	IF saturation detector channel 2 enabled	IF saturation detector channel 2 disabled
d_out37	Rx	IF saturation detector channel 3 enabled	IF saturation detector channel 3 disabled

8 Typical applications

8.1 Introduction

The MR2001 is an expandable three package solution for automotive radar modules. The chipset consists of a VCO (voltage controlled oscillator), a two-channel Tx transmitter, and a three-channel Rx receiver. The MR2001R is a high performance, highly integrated, three-channel, receiver (RX) ideally suited for automotive radar applications. In conjunction with the MR2001V, a four-channel voltage controlled oscillator, and an MR2001T, a two-channel transmitter, it provides an expandable three package solution for automotive radar modules.

The chips are connected together via the LO signal around 38 GHz. The individual control of each chip is realized by SPI. The main controller and modulation master is a single microprocessor (MCU) with integrated high-speed analog to digital converters (ADC) and appropriate signal processing capability such as fast fourier transforms.

The front-end solution is specifically architected to be controlled by NXP's Qorivva MPC5775 MCU. Especially the baseband functionality (high-pass filters, variable gain amplifiers, anti-aliasing filters) on the receiver chips has been designed to work with the MPC5775 MCU.

8.2 Typical application

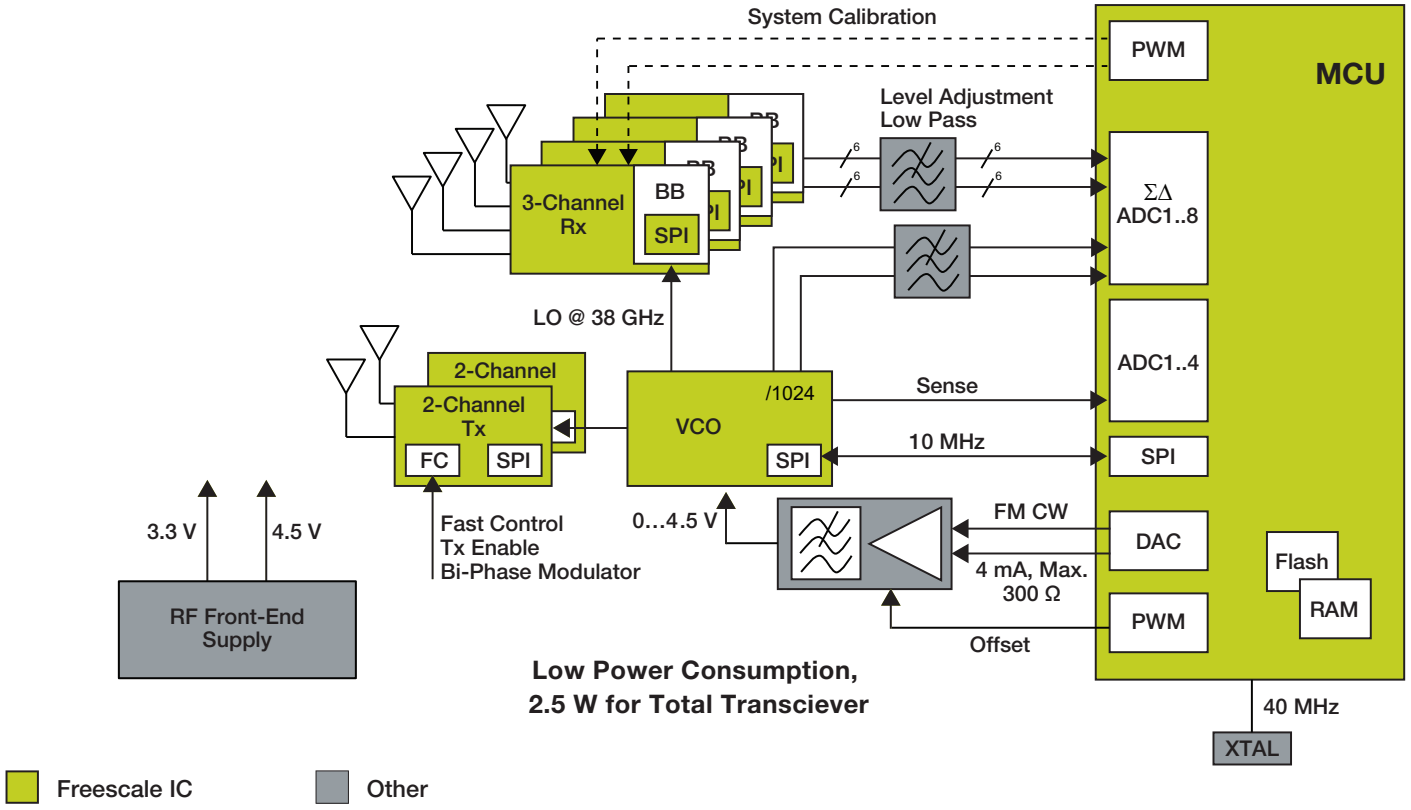


Figure 13. Typical application diagram

8.3 Measurement results

In the following chapters can find some typical measurement results which should help to guide a Radar system design.

8.3.1 Common results

8.3.1.1 Temperature sensor

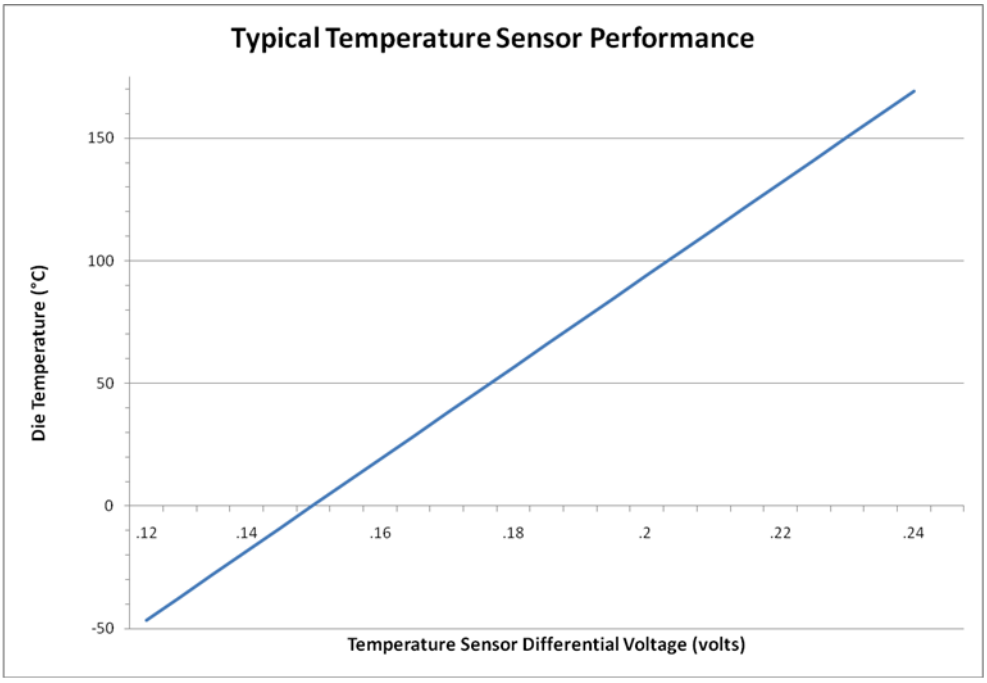


Figure 14. Typical slope of the temperature sensor of all 3 chips.
The derived equation can be used to calculate the on-chip temperature at the position of the sensor

The derived equation: Die Temp[°C]= ΔV_{TEMP} * 1875.0 - 280.94, with ΔV_{TEMP} the difference between the two sequential reading on the sense output, can be used to calculate the on-chip temperature. See 0x08 RX sensor settings.

8.3.1.2 Thermal resistance

Figure 15 shows electrical measurements done on the 2-channel transmitter chip mounted on a multi-layer FR4/RO3003 PCB mounted on a mechanical carrier, which is attached to an on-wafer chuck. Due to the test set-up the extracted thermal resistance is combination of the PCB to heatsink thermal resistance and the resistance of the RCP itself. Taking this into account, the thermal resistance of the RCP package itself is in the range of approx. 15 K/W.

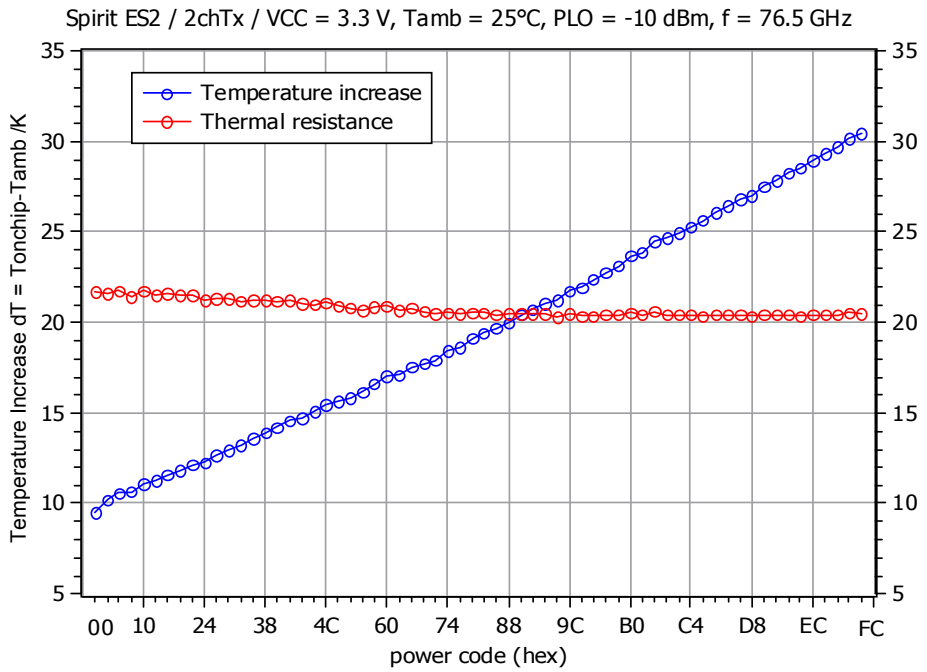


Figure 15. Electrical measurements of the thermal resistance of the RCP including PCB (FR4/RO3003), mechanical carrier and attachment to the on-wafer chuck.

8.3.2 3-Channel receiver Rx

8.3.2.1 LO power detector threshold voltage at 125 °C

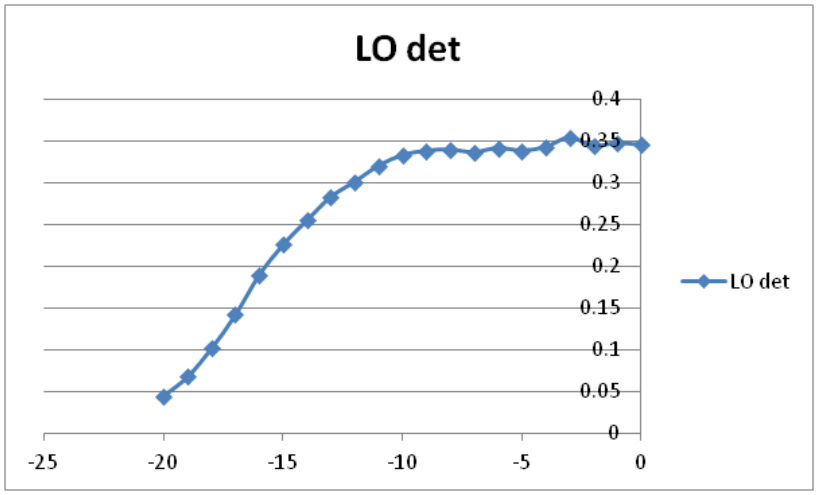


Figure 16. LO Power detector threshold voltage. voltage values > 300 mV indicate sufficient LO input power to guarantee full functionality of the receiver

8.3.2.2 Noise and gain vs. frequency and channel

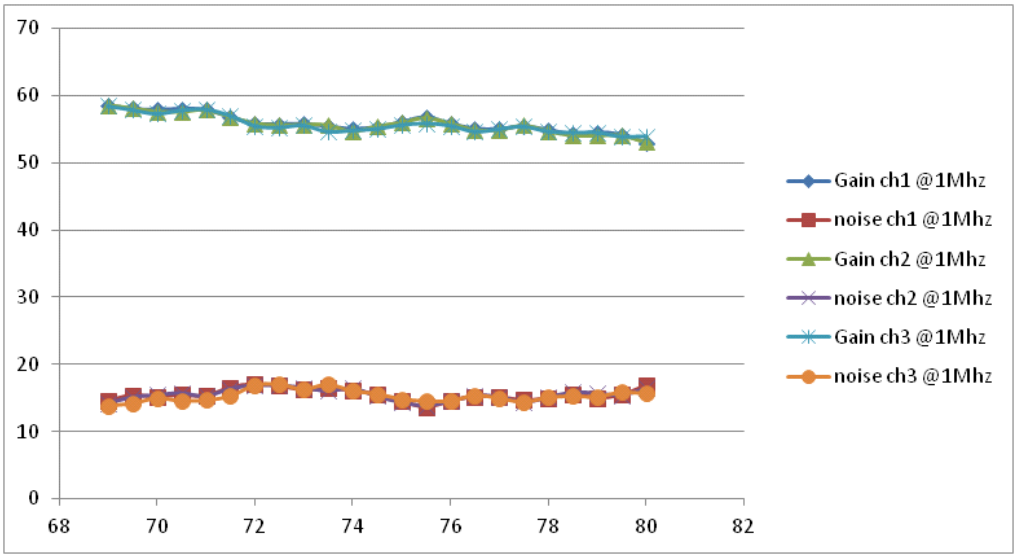


Figure 17. Noise and gain vs. rf-frequency at max. gain settings (VGA1 = 22 dB, VGA2 = 16 dB) at an baseband frequency of 1.0 MHz for all three receiver channels

8.4 External components

8.4.1 Biasing

8.4.1.1 External blocking capacitors

To achieve defined specifications, the supply to the chip must be regarding spurious and noise level as good as possible. For this reason, typically external filters are added between the sensor supply domain and the on-chip supply domains. Figure 18 shows such a typical supply scheme. The blocking caps should be placed as close as possible to the package. This is dependent on application board material and manufacturer.

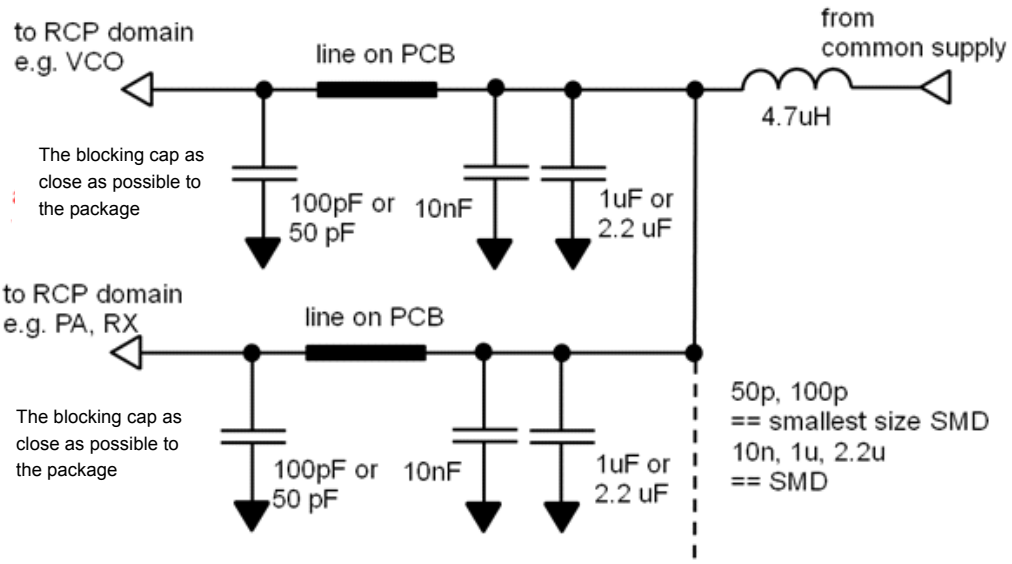


Figure 18. Typical arrangement and values of blocking capacitors to supply the chips

8.4.1.2 External biasing resistors

To operate the MR2001 chip-set, it is mandatory to connect each chip to two external resistors RN, RP, respectively. Without these two resistors the chips cannot be functional.

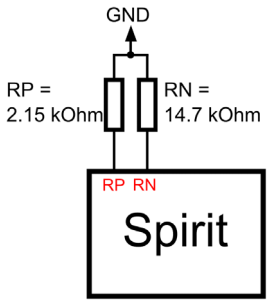


Figure 19. Required external resistors RN and RP for each individual MR2001Chip

External resistors	Value	Recommendation
RP	2.15 kΩ	E96, ±1.0%, TK = ±100 ppm/K SMD, 0402 or smaller, 50 μA current
RN	14.7 kΩ	E96, ±1.0%, TK = ±100 ppm/K SMD, 0402 or smaller, 50 μA current

The two external resistors are part of the on-chip bandgap references. Due to the lower tolerances of the external resistors (±1.0% compared to on-chip ±10%) the supply current variation from package to package is drastically reduced.

8.4.2 Sense and IF outputs

8.4.2.1 Tri-state sense outputs

The MR2001 chip-set provides tri-state sensing output signal which allows simplified wiring and signaling. All sense signals can be connected together to share the same hardwired signal line.

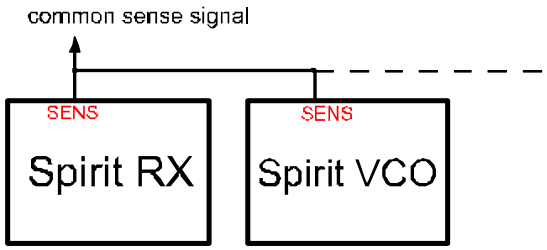


Figure 20. Block diagram and the relevant pin signals

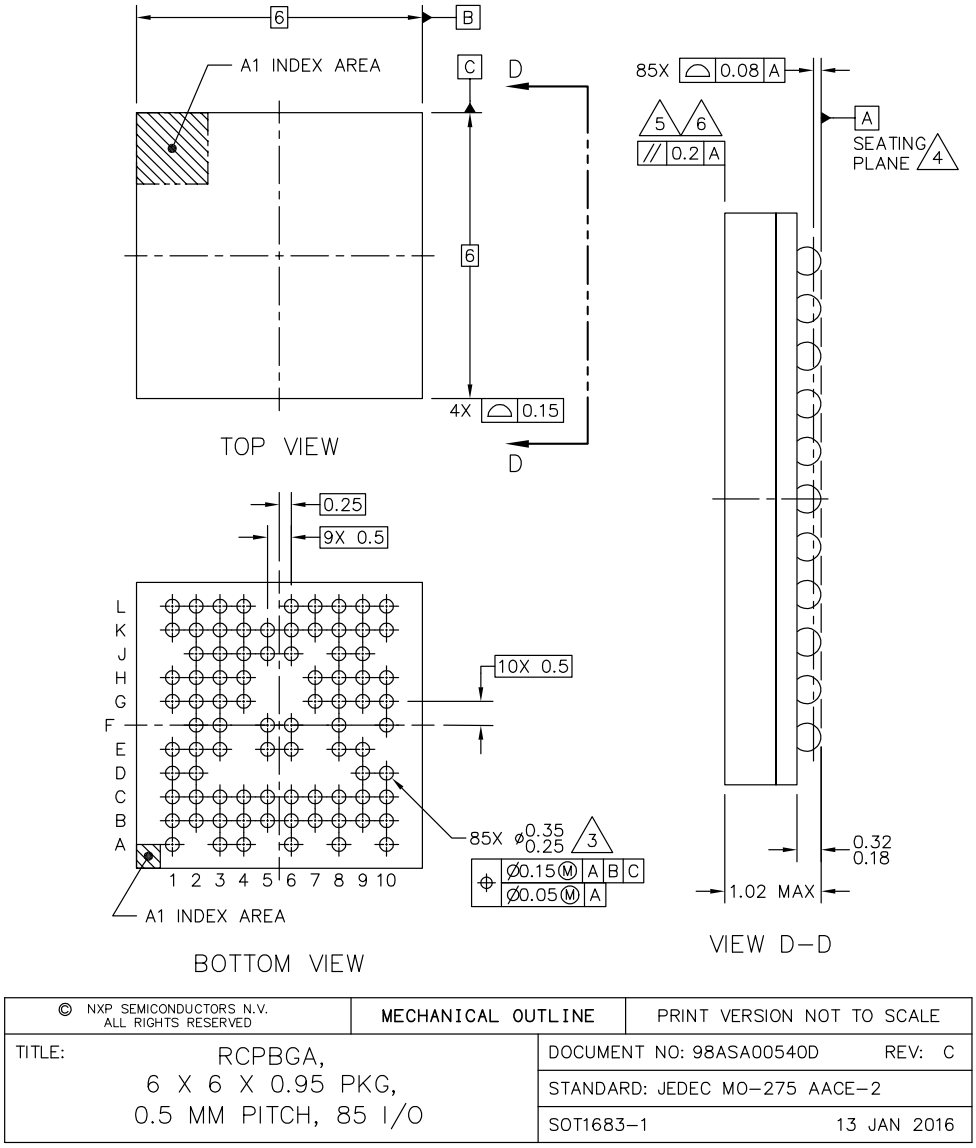
9 Packaging

9.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 13. Packaging Information

Package	Suffix	Package outline drawing number
6.0 x 6.0 mm RCP, (10 x 11 array) 0.5 mm pitch	VK	98ASA00540D



MR2001R

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. SCORING OR GROOVES ON TOP SURFACE OF PACKAGE IS NOT PERMITTED.
7. NO VOIDS IN ENCAPSULATION PERMITTED.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: RCPBGA, 6 X 6 X 0.95 PKG, 0.5 MM PITCH, 85 I/O	DOCUMENT NO: 98ASA00540D REV: C
	STANDARD: JEDEC MO–275 AACE–2
	SOT1683–1 13 JAN 2016

9.2 PCB and RCP environment

9.2.1 NXP test board

9.2.1.1 RO3003 on FR4

For the NXP test boards a multi-layer PCB composed of 127 µm thick Rogers 3003 on top of standard FR4 core is used. The manufacturer for these boards is Elekonta/Marek (http://www.elekonta.de/).

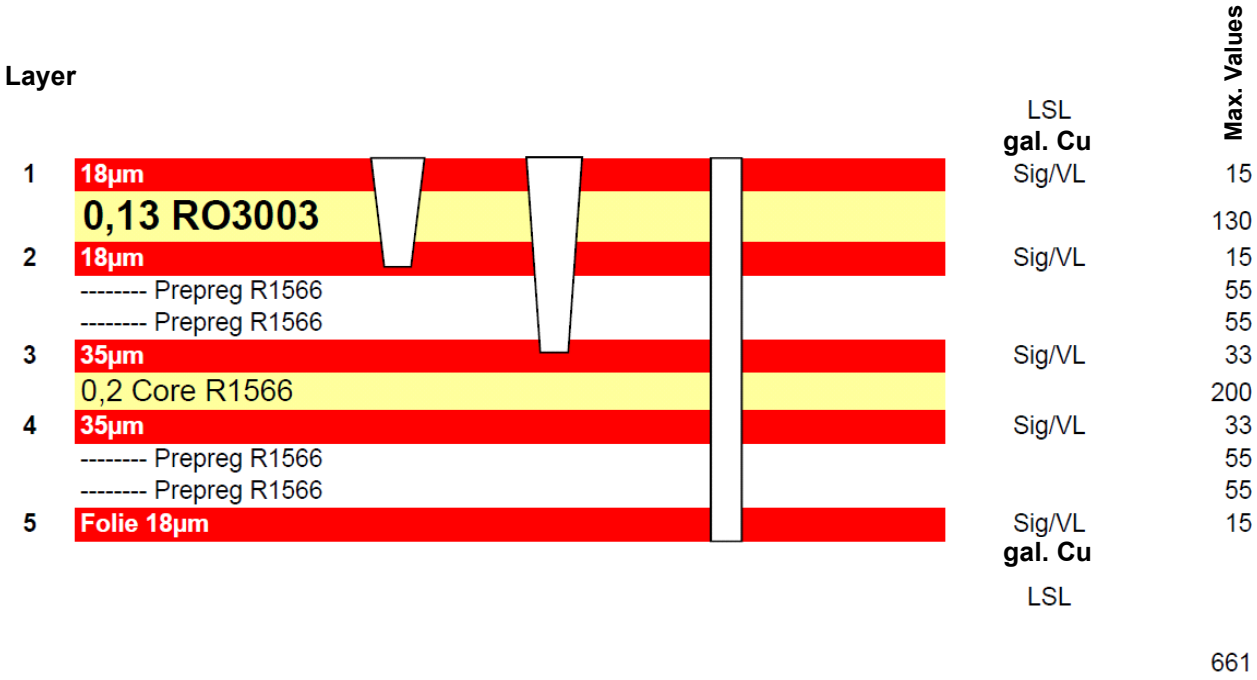
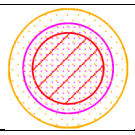
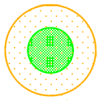


Figure 21. RO3003 on top of a FR4 core

9.2.1.2 Layout rules

The Figure 16 shows the solder ball arrangement including thermal and rf vias of typical PCB. Solder ball locations are shown in magenta with a label in blue, thermal via's have a wider diameter and are also shown in magenta without any blue label, important gnd via's to achieve rf performance are shown in green. Thermal vias are located in the area where no solder ball is available, so that they can occupy the full area of a solder ball.

Type	Shape	Geometry
solder ball		~∅ 300 um
thermal via		> ∅ 200 um, thru PCB (non filled, or filled)
gnd via for rf performance		∅ 200 um (non filled, or filled)

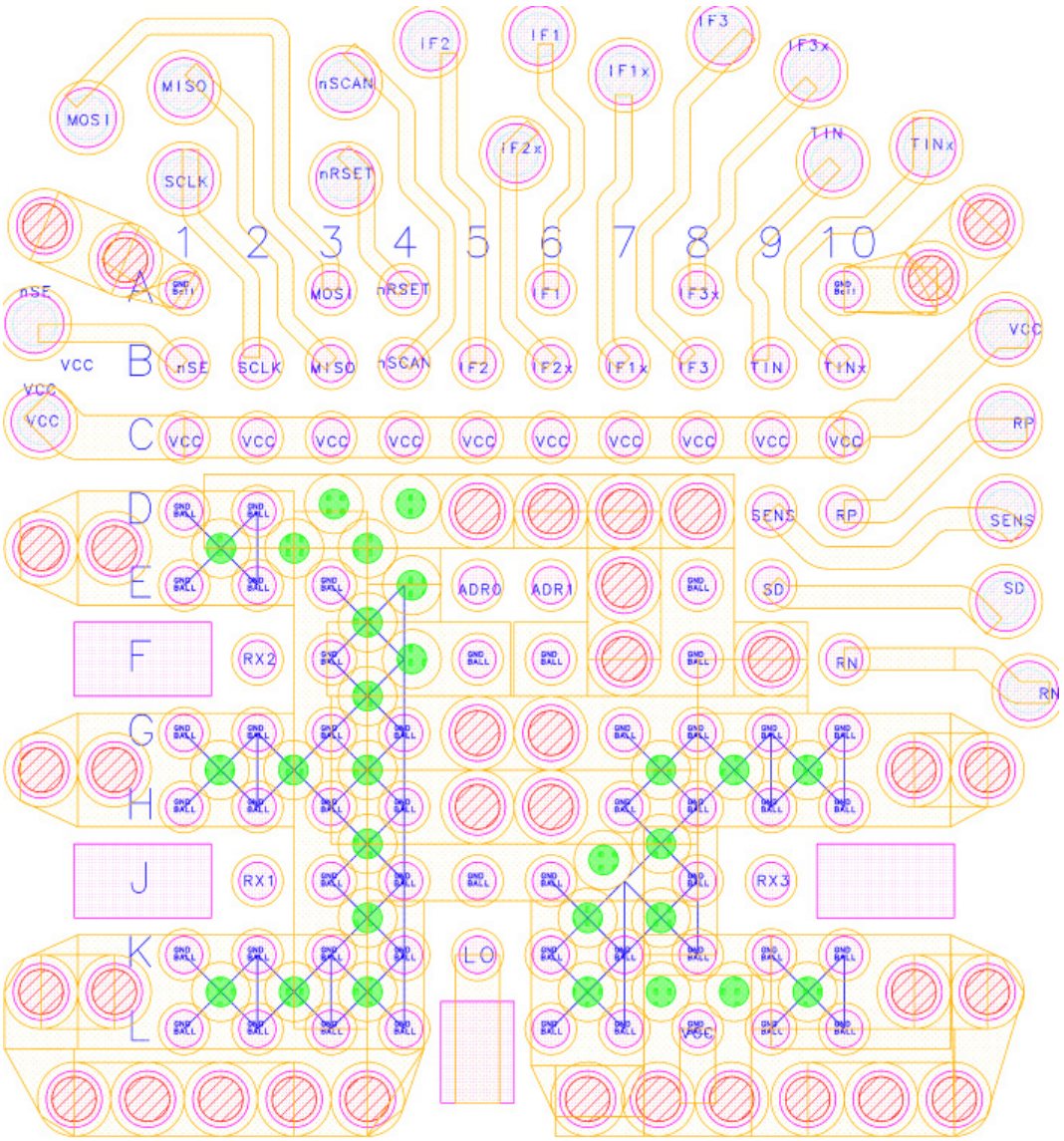


Figure 22. Top view of the Rx solder ball arrangement (magenta with blue label) Including Gnd vias (green, 200 µm) to obtain rf performance and thermal vias (> 200 µm) to guarantee temperature range

The layout of the RCPs and the solder ball arrangement have been already done to allow space for thermal vias in the area where no solder balls are placed. It is recommended that this area is fully filled with thermal vias to lower the thermal resistance.

9.2.1.3 Achieving RF performance

To achieve low noise figures, high output power and high channel-to-channel isolation on a PCB it is required to build a kind of metal cage around the single-ended rf solder balls. In Figure 23 the layout view of the input channel1 and channel2 of the receiver is shown.

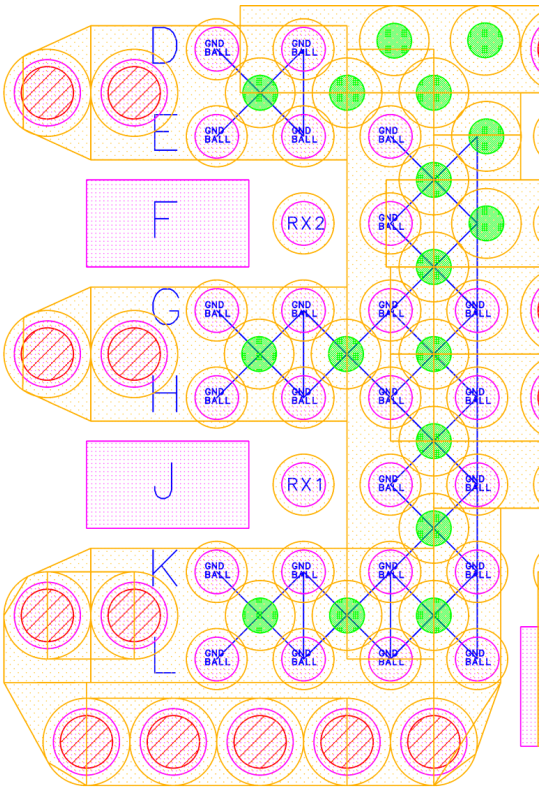


Figure 23. Rx location of Gnd via's (green circles) to improve rf performance

Around the Rx input channel1 and channel 2 gnd-via's (200 μm) are placed at a pitch of 500 μm between the solder balls to enhance the rf performance (e.g. noise figure, channel-to-channel isolation). The gnd-via's typically improve the isolation by 20 dB, without such kind of layout consideration the isolation can be degraded down to 10 dB only. Additionally without such gnd guards also the noise figure and the input matching can be strongly degraded. Due to the single-ended input configuration of the receiver, this chip show high sensitivity to the demonstrated design and layout considerations.

9.2.1.4 Single-ended RF connection at 77 GHz (PCB microstrip lines)

Figure 24 shows the layout of the receiver input channel 3 with a microstrip transmission line matching circuitry to achieve matching (> 10 dB loss) and lowest noise figures.

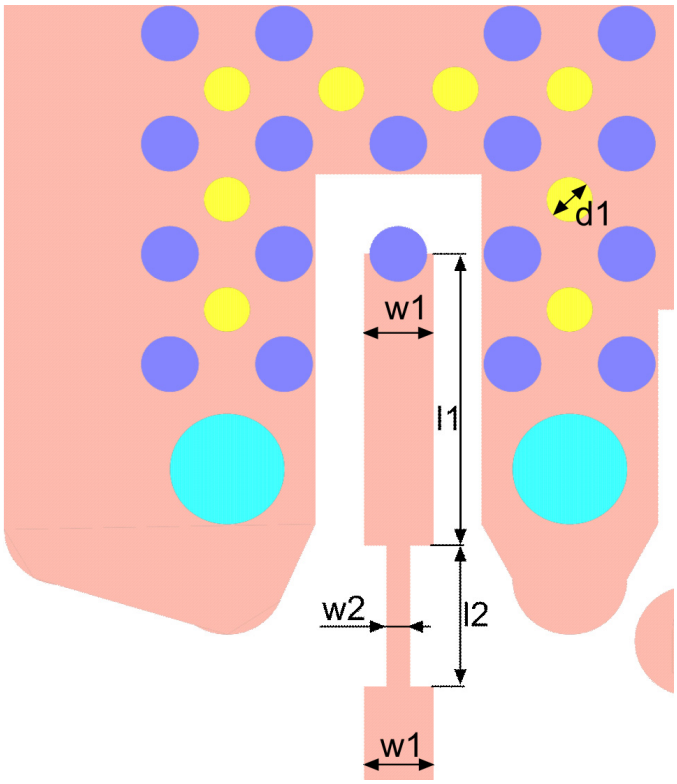


Figure 24. Receiver input channel 3 layout and matching circuitry to achieve best matching and lowest noise figures

top PCB metal transmission line width 1	w1	300 µm
top PCB metal transmission line length 1	l1	1320 µm
top PCB metal transmission line width 2	w2	100 µm
top PCB metal transmission line length 2	l2	641 µm
rf ground via in PCB	d1	∅200 µm

9.2.1.5 Single-ended RF connection at 38 GHz (PCB microstrip lines)

For 38 GHz input and output signals no special matching structure on the PCB is required. A standard 50 microstrip transmission line directly connected to the solder ball is fully sufficient.

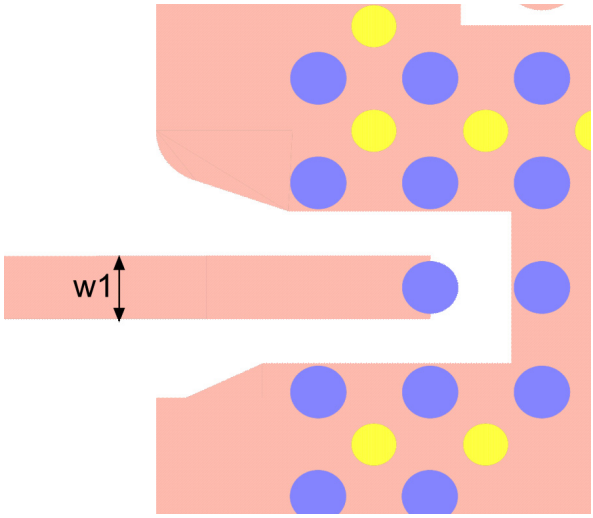


Figure 25. Example for the rf connection of a 38 GHz input and output signal. Shown in the picture is the LO input of the receiver chip

9.3 Assembly conditions

Please find below basic recommendations for the NXP RCP assembly:

- Avoid non solder mask defined (NSMD) defined pads
- Pad size 280 µm minimum
- Solder mask defined board pad
- Solder mask opening 200 µm minimum
- Stencil thickness 100 µm
- Solder paste opening 200 µm
- Lead-free solder paste (SAC405)
- ±35 µm placement of component
- Reflow following paste supplier suggested temperatures, or…
- Reflow peak is 260 °C, time above liquidus (217 °C) for 60 to 150 seconds

Figure 26. Solder mask (SMD) and non-solder mask defined (NSMD) pads

The typical reflow profile for the chip-set is shown in Figure 27.

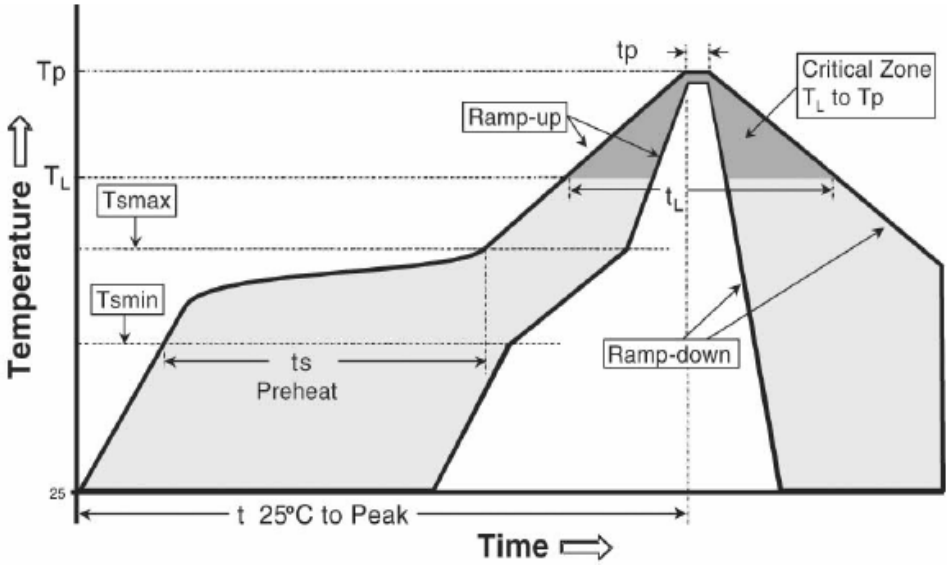


Figure 27. Typical spirit reflow profile

Profile parameter	
Average ramp-up rate (TSmax to Tp)	3.0 °C/second max.
Pre-heat • Temperature Min. (TSmin) • Temperature Max. (TSmax) • Time (TSmin to TSmax) (ts)	150 °C 200 °C 60 – 120 seconds
Time maintained above: • Temperature (TL) • Time (tL)	217 °C 60-150 seconds
Peak Temperature (Tp)	260 °C
Time within 5.0 °C of actual Peak Temperature (tp)	10 – 30 seconds
Ramp-down Rate	6.0 °C/second max.
Time 25 °C to Peak Temperature	8 minutes max.

Notes

8. Reflow profile as per IPC/JEDEC J-STD-020D.1

10 Revision history

Revision	Date	Description of changes
1.0	11/2014	• Initial release
2.0	12/2014	• Made typographic corrections to bring the document into compliance.
	1/2015	• Corrected two typographic errors. No content change.
3.0	2/2015	• Clarification on RX Baseband Test Mode implementation • Clarification on SPI interface • Updated internal block diagram
4.0	11/2015	• Included note on G_RF to clarify reference plane after matching circuit on board • Updated reflow profile table as per IPC/JEDEC J-STD-020D.1
5.0	9/2016	• Updated to NXP document format and style • Updated Figure 2 • Removed RF test concept • Corrected SPI access for temperature sensor • Updated temperature sensor graph • Corrected reflow profile parameters

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9/2016