Technical Data

MC44CD03 Version 3.1
30 JAN 2006

MC44CD03
1.67GHz Zero-IF Direct Conversion Receiver

freescale semiconductor

MC44CD03

Thin QFN-EP Package

1.67GHz Zero-IF Direct Conversion Receiver Front-End IC for USA Hand Held Portable Convergence Terminals

Ordering Information

Device	Temp Range	Package
MC44CD03FC,R2	-30°C to +85°C	Thin QFN-EP (0.65mm max. thickness)
NOTE: For tape and reel, add R2 suffix.		

MC44CD03 Data Sheet
Version 3.1

Original Release Date: 04 MARCH 2005
Revised: 30 JAN 2006

WMSG
EMEA Radio Product Division
Freescale, Inc.

Revision History

Version Number	Revision Date	Description of Changes	
1.0	4 MARCH 2005	Initial version.	
2.0	10 OCT 2005	Change Request list MC44CD03_CRlist2.0_10OCT2005	
		CR_list2.0_01: Clock Select Functionality Added (block diagram updated, I2C registers updated, additional paragraph for functionality description and electrical specifications added, OSC functional description updated, Initialization/Application paragraph updated)	p18, p23-36, p43, p55-58, p65-66, p67-76, p99
		CR_list2.0_02: New Pinning Diagram	p19-22
		CR_list2.0_03: New IIP2 Specification	p82-83
		CR_list2.0_04: RFAGC and BBAGC slopes updated	p45, p52, p85, p90
		CR_list2.0_05: Maximum Channel Attenuation	p89
		CR_list2.0_06: Remove the RFAGC programmability	p30, p45
		CR_list2.0_07: Memory Map updated	p23-36
		CR_list2.0_08: LOP buffer specification update	p63, p97
		CR_list2.0_09: RF Input Matching Network Updated	p67-72
		CR_list2.0_10: PLL Typical Loop Filter Updated	p67-70
		CR_list2.0_11: AGCs application components correction	p70
		CR_list2.0_12: Specification for CDM ESD added	p79
		CR_list2.0_13: Removed Mixer datasheet electrical specification items	
		CR_list2.0_14: New IIP3 specification	p82
		CR_list2.0_15: New package reference	All pages
		CR_list2.0_16: 1dB compression point specification added	p82
		CR_list2.0_17: BBAGC input impedance specification added	p90
		Initialization/Application Chapter updated (more details provided on application schematics, BOM, RF input network, input impedance, SAW filter... Also the application schematic and BOM now refers to a SAW filter and no more to a balun).	p67-76
		Glossary updated	p14-15
		All sections: typos and general comments updated	All pages

Version Number	Revision Date	Description of Changes	
3.0	10 JAN 2006	Changed phase noise limit value from -33dBc to -30dBc (parameter 9.4) and removed backstop noise parameter for consistency Changed IP2 out of band limit value from 5dBm to 2dBm (parameter 3.2) and removed IP2 in band parameter Corrected typos (startup time, pin 31/37) and MLP table 4.4 inversion Added MSL profile in electrical specifications Changed marking specification (no DVB-H logo) Added explanations on how to use the bit PADCTRL (2 write operations required) Modified LO leakage specification conditions	All pages
3.1	30 JAN 2006	Removed NDA requirement	All pages

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Section 1 Introduction

1.1 Overview

The MC44CD03 is a Single Chip Narrowband Zero-IF Direct Conversion Receiver Front-End IC intended to be associated with an IQ baseband OFDM demodulator (**Figure 1-1**).

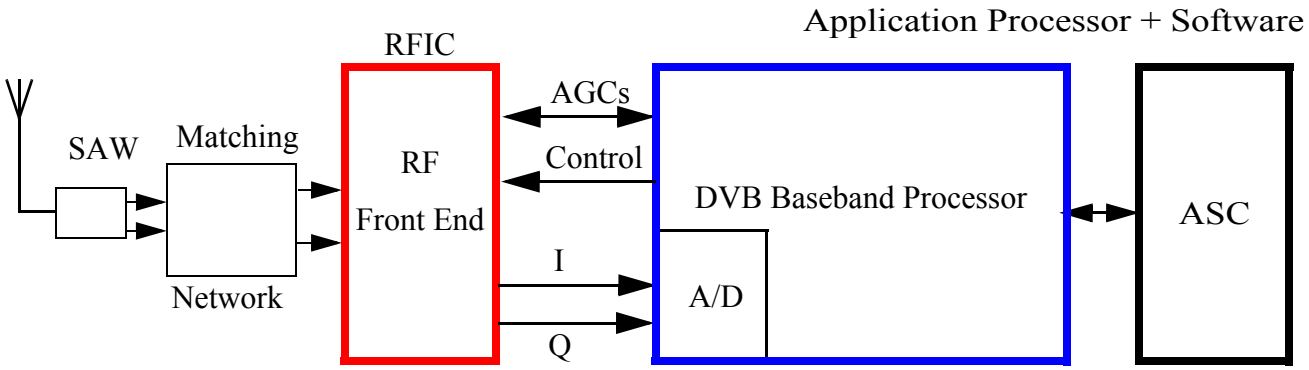


Figure 1-1 Block Diagram of a DVB-H chipset

The MC44CD03 chip is targeted for terminals dedicated in Integrated Cellular Phones (Category 3 for Hand Held Portable Convergence Terminals). This category is described in the EICTA-TAC-MBRAI RF Specification (reference [1]), and exhibits the following attributes:

- Both cellular and DVB-H radios integrated in the terminal.
- Battery powered.
- Moving during reception.
- Low gain integrated antenna.

The system is based on the US DVB-H standard and shall be capable of correctly demodulating all modes specified in the EN 300 744 specification (reference [2]), except the code rates 5/6 and 7/8.

The MC44CD03 chip covers the range of 1665-1680MHz. It operates on center frequencies 1667.5MHz, 1672.5MHz, or 1677.5MHz. The channel bandwidth is 5MHz and the US DVB-H signal bandwidth in this channel is 4.76MHz.

This device is targeted to provide an optimum solution where the power consumption is the major constraint for small battery operated devices.It is designed using the CDR1BiGCMOS process with the SiGe (HBT) option and electroplated copper inductors and transformers.

MC44CD03 is available in a Lead-free 40 pin Thin QFN package (0.65mm max. thickness).

1.2 Glossary

AAF
Baseband Anti Aliasing Filter.

ASC
Application Specific Controller, an external processor in charge of computing complex functions in the DVB-H system.

MC44CD03
The code name of the USA DVB-H RF front-end chip.

DVB-H
Digital Video Broadcast system, optimized for handheld applications. This category is described in the EICTA-TAC-MBRAI RF Specifications.

Deep-Sleep Mode
An operating mode characterized by the ENABLE pin held low leading to minimum power consumption. .

EICTA-TAC
European Information, Communications and Consumer Electronics Industry Technology Association Result of the merge of EICTA (European Information and Communications Technology Industry Association) and EACEM (European Association of Consumer Electronics Manufacturers).

HBT
Hetero-junction Bipolar Transistor, like Silicon-Germanium (Si-Ge) devices.

I2C
Inter IC bus. A bidirectional, serial data transfer protocol.

LPF
Baseband Low Pass Filter sub-module. The filter whose ouput is the I and Q components to the baseband processor during receive.

LVDS
Low Voltage Differential Signaling. LVDS is targeted for general purpose high speed applications requiring very low noise. This technology is defined by the ANSI/TIA/EIA-644 industry standard.

MBRAI
Mobile and Portable DVB-T Radio Access Interface Specification.

MIXER
The I and Q mixer sub-module.

MLP
The Multi-Level pin sub-module is dedicated to the configuration of the chip with regards to the reference clock frequency and the clock output signal shaping.

Normal Mode

An operating mode characterized by the ENABLE pin set, the SCAN_MODE pin cleared and the TSTM bit cleared in the MODE register (address $00).

OFDM

Orthogonal Frequency Division Multiplexing.

OSC

The 36MHz or 26MHz crystal oscillator sub-module.

PLL

Phase Locked Loop sub-module.

PMA

Post Mixer Amplifier sub-module.

Power Down Mode

An operating mode characterized by the ENABLE pin set, the SCAN_MODE pin cleared, the TSTM bit cleared and the PDM bit set in the MODE register (address $00).

RCI

The Radio Control Interface sub-module.

REM

Reference Management (bias support) sub -module. The block providing current/voltage references to the rest of the chip

RFLNA

RF Low Noise Amplifier sub-module.

SAW filter

Surface Acoustic Wave filter .

1.3 Features

The MC44CD03 is a 1.67GHz Zero-IF Direct Conversion Receiver Front-End IC. It receives the RF signal from an associated SAW filter. The MC44CD03 provides I and Q terms to the associated baseband demodulator. The device is controlled through an I2C bus and provides interface signals to the baseband processor (e.g. reference clock). The MC44CD03 receives control signals for specific functions or features such as the internal LNA and baseband AGC controls.

The device exhibits the following features:

- Normal power operation (2.775V, 100mA current drain, i.e. 280mW in normal mode)
- Reduced power operation (235 mW) with less filtering
- Power down and deep sleep battery save modes of operation
- Low external components count
- I2C bus controlled
- Integrated low phase noise PLL with 3.5GHz VCO and quadrature generator for precise I and Q local oscillator generation
- 500kHz synthesizer step size
- Integrated RF low noise amplifier (LNA) with gain control and differential inputs
- Integrated balanced I and Q down mixers
- Integrated post mixer amplifiers (PMA)
- Integrated (and capable of being disabled) I and Q baseband 4th order inverse Chebyshev channel filter and 2nd order Butterworth complementary low pass filter, and amplifiers with gain control
- Integrated filter tracking loop to maintain the cutoff frequency over all process variations
- 36MHz or 26MHz crystal oscillator with clock outputs (either custom LVDS or single-ended) to the baseband demodulator.
- A general purpose digital output.
- Lead free Thin QFN 40 6x6mm^2, 0.5mm pitch exposed pad package

1.4 Modes of Operation

This circuit supports four modes of operation.

- Normal - The device operates normally.
- Low Power Operation- The device operates with reduced filtering and current consumption.
- Power Down - The device is turned OFF except for the crystal oscillator and associated reference clock buffers which are kept active. The integrated superfilter providing the supply to the VCO is also kept ON for PLL start-up purposes.
- Deep Sleep - The device is fully disabled and the power consumption is reduced to a minimum.

1.5 Block Diagram

Following depicts the block diagram of the MC44CD03 chip and several external components. The receive path starts with a SAW filter very close to the antenna which converts the single ended input to a differential output (Zo=100 ohms differential). An LC network is used to match the impedance between the SAW filter and the ~90 ohms differential RF inputs (RF_IN, RF_INB) of the chip.

The RF section of the MC44CD03 is made of an internal Low Noise Amplifier (LNA) with AGC, a set of quadrature mixers, a Post Mixer Amplifier, and an integrated 3.5GHz VCO controlled by a PLL.

The LNA with AGC drives the quadrature mixers that convert the RF signal to baseband quadrature I and Q. The output of the mixer connects directly to the post-mixer amplifier (PMA). Integrated capacitors are used to provide a primary low frequency filtering pole at the mixer and PMA outputs.

The local oscillator (LO) signal is provided by a fully integrated VCO running at twice the desired frequency that drives a divide-by-2 quadrature generator. The frequency synthesis is made by means of an integer mode PLL with 500kHz PD reference frequency. The VCO supply voltage is provided by an on-chip low noise voltage regulator (“super-filter”).

The baseband section comprises two separate I and Q paths, each containing a post mixer amplifier (PMA) with register controlled gain adjustment capability, a channel filter (4th order inverse Chebyshev) with AGC stages, a complementary low-pass filter (2nd order Butterworth), and an output buffer. The baseband signal path has 8 filtering poles distributed between mixer and PMA (2 poles), the channel filter poles (4 poles), and 2 additional poles for GSM blocker filtering. In the case where no adjacent channels are present, the Chebyshev filter can be disabled for reduced power consumption. In the case where an anti-aliasing filter AAF is integrated into the baseband demodulator, the 2nd order Butterworth can be disabled for reduced power consumption.

A 36 MHz or 26MHz crystal oscillator provides the reference clock to the baseband demodulator .

The IC is controlled through an Inter IC (I2C) bus.

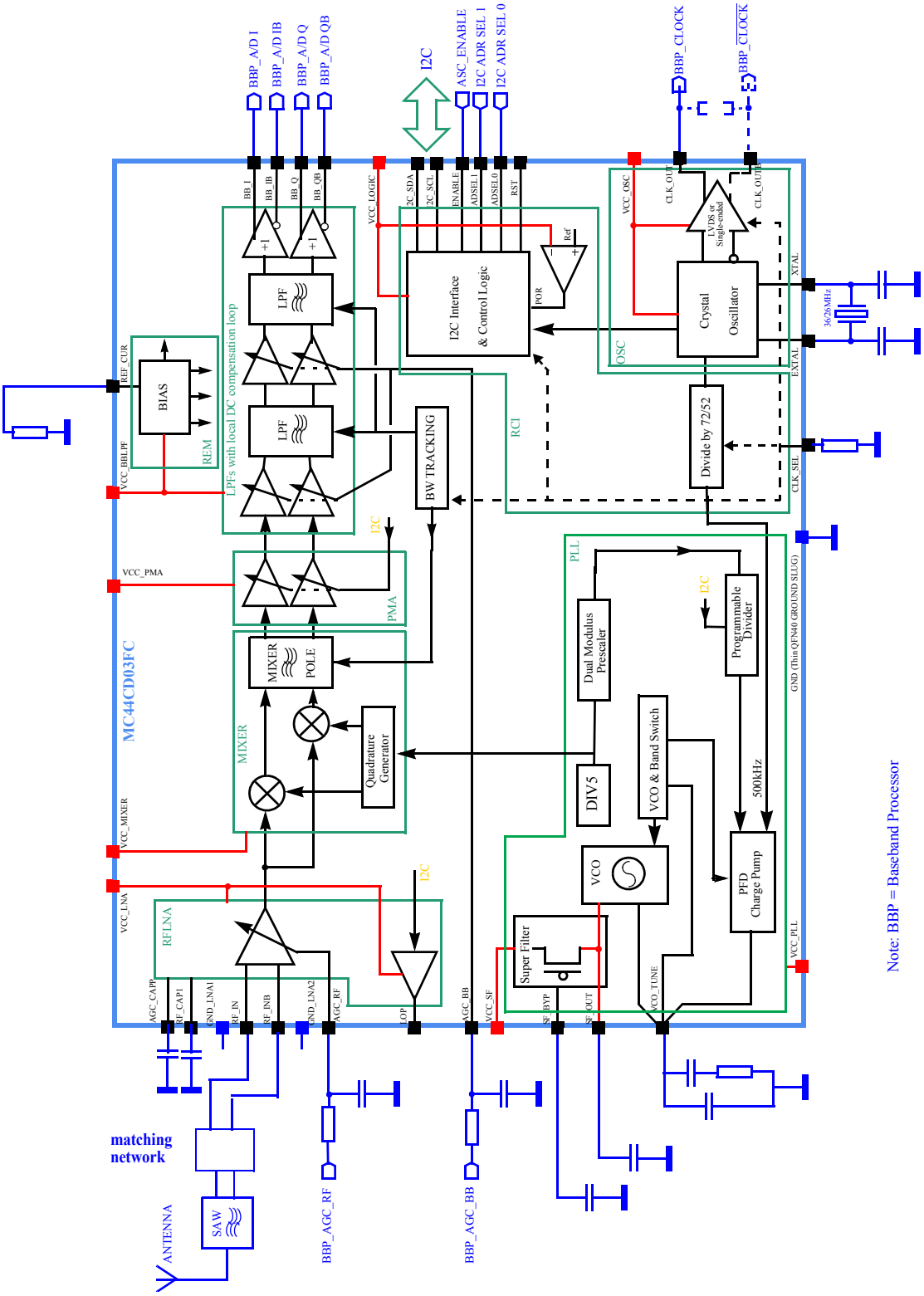


Figure 1-2 Simplified Block Diagram of SAM Chip and External Components

Section 2 Pin Description

2.1 MC44CD03 Pin Assignment & Package

The MC44CD03 chip is mounted in a lead free 40 pin Thin QFN package (0.65mm max. thickness) with exposed die pad. This exposed flag (“slug”) permits an improved ground connection. This housing exhibits a 6x6 mm^2 footprint and uses a 0.5mm pitch. For guidelines concerning Printed Circuit Board (PCB) design and assembly, package performances such as thermal resistance or Moisture Sensitivity Level (MSL) ratings please refer to application note (reference [3]).

WARNING

Most of the internal ground pins as well as the substrate of the IC are connected to the exposed pad. The exposed pad must be grounded in the application.

The MC44CD03 pin assignment in the Thin QFN40 package is shown in **Figure 2-1**.

Pins declared as NC (Not connected) have no corresponding internal connection, and have no constraint at the application level.

Pins declared as RESERVED are dedicated to test analysis and must be left floating at application level.

The reset pin 15 (RST), when not used, can be left uncommited as it makes use of an internal pull-down resistor.

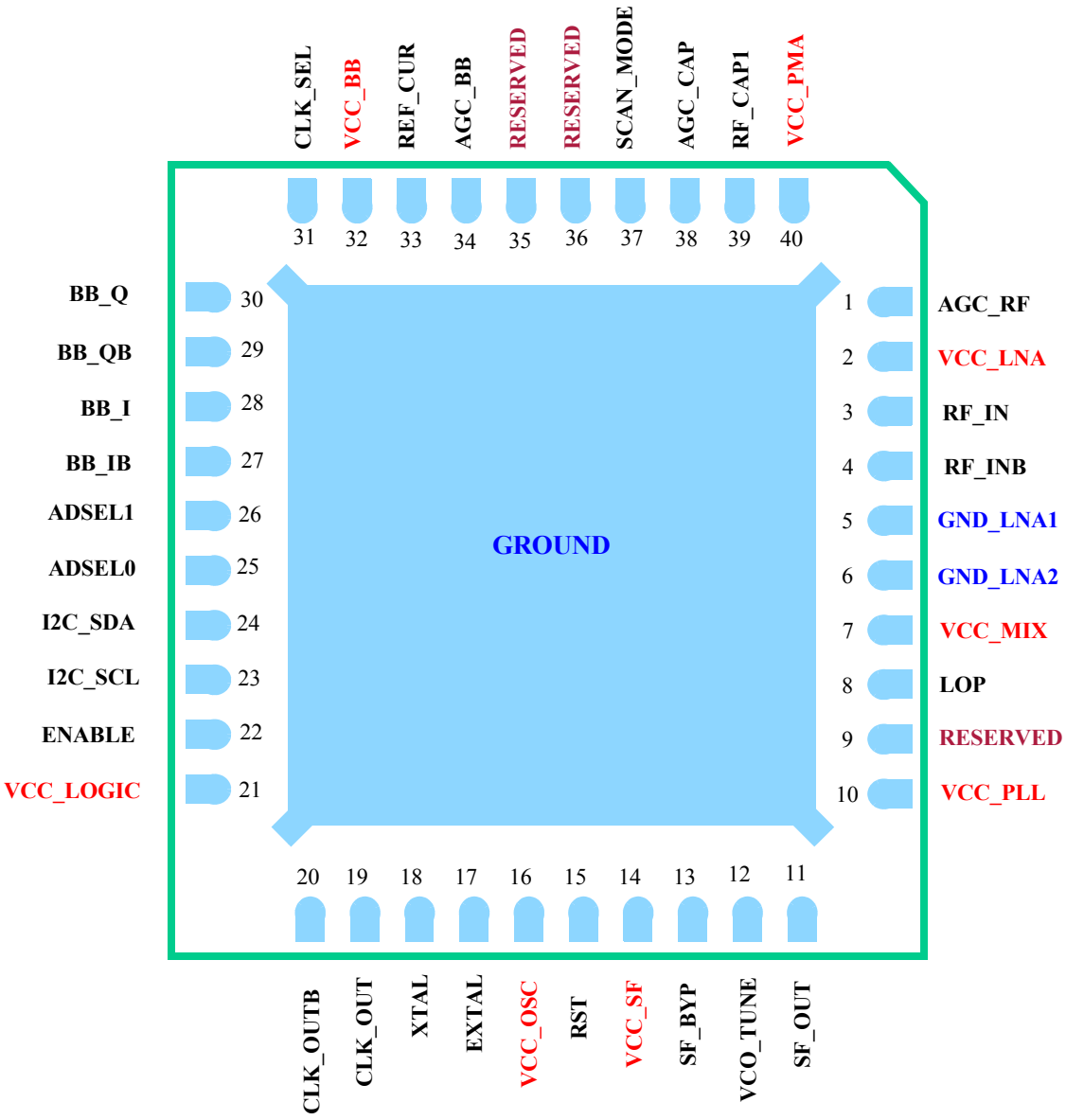


Figure 2-1 MC44CD03 Thin QFN40 Package Bottom View Showing The Ground Slug

2.2 MC44CD03 Pin List

Following **Table 2-1** summarizes the description of every pin bonded in the Thin QFN40 production package.

Table 2-1 MC44CD03 Thin QFN40 Pin List

Pin Number	Pin Name	Pin Description	Nature	Type
1	AGC_RF	RF LNA AGC control voltage	I	Analog
2	VCC_LNA	LNA power supply	P	Supply
3	RF_IN	RF input	I	Analog
4	RF_INB	RF $\overline{\text{input}}$	I	Analog
5	GND_LNA1	LNA ground (1)	P	Supply
6	GND_LNA2	LNA ground (2)	P	Supply
7	VCC_MIXER	Mixer supply	P	Supply
8	LOP	Logical Output Port	O	Digital
9	RESERVED	Reserved	R	Test
10	VCC_PLL	PLL part supply	P	Supply
11	SF_OUT	Super Filter output voltage	C	Analog
12	VCO_TUNE	VCO tuning voltage	I/O	Analog
13	SF_BYP	Super Filter bypass capacitor	C	Analog
14	VCC_SF	Super Filter supply	P	Supply
15	RST	Reset	I	Digital
16	VCC_OSC	Crystal oscillator supply	P	Supply
17	EXTAL	Crystal oscillator input	I	Analog
18	XTAL	Crystal oscillator output	O	Analog
19	CLK_OUT	Reference clock buffered output	O	Digital
20	CLK_OUTB	Reference clock buffered $\overline{\text{output}}$	O	Digital
21	VCC_LOGIC	Control logic supply	P	Supply
22	ENABLE	Enable control pin for deep slep mode	I	Digital
23	I2C_SCL	I2C clock	I	Digital
24	I2C_SDA	I2C data	I/O	Digital
25	ADSEL0	I2C physical address selection bit 0	I	Digital
26	ADSEL1	I2C physical address selection bit 1	I	Digiital
27	BB_IB	I baseband $\overline{\text{output}}$ signal	O	Analog
28	BB_I	I baseband output signal	O	Analog

Table 2-1 MC44CD03 Thin QFN40 Pin List

Pin Number	Pin Name	Pin Description	Nature	Type
29	BB_QB	Q baseband $\overline{\text{output}}$ signal	O	Analog
30	BB_Q	Q baseband output signal	O	Analog
31	CLK_SEL	Multi-level pin for Reference clock and Clock output Configuration	I	Analog
32	VCC_BB	Baseband filter supply	P	Supply
33	REF_CUR	Reference current	C	Analog
34	AGC_BB	Baseband AGC control voltage	I	Analog
35	RESERVED	Reserved	R	Test
36	RESERVED	Reserved	R	Test
37	SCAN_MODE	Scan chain mode entry	I	Digital
38	AGC_CAP	AGC decoupling cap	C	Analog
39	RF_CAP1	RF decoupling capacitor	C	Analog
40	VCC_PMA	Post mixer amplifier supply	P	Supply
EXPOSED FLAG	GND	General Ground	P	Supply

Table 2-2 Pin Nature Description

Nature	Description
I	Input
O	Output
I/O	Input/Output
P	Power (VCC or GND)
R	Reserved
NC	Internally not connected
C	Passive Components (loop filters, filtering or storage capacitor)

Section 3 I2C Communication And Registers

3.1 Overview

This section describes the MC44CD03's memory map and registers accessible through the I2C interface. The full control of the chip is accomplished via the 2-wires I2C-bus used as either slave-receiver or slave-transmitter. The MC44CD03 chip is fully compliant with the I2C-bus specification standard version 2.1. Up to 400kbit/s bus speed can be used in accordance with the I2C Fast-Mode specifications. The I2C interface stage is electrically 1.8V and 2.7V compliant.

The I2C interface of MC44CD03 cannot be used in deep-sleep mode. The address made of seven bits out of which the five most significant bits are set to 11000 as per the I2C requirements. Through a monitoring of the state of the pins ADSEL0 and ADSEL1, it is possible to modify the actual device I2C address out of four possible choices to accommodate systems where more than one MC44CD03 chip sits in the same bus (for antenna diversity reasons in mobile applications for example). The device address as a function of the ADSEL0 and ADSEL1 pins in case of both read and write operations is indicated in **Table 3-1**.

Table 3-1 MC44CD03's I2C Device Address vs. ADSEL1 & ADSEL0 Pins State

A6	A5	A4	A3	A2	A1 = ADSEL1	A0 = ADSEL0	R/$\overline{W}$	I2C Device Address
1	1	0	0	0	0	0	0	$C0
1	1	0	0	0	0	0	1	$C1
1	1	0	0	0	0	1	0	$C2
1	1	0	0	0	0	1	1	$C3
1	1	0	0	0	1	0	0	$C4
1	1	0	0	0	1	0	1	$C5
1	1	0	0	0	1	1	0	$C6
1	1	0	0	0	1	1	1	$C7

The MC44CD03 device supports the sub-addressing in order to speed up the write access of the register map. The read operation conforms to classical I2C practices. **Figure 3-1** depicts the write and read messages.

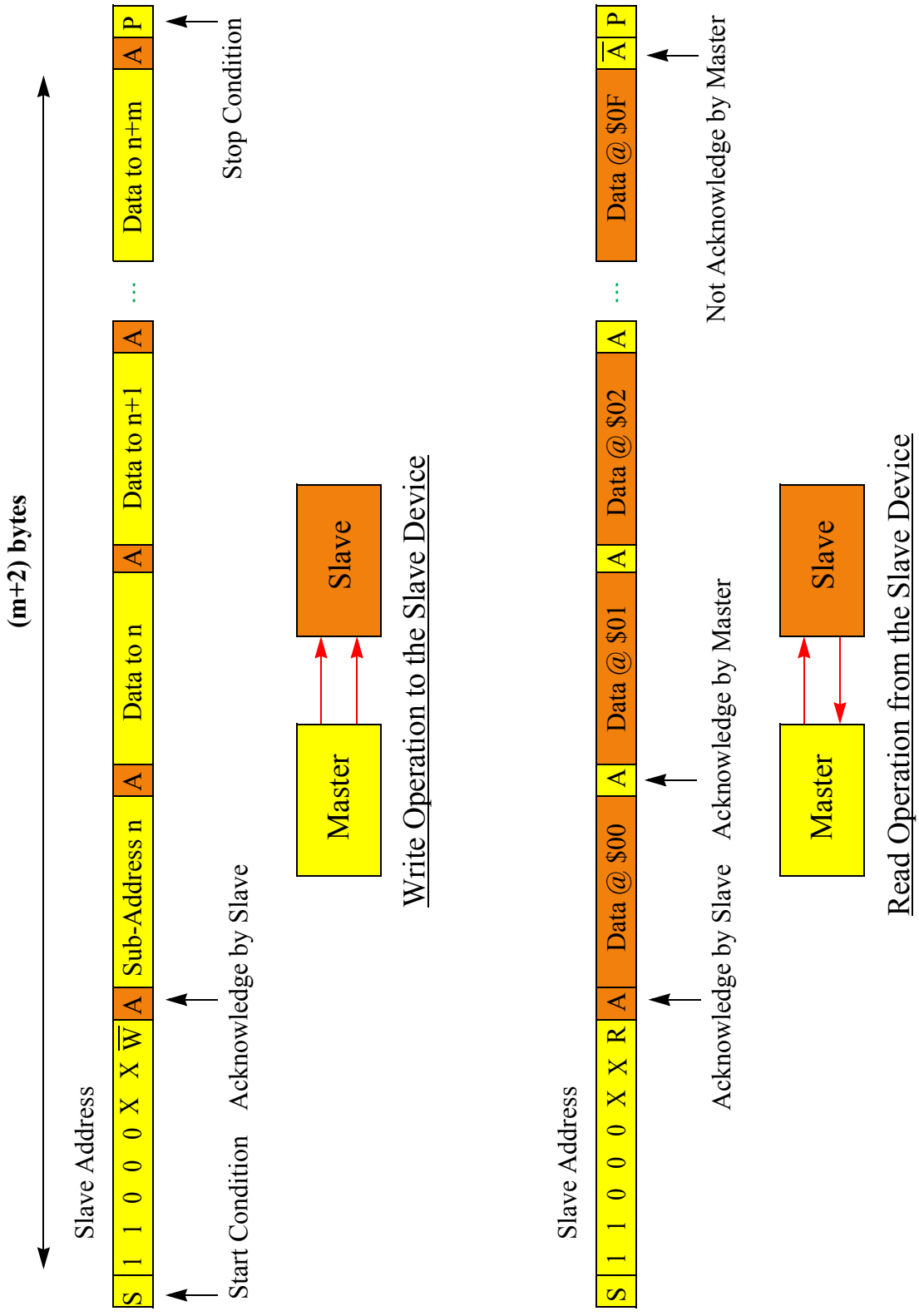


Figure 3-1 I2C Write & Read Operations

3.2 Memory Map

MC44CD03 contains a set of 16 registers in the $00 to $0F address space. The user registers constitute the bottom of the register addressable space while test registers are placed at the higher sub-addresses. A summary of these registers is given in **Table 3-2** while their accessibility in normal mode is detailed in section **3.3**.

Table 3-2 MC44CD03 Register Map

Register Name	Register Address	Description	Reset Value
MODE	$00	Mode Register	$00
PLLR1	$01	PLL Control Register #1	$05
PLLR2	$02	PLL Control Register #2	$3A
LNACR1	$03	LNA Control Register #1	$05
SPARE_REG	$04	Spare Register. No bits used.	$00
LNAOSCR	$05	Low Noise Amplifier & Oscillator Control Register	$20
MISCR	$06	Miscellaneous Control Register	$00
MDTST1	$07	Reserved	$00
MDTST2	$08	Reserved	$00
LPFTST	$09	Reserved	$00
PLLTST1	$0A	Reserved	$00
PLLTST2	$0B	Reserved	$04
RFTST	$0C	Reserved	$00
TLTST	$0D	Reserved	$00
VTBSTA	$0E	Reserved	$00
TLSTA	$0F	Reserved	$00

3.3 Register Descriptions

3.3.1 MODE — Mode Register

The MODE register dictates MC44CD03's operating mode.

Register address $00

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	PDM	PLLBI	TSTM
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-2 MC44CD03 Mode Register (MODE)

Bits 2-0 of the MODE register are readable and writable anytime. Bits 7-3 cannot be written and always read "0".

PDM — Power Down Mode.

If the ENABLE pin is held high, this bit places the MC44CD03 chip in power down mode with only the oscillator core and associated output clock drivers activated. This feature is used in case of time slice operation where the receiving of the DVB-H signals is pulsed with a low duty cycle to save power consumption. The ENABLE pin has precedence over the PDM control bit, which means that whenever the ENABLE pin is held low, the PDM bit state is cleared and the part placed in deep sleep mode.

1 = MC44CD03 chip is in power down mode if the ENABLE pin is asserted.
0 = MC44CD03 chip is in normal mode if the ENABLE pin is asserted.

PLLBI — PLL Band Change Inhibit.

This bit freezes the PLL VCO and associated sub-band in its current operating configuration. This feature is useful to rapidly regain lock after the circuit has been placed in a power saving mode.

1 = Band lock activated.
0 = Band lock de-activated (automatic VCO and sub-band searching is possible).

TSTM — Analog Test Mode.

The setting of the TSTM bit places the chip in test mode.

1 = Test mode is activated.
0 = Test mode is not activated.

Asserting the TSTM bit by itself does not produce any modification to MC44CD03's operation, it simply enables test functions to be activated and test outputs to be observed. The reset values of the test bits are read at 0 in normal mode.

3.3.2 PLLR1 — PLL Control Register #1

The PLLR1 register contains the refclk bit along with the three most significant bits of the programmable divider.

Register address $01

	7	6	5	4	3	2	1	0
R	0	0	0	0	REFCLK	PD10	PD9	PD8
W								
Reset:	0	0	0	0	0	1	0	1

= Unimplemented or Reserved

Figure 3-3 PLL Control Register #1 (PLLR1)

In all mode, bits 3-0 of the PLLR1 register are readable and writable anytime. Bits 7-4 cannot be written and always read “0”.

REFCLK— Sets the chip in line with the reference clock frequency used (either 36MHz or 26MHz reference clock).

Only active when the I2C bit PADCTRL (reg $05) is set to 1 (otherwise, as PADCTRL=0, the reference clock frequency is controlled by the multi-level pin#31 CLK_SEL).

1 = 26MHz
0 = 36MHz

PD10-8 — Programmable Divider MSBs.

These three bits are complemented by the 8 bits of the PLLR2 register to form the 11 bits used to define the programmable divider ratio part of the PLL feedback divider. A sequential logic exists to transfer the register bits PD[10:0] into the programmable divider when it has finished to count-down.

WARNING

Any change in the programmable divider ratio must be performed using two write operations in any order in any of the PLLR1 (3 MSBs) and PLLR2 (8 LSBs) registers. There is no need for the two write operations to take place within two consecutive cycles.

WARNING

It is forbidden to write PD<10:0>=$0000 in the PLLR1 and PLLR2 registers as this value jeopardizes the programmable divider functioning.

If we call PD the decimal content of the 11 bits constituting the programmable divider ratio, the synthesized LO frequency is given by the following equation:

$$F_{LO}\ [MHz] = PD \times 5/4$$

For instance, in order to lock in the channel centered at 1672.5MHz, PD<10:0> must be programmed at 1338 (dec).
Note that the VCO inside the PLL module runs at a frequency equals to 2x F_{LO}.

3.3.3 PLLR2 — PLL Control Register #2

The PLLR2 register contains the 8 LSBs of the programmable divider ratio.

Register address $02

	7	6	5	4	3	2	1	0
R W	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Reset:	0	0	1	1	1	0	1	0

= Unimplemented or Reserved

Figure 3-4 PLL Control Register #2 (PLLR2)

All bits in the PLLR2 register are readable and writable anytime. See description and warnings in the previous section.

3.3.4 LNACR1— Low Noise Amplifier Control Register #1

The LNACR1 register contains bits to control the Low Noise Amplifier operation.

Register address $03

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	CF_SEL1	CF_SEL0	LNACUR0
W								
Reset:	0	0	0	0	0	1	0	1

= Unimplemented or Reserved

Figure 3-5 Low Noise Amplifier Control Register #1 (LNACR1)

In all modes, bit 2-0 in register LNACR1 are readable and writable anytime. Bits 7-3 cannot be written and always read “0”.

CF_SEL[1:0]— Tunes centre frequency of LNA.

LNACUR0 — LNA Drain Current Selector.

Selects between normal and high current drain in LNA.
1 = Normal current mode.
0 = High current mode for improved IIP3 performances.

3.3.5 SPARE_REG — Spare Register

The SPARE_REG includes unused bits.

Register address $04

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-6 Spare Register (SPARE_REG)

3.3.6 LNAOSCR — Low Noise Amplifier & Oscillator Control Register

The LNAOSCR register contains bits to adapt the RFAGC loop and to control the clock output buffer.

Register address $05

	7	6	5	4	3	2	1	0
R W	CLKBUF	CLKDD	ALC1	ALC0	ILVDS	PADCTRL	AGCOFF1	AGCOFF0
Reset:	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-7 Low Noise Amplifier & Oscillator Control Register (LNAOSCR)

In all modes, bits 7-0 in register LNAOSCR are readable and writable anytime.

CLKBUF — Reference Clock Buffer Selector.

This bit selects either the single-ended or LVDS buffer. Only active when the I2C bit PADCTRL (reg $05) is set to 1 (otherwise, as PADCTRL=0, the reference clock buffer selection is controlled by the multi-level pin#31 CLK_SEL).

1 = The single-ended buffer is selected.

0 = The LVDS buffer is selected.

CLKDD — Reference Clock Output Driver Disable.

In case the reference clock generated by the MC44CD03 chip is not used, the CLKDD bit can be set HIGH to switch OFF the corresponding output driver (pins CLK_OUT, CLKOUTB), hence saving power consumption and minimizing radiated emissions.

1 = Reference clock output driver is disabled.

0 = Reference clock output driver is enable.

ALC1-0 — Amplitude Oscillator Control.

Determines according to **Table 3-3** the peak to peak sinewave clock amplitude at the XTAL pin.

Table 3-3 Crystal Oscillator Sine Wave Amplitude vs. ALC[1:0]

ALC[1:0]	Sine Wave Amplitude (Vpp)
00	-
01	-
10	1
11	-

ILVDS — Selects the LVDS buffer output current OR the Single-Ended buffer Clock Shape.

This bit can either select the output current of the clock output customized LVDS buffer if this buffer is selected or selects the single-ended buffer clock shape.

1 = The output current is set to 1mA if the LVDS buffer is selected (CLKBUF=0) or sets the CMOS 1.8V square wave if the single-ended buffer is selected (CLKBUF=1).

0 = The output current is set to 500uA if the LVDS buffer is selected (CLKBUF=0) or sets the sine like wave if the single-ended buffer is selected (CLKBUF=1).

PADCTRL — Gives priority either to the multi-level pin#31 CLK_SEL or to the I2C to configure the MC44CD03 chip and its clock outputs with regards to the reference clock frequency and the application requirements.

1 = The I2C bits REFCLK (reg $01) and CLKBUF ($05) have priority.

0 = The multi-level pin#31 CLK_SEL has priority.

WARNING

When using the PADCTRL bit, two I2C messages are needed to program the device properly because of the registers order.

First I2C message: Write PADCTRL=1.
Whatever value is written during the same message in REFCLK bit will be ignored.

Second I2C message: Rewrite PADCTRL=1. REFCLK value will be taken into account.

AGCOFF1-0 — AGC Loop Offset Selector.

These 2 bits control the offset of the AGC loop as indicated **Table 3-4**.

Table 3-4 AGC Loop Offset vs. AGCOFF[1:0]

AGCOFF[1:0]	RFAGC Knee voltage shift relative to nominal (mV)
00	0

Table 3-4 AGC Loop Offset vs. AGCOFF[1:0]

AGCOFF[1:0]	RFAGC Knee voltage shift relative to nominal (mV)
01	NOT TO BE USED
10	NOT TO BE USED
11	NOT TO BE USED

3.3.7 MISCR— Miscellaneous Control Register

The MISCR register contains bits controlling the post-mixer amplifier (PMA), the anti-aliasing lowpass filter, the Logical Output Port (LOP) state, and some PLL test feature.

Register address $06

	7	6	5	4	3	2	1	0
R	PFDTST0	0	LNABO	LNAGS	PMAG1	PMAG0	AAFD	CHEBD
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-8 Miscellaneous Control Register (MISCR)

In all modes, bits 5-0 and bit 7 in register MISCR are readable and writable anytime. Bits 6 cannot be written and always read “0”.

PFDTST0 — PLL Test Feature.

To be left at 0 (reset value) for normal operation.

LNABO — Topology of the Logical Output Port.

1 = The LOP buffer exhibits an open-drain, pull-down output.
0 = The LOP buffer exhibits a CMOS output.

LNAGS — State of the Logical Output Port.

1 = Pad LOP receives a logical “1”.
0 = Pad LOP receives a logical “0”.

PMAG1-0 — Post Mixer Amplifier Gain Setting.

The Post-Mixer Amplifier gain as a function of the state of the PMAG bits is indicated in **Table 3-5**.

Table 3-5 PMA gain vs. PMAG[1:0]

PMAG[1:0]	Gain (dB)
00	13

Table 3-5 PMA gain vs. PMAG[1:0]

PMAG[1:0]	Gain (dB)
01	11
10	15
11	13

AAFD — 2nd order Butterworth complementary low pass filter disable.

This bit disable the second-order butterworth low pass filter at the output of the fourth-order Chebyshev filter.

1 = Complementary filter disable.
0 = Complementary filter enable.

CHEBD — 4th order inverse Chebyshev channel filter disable.

This bit disable the two 2nd-order Chebyshev low pass filter.

1 = Disable the filter.
0 = Enable the filter.

3.3.8 MDTST1 — Module Disable Test Register #1

MDTST1 is a register reserved for test purposes.

Register address $07

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-9 Module Disable Test Register #1 (MDTST1)

In normal mode, the MDTST1 register reads $00 and cannot be written.

3.3.9 MDTST2 — Module Disable Test Register #2

MDTST2 is a register reserved for test purposes.

Register address $08

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-10 Module Disable Test Register #2 (MDTST2)

In normal mode, the MDTST2 register read $00 and cannot be written.

3.3.10 LPFTST — Baseband Low Pass Filter Test Register

LPFTST is a register reserved for test purposes

Register address $09

	7	6	5	4	3	2	1	0
R W	0	0	0	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-11 Baseband Low Pass Filter Test Register (LPFTST)

In normal mode, the LPFTST register reads $00 and cannot be written.

3.3.11 PLLTST1 — PLL Test Register #1

PLLTST1 is a register reserved for test purposes

Register address $0A

	7	6	5	4	3	2	1	0
R W	0	0	0	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-12 PLL Test Register #1 (PLLTST1)

In normal mode, register PLLTST1 reads $00 and cannot be written.

3.3.12 PLLTST2 — PLL Test Register #2

PLLTST2 register reserved for test purposes.

Register address $0B

	7	6	5	4	3	2	1	0
R W	0	0	0	0	0	0	0	0
Reset:	0	0	0	0	0	1	0	0

= Unimplemented or Reserved

Figure 3-13 PLL Test Register #2 (PLLTST2)

In normal mode, register PLLTST2 reads $00 and cannot be written.

3.3.13 RFTST — RF Blocks Test Register

RFTST is a register reserved for test purposes.

Register address $0C

	7	6	5	4	3	2	1	0
R W	0	0	0	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-14 RF Blocks Test register (RFTST)

In normal mode, the RFTST register reads $00 and cannot be written.

3.3.14 TLTST — Tracking Loop Test Register

TLTST is a register reserved for test purposes.

Register address $0D

	7	6	5	4	3	2	1	0
R W	0	0	0	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-15 Tracking Loop Test Register (TLTST)

In normal mode, the TLTST register read $00 and cannot be written.

3.3.15 VTBSTA — VCO Tuning Band Status Register

VTBSTA is a register reserved for test purposesTable3-15.

Register address $0E

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-16 VCO Tuning Band Status Register (VTBSTA)

In normal mode, the VTBSTA register reads $00 and cannot be written.

3.3.16 TLSTA — Tracking Loop Status Register

TLSTA is a register reserved for test purposes.

Register address $0F

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-17 Tracking Loop Status Register (TLSTA)

In normal mode, the TLSTA register reads $00 and cannot be written.

Section 4 Functional Description

The following sub-sections address some general key points about the MC44CD03 device operation and detail the functional descriptions of each sub-block in their respective operating modes.

4.1 Modes Of Operation

The MC44CD03 device includes four different power modes controlled by a combination of hardware (ENABLE pin) and software (state of the PDM bit in the MODE register at I2C address $00 and low power mode bits LPFD and AAFD of the BB section at I2C address $06). The modes are summarized in **Table 4-1**. The PDM bit is automatically reset to 0 while entering in Deep Sleep mode. It is therefore impossible to switch from Deep Sleep to Power Down mode without going though the Normal mode. Finally, MC44CD03 requires 20ms to be stable when waking-up from Power Down mode to Normal mode, and 200ms when waking-up from Deep Sleep mode to Normal mode.

Table 4-1 Power Operating Mode vs. ENABLE & PDM States

ENABLE Pin	PDM Bit	AAFD bit	LPFD bit	Mode
0	X[1]	X[1]	X[1]	Deep Sleep
1	0	0	0	Normal
1	0	1	0	Low Power
		0	1	
		1	1	
1	1	X[1]	X[1]	Power Down

NOTES:
1. Don't Care.

4.1.1 Normal Operation Mode

This is the normal operating mode of the receiver where all the internal stages are activated.
In this mode, the current consumption under typical conditions (VCC=2.775V and Temp.=27°C) is defined in the General MC44CD03 Electrical Specification, appendix A.3, ID 1.1.

4.1.2 Low Power Operation Modes

The filtering in the baseband section can be programmed, depending on the adjacent channel scenario, and filter partitionning at system level.

If there are no adjacent channels, the 4th order inverse Chebyshev channel filter can be turned off (LPFD=1), thereby reducing the total power consumption by typically 30mW.

If there is no need for attenuation at remote frequencies (177.7MHz offset spec), the 2nd order Butterworth complementary low pass filter can be turned off as well (AAFD=1), for a total power savings of typically 15mW.

Both low power modes can be cumulated for a typical total saving of 45mW. These settings do not modify the AGC capabilities of the baseband section.

4.1.3 Power Down Mode

In this mode MC44CD03will have a very low current drain. The 36/26 MHz reference oscillator core and its buffer are activated to provide the clock signal to the baseband demodulator. The logic section remains powered such that the received channel settings remain stored in their corresponding I2C registers. The superfilter (that provides the supply voltage to the VCO) is also activated to reduce VCO/PLL settling times. All the others blocks are disabled.
In this mode, the current consumption under typical conditions (VCC=2.775V and Temp.=27°C) is defined in the General MC44CD03 Electrical Specification, appendix A.3, ID 1.2.

4.1.4 Deep Sleep Mode

This mode is intended to have the lowest current drain. All stages are fully disabled except the power-on reset function which continuously monitors the voltage on the VCC_LOGIC pin to produce a reset and then place the chip in a known configuration in case of power failure or brown-out. The logic section remains powered and the received channel settings remain stored in their corresponding I2C registers. The circuit enters into deep-sleep mode through the control of an external pin that has priority on the power down/normal mode selection as shown in **Table 4-1**.
In deep-sleep mode, the reset (external pin RST) function, the address select (external pins ADSEL0 and ADSEL1) function, and the IC configuration with regards to clock requirements (external pin CLK_SEL) function are disabled. These functions are available when the circuit is in Normal, Low Power, or Power down modes only.

In this mode, the current consumption under typical conditions (VCC=2.775V and Temp.=27°C) is defined in the General MC44CD03 Electrical Specification, appendix A.3, ID 1.3.

4.2 Power Distribution And Consumption

Figure 4-1 is a diagram of the power distribution inside the MC44CD03 IC. In order to minimize disturbances between blocks and to permit efficient decoupling, the modules are powered using dedicated ground and power supply lines. At the package level, the availability of a ground slug which directly solders to the radio PCB under the Thin QFN40 case allows a low inductance, good quality ground connection to be available for the whole IC through down bonding to the flag of all the dedicated module grounds.

All the VCC pins are supposed to be connected to a single master VCC source with adequate capacitive decoupling as close as possible from the integrated circuit and in particular, a local, decoupling capacitor at the RF LNA level to get rid of the harmonics and keep only a clean DC current in the GND_LNA1,2 wires. A particular case concerns the powering of the VCO inside the PLL module. A voltage regulator

("super-filter") is in charge of supplying current to this critical part of the MC44CD03 IC. This is necessary to reach the expected phase noise performance.

The following **Table 4-2** illustrates the overall power consumption of the MC44CD03.

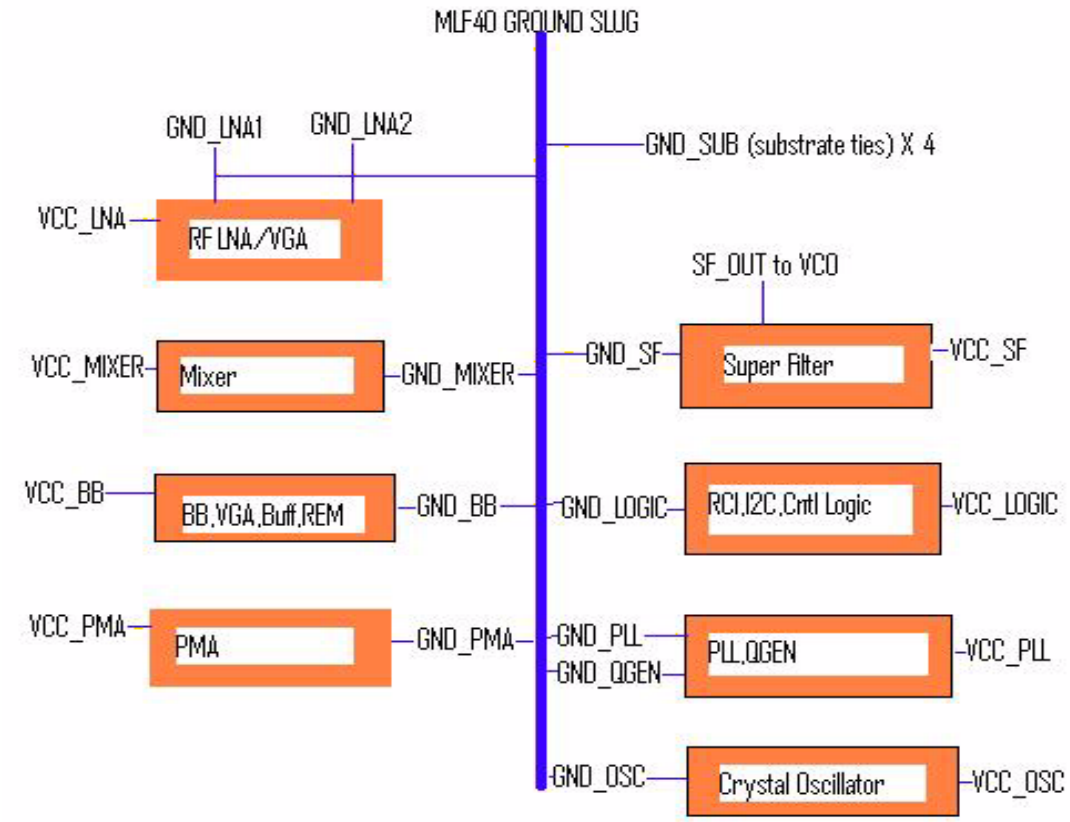


Figure 4-1 Power Distribution Chart Inside MC44CD03

Table 4-2 Power Consumptions in the MC44CD03 Chip

MODULE	BLOCK	VCC PIN	BLOCK CURRENT		Circuit Mode		
			High [1]	Low [2]	DEEP SLEEP	POWER DOWN	NORMAL
MC44CD03	WHOLE CHIP	ALL	TOTAL CURRENT [mA]		20 µA [2]	3.6 mA [1]	100.6 mA [1]
			POWER @ VCC=2.775V [mW]		55.5 µW [2]	10 mW [1]	280 mW [1]

NOTES:
1. Target values under typical conditions: VCC=2.775V and Temp.=27°C.
2. Maximum values over all supply voltages and temperature conditions.

4.3 Filtering

The overall characteristic is formed by the analog filtering in MC44CD03, and digital filtering in the baseband demodulator. Therefore the task of the MC44CD03 analog filter is to provide enough attenuation to the adjacent channel power in order not to saturate filtering stages in front of the baseband demodulator AD converter, and to provide sufficient stop-band attenuation to cope with the baseband IC ADC sampling requirements. The final channel filtering is performed digitally inside the baseband demodulator.

The system has to cope with different digital DVB-H adjacent channel interferers, and strong far away GSM blockers. The corresponding patterns are described in the system specifications document. Those patterns define the channel filtering performance the MC44CD03 chip must achieve.

The MC44CD03 channel filtering section consists of a 4^{th} order baseband channel low pass filter (inverse Chebyshev structure) with variable gain amplifiers and differential output buffers.

A first stage of additional filtering lies in the mixer and PMA output poles.

The MC44CD03 shall support a 5MHz channel bandwidth.

The inverse Chebyshev characteristic is chosen in order to have a limited amplitude ripple in the passband.

The channel filter is followed by the baseband complementary low pass filter AAFs (2nd order Butterworth structure) to provide the required stop band attenuation and remote frequency rejection.

The I/Q output signals are provided by output buffers for driving purposes. The I/Q signals must fulfill the following requirements:

- Differential signal amplitude: 1.4Vpp maximum;
- Baseband differential input resistance: 10kΩ minimum;
- Baseband input capacitance: 5pF maximum.Control LoopsControl Loops

4.4 Control Loops

4.4.1 AGC Loops

The non-interrupted mode of the OFDM modulation for DVB-H forces a quasi continuous control of the AGC correction loop.

The AGC system is split between RF AGC (in the LNA) and baseband AGC. Both those AGCs are controlled through two dedicated pins by analog signals provided by Sigma-Delta (ΣΔ) DACs at the baseband demodulator IC output.

The AGC correction algorithms are left to the baseband demodulator IC.

The Post Mixer Amplifier (PMA) also exhibits gain control capabilities (through I2C programming), but this capability is not part of AGC system.

4.4.1.1 RF AGC Control Loop

The AGC is directly controlled by an RC filtered pulse width modulated signal (filtered 1-bitΣΔ output) provided by the baseband demodulator with the following properties:

- Voltage range: from 0.1V to 1.8V.
- Impedance: RC filter with 10 kΩ in series and 22 nF to ground.

4.4.1.2 Baseband AGC control loop

AGC stages are inserted in the filtering chain in order to cover the overall dynamic range specifications. An AGC range of 35 dB minimum is required. Due to the large gain required in the baseband section, local DC offset correction loops for I and Q are necessary to avoid saturation in cascaded stages. For this purpose each channel has its specific DC cancellation loop with an external storage capacitor.

The AGC is directly controlled by a RC filtered pulse width modulated signal (filtered 1-bit ΣΔ output) provided by the baseband demodulator with the following properties:

- Voltage range: from 0.1V to 1.8V.
- Impedance: RC filter with 10 kΩ in series and 22 nF to ground.

4.4.2 DC Offset Correction

Despite the AC coupling on I/Q signals between the MC44CD03 device and the baseband processor, and due to the high gain level required at baseband stages, the baseband section includes local DC offset correction loops to avoid signal distortion. No interaction with the baseband demodulator IC is required.

4.4.3 Filter Tracking

The MC44CD03 chip supports single 5MHz OFDM modulation bandwidth. The filter calibration is ensured by an autonomous tracking bandwidth system derived from the crystal oscillator reference, with a maximum frequency drift of 6%|.

4.4.4 Common Mode Voltages

4.4.4.1 I/Q Buffers Outputs

The MC44CD03 chip and the baseband-demodulator IC are AC coupled (1kHz). No common mode voltage control loop is thus necessary.

4.4.4.2 CLK_OUT Outputs

The MC44CD03 chip either delivers a custom LVDS clock reference or a single-ended clock reference to the baseband processor. The reference clock buffer mode is selected by I2C programming.

The LVDS delivery of the clock reference between the MC44CD03 chip and the baseband processor implies the flowing of differential currents carrying the frequency information. A resistor is used at the baseband input level to generate a differential, small amplitude clock voltage. The common mode voltage

of the CLK_OUT and CLK_OUTB pins is derived from a very accurate bandgap reference voltage, and therefore requires no common mode feedback system to ensure proper interfacing between the two chips.

The single-ended buffer of the clock reference provides either a 1.8V CMOS signal or a sine-like 1.5Vpp signal with 0.9V common mode voltage on pin CLK_OUT, while pin CLK_OUTB remains open.

4.4.5 I/Q Mismatch

The whole I/Q static mismatch compensation is performed in the baseband demodulator IC, not in the RF front-end chip.

4.5 Reference Clock Configuration

The MC44CD03 chip is able to handle two different reference clock frequencies, 26MHz and 36MHz. This reference frequency is either generated by means of a crystal oscillator (using an external 26MHz or 36MHz crystal element connected between pin #17 EXTAL and pin #18 XTAL), or externally provided to the chip on its pin #17 EXTAL.
The MC44CD03 chip is also capable to provide two different clock output signal shapings (either custom LVDS or single-ended) to the baseband demodulator IC through the clock output pins #19 CLK_OUT and #20 CLK_OUTB.

At power on reset, a proper setting of the IC with regards to the reference clock frequency is suitable to fit the application requirements. Particularly, a correct power on reset configuration of the clock output signal is required, as this signal is potentially used to wake-up and clock the baseband demodulator IC.

Therefore, a multi-level pin (pin #31 CLK_SEL) is dedicated to adequately preset the MC44CD03 chip and its clock output signal in the configuration required by the application. See the MLP (multi-level pin) module description chapter for details.

4.6 RFLNA Functional Description

4.6.1 General

The purpose of this section is to detail the RFLNA module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Deep Sleep & Power Down Mode.

4.6.2 Normal Mode

The Normal mode corresponds to the RFLNA operating in the receive chain in a regular manner.

In the RF path, the MC44CD03's internal LNA is preceded by an external matching network which converts the LNA differential input impedance to 100Ω. A preceding external SAW filter is used to achieve a linear single-ended to differential conversion.

4.6.2.1 Low Noise Amplifier

The principal function of the LNA is to programmably amplify the differential input signal and drive the MIXER.

4.6.2.2 AGC

The LNA provides AGC capabilities using a current steering technique. The AGC is directly controlled on input pin AGC_RF (pin1) by an RC filtered pulse width modulated signal (a filtered 1-bit delta-sigma) provided by the baseband processor with the following properties:

- Voltage range: from 0.1V to 1.8V (Vcc=2.775V);
- Impedance: RC filter with 10kΩ in series and 22nF to ground.

The AGC characteristic is "linear in dB", with a 35dB/V slope nominally. Thus, max gain occurs when 1.8V nominally is applied to the AGC_RF pin, and decreasing this voltage reduces the LNA gain. The knee voltage from which the gain starts decreasing is set around 1.6V typically.

4.6.3 Deep Sleep & Power Down Mode

The LNA module will be in low power mode (current consumption <1µA nominally) when

- ENABLE (pin 22) is held at logic low
- ENABLE is held at logic high and the PDM bit (in the MODE register at 12C address $00) is asserted.

4.7 MIXER/QGEN Functional Description

4.7.1 General

The purpose of this section is to detail the MIXER/QGEN module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Deep Sleep & Power Down Mode.
3. Test Mode.

4.7.2 Normal Mode

The Normal mode corresponds to the MIXER/QGEN operating in the receive chain in a regular manner.

4.7.2.1 IQ Mixers

A differential I/Q downmixer converts the RF signal to baseband I and Q channels. A double balanced Gilbert Cell mixer is used for each I and Q section of the downconverter. The output of the downmixer is low-pass filtered prior to the PMA. This filter attenuates unwanted mixing results (27MHz cut-off frequency untracked).

4.7.2.2 Quadrature Generation

The VCO operates at 2x the RF receive frequency, hence local oscillator generation is achieved by means of a divide-by-2 circuit, with differential quadrature outputs taken from the master and slave latches within the D-type flip-flop implementing the divider function.

The VCO output directly feeds a buffer circuit at the QGEN input, which features a local feedback loop to correct for phase imbalances in the VCO by adjusting the buffered VCO signal to give a 50% duty-cycle. This is key to achieve accurate quadrature at the master-slave outputs of the divide-by-2 circuit.

4.7.2.3 Biasing

The MIXER and QGEN modules have their own internal PTAT/CTAT bias generators, and do not require connections to the REM block.

4.7.3 Deep Sleep & Power Down Mode

The MIXER and QuadGen modules will be in low power mode (current consumption <1µA respectively) when

- ENABLE (pin 22) is held at logic low.
- ENABLE is held at logic high and the PDM bit (in the MODE register at I2C address $00) is asserted.

4.8 PMA Functional Description

4.8.1 General

The purpose of this section is to detail the PMA module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Deep Sleep & Power Down Mode.

4.8.2 Normal Mode

The Normal mode corresponds to the PMA operating in the receive chain in a regular manner.

4.8.2.1 Principle of Operation

The PMA consists of two single ended unity gain buffers and a differential amplifier. These unity gain buffers then feed the differential amplifier. The basic topology of the PMA is an inverting amplifier that has both resistive and capacitive feedback which sets the pole of the filter.

The PMA has an untracked 3dB bandwidth of 38MHz and three gain settings. There is also a DC offset compensation circuit (DCOC) to remove any dc offsets that could saturate the baseband.

4.8.2.2 Gain Adjustment

The gain of the PMA is set by the ratio of the feedback resistor and the input resistor. To vary the gain the feedback resistor value is adjusteded by switching in different resistor sizes. This gain control is not part of the AGC but is controlled by the I2C. The PMA has three gain settings: 11dB, 13dB and 15dB.

4.8.2.3 DC Offset Compensation

The need for DCOC arises because of the offsets intoduced by the Mixer and PMA. In order to ensure that the Baseband section is not saturated the DCOC circuitry was added at the output of the PMA. A closed loop dc offset removal architecture is used. The offset compensation is done from the output of the PMA to the input of the PMA.

4.8.3 Deep Sleep & Power Down Mode

The PMA module will be in low power mode (current consumption <1µA) when

- ENABLE (pin 22) is held at logic low.
- ENABLE is held at logic high and the PDM bit (in the MODE register at I2C address $00) is asserted.

4.9 LPF Functional Description

4.9.1 General

The purpose of this section is to detail the LPF module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Deep Sleep & Power Down Mode.

4.9.2 Normal Mode

The Normal mode corresponds to the LPF operating in the receive chain in a regular manner.

4.9.2.1 Principle Of Operation

The overall filter characteristic is formed by the analog filtering in the MC44CD03 device, and digital filtering inside the baseband processor chip. Therefore the task of the internal analog filter is to provide enough attenuation to the adjacent channel power, but also to some remote frequency blockers (GSM blocker at 177.7MHz offset from the input band)in order not to saturate filtering stages at the baseband processor's inputs. The final channel filtering is performed digitally inside the demodulator chip. The filtering is dimensioned in order to cope with the baseband IC ADC sampling effects.

The LPF module filtering section consists of a 4^{th} order inverse Chebyshev low pass filter with AGC amplifiers (0-35dB range) required to match the DVB standard specifications, and output buffers. The mixer and PMA output poles (typically 30MHz) provide the 1st stages of filtering. The LPF module supports one single 5MHz channel bandwidth.

The inverse Chebyshev architecture was chosen for its sharp cutoff transition, and its maximally flat characteristic in the pass band. This filter is made of two Tow Thomas biquad filter structures with resistors and switched capacitors for bandwidth tracking (continuous transconductance structures are avoided because of their poor noise and linearity performances).

The complementary low pass filter is a second order Butterworth structure with a 4MHz 3dB cut-off frequency.

4.9.2.2 Bandwidth Tracking

A tracking bandwidth system compensates for temperature and process variations. A +/-6% maximum bandwidth drift is tolerated for the channel 4th order inverse Chebyshev filter. A 2% variation comes from the possible frequency offset of approximately 70kHz due to asynchronous down-conversion. The tracking bandwidth correction accuracy is thus fixed to 6%. This tracking system is autonomous, as it detects the frequency shift and automatically corrects it once 6% drift are reached (no need for external control), by switching the capacitors of the biquad structures. The bandwidth tracking range must cover the whole variations of temperature and process, typically +/- 35%.

The complementary 2nd order Butterworth low pass filter is not as tightly controlled, but has a +/-15% maximum bandwidth drift.

The tracking loop measures an RC time constant and using a four bit word selects the appropriate capacitor values in the biquad cells.

4.9.2.3 Gain Control

AGC stages are inserted in the filtering chain in order to cover the overall dynamic range specifications of the US DVB-H standard. Even if the MC44CD03 I/Q outputs are AC coupled to the baseband processor chip (1kHz cut-off frequency), and due to the large gain required in the MC44CD03 baseband section (+35dB min. AGC), local DC offset correction loops are necessary to avoid saturating the cascaded stages (see also **4.9.2.5**).

The AGC is directly controlled by a RC filtered pulse width modulated signal (filtered 1-bit SD output) provided by the baseband processor with the following properties:

- Voltage range: from 0.1V to 1.8V.
- Impedance: RC filter with 10kΩ in series and 22nF to ground.

The AGC characteristics is «linear in dB», with a +35dB/V slope nominally. Thus, max gain occurs when 1.8V nominally is applied to the AGC_BB pin, and decreasing this voltage reduces the BB gain. The «knee» voltage from which the gain starts decreasing is set around 1.6V typically.

4.9.2.4 Output buffers

There is a set of four single ended buffers that drive each of the I and Q phase signals (Ip, In, Qp and Qn signals). A compromise was found to try and drive the maximum possible load while keeping silicon area and current consumption as low as possible.

The nominal differential output load considered for the design is 10KOhm // 5pF.

4.9.2.5 DC Offsets Compensation

DC compensation is embedded on chip, and is provided around each VGA block inside the I and Q paths.

4.9.2.6 LPF Control Bits

Following **Table 4-3** summarizes the register bits required for controlling the baseband filter and its AGC system.

Table 4-3 LPF Control Bits

Bit name	Signal Names	Register @ address	Normal/ Test	Function
AAFD	aff_dis	MISCR @ $06	Normal	Disable Butterworth filter
LPFD	lpf_dis	MISCR @ $06	Normal	Disable Inverse Chebyshev channel filter

4.9.3 Deep Sleep & Power Down Mode

The LPF module will be in low power mode when:

- ENABLE (pin 22) is held at logic low.
- ENABLE (pin 22) is held at logic high and the PDM bit (in the MODE register at I2Caddress $00) is asserted.

In this mode the current consumption of respectively the LPF module and the output buffers is at most 3uA and 1uA.

4.10 OSC Functional Description

4.10.1 General

The purpose of this section is to detail the OSC module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Power Down Mode.
3. Deep Sleep

4.10.2 Normal Mode

The Normal Mode corresponds to the OSC module operating in a regular manner, i.e. in oscillation mode. The OSC module is set into normal mode once a high level is applied on the MC44CD03 input pin #22 ENABLE.

4.10.2.1 Crystal Oscillator Principle

The OSC module is made of a 36 or 26MHz crystal oscillator based on the Pierce architecture. The active part of the oscillator is integrated on chip (active device of the negative impedance and biasing), while the passive parts (feedback capacitors and 36/26MHz crystal element) are external and connected around the input pins #17 EXTAL and #18 XTAL.

The start-up of the oscillator is sped up by the use of a boost mode. The principle is to increase the biasing current at start-up, and to reduce it for normal mode operation after a pre-defined number of clocks is counted. This system ensures proper start-up and oscillation amplitude.

The 36 or 26MHz sinusoïdal oscillation signal is buffered and turned into a 36 or 26MHz CMOS signal, to provide the clock for the digital core of the MC44CD03 chip, the input clock of the reference divider of the PLL (division ratio eitheir 72 or 52 to generate 500kHz), and the reference clock for the baseband demodulator chip through the clock output buffer (either custom LVDS buffer driving the output pins #19 CLK_OUT and #20 CLK_OUTB, or the single-ended buffer driving the output pin #19 CLK_OUT).

4.10.2.2 Recommended Crystal Characteristics

The selected crystals are the NX3225DA 36MHz (W-191-563) or 26MHz (W-191-653) quartz's from the NDK company . The following **Table 4-4** and **Table 4-5** summarize their key characteristics.

Table 4-4 36MHz NX3225DA Quartz Key Characteristics

Feature	Typical Value
Operating Mode	Fundamental
Motional Inductance	4.90 mH
Motional Capacitance	3.99 fF
Motional Resistance[1]	50 Ω

Table 4-4 36MHz NX3225DA Quartz Key Characteristics

Feature	Typical Value
Case Capacitance	1 pF
Loading Capacitance	8 pF

NOTES:
1. Maximum value upon startup.

Table 4-5 26MHz NX3225DA Quartz Key Characteristics

Feature	Typical Value
Operating Mode	Fundamental
Motional Inductance	3.75 mH
Motional Capacitance	10 fF
Motional Resistance[1]	50 Ω
Case Capacitance	1 pF
Loading Capacitance	8 pF

NOTES:
1. Maximum value upon startup.

4.10.2.3 ALC Principle

Two I2C bits (ALC<1:0>) are dedicated to the setting of the biasing current of the active device of the oscillator, allowing a coarse control of the oscillation amplitude for crystal loading and phase noise optimization.

4.10.2.4 External Reference Clock

The EXTAL input pin of the OSC module can be used as the input gate for an external reference clock, that is then used as the reference clock for the whole chip including PLL. In that case, the OSC circuit does not behave anymore as a crystal oscillator (and the external crystal element and feedback capacitors must be removed from the application schematic - refer to the application information chapter of this document for additional details), but as as buffer for this reference clock.
Extreme care must be taken concerning the amplitude, duty-cycle, and jitter (phase noise) of the external reference clock not to impact digital core nor PLL performances. Constraints are detailed in the electrical specification chapters of this document.

4.10.2.5 Reference Clock Frequency

The MC44CD03 chip is able to handle two different reference clock frequencies 36MHz and 26MHz. Different modules of the chip (digital core, PLL, tracking loop filter, clock outputs...) need to be configured according to the reference clock frequency used.

As the I2C bit PADCTRL (reg $05) is held at logic low, the chip configuration with regards to the clock frequency is set by the DC level applied on multi-level pin#31 CLK_SEL (see the MLP Functional Description chapter for more details). As the I2C bit PADCTRL is turned high, the chip configuration is forced by the value of the I2C bit REFCLK (reg $01).
The reset value of the I2C bit PADCTRL is 0, such as at power on reset, priority is given to the multi-level pin#31 CLK_SEL to configure the MC44CD03 chip according to the reference clock frequency used.

4.10.2.6 Reference Clock Ouput Interface

Two different clock buffers LVDS or single-ended can be used for interfacing the 36 or 26MHz reference clock from the MC44CD03 chip to the baseband demodulator circuit. Both those buffers cannot be activated simultaneously.

As the I2C bit PADCTRL (reg $05) is held at logic low, the clock buffer selection is set by the DC level applied on multi-level pin#31 CLK_SEL (see the MLP Functional Description chapter for more details). As the I2C bit PADCTRL is turned high, the clock buffer selection is forced by the value of the I2C bit CLKBUF (reg $05) (see the I2C Communication and Registers chapter for more details).
The reset value of the I2C bit PADCTRL is 0, such as at power on reset, priority is given to the multi-level pin#31 CLK_SEL to configure the clock buffer according to the application requirements.

4.10.2.6.1 Custom LVDS interface

A custom Low Voltage Differential Signaling (LVDS) technology is used for interfacing the 36 or 26MHz reference clock from the MC44CD03 chip to the baseband demodulator circuit. Such a technology allows low noise and low electromagnetic interference spreading over the radio board.

If the LVDS buffer is selected, the MC44CD03 chip provides the 36 or 26MHz differential output currents on its output pins #19 CLK_OUT and #20 CLK_OUTB. The signal swing is generated through a load consisting of an external differential resistor. Two different current settings can be programmed through the I2C bit ILVDS (reg $05). The custom LVDS swing is developed around a common mode level that is derived from a bandgap voltage sufficiently accurate to avoid the use of any common mode control loop.

The LVDS buffer can be disabled by setting the I2C bit CLKDD to logic level high.

4.10.2.6.2 Single-ended Clock interface

A single-ended buffer is also available for interfacing the 36 or 26MHz reference clock from the MC44CD03 chip to the baseband demodulator circuit.

If the single-ended buffer is selected, the MC44CD03 chip provides the 36 or 26MHz output signal on the output pin #19 CLK_OUT. The output signal is either 1.8V CMOS shaped as the I2C bit ILVDS (reg $05) is set to 0, or 1.5Vpp analog-like as the I2C bit ILVDS (reg $05) is set to 1.

The single-ended buffer can be disabled by setting the I2C bit CLKDD to logic level high.

4.10.3 Power Down Mode

There is no Power Down Mode (PDM) for the OSC module. When the MC44CD03 chip is in PDM, the OSC module remains in Normal Mode, providing the reference clock to the digital core, and to the baseband demodulator circuit through the selected clock buffer (either custom LVDS or single-ended).

4.10.4 Deep Sleep Mode

In Deep Sleep Mode, the OSC module is turned off by removing its biasing current. Oscillations and derived clocks are disactivated. The OSC module is set into deep sleep mode once a low level is applied on the input pin #22 ENABLE.

4.11 PLL Functional Description

4.11.1 General

The purpose of this section is to detail the PLL module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Deep Sleep & Power Down Mode.

4.11.2 Normal Mode

The Normal mode corresponds to the PLL operating in the receive chain in a regular manner.

4.11.2.1 PLL Characteristics

The MC44CD03 chip is able to receive the DVB 5-MHz channels in the band ranging from 1667.5MHz to 1677.5MHz. The frequency synthesizer of the MC44CD03 chip is based on an integer mode PLL with 500 kHz reference frequency, derived from a 36 or 26 MHz crystal oscillator clock.

4.11.2.2 Loop Filter Considerations

Following **Figure 4-2** depicts the effective PLL loop filter. It can be noted that components Ri and Ci are actually parasitic components inside the MC44CD03 chip, nevertheless it is important to take them into account to be able to correctly predict the PLL behavior.

The choice of the loop bandwidth is mainly driven by phase noise, spur rejection considerations and stability. The major constraint is the integrated noise over the OFDM bandwidth 1kHz-2.5MHz. The PLL acts as a high pass filter for VCO noise, while adding its own noise source in its band (mainly charge pump and reference oscillator). The higher the PLL bandwidth , the more the PLL in-band noise sources contribute to the overall integrated noise, while VCO noise contribution decreases. The choice of the charge pump gain is therefore closely related to the PLL bandwidth and noise.

The PLL bandwidth must be sufficiently low to ensure a good rejection of the reference frequency spurs, falling into the OFDM bandwidth (at 500 kHz offset from carrier and harmonics). The level of those spurs will also be directly correlated to the quality of the matching between the up and down current sources of the charge pump.The target loop bandwidth has been set to 65kHz typical.

Lock time must also be considered for the choice of the PLL bandwidth.

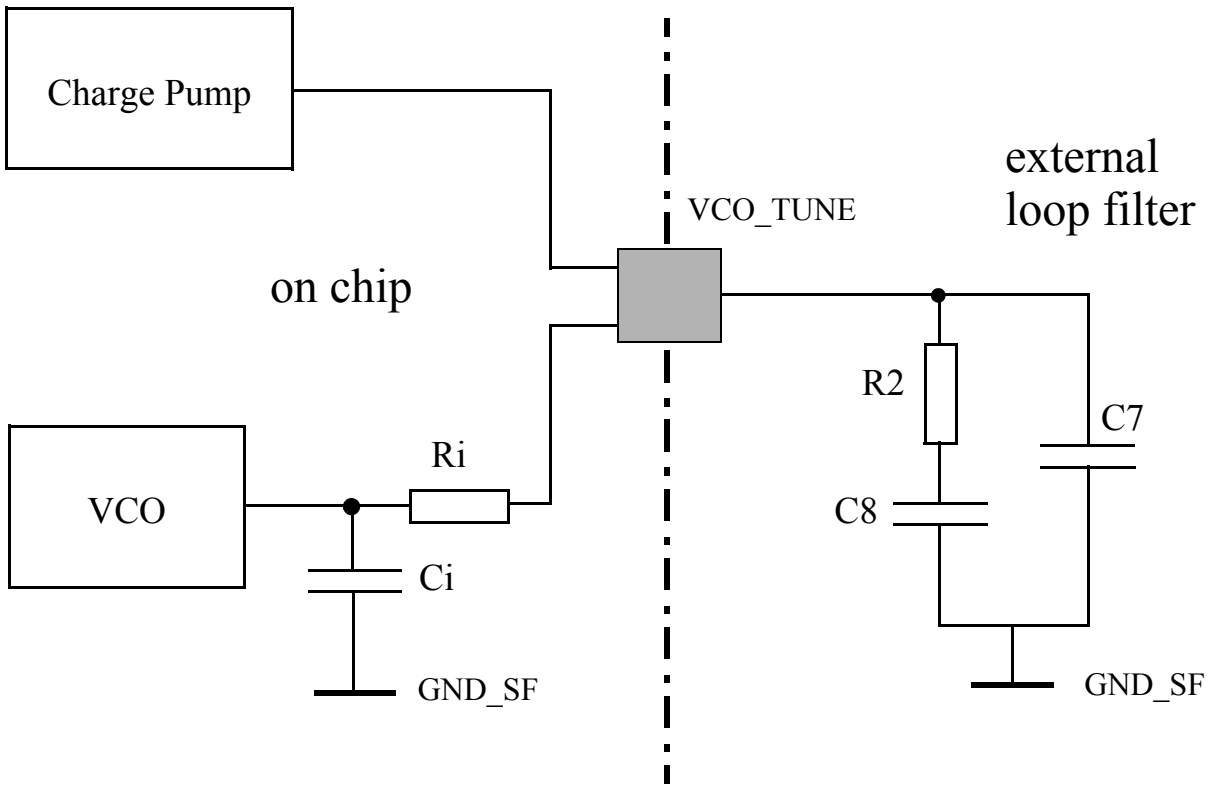


Figure 4-2 Effective PLL Loop Filter Schematic

4.11.3 Deep Sleep & Power Down Mode

The PLL module presents two different behaviours either when the IC is in Power Down mode or in Deep Sleep mode.

In Power Down mode (ENABLE (pin 22) is held at logic high and the PDM bit (in the MODE register at I2C address $00) is asserted, all the PLL blocks (charge-pump, frequency dividers, phase detector, VCOs...) are powered OFF, while the Superfilter providing the power supply to the VCOs remains active. The resulting current consumption under VCC_PLL is less than 1µA, while the current consumption under VCC_SF is around 400µA in typical conditions.

In Deep Sleep mode (ENABLE (pin 22) is held at logic low), all the PLL blocks are powered OFF. The resulting current consumption under VCC_PLL is less than 1µA, while the current consumption under VCC_SF is less than 1.5µA.

Figure 4-3

4.12 REM Functional Description

4.12.1 General

The purpose of this section is to detail the REM module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Deep Sleep & Power Down Mode.

4.12.2 Normal Mode

The Normal mode corresponds to the REM operating in the receive chain in a regular manner.

This block contains a bandgap voltage reference whose buffered output is distributed inside the chip as required by other blocks. The bandgap voltage is also used to generate currents defined by an external resistor connected to pin 33(REF_CUR). Those currents are then provided to some other blocks of the circuit.

4.12.3 Deep Sleep & Power Down Mode

The REM module will be in low power mode (current consumption <0.5µA) when

- ENABLE (pin 22) is held at logic low.
- ENABLE is held at logic high and the PDM bit (in the MODE register at I2C address $00) is asserted.

4.13 LOP Functional Description

4.13.1 General

The purpose of this section is to detail the LOP module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Deep Sleep & Power Down Mode.

4.13.2 Normal Mode

The Normal mode corresponds to the LOP operating as a digital output port, driving the output pin #8 LOP. The topology (CMOS output or open drain pull down output) and state of this pin are controlled by the I2C bits LNABO and LNAGS as described below.

LNABO — Topology of the Logical Output Port.
1 = The LOP buffer exhibits an open-drain, pull-down output with 35 Ohms maximum series resistor (large NMOS device connected to ground).
0 = The LOP buffer exhibits a CMOS output made of large devices (35 Ohms maximum series resistance for the NMOS - 120 Ohms maximum series resistance for the PMOS).

LNAGS — State of theLogical Output Port.
1 = pin #8 LOP receives a logical "1".
0 = pin #8 LOP receives a logical "0".

The specific application of this driver is to provide test modes for the PLL. Examples of are described in Section 5 Initialization/Application Information of this document.

The LOP module is purely digital, draining no current at all, except the current sourced/sinked on the pin #8 LOP depending on the external application circuit.

4.13.3 Deep Sleep & Power Down Mode

As the LOP module is purely digital draining no current, no specific Deep Sleep nor Power Down configurations exist.

Nevertheless, when the MC44CD03 is in power down mode, the LOP module is still activated and maintains its output state if no change is applied on the I2C bits LNABO and LNAGS. It also maintains its output state when recovering Normal mode from Power Down mode.

4.14 MLP Functional Description

4.14.1 General

The purpose of this section is to detail the MLP module's modes of operation. The following modes and operations are described:

1. Normal Mode.
2. Deep Sleep & Power Down Mode.

4.14.2 Normal Mode

The Normal mode corresponds to the MLP operating as a multi-level pin dedicated to properly configure the MC44CD03 chip and its output clock signal at power on reset, with regards to the reference frequency used (either 26MHz or 36MHz) and the baseband demodulator IC clock input requirements.

The pin #31 CLK_SEL is a 4-level pin that makes use of an internal 240kOhms pull-up resistor, and three analog comparators (three comparison thresholds), resulting in four different chip configurations. The four typical DC levels to be applied on pin #31 CLK_SEL, the corresponding external application scheme, and the resulting chip configurations are described in **Table 4-4** below.

Table 4-4 Multi-level Pin Configuration Table

Level #	Typical DC level applied on pin #31	Typical application on pin #31	Resulting Chip configuration
0	0	GROUND	36MHz reference frequency LVDS signal shaping on clock output pins
1	Vcc/3	120 kOhms to GROUND	36MHz reference frequency single-ended signal shaping on clock output pins
2	2Vcc/3	470 kOhms to GROUND	26MHz reference frequency LVDS signal shaping on clock output pins
3	Vcc	VCC or Open	26MHz reference frequency single-ended signal shaping on clock output pins

As the enable signal is applied on pin #22 ENABLE, the multi-level pin module configures the MC44CD03 chip according to the DC input level applied on pin #31.

The MLP module is made of comparators draining very low current when activated (few µA).

The MLP module forces the configuration of the MC44CD03 chip as long as the I2C bit PADCTRL (reg $05) is forced low.
As the I2C bit PADCTRL is forced high, priority is given to the I2C bits REFCLK (reg $01) and CLKBUF (reg $05) to turn the MC44CD03 chip and its clock outputs according to the application requirements (see the I2C Communication and Register chapters for more details).
The reset state of bit PADCTRL is 0.

4.14.3 Deep Sleep & Power Down Mode

There is no power down mode for multi-level pin MLP module. When the MC44CD03 chip is in Power Down Mode PDM (ENABLE pin is held at logic high, and I2C bit PDM reg$00 is asserted), the multi-level pin MLP module has the exact same functionality than in Normal Mode.

In deep-sleep mode (pin #22 ENABLE is held at logic low), the MLP module is disabled, and drains less than 0.5µA.

Section 5 Initialization/Application Information

This section provides stepwise instructions for initializing and using the MC44CD03 Chip.

5.1 Reset Sources

1. VCC_LOGIC Voltage Monitor. The level sensitive VCC_LOGIC under-voltage detector supervises the CMOS control logic of the I2C sub-module. The detector circuit cannot be disabled and thus guarantees stable register content and hazard free logic operation.
2. External Reset. In case the RST pin is bonded out, this pin can be driven high by overriding the internal pull-down resistance and asserting the internal reset signal . This functionality is mainly provided for test and evaluation purposes.

5.2 Application Information

5.2.1 Application Schematic

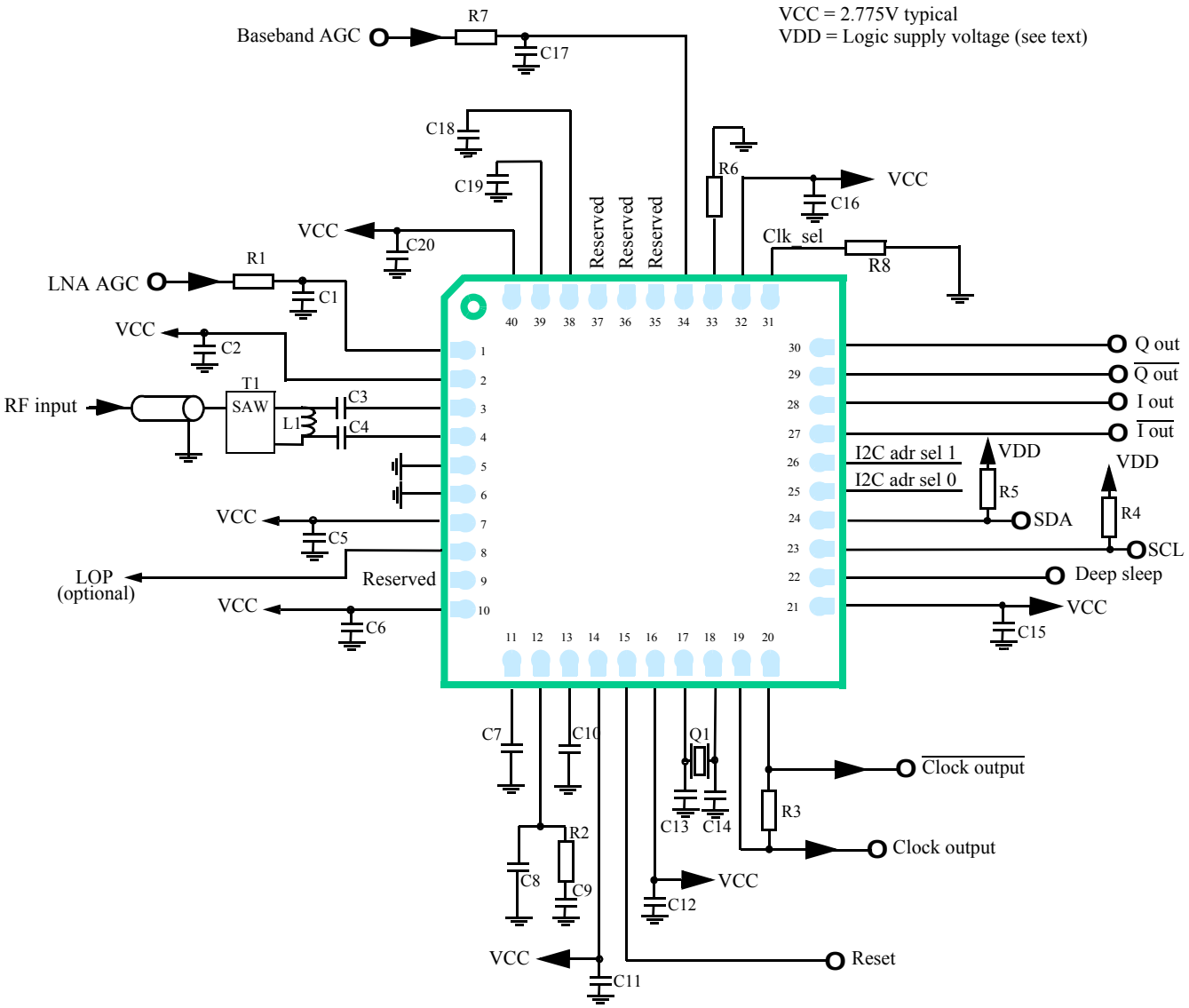


Figure 5-1 MC44CD03 application schematic (differential reference output clock)

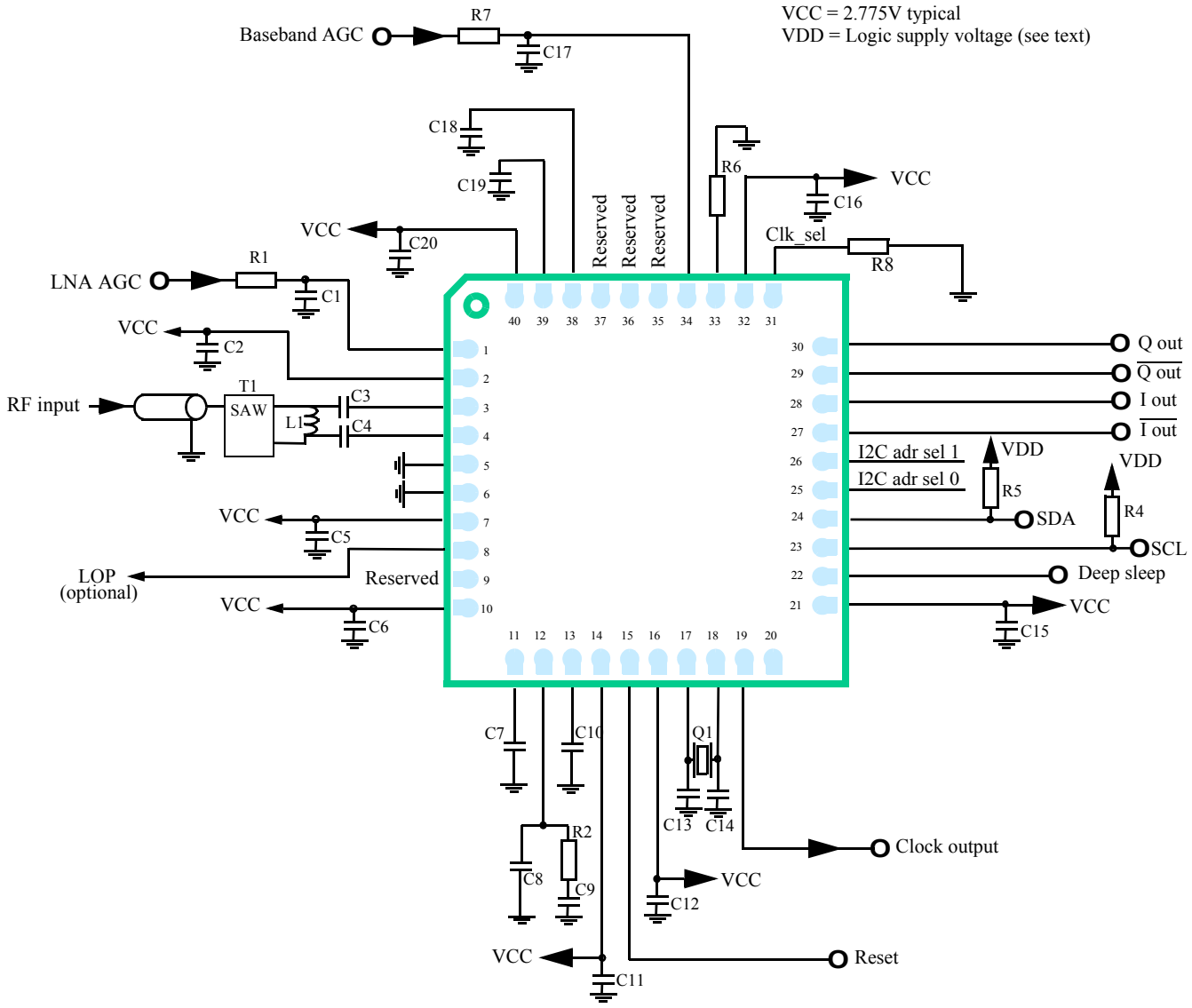


Figure 5-2 MC44CD03 application schematic (single ended reference output clock)

5.2.2 Bill Of Material

Table 5-1 MC44CD03 Typical Application BOM

Part number	Value	Description
C1	22nF	LNA AGC PWM filter capacitor
C2	100nF	VCC LNA decoupling capacitor
C3	3.9pF to 6.8pF	RF input capacitor 1
C4	3.9pF to 6.8pF	RF input capacitor 2
C5	100nF	VCC Mixer decoupling capacitor
C6	100nF	VCC PLL decoupling capacitor
C7	4.7µF ceramic	Super-Filter Output filtering capacitor
C8	100p	RF PLL loop filter capacitor 1
C9	680p	RF PLL loop filter capacitor 2
C10	4.7µF ceramic	Super-Filter Bypass filtering capacitor
C11	100nF	VCC Super-FIlter decoupling capacitor
C12	100nF	VCC OSC decoupling capacitor
C13	12pF	Crystal oscillator tuning capacitor
C14	12pF	Crystal oscillator tuning capacitor
C15	100nF	VCC LOGIC decoupling capacitor
C16	100nF	VCC BB decoupling capacitor
C17	22nF	Baseband AGC PWM filter capacitor
C18	10nF	AGC decoupling capacitor
C19	1nF	RF decoupling capacitor
C20	100nF	VCC PMA decoupling capacitor
L1	4.7nH to 5.6nH	RF input inductance
R1	10KΩ	LNA AGC PWM filter resistor
R2	10KΩ	RF PLL loop filter resistor
R3	510Ω	LVDS external load resistor (only in diff clock mode)
R4	4.7KΩ to 47KΩ	SCL line pull-up (if required)
R5	4.7KΩ to 47KΩ	SDA line pull-up (if required)
R6	18KΩ 1%	Current reference resistor
R7	10KΩ	Baseband AGC PWM filter resistor
R8	see configuration table	Multi-level pin resistor for reference frequency and clock buffers configuration
Q1	36 or 26MHz	Crystal NX3225 or NX2520 (NDK)
T1	TBD	SAW filter with single-ended to differential conversion (see below)
IC1	MC44CD03	RF Front-End IC

5.2.3 Applications Recommendations

5.2.3.1 SAW filter

As the required frequency bandwidth is limited for this application, it is possible to use a SAW filter for the rejection of the out of band interference signals. This SAW filter can also convert the single ended 50 ohms input impedance into a differential 100 ohms input impedance of the RFIC. Such SAW filter components are on development and will be soon available on the market with low insertion loss and rejection of GSM 1900 and WCDMA TX bands.

However it is possible also to use only a balun that provides a 1:2 impedance ratio, at the expense of band rejection. This solution is adopted on our evaluation kits and use a TDK HHM1585A3 balun.

5.2.3.2 RF Inputs

The balanced RF inputs of the device require an external matching network to ensure impedance matching between the SAW filter and LNA chip inputs. As the LNA inputs are about 90 ohms differential and the balun + SAW output is 100 ohms differential the matching network is required for the impedance mismatch. The values of the matching network are defined to get the optimum return loss within the frequency band. These values usually remain in the range described in the following figure.

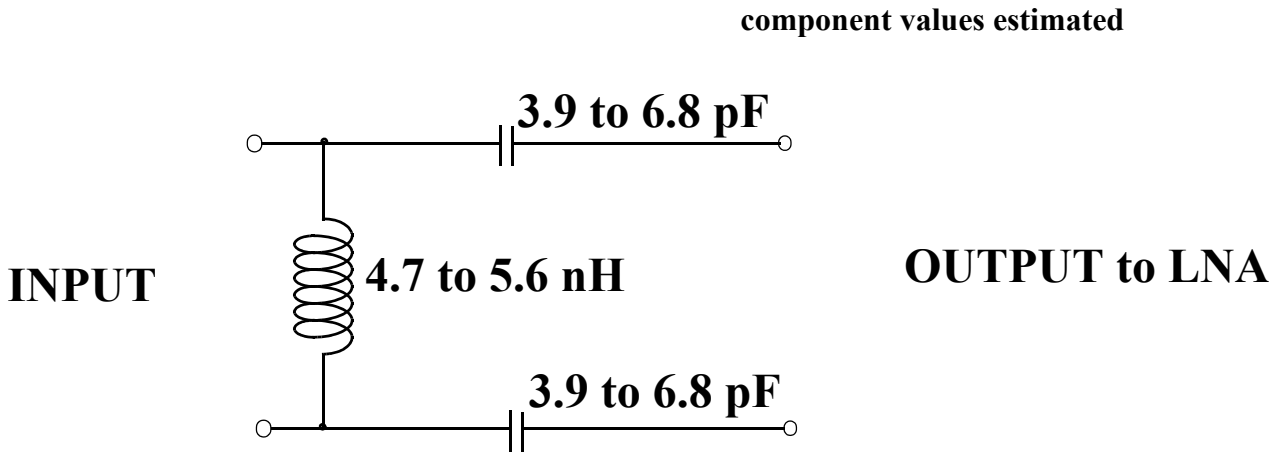


Figure 5-3 Typical input matching network

For instance on our evaluation kit we use a inductance of 5.6 nH associated to 2 capacitors of 6.8 pF. The resulting S11 is described below for a typical case.

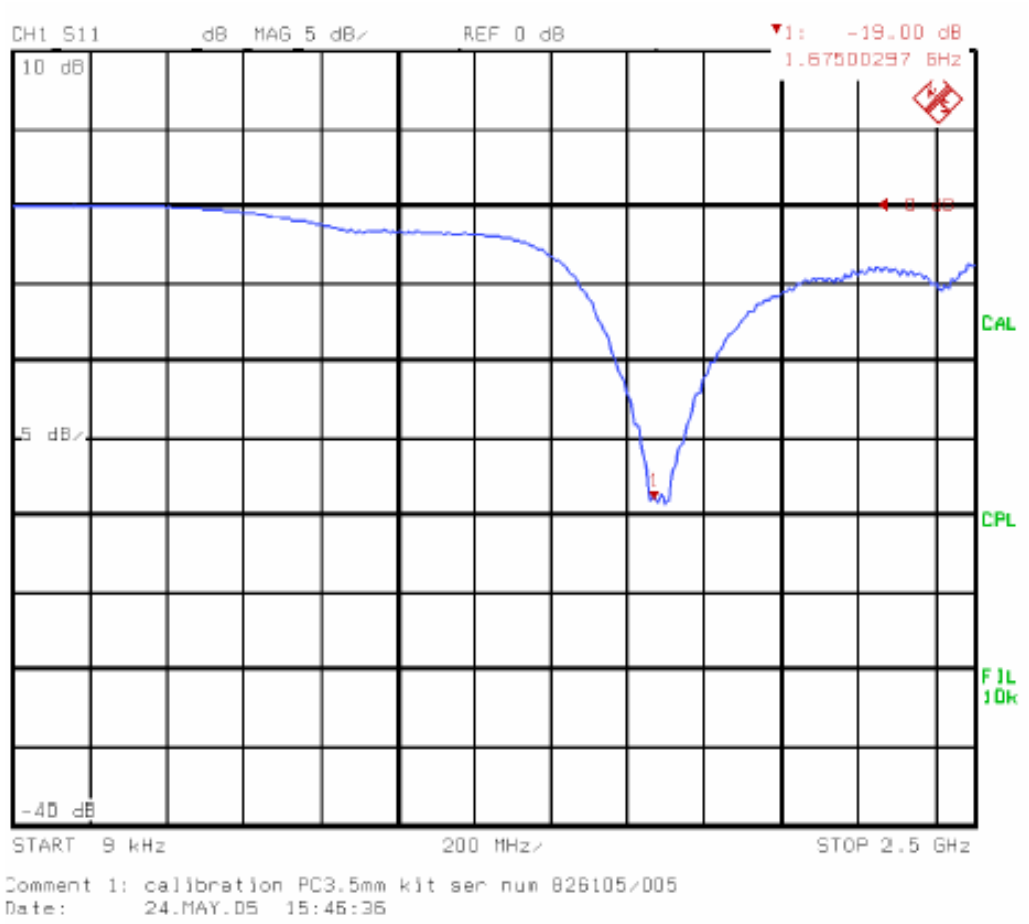


Figure 5-4 Typical input matching network

5.2.3.3 I And Q Baseband Outputs

The I/Q output signals are provided by output buffers for driving purposes. The I/Q signals must fulfill the following requirements:

- differential signal amplitude: 1.4Vpp maximum;

- Baseband differential input resistance: 10KOhms minimum;

- Baseband input capacitance: 5pF maximum;

- Typical DC output common mode voltage: Vcc /2 = 1.38 V

All I/Q outputs are usually AC coupled to the baseband demodulator but can be DC coupled to the IQ dual ADC of the baseband demodulator if the DC conditions are respected.

5.2.3.4 Decoupling And Power Distribution

All supply voltage pins of the device (including the SF_OUT and SF_BYP pins) have to be decoupled as close as possible to the device. It is recommended to provide a ground plane that will be directly connected to the exposed pad. The exposed pad of the device is the main ground.

5.2.3.5 General PCB layout considerations

Both RF inputs must be routed with care to the matching network and the balun. It is important to get a line impedance as close as possible from the required 50 ohms of each input. The total differential impedance is then 100 ohms.

Some sensitive parts (PLL loop filter pin#12, crystal oscillator pins#17 and #18) have to be placed close to their corresponding pins.

If needed the clock outputs must be connected carefully to the baseband demodulator.

5.2.3.6 Crystal Oscillator

The target crystal device is a 36MHz or 26 MHz NX3225DA sub-miniature part from the NDK company. Reference [4] gives the specifications for the 36MHz crystal and Reference [6] for the 26MHz crystal. **Table 5-2** summarizes the characteristics of the quartz for both crystals.

The oscillator (OSC) block generates the time references for the whole DVB-H system. The resulting clock is provided to the baseband demodulator IC through custom clock outputs (either LVDS or single-ended 1.8V CMOS or single-ended 1.5Vpp analog-like), to the digital core of MC44CD03 as synchronization clock, and as reference frequency for the PLL.

Table 5-2 NDK NX3225DA Quartz Characteristics

Preliminary Reference	NX3225 or NX2520 36MHz or 26 MHz
Nominal Frequency	F_0 = 36 or 26 MHz
Resonating Mode	Fundamental
Frequency Tolerance @ 25°C	+/- 10 ppm maximum
Recommended Temperature Range	-20 to +70°C
Functioning Temperature Range	-20 to +85°C
Frequency Stability in the -20 - 70°C temperature range	+/- 10 ppm maximum
CL, Loading Capacitor[1]	8pF

NOTES:

1. If Cc is the total capacitance across the crystal (dominated by the case capacitance), If Cte and Ctx are the values of the tuning capacitors plus any stray contributors between respectively the EXTAL or XTAL pin and ground, then
CL = Cc + Cte*Ctx/(Cte+Ctx). If Cte=Ctx then CL = Cc + Cte/2

The selection of the reference clock frequency value (26 or 36MHz) is either controlled by the multi-level pin#31 CLK_SEL, or by the I2C bus, as described in the dedicated paragraph «Reference clock frequency and clock output buffer selection» below.

5.2.3.7 Using an external reference frequency

Instead of using the crystal oscillator, it is possible to provide the 36MHz or 26MHz reference clock to the chip through the EXTAL pin (pin #17). The application schematic is described in **Figure 5-5**.
The reference clock can be provided as a sinewave clock for harmonic content reduction, or as a rail-to-rail 1.875V or 2.775V digital clock. In any case, the clock must present sufficient amplitude, adequate duty-cycle, and very low jitter, so as not to impact chip functionality nor PLL phase noise performances. The detailed specifications related to this external reference clock are provided in the OSC Electrical Specifications chapter of this document.
The device has its own internal bias on the EXTAL pin, so the external sinewave reference clock must be AC biased through an external capacitor. This capacitor is not needed in case of rail-to-rail digital clock.

The selection of the reference clock frequency value (26 or 36MHz) is either controlled by the multi-level pin#31 CLK_SEL, or by the I2C bus, as described in the dedicated paragraph «Reference clock frequency and clock output buffer selection» below.

..

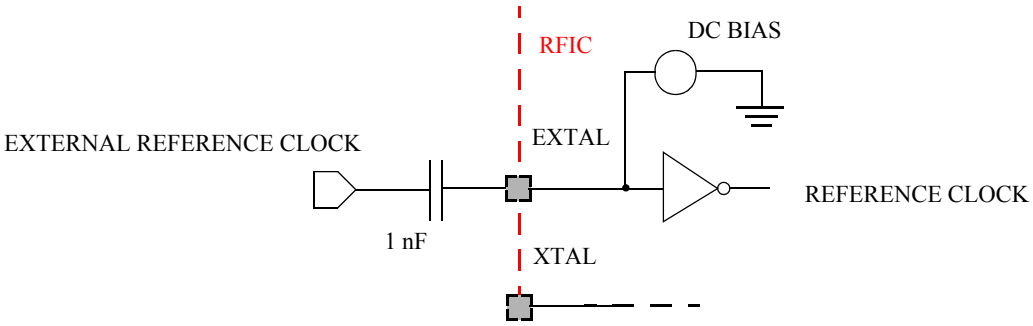


Figure 5-5 Driving the EXTAL pin with an external reference clock

5.2.3.8 Providing the reference crystal clock to the baseband demodulator

To reduce the number of crystals of the whole receiver solution, it is possible to output the reference crystal oscillator clock to the baseband demodulator. There are 2 main configurations, that cannot be used simultaneously.

The first one uses a differential mode to get a better immunity to the common mode parasitic signals. In this case the chip provides the 36 or 26 MHz differential output currents on its output pins #19 CLK_OUT and #20 CLK_OUTB. The signal swing is generated through a load consisting of an external differential resistor. Two different current settings can be programmed through the I2C bit ILVDS. The custom LVDS swing is developed around a common mode level that is derived from a bandgap voltage sufficiently accurate to avoid the use of any common mode control loop. The custom LVDS buffer can be disabled by setting the I2C bit CLKDD to high logic level.

The second one uses the single ended mode. In that case, the chip provides the 36 or 26MHz output signal on the output pin #19 CLK_OUT. The output signal is either 1.8V CMOS shaped as the I2C bit ILVDS is set to 1, or 1.5Vpp analog-like as the I2C bit ILVDS is set to 0. The single-ended buffer can be disabled by setting the I2C bit CLKDD to high logic level.

The selection of the reference clock frequency value (26 or 36MHz) as well as the selection of the clock buffer mode (LVDS or single-ended) is either controlled by the multi-level pin#31 CLK_SEL, or by the I2C bus, as described in the dedicated paragraph «Reference clock frequency and clock output buffer selection» below.

5.2.3.9 Reference clock frequency and clock output buffer configuration

At power on reset, a proper setting of the IC with regards to the reference clock frequency is suitable to fit the application requirements. Particularly, a correct power on reset configuration of the clock output signal is required, as this signal is potentially used to wake-up and clock the baseband demodulator IC.

Therefore, a multi-level pin (pin #31 CLK_SEL) is dedicated to adequately preset the MC44CD03 chip and its clock output signal in the configuration required by the application.
The selection of both the reference clock frequency (either 26 or 36MHz) and the clock output buffer mode (either LVDS or single-ended) is be done by adjusting the value of the external resistor connected to pin#31 CLK_SEL according to **Table 5-3**.

Table 5-3 Multi-level Pin Configuration Table

External resistor value (pull-down) on pin#31 CLK_SEL	Typical DC level on pin#31 CLK_SEL	Clock mode selected
Vcc or Open	Vcc	26MHz reference clock frequency single-ended clock buffer
470 K	2Vcc/3	26MHz reference clock frequency LVDS clock buffer
120 K	Vcc/3	36MHz reference clock frequency single-ended clock buffer
GND	0	36MHz reference clock frequency LVDS clock buffer

When single-ended mode is chosen, the format is square wave at start-up (I2C bit ILVDS=0 in reg $05), this allows making sure that the BB chip will wake-up. The shape can then be programmed to sine wave if desired (ILVDS=1).Similarly, when LVDS mode is chosen, the LVDS current is set to 500uA at start-up (ILVDS=0). This can be modified to 1mA via I2C (ILVDS=1).

Priority can be given to the I2C to select the reference clock frequency and the clock buffer mode by asserting the I2C bit PADCTRL to 1 (reg $05). In that case, the control is given to the I2C bits REFCLK (reg $01) and CLKBUF (reg $05).
At power on reset, the value of this PADCTRL bit is 0, such as the priority is left to the multi-level pin#31 CLK_SEL.

5.2.3.10 PLL Loop Filter Calculation

The 3rd order PLL uses an external 2nd order loop filter as described in **Figure 5-6**.

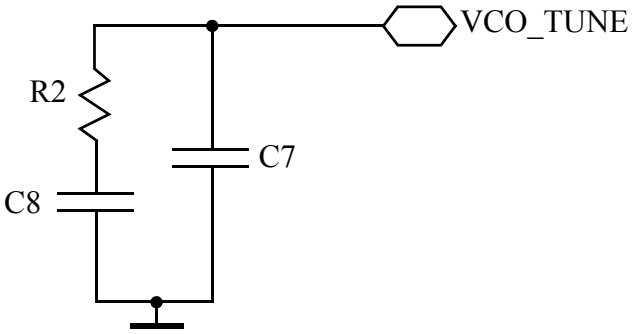


Figure 5-6 External 2nd Order Loop Filter

The choice of the loop bandwidth is mainly driven by phase noise and spur rejection considerations. The major constraint is the integrated noise over the OFDM bandwidth 1 kHz -2.25MHz. The PLL acts as a high pass filter for VCO noise, while adding its own noise source in its band (mainly charge pump and reference oscillator). The higher the PLL bandwidth, the more the PLL in-band noise sources contribute to the overall integrated noise, while the VCO noise contribution decreases. The choice of the charge pump gain is therefore closely related to the PLL bandwidth.

The PLL bandwidth must be sufficiently low to ensure good rejection of the reference frequency spurs, falling into the OFDM bandwidth (at 500 kHz offset from carrier and harmonics). The level of those spurs will be directly correlated to the quality of the matching between the up and down current sources of the charge pump.

Lock time must also be considered for the choice of the PLL bandwidth.

5.2.3.11 RF And Baseband AGC

The AGC inputs of the device (both RF and Baseband BB) are controlled by the baseband demodulator via a PWM filtering network (RC combination). This combination is intended to filter the pulse modulation that operates at the system clock level of the demodulator.

The recommended combination is R = 10K and C = 22nF

5.2.3.12 Using the LOP Pin

It is possible to use the LOP output pin to control an external LNA or as a general purpose output pin (GPO).

For this application, as the device presents already a suitable noise figure it is not mandatory to use an external LNA.

Section 6 References

[1] EICTA-TAC-MBRAI: Mobile DVB-T RF Specification.

[2] Digital Video Broadcast (DVB); Framing Structure, channel coding and modulation for digital terrestrial television. ETSI EN 300 744 V.1.5.1 November 2004

[3] Application note for Thin QFN 40 pins package currently under development.

[4] NDK specifications for the W-191-563 36MHz quartz, case NX3225DA. Document reference EXS11B-00775.

[5] Philips I2C Specifications Version 2.1 January 2000. Document Order Number 9398 393 40011.

[6] NDK specifications for the W-191-653 26MHz quartz, case NX3225DA. Document reference EXS10B-005546.

[7] ETSI EN 302 304:"Digital Video Broadcasting (DVB); Transmission System for Hand-Held Terminals (DVB-H) V1.1.1 November 2004

Appendix A Electrical Specifications

A.1 MC44CD03 Thermal Specifications

Table A-1 Thermal Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient[1]	RΘJA	Free air		82		°C/W

NOTES:
1. As per JEDEC EIA/JESD51-2.

A.2 MC44CD03 Moisture Sensitivity Level Consideration

The device meets moisture sensitivity level 3 (lead-free reflow profiles with peak temperature of 260°C).

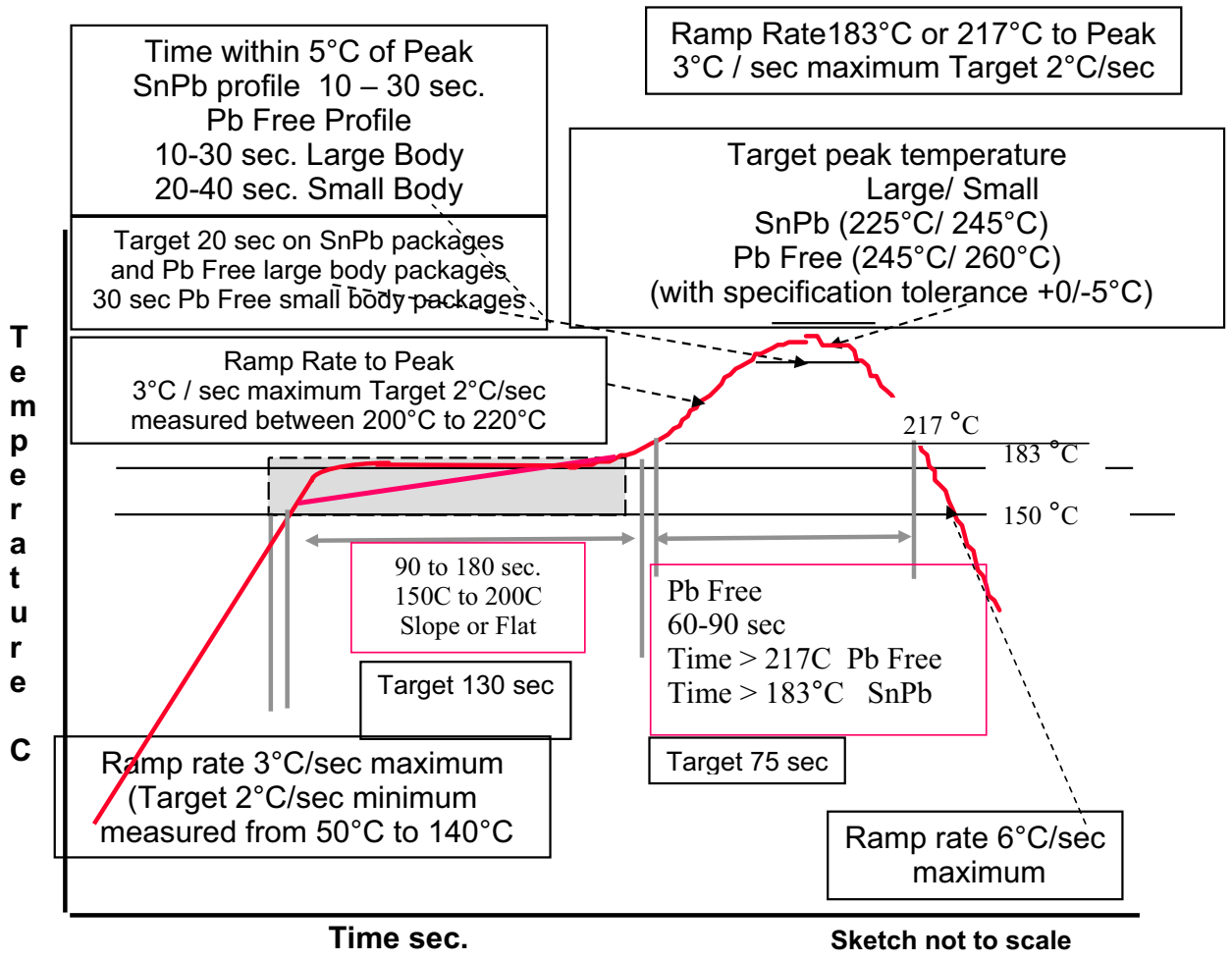


Figure 6-1 High temperature reflow profile

A.3 MC44CD03 ESD Specifications

Table A-2 ESD Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Machine Model ESD	ESD MM	JEDEC JESD22-A115	200			V
Human Body Model ESD	ESD HBM	JEDEC JESD22-A114	2000			V
Charge Device Model ESD	ESD CDM	JEDEC JSED22-C101C	500			V

A.4 General MC44CD03 Electrical Specifications

Unless otherwise noted all specifications are given for a supply voltage set to 2.775V and an operating temperature TA=-30 to +85°C. The correspondence between the type associated with a parameter and the specification method is given below:

- A = 100% tested
- B = 100% correlation tested
- C = Characterized on samples
- D = Guaranteed by design

Table A-3 Engineering Electrical Specs

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
	Supply Voltage	2,7,10 14,16,21 32,40		2.63	2.775	2.92	V	
	Supply Voltage Max Rating[1]	2,7,10 14,16,21 32,40				3.15	V	
	Power Consumption	2,7,10 14,16,21 32,40	Normal Mode[2]		280		mW	
	Operating Temperature			-30		85	°C	
	Storage Temperature			-65		150	°C	
1.1	Normal Operation Current	2,7,10 14,16,21 32,40	Normal Mode	tbd	100.6	tbd	mA	
1.2	Power Down Current	2,7,10 14,16,21 32,40	Power Down Mode[3]		3.6	tbd	mA	

Table A-3 Engineering Electrical Specs

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
1.3	Deep Sleep Current	2,7,10 14,16,21 32,40	Deep Sleep Mode[4]			20	µA	
1.4	Load Regulation	2,7,10 14,16,21 32,40				tbd	mV/mA	
1.5	Line Regulation	2,7,10 14,16,21 32,40	GSM Slot			1	mV	
1.6	PSRR	2,7,10 14,16,21 32,40	GSM Slot (about 1.8kHz)	40			dB	
1.7	IC Wake-up Time from power down		Conditions[5]		5	20	ms	
1.8	IC Wake-up Time from deep sleep		Conditions[6]		6	200	ms	

NOTES:

1. Maximum ratings are those values beyond which damage to the device may occur. For functional operation, voltage should be restricted to the Recommended Operating Condition.
2. ENABLE Pin at Vcc level. PDM bit cleared in the MODE register (address $00).
3. ENABLE Pin at Vcc level. PDM bit set in the MODE register (address $00).
4. ENABLE pin grounded.
5. Definition of the setup: measured at I/Q outputs when reaching 90% of the final amplitude.
6. Definition of the setup: measured at I/Q outputs when reaching 90% of the final amplitude.

A.5 MC44CD03 RF Performances

The RF path between the antenna and the MC44CD03 chip includes:

- An external SAW filter with the following characteristics:
  - Power gain: G = -2dB
  - Noise figure: NF = +2dB maximum
  - Rin single ended 50 ohms; Rout differential 100 ohms
- A matching network between the differential 100 ohms SAW output to the differential chip input

Table A-4 describes the general receiver specifications, derived from the DVB-T standard specifications.

WARNING

The reference point for all the specifications displayed in Table A-4 is the antenna output (external SAW input). The typical SAW characteristics indicated above are then assumed. This reference point is changed to the IC (internal LNA) inputs in Table A-5.

Unless otherwise noted all specifications are given for a supply voltage set to 2.775V and an ambiant temperature TA=-30 to +85°C.

Table A-4 DVB Receiver RF Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
2.1	RF Input Range	3,4		1665		1680	MHz	
2.2	Max. Input Level for the wanted signal and adjacent signal	3,4				-25	dBm	
2.3	Input Sensitivity	3,4	QPSK, CR=1/2, gaussian noise	-95.6			dBm	
2.5	Overall Maximum Gain[1]	3,4			80		dB	
2.6	Reverse LO leakage	3,4	Measured at balun[2] input from 3330MHz to 3360MHz			-35	dBm	C

NOTES:
1. PMAG[1:0]=11 in the MISCR register.
2. Balun reference TDK HHM1585A3.

Table A-5 MC44CD03 RF Performances (lossless external SAW or Balun)

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
3.1	Noise Figure	3,4	Max Gain			4	dB	
3.2	Input IP2	3,4	Out-of-band interferer See **Table A-7**	2			dBm	
3.3	Input IP3	3,4	See **Table A-6**	-10			dBm	
3.4	Overall AGC Range	3,4	Both RF & BB AGC	70	75		dB	
3.5	Return losses[1]	3,4			10		dB	
3.10	Overall Maximum Voltage Gain[2]	3,4			79		dB	
3.11	Max. Input Level for wanted and unwanted signal	3,4				-25	dBm	
3.12	Input Sensitivity	3,4		-95.6			dBm	
3.13	Noise Figure degradation in presence of GSM blocker or adjacent channel[3]	3,4	Any gain condition			10	dB	
3.14	1dB Compression Point[4]	3,4		-20			dBm	

NOTES:
1. Maximum return losses as the matching network between the SAW filter and the differential RF inputs of the chip is optimized.
2. PMAG[1:0]=11 in the MISCR register.
3. -25dBm DVB-T adjacent channel or -25dBm with GSM blocker at 1850.2 MHz.
4. Measured with -20dB RF LNA gain reduction and maximum baseband gain.

Table A-6 Input IP3 Measurement Conditions

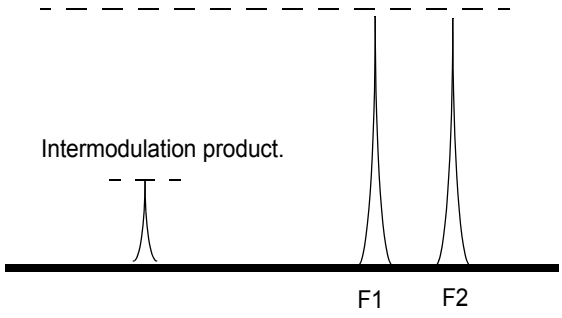
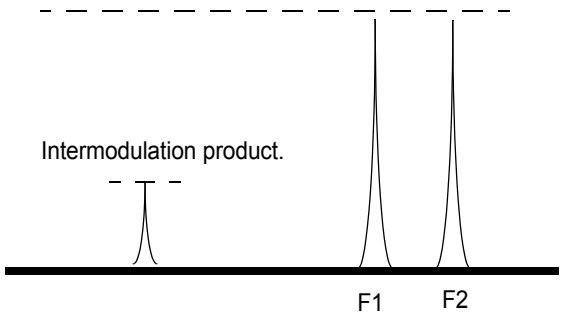
Device & Signals Set-up	Measurements Set-up
2-tone measurements The intermodulation product falls back in the wanted channel. Conditions: RF inputs @ -25 dBm. 24 dB RF LNA gain reduction. 26dB BB AGC gain reduction The RF PLL is tuned on the central frequency of the corresponding DVB-H channel 1672.5 MHz. F1 = 1675.12 MHz, F2 = 1679.12 MHz that gives an intermodulation product at1671.12 MHz . F1 = 1665.88 MHz, F2 =1669.88 MHz that gives an intermodulation product at 1673.88 MHz The baseband IM3 product is at 1.38 MHz	

Table A-7 Input IP2 Measurement Conditions

Device & Signals Set-up	Measurements Set-up
2-tone measurements The intermodulation product falls back in the wanted channel. Conditions: RF inputs @ -25 dBm. 24 dB RF LNA gain reduction. 26dB BB AGC gain reduction Out-of-band interferers: IIP2 min = +15dBm The RF PLL is tuned on the central frequency of the corresponding DVB-H channel 1667.5 MHz. F1 = 1673.2 MHz, F2 = 1675 MHz that gives an intermodulation product at 1.8 MHz .	

A.6 RFLNA Electrical Specifications

Table A-8 RFLNA Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
3.6	RF AGC Range	1			40		dB	
3.7	RF AGC Slope	1		tbd	+ 35	tbd	dB/V	
3.8	RF AGC Voltage Range	1		0.1		1.8	V	
3.9	RF AGC Input Impedance	1	Resistor to Supply	400			kΩ	
3.10	RF AGC Gain variations over reduced temperature range (-10 to 50 C)	3,4		-2	-	+2	dB	
3.11	RF AGC Gain variations over process and temperature	3,4		-6	-	+6	dB	

A.7 PMA Electrical Specifications

Table A-9 PMA Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
12.1	Maximum Voltage Gain		PMAG[1:0]=00[1]		15		dB	
12.2	Intermediate Voltage Gain		PMAG[1:0]=10		13		dB	
12.3	Minimum Voltage Gain		PMAG[1:0]=01		11		dB	
12.4	Output Frequency Range (set by the pole at the output)		@ -3dB	19	38	57	MHz	

NOTES:
1. Reset value.

A.8 LPF Electrical Specifications

Table A-10 LPF Performances[1]

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
5.1	Attenuation	27,28 29,30	@ 2.5MHz		1	5	dB	
5.2	Stopband Attenuation	27,28 29,30	@ 3.8MHz	16			dB	
5.3	GSM Blocker Rejection	27,28 29,30	@ 177.7MHz	60			dB	
5.4	Group Delay	27,28 29,30			400	1120	ns	
5.5	In-band Ripple	27,28 29,30				2	dB	
5.6	Constant IQ Gain Imbalance	27,28 29,30		-3		3	dB	
5.7	Constant IQ Phase Imbalance	27,28 29,30		-10		10	degree	
5.8	Frequency dependant IQ Gain and Phase Imbalance	27,28 29,30	See **Table A-11**			-35	dBc	
5.9	AC Coupling Cut-off	27,28 29,30	@ -3dB			1	kHz	
5.10	Output DC Offset	27,28 29,30				40	mV	
5.11	Output Voltage Range	27,28 29,30	Differential			700	mVp	
5.12	I/Q Output Impedance (Single Ended Referred to Ground)	27,28 29,30			TBD		kΩ	
5.13	Output DC Level	27,28 29,30			1.3		V	
	Baseband AGC							
6.1	Total BB AGC Range	34		35			dB	
6.2	AGC Input Voltage Range	34		0.1		1.8	V	

Table A-10 LPF Performances[1]

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
6.3	BB AGC Slope	34			+ 35		dB/V	
6.4	AGC Input Impedance	34		400			kΩ	
6.5	BB AGC Gain variations over reduced temp. range -10°C to 50°C			-1		1	dB	
6.6	BB AGC Gain variations over process and temperature			-6		+6	dB	

NOTES:
1. All filtering performance specifications (items 5.1 to 5.8) are defined as both the channel filter and the anti-aiasing filter are turned on (chip enabled and I2C bits PDM (reg$00), AAFD and CHEBD (reg $06) set to logic level low).

Table A-11 IQ Gain and Phase Imbalance Contribution to S/N Degradation

Device & Signals Set-up	Measurements Set-up
Sweep tone measurement of total IQ amplitude and phase imbalance (constant and ripple) for the following RF input signal: From F1 to F2 = 1672.5 to 1674.875 MHz and for three different baseband AGC settings: Low gain: minimum baseband gain Medium gain: (max. gain - min. gain)/2 High gain: maximum baseband gain Detecting the amplitude $\gamma(f)$ and phase $\Delta\varphi(f)$ difference between baseband I- and Q- outputs. Calculating mean value, deviation and interference variance according to: $$\varepsilon(f) = \frac{\gamma(f) - 1}{\gamma(f) + 1}$$ $$\sigma_\varepsilon = \sqrt{\overline{[\varepsilon(f) - \overline{\varepsilon(f)}]^2}}$$ $$\sigma_{\Delta\varphi} = \sqrt{\overline{[\Delta\varphi(f) - \overline{\Delta\varphi(f)}]^2}}$$ Interference variance: $$\sigma^2 = \frac{1}{\sigma_\varepsilon^2 \cdot \left(\cos\left(\frac{\sigma_{\Delta\varphi}}{2}\right)\right)^2 + \left(\sin\left(\frac{\sigma_{\Delta\varphi}}{2}\right)\right)^2}$$	

A.9 OSC Electrical Specifications

Unless otherwise noted, the following specifications assume the proper mounting of a 36 or 26MHz crystal element, associated with external tuning capacitors.

Table A-12 OSC Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
Crystal Oscillator								
7	Recommended Crystal: 36MHz NDK 3225 DA reference W-191-563							
7.0	Reference Clock Frequency[1]	17			26 or 36		MHz	
7.1	Motional Capacitance	17,18	36MHz 26MHz		3.99 10		fF	
7.2	Motional Inductance	17,18	36MHz 26MHz		4.9 3.75		mH	
7.3	Parallel Capacitance	17,18		0.85	1	1.15	pF	
7.4	Series Resistance	17,18				50	Ω	
7.5	Load Capacitance	17,18			8		pF	
LVDS Outputs[2]								
8.1	Differential Output Clock Current	19,20	i_lvds_adj = 0 i_lvds_adj = 1	0.375 0.750	0.5 1.0	0.625 1.250	mApk mApk	
8.2	Common Mode Voltage	19,20		0.85	0.95	1.05	V	
8.3	External Load (differential)	19,20	i_lvds_adj = 0 i_lvds_adj = 1		500 250		Ω	
8.4	Start-up Time	19,20	See Note[3]			5	ms	
8.5	Output Clock Duty Cycle	19,20		45	50	55	%	
8.6	Output Clock Jitter	19,20	cycle-to-cycle (1MHz bandwitdh)			35	ps	
8.7	Maximum Load Capacitance (differential)	19,20				1	pF	
Single-ended Buffer Output[4]								
8.8	Output Voltage Swing	19	i_lvds_adj = 0 i_lvds_adj = 1		1.5 [0:1.8]		Vpp CMOS	
8.9	Common Mode Voltage	19	i_lvds_adj = 0 i_lvds_adj = 1		0.9 NA		V NA	
8.10	Start-up Time	19	See Note[5]			5	ms	

Table A-12 OSC Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
8.11	Output Clock Duty Cycle	19		45	50	55	%	
8.12	Output Clock Jitter	19	cycle-to-cycle (1MHz bandwitdh)			35	ps	
8.13	Maximum Load Capacitance (differential)	19				5	pF	
External Reference Clock[6]								
8.14	Reference Clock Frequency[7]	17			26 or 36		MHz	
8.15	Reference Clock Amplitude	17		220			mVrms	
8.16	Reference Clock Duty-Cycle	17		45		55	%	
8.17	Reference Clock Jitter	17	cycle-to-cycle integrated from 1kHz to 100kHz			0.5	ps	
8.18	Reference Clock Phase Noise	17	@ 1kHz offset			-120	dBc/Hz	

NOTES:

1. The reference clock frequency value is either selected by a proper setting of the DC input voltage of the multi-level pin pin#31 CLK_SEL as the I2C bit PADCTRL =0 (reg $05), or selected by the value of the I2C bit REFCLK (reg $01) as PADCTRL=1 (reg $05).
2. The implementation of LVDS inside the MC44CD03 chip does not obey ANSI/TIA/EIA-644. The LVDS buffer is either selected by a proper setting of the DC input voltage of the multi-level pin pin#31 CLK_SEL as the I2C bit PADCTRL =0 (reg $05), or selected by forcing the I2C bit CLKBUF (reg $05) to 0 as PADCTRL=1 (reg $05).
3. Measured from assertion of the ENABLE pin to delivery of output clock on the CLK_OUT/B pins.
4. The single-ended buffer is either selected by a proper setting of the DC input voltage of the multi-level pin pin#31 CLK_SEL as the I2C bit PADCTRL =0 (reg $05), or selected by forcing the I2C bit CLKBUF to 1 as PADCTRL=1 (reg $05).
5. Measured from assertion of the ENABLE pin to delivery of output clock on the CLK_OUT pin.
6. Specifications as the external reference clock is externally provided to the chip through the EXTAL input pin.
7. The reference clock frequency value is either selected by a proper setting of the DC input voltage of the multi-level pin pin#31 CLK_SEL as the I2C bit PADCTRL =0 (reg $05), or selected by the value of the I2C bit REFCLK (reg $01) as PADCTRL=1 (reg $05).

A.10 PLL Electrical Specifications

Unless otherwise noted, the following specifications assume the proper mounting of a loop filter made of R2=27 kΩ, C8= 820 pF and C7= 120 pF.

Table A-13 PLL Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
9.1	VCO Frequency Range			3335		3355	MHz	
9.1	PLL Frequency Range			1667.5		1677.5	MHz	
9.2	VCO_TUNE Minimum Voltage	12		0.5			V	
9.3	VCO_TUNE Maximum Voltage	12				1.7	V	
9.4	PLL In-band Accumulated Folded Phase Noise 1kHz-2.5MHz					-30	dBc	
9.5	PLL SSB Phase Noise @ 400kHz offset					-108	dBc/Hz	
9.6	PLL SSB Phase Noise @ 177.7MHz offset				-163	-155	dBc/Hz	
9.7	Reference Frequency[1]				500		kHz	
9.8	Reference Frequency Spurs @ Fref offset in channel band					-38	dBc	

NOTES:
1. Derived from crystal oscillator

A.11 REM Electrical Specifications

Table A-14 REM Performances

ID	Parameter	Pin	Conditions	Min	Typ	Max	Unit	Type
1.8	DC operating voltage of the REF_CUR pin	33			1.11		V	A

A.12 LOP Electrical Specifications

Table A-15 LOP Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
13.2	LOP Buffer Rise Time[1]	8	CLoad=10pF		3	4	ns	
13.3	LOP Buffer Fall Time[2]	8	CLoad=10pF		1.5	2.5	ns	
13.4	LOP Buffer RdsON[3] LNAGS=X / LNABO=1 LNAGS=1 / LNABO=0	8	Iload=5mA sourced sinked			 35 120	 Ω Ω	

NOTES:
1. LNBAO=0 in the MISCR register. Measured from 10% to 90% output swing.
2. LNBAO=0 in the MISCR register. Measured from 90% to 10% output swing.
3. LNAGS and LNABO in the MISCR register. Static measurement.

A.13 MLP Electrical Specifications

ID	Parameter DC level on pin#31[1]	Pin(s)	Conditions	Resulting Chip Configuration
13.1	Vdc < (Vcc/6)-100mV	31	PADCTRL=0 (reg $05)	36MHz reference frequency LVDS signal shaping on clock output pins
13.1	Vdc >(Vcc/6)+100mV and Vdc<(Vcc/2)-100mV	31	PADCTRL=0 (reg $05)	36MHz reference frequency single-ended signal shaping on clock output pins
13.1	Vdc >(Vcc/2)+100mV and Vdc<(5Vcc/6)-100mV	31	PADCTRL=0 (reg $05)	26MHz reference frequency LVDS signal shaping on clock output pins
13.1	Vdc >(5Vcc/6)+100mV	31	PADCTRL=0 (reg $05)	26MHz reference frequency single-ended signal shaping on clock output pins

NOTES:

1. DC level on pin#31 CLK_SEL is preferably generated by connecting an external resistor to ground as described in the chapter MLP Functional Description and the chapter Initialization/Application Information of this document.

A.14 RCI Electrical Specifications

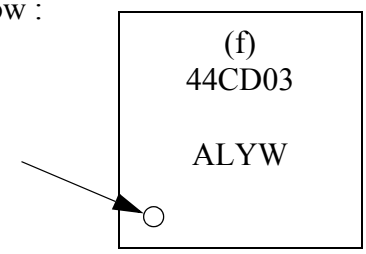
Table A-17 RCI Performances

ID	Parameter	Pin(s)	Conditions	Min	Typ	Max	Unit	Type
10.1	SDA/SCL Low Input Level	23,24				0.3	V	A
10.2	SDA/SCL High Input Level	23,24		1.5			V	A
10.3	ACK Low Output Level	24	Sinking 3mA load current			0.3	V	A
10.4	I2C Communication Speed	23,24	See Reference [5]			400	kbits/s	A
10.5	Digital Inputs Low Input Level	15,22,25,26,37		0		0.3	V	A
10.6	Digital Inputs High Input Level	15,22,25,26,37		1.5		Vcc	V	A
10.7	Digital Inputs Input Capacitance	15,22,25,26,37			1		pF	A
10.8	RESET Pull-down Resistor	15			120		kΩ	A
10.9	SCAN_ENABLE Pull-down Resistor	37			120		kΩ	A

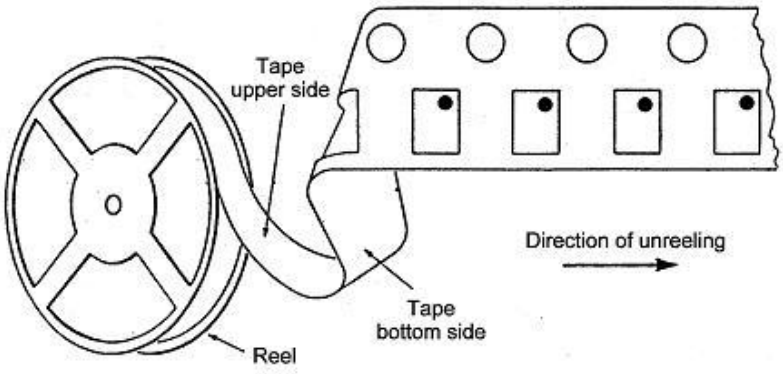
Appendix B Case Outline & Mechanical Drawings

Upon standard specification 12MRH00191A, marking is described as follow :

- Format code = 126
- (f) = Freescale logo
- YW = abbreviation for assembly year and week
- A = assembly site code, L = wafer lot code

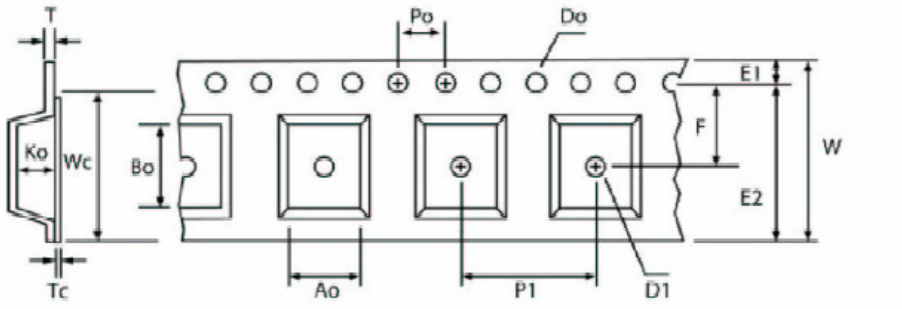


"YW" Year / Work week definition table		
YEAR	WORK WEEK	CODE
2005	1	GA
	26	GZ
	27	HA
	52	HZ
2006	1	JA
	26	JZ
	27	KA
	52	KZ
2007	1	LA
	26	LZ
	27	MA
	52	MZ
2008	1	NA
	26	NZ
	27	PA
	52	PZ
Note that "I" & "O" leading characters have been skipped		



Samples are tape & reeled in accordance with the Freescale standard, per 2000, under the following conditions using Advantek P/N: ML0606-A

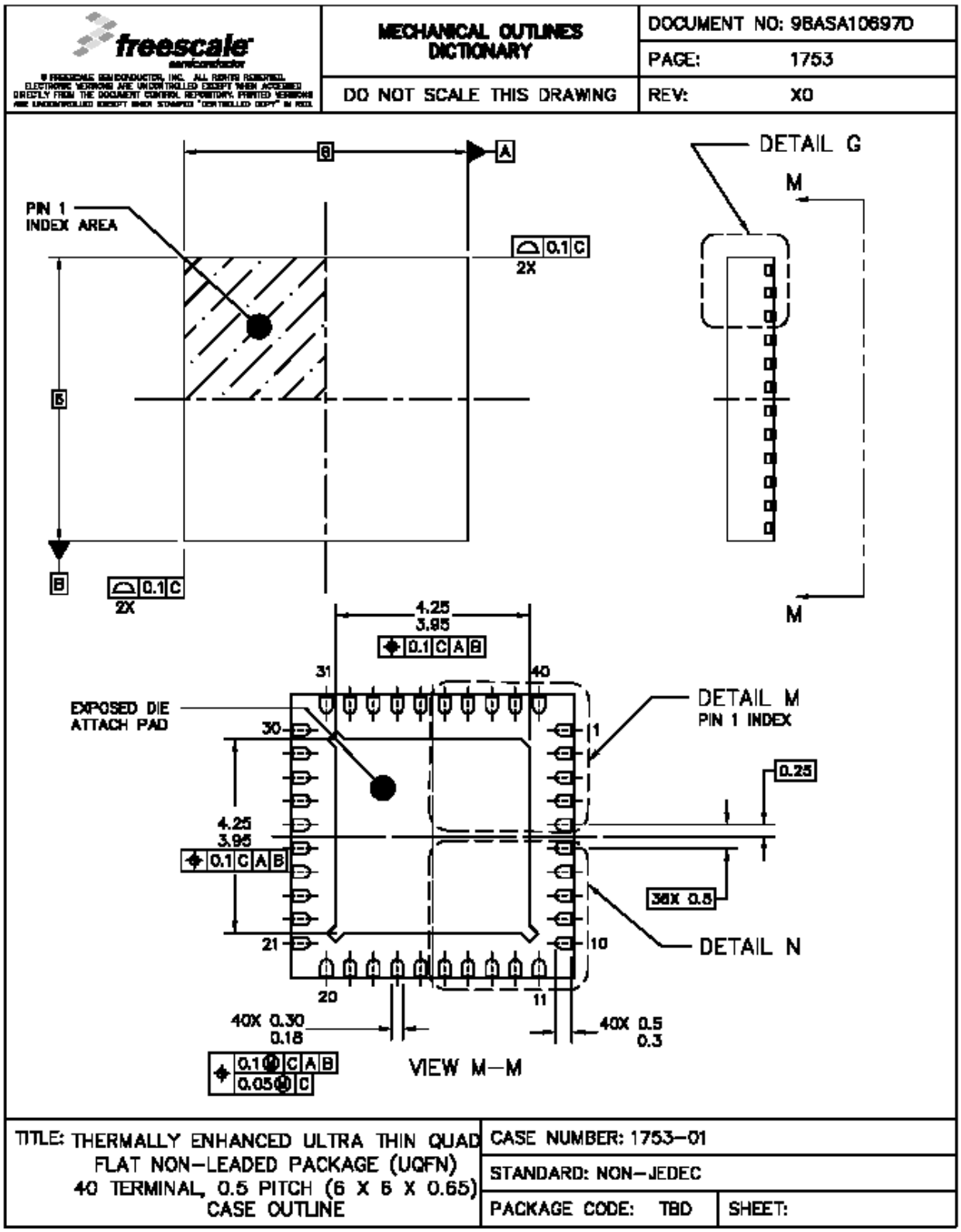
- Tape Pitch: 12 mm part to part
- Tape Width: 16mm
- Reel diameter: 13 inches



Vendor / Tape Part #	Ao	Bo	Do	D1	E1	F	Ko	Po	P1	T	W
Advantek ML0606-A	6.3	6.3	1.5	1.5	1.75	7.5	1.10	4.0	12.0	.30	16.0

*Note: All dimensions in millimeters

The document 98ASA10697D is reproduced hereafter without scaling for convenience.
Until additional documentation is available refer to reference [3].


freescale semiconductor
MECHANICAL OUTLINES
DICTIONARY
DOCUMENT NO: 98ASA10697D
PAGE: 1753
DO NOT SCALE THIS DRAWING
REV: XO
PIN 1
INDEX AREA
0.1 C
2X
DETAIL G
M
4.25
3.95
0.1 C A B
31
40
EXPOSED DIE
ATTACH PAD
30
1
DETAIL M
PIN 1 INDEX
0.25
36X 0.5
DETAIL N
21
10
20
11
40X 0.30
0.18
40X 0.5
0.3
0.10 C A B
0.05 C
VIEW M–M
TITLE: THERMALLY ENHANCED ULTRA THIN QUAD
FLAT NON–LEADED PACKAGE (UQFN)
40 TERMINAL, 0.5 PITCH (6 X 6 X 0.65)
CASE OUTLINE
CASE NUMBER: 1753–01
STANDARD: NON–JEDEC
PACKAGE CODE: TBD
SHEET:

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, AND DIE ATTACH PAD.
5. MINIMUM METAL GAP SHOULD BE 0.2 MM.

TITLE: THERMALLY ENHANCED ULTRA THIN QUAD FLAT NON–LEADED PACKAGE (UQFN) 40 TERMINAL, 0.5 PITCH (6 X 6 X 0.65) CASE OUTLINE	CASE NUMBER: 1753–01	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: TBD	SHEET:

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LTR	ORIGINATOR	REVISIONS	DRAFTER	DATE
XO	ANANDA DE SILVA	RELEASED FOR ENG. PATH TO PRODUCTION	TAYLOR LIU	12 SEP 2005

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