Order this document by
MC68HC05C4AD/D
Rev. 4.3

MC68HC05C4
MC68HC05C8
MC68HC805C4
MC68HCL05C4
MC68HCL05C8
MC68HSC05C4
MC68HSC05C8

Addendum to
MC68HC05C4
8-Bit Microcomputer Unit (MCU)

ADI991R2

This Addendum provides corrections to the *MC68HC05C4 Advanced Information Data Sheet* (ADI991R2). Correction material contained in this *Addendum (MC8HC05C4AD/D Rev. 4.1)* applies to data sheet Sections 10 and 11, and Appendices C and D.

Addendum Section 10 provides new ordering information. Pages 10-1, 10-2, and the MC68HC05C4/C8 Ordering Form **should be removed** from the Advanced Information Data Sheet.

Addendum Section 11 provides additional 42-pin shrink DIP and 44-pin QFP mechanical data information. Information contained on pages 11-1, 11-2, and 11-3/11-4 are still valid, and **must not be removed** from the Advanced Information Data Sheet.

Addendum Appendix C provides revised information for the MC68HC805C4. Pages C-1 through C-10 and the MC68HC805C4 Ordering Form **should be removed** from the Advanced Information Data Sheet.

Addendum Appendix D provides information for the MC68HC05C4 emulation. Pages D-1 through D-4 **should be removed** from the Advanced Information Data Sheet.

This Addendum also provides MC68HCL05C4/C8 and MC68HSC05C8 HCMOS 8-Bit Microcomputer information.

MC68HCL05C4 and MC68HCL05C8 Low Power HCMOS 8-Bit Microcomputers

This Addendum also introduces the MC68HCL05C4 and MC68HCL05C8 which are members of the M68HC05 Family of low-cost single-chip HCMOs microcomputers. Both the MC68HCL05C4 and MC68HCL05C8 are low-power versions of the MC68HC05C4.

All material described in the *MC68HC05C4 Advanced Information Data Sheet* (ADI991R2) applies to the MC68HCL05C4 and MC68HCL05C8 with the exceptions in Appendices E and F of this Addendum.

MC68HSC05C8 High-Speed HCMOS 8-Bit Microcomputer

This Addendum also introduces the MC68HSC05C8 which is a member of the M68HC05 Family of low-cost single-chip HCMOS microcomputers. The MC68HSC05C8 is a high-speed version of the MC68HC05C4.

All material described in the *MC68HC05C4 Advanced Information Data Sheet* (ADI991R2) applies to the MC68HSC05C8 with the exceptions described in Appendix G of this Addendum.

MC68HC05C4AD/D
Rev. 4.3

SECTION 10
ORDERING INFORMATION

This section contains instructions for ordering custom-masked ROM MCUs.

10.1 MCU ORDERING FORMS

To initiate an order for a ROM-based MCU, first obtain the current ordering form for the MCU from a Freescale representative. Submit the following items when ordering MCUs:

- A current MCU ordering form that is **completely filled out** (Contact your Freescale sales office for assistance.)
- A copy of the customer specification if the customer specification deviates from the Freescale specification for the MCU
- Customer's application program on one of the media listed in **10.2 APPLICATION PROGRAM MEDIA**

The current MCU ordering form is also available through the Freescale Freeware Bulletin Board Service (BBS). The telephone number is (512) 891-FREE. After making the connection, type bbs in lowercase letters and press the return key to start the BBS software.

10.2 APPLICATION PROGRAM MEDIA

Please deliver the application program to Freescale in one of the following media:

- Macintosh®[1] 3-1/2-inch diskette (double-sided 800K or double-sided high-density 1.4M)
- MS-DOS®[2] or PC-DOS®[3] 3-1/2-inch diskette (double-sided 720K or double-sided high-density 1.44M)
- MS-DOS® or PC-DOS® 5-1/4-inch diskette (double-sided double-density 360K or double-sided high-density 1.2M)
- EPROM(s) 2716, 2732, 2764, 27128, 27256, or 27512 (depending on the size of the memory map of the MCU)

Use positive logic for data and addresses.

[1]Macintosh is a registered trademark of Apple Computer, Inc.
[2]MS-DOS is a registered trademark of Microsoft, Inc.
[3]PC-DOS is a registered trademark of International Business Machines Corporation.

10.2.1 Diskettes

If submitting the application program on a diskette, clearly label the diskette with the following information:

- Customer name
- Customer part number
- Project or product name
- Filename of object code
- Date
- Name of operating system that formatted diskette
- Formatted capacity of diskette

On diskettes, the application program must be in Motorola's S-record format (S1 and S9 records), a character-based object file format generated by M6805 cross assemblers and linkers.

NOTE

Begin the application program at the first user ROM location. Program addresses must correspond exactly to the available on-chip user ROM addresses as shown in the memory map. **Write $00 in all non-user ROM locations or leave all non-user ROM locations blank**. See the current MCU ordering form for additional requirements.

If the memory map has two user ROM areas with the same addresses, then write the two areas in separate files on the diskette. Label the diskette with both filenames.

In addition to the object code, a file containing the source code can be included. Freescale keeps this code confidential and uses it only to expedite ROM pattern generation in case of any difficulty with the object code. Label the diskette with the filename of the source code.

10.2.2 EPROMs

If submitting the application program in an EPROM, clearly label the EPROM with the following information:

- Customer name
- Customer part number
- Checksum
- Project or product name
- Date

NOTE

Begin the application program at the first user ROM location. Program addresses must correspond exactly to the available on-chip user ROM addresses as shown in the memory map. **Write $00 in all non-user ROM locations**. See the current MCU ordering form for additional requirements.

Submit the application program in one EPROM large enough to contain the entire memory map. If the memory map has two user ROM areas with the same addresses, then write the two areas on separate EPROMs. Label the EPROMs with the addresses they contain.

Pack EPROMs securely in a conductive IC carrier for shipment. Do not use Styrofoam.

10.3 ROM PROGRAM VERIFICATION

The primary use for the on-chip ROM is to hold the customer's application program. The customer develops and debugs the application program and then submits the MCU order along with the application program.

Freescale inputs the customer's application program code into a computer program that generates a listing verify file. The listing verify file represents the memory map of the MCU. The listing verify file contains the user ROM code and may also contain non-user ROM code, such as self-check code. Freescale sends the customer a computer printout of the listing verify file along with a listing verify form.

To aid the customer in checking the listing verify file, Freescale will program the listing verify file into customer-supplied blank EPROMs or preformatted Macintosh or DOS disks. All original pattern media are filed for contractual purposes and are not returned.

Check the listing verify file thoroughly, then complete and sign the listing verify form and return the listing verify form to Freescale. The signed listing verify form constitutes the contractual agreement for the creation of the custom mask.

10.4 ROM VERIFICATION UNITS (RVUs)

After receiving the signed listing verify form, Freescale manufactures a custom photographic mask. The mask contains the customer's application program and is used to process silicon wafers. The application program cannot be changed after the manufacture of the mask begins. Freescale then produces ten MCUs, called RVUs, and sends the RVUs to the customer. RVUs are usually packaged in unmarked ceramic and tested to 5 Vdc at room temperature. RVUs are not tested to environmental extremes because their sole purpose is to demonstrate that the customer's user ROM pattern was properly implemented.

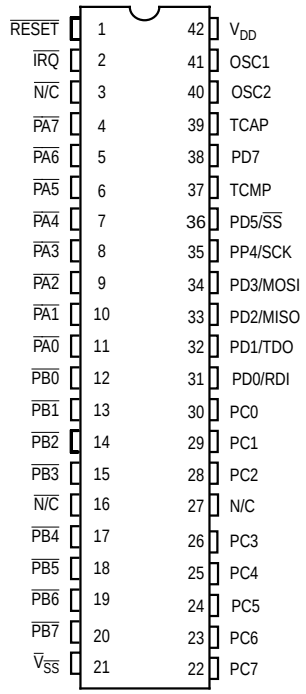
The ten RVUs are free of charge with the minimum order quantity but are not production parts. RVUs are not guaranteed by Freescale Quality Assurance.

SECTION 11
MECHANICAL DATA

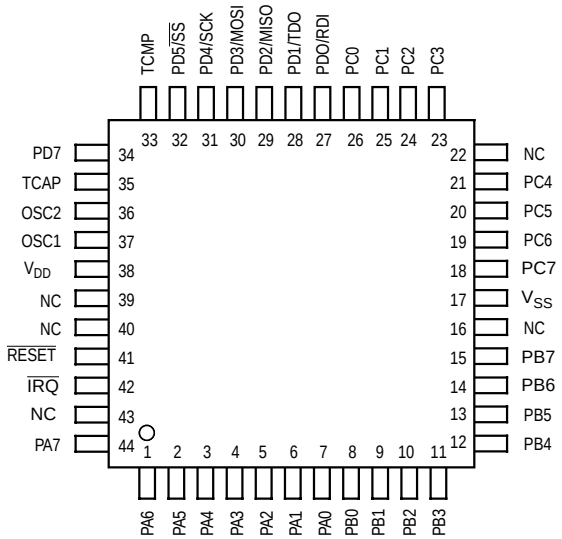
This section contains additional pin assignments and package dimension information that supplements the *MC68HC05C4 Advanced Information Data Sheet* (ADI991R2) mechanical data section.

11.1 PIN ASSIGNMENTS

42-Pin Shrink DIP Package

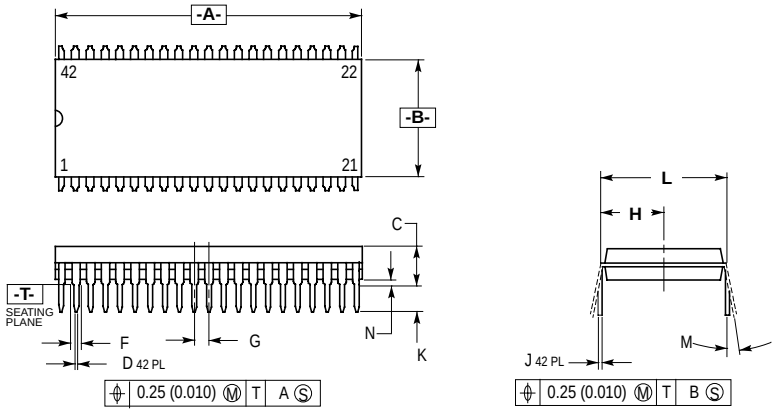


44-Pin QFP Package



11.2 PACKAGE DIMENSIONS

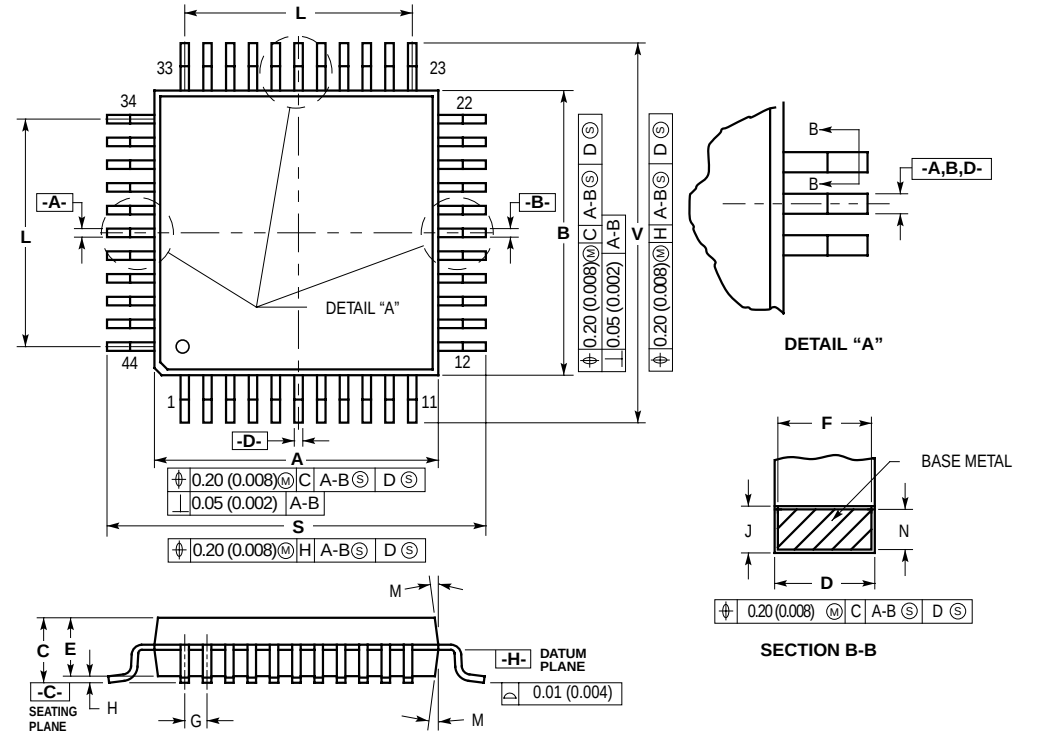
CASE 858-01

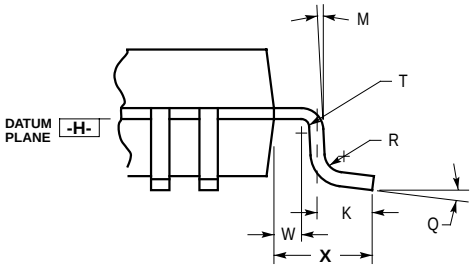


NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	0.81	1.17	0.032	0.046
G	1.778 BSC		0.070 BSC	
H	7.62 BSC		0.300 BSC	
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 824





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5	10	5	10
N	0.13	0.17	0.005	0.007
Q	0	7	0	7
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0	—	0	—
V	12.95	13.45	0.510	0.530
W	0.40	—	0.016	—
X	1.6 REF		0.063 REF	

APPENDIX C
MC68HC805C4

The MC68HC805C4 microcomputer unit (MCU) device is similar to the MC68HC05C4 MCU device with the exception of the EEPROM feature. This feature of the MC68HC805C4 MCU enables the user to emulate the MC68HC05C4 MCU device. Information pertaining to the EEPROM emulation feature is contained in **APPENDIX D MC68HC05C4 EMULATION**. The entire data sheet of the MC68HC05C4 MCU applies to the MC68HC805C4 MCU with the exceptions provided in this appendix.

C.1 INTRODUCTION

Information contained in **SECTION 1 INTRODUCTION** (general information, features, and block diagram) of this document applies to the MC68HC805C4 MCU device except for the areas described in the following paragraphs.

C.1.1 Features

The features of the MC68HC805C4 MCU are as follows:

- Emulation of MC68HC05C4
- 4160 Bytes of EEPROM (Replaces 4160 Bytes of ROM on MC68HC05C4)
- On-Chip Bootstrap Firmware for Programming Use
- User Callable Subroutines to Simplify Programming*
- Breakpoint Register for Software Debugging
- Self-Check Mode Replaced by Bootstrap Capability
- Software Programmable External Interrupt Sensitivity (Default is Edge- and Level-Sensitive)

C.1.2 Block Diagram

Figure C-1 illustrates the MC68HC805C4 MCU device block diagram.

C.2 FUNCTIONAL PIN DESCRIPTION, INPUT/OUTPUT PROGRAMMING, MEMORY, CPU REGISTERS, AND SELF-CHECK

Information contained in **SECTION 2 FUNCTIONAL PIN DESCRIPTION, INPUT/OUTPUT PROGRAMMING, MEMORY, CPU REGISTERS, AND SELF-CHECK** of this document applies to the MC68HC805C4 MCU device except for the areas described in the following paragraphs.

*Contact local Freescale representative.

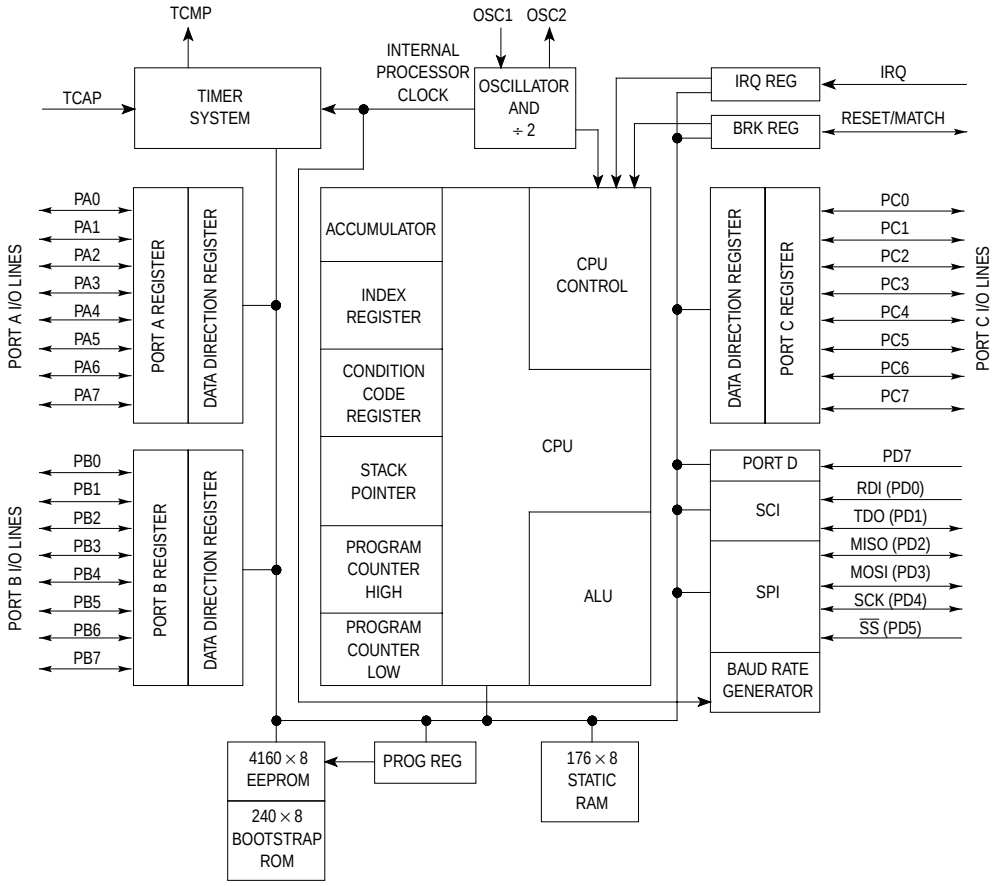


Figure C-1. MC68HC805C4 Microcomputer Block Diagram

C.2.1 Reset/Match ($\overline{\text{RESET}}$/$\overline{\text{MATCH}}$)

The $\overline{\text{RESET}}$/$\overline{\text{MATCH}}$ pin (pin 1) provides two functions. These functions are used to master reset the MCU or generate an address match breakpoint pulse. When master resetting, pin 1 is an input to the MCU device. When generating the breakpoint pulse, pin 1 is an output from the MCU. Refer to **C.5 HARDWARE BREAKPOINT REGISTERS** for additional information pertaining to the $\overline{\text{RESET}}$/$\overline{\text{MATCH}}$ pin.

C.2.2 V_{PP}

External V_{PP} (19.75 Vdc ± 0.25 Vdc) must be supplied to the V_{PP} pin (pin 3) for programming and erasing the EEPROM arrays.

C.2.3 Memory

Figure C-2 illustrates the MC68HC805C4 MCU device address map. As shown, page zero resides from $0000 through $00FF, and is accessed with short instructions.NOTE

NOTE

All user defined reset and interrupt vectors are implemented in EEPROM.

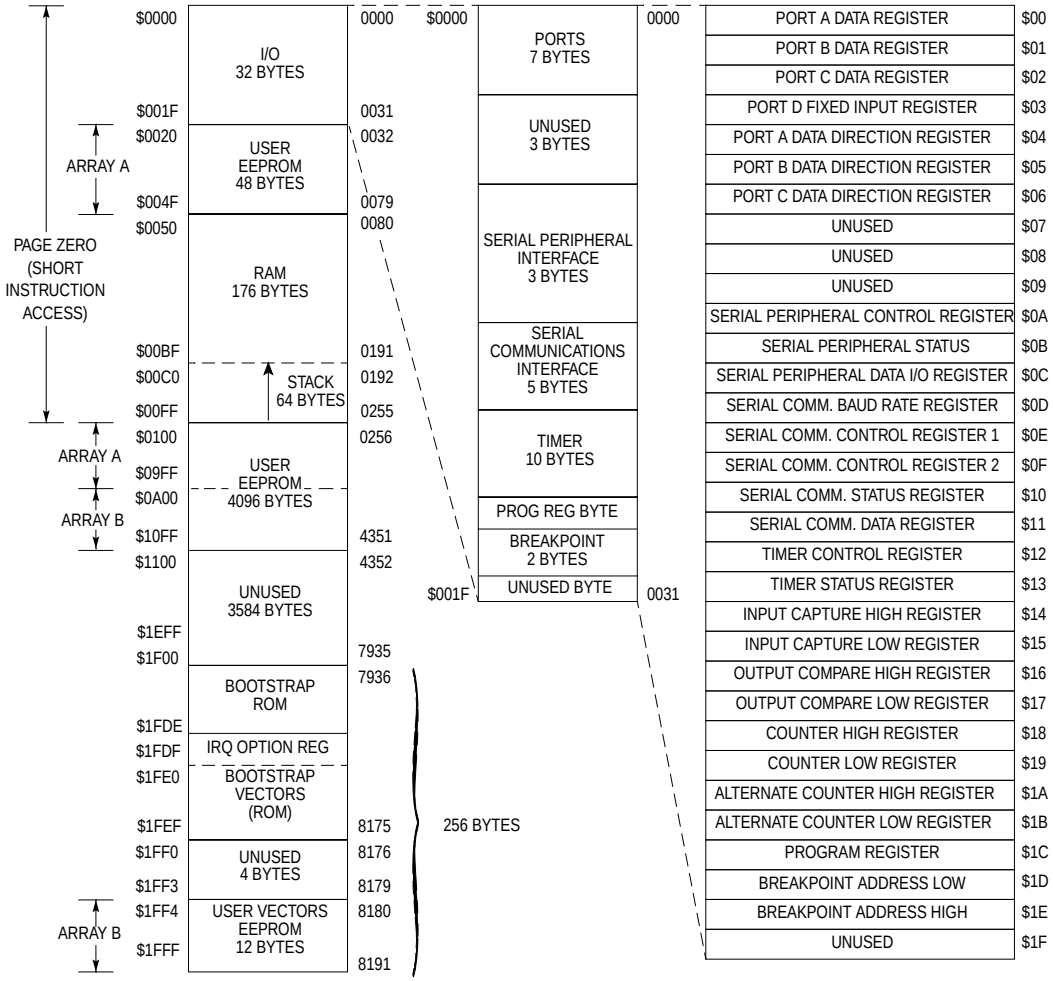


Figure C-2. MC68HC805C4 Memory Map

C.2.4 Self-Check

The self-check ROM is replaced with the bootstrap ROM, therefore the self-check capability is not applicable for the MC68HC805C4 device. Timer test and ROM checksum subroutines are part of the self-check routine. Therefore, both subroutines are also not applicable.

C.3 RESETS, INTERRUPTS, AND LOW POWER MODES

Information contained in **SECTION 3 RESETS, INTERRUPTS, AND LOW POWER MODES** of this document applies to the MC68HC805C4 MCU device except for the areas described in the following paragraphs.

C.3.1 External Interrupt

The MC68HC05C4 MCU $\overline{\text{IRQ}}$ pin sensitivity is mask programmable. Either negative edge- and level-sensitive triggering, or negative edge-sensitive triggering are available as a mask option. The MC68HC805C4 MCU uses the IRQ option register residing at location $1FDF to control the $\overline{\text{IRQ}}$ pin sensitivity.

IRQ Option Register

Bit 7	6	5	4	3	2	1	Bit 0	
0	0	0	0	0	0	IRQ	0	$1FDF

B7–B2 Logic zero

B1 When the interrupt request (IRQ) bit is set (logic one), the $\overline{\text{IRQ}}$ pin is negative edge- and level-sensitive. When the IRQ bit is cleared (logic zero), the $\overline{\text{IRQ}}$ pin is negative edge sensitive. The IRQ bit is set by system reset. This control bit can only be cleared once following a reset.

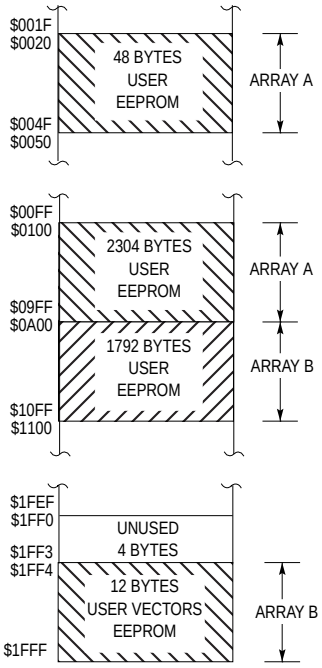
B0 Logic zero

C.3.2 Low Power Modes

Low power mode information for the MC68HC05C4 device is applicable for the MC68HC805C4 MCU device.

C.4 EEPROM

Information in this section pertains to the MC68HC805C4 MCU EEPROM. The MCU EEPROM consists of 4144 bytes of user EEPROM (which includes 48-bytes in page zero), and 16 bytes of user vector EEPROM. As shown in Figure C-2, the user EEPROM resides at locations $0020-$004F, and $0100-$10FF. User vector EEPROM resides at locations $1FF0-$1FFF. The MCU EEPROM is implemented as two separate EEPROM arrays. These arrays (shown below) are designated as A and B. Array A consists of page zero EEPROM ($0020-$004F) and locations $0100-$09FF; and array B consists of locations $0A00-$10FF, and locations $1FF0-$1FFF. Each array has assigned programming address and data buses which are latched while a programming function is being performed. Separate arrays allow program execution in one array, while writing/erasing in the other array.



Two types of EEPROM programming (single-byte or multi-byte) can be performed. Single-byte EEPROM programming is accomplished via the program register residing at location $001C. Multi-byte EEPROM programming is used to load a user program into the MC68HC805C4 MCU EEPROM in order to emulate the MC68HC05C4 device. This type of programming is accomplished via the bootstrap mode operation which is described in **APPENDIX D MC68HC05C4 EMULATION**.

C.4.1 Program Register

The program register (shown below) is used to perform single-byte EEPROM programming.

Program Register

Bit 7	6	5	4	3	2	1	Bit	
0	EEEN	0	0	ERASE	LATA	LATB	EEPGM	$1C

B7 Logic zero.

B6 The EEEN bit must be enabled for any EEPROM write/erase operation. Reset clears the EEEN bit. The EEEN bit should be cleared upon completion of any EEPROM write/erase operation, or before entering the low power modes (via the STOP or WAIT instructions) to reduce power usage. This bit is both readable and writable.

B5/B4 Logic zero.

B3 When the erase (ERASE) bit is set, the erase mode of the EEPROM programming operation is enabled. Reset clears the ERASE bit. When the ERASE bit is cleared, normal read or program modes can be specified. This bit is both readable and writable.

B2 Prior to an array A write or erase operation, the latch A (LATA) bit must be set. This enables the EEPROM array A data and address buses to be latched for programming/erasing on the next byte write cycle. Reset clears the LATA bit. When the LATA bit is cleared, array A data and address buses are unlatched for normal CPU operations. This bit is both readable and writable.

B1 Prior to an array B write or erase operation, the latch B (LATB) bit must be set. This enables the EEPROM array B data and address buses to be latched for programming/erasing on the next byte write cycle. Reset clears the LATB bit. When the LATB bit is cleared, array B data and address buses are unlatched for normal CPU operations. This bit is both readable and writable.

B0 When the electrically erase/program (EEPGM) bit is set, V_{PP} power is applied to the EEPROM array for programming or erasing modes of operation. Reset clears the EEPGM bit. This bit is readable, but only writable when LATA or LATB bits are set and a write operation to the corresponding array has occurred. If LATA and LATB bits are cleared, EEPGM bit cannot be set.

C.4.2 Single-Byte Programming

Figure C-3 illustrates the MC68HC805C4 EEPROM single-byte programming operation. The write cycle timing listed in the flowchart is preliminary and subject to change.

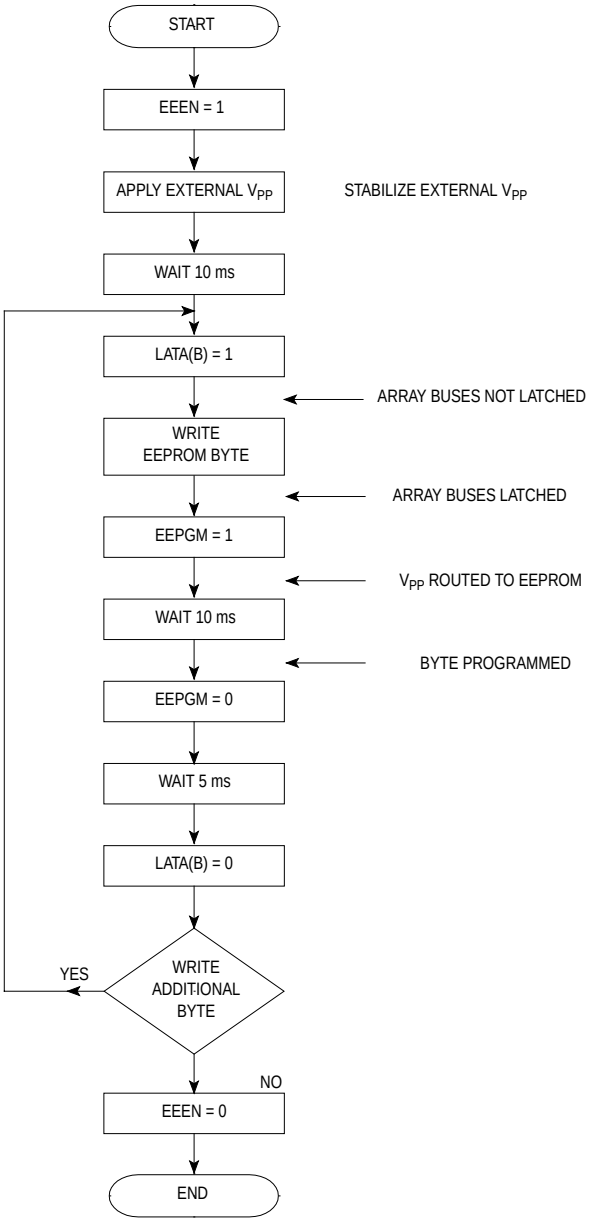


Figure C-3. Single-Byte EEPROM Programming

C.4.3 Erasing

Each array can be erased independently or simultaneously. Figure C-4 illustrates the MC68HC805C4 EEPROM erasing operation. EEPROM erasing operation takes up to 100 milliseconds. If both arrays A and B are erased simultaneously, the operation takes up to 200 milliseconds. Both arrays may be erased by setting both LATA and LATB bits, and writing (any kind of data) to a byte in both arrays before setting the EEPGM bit.

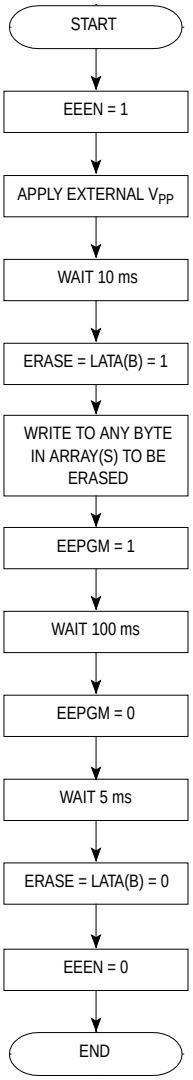


Figure C-4. EEPROM Erasing

C.5 HARDWARE BREAKPOINT REGISTERS

The hardware breakpoint registers (shown below) are used as a program debugging aid.

Breakpoint Address Register Low (ARL)

Bit 7	6	5	4	3	2	1	Bit 0	
A7	A6	A5	A4	A3	A2	A1	A0	$1D

B7–B0 Breakpoint address bits A7 through A0. Reset clears address bits A7 through A0.

Breakpoint Address Register High (ARH)

Bit 7	6	5	4	3	2	1	Bit	
0	0	MATCH	A12	A11	A10	A9	A8	$1E

B7/B6 Logic zero.

B5 When the match (MATCH) enable bit is set, the address match comparator is enabled. Reset clears the MATCH bit.

B4–B0 Breakpoint address bits A12 through A8. Reset clears address bits A12 through A8.

A breakpoint address is written into address registers ARL and ARH by the user. The lower eight bits (A0–A7) of the breakpoint address are written into the ARL. The upper five bits (A8–A12) of the breakpoint address are written into the ARH. ARL and ARH are then concatenated to form the breakpoint address. When the processor fetches an instruction with the same address as the breakpoint address, $\overline{\text{RESET}}$/$\overline{\text{MATCH}}$ pin goes low for one-half machine cycle. The pin is then driven high (completing the breakpoint pulse) for one-half cycle to ensure that no false resets are generated on successive cycles. This operation will not alter program flow.

The $\overline{\text{RESET}}$/$\overline{\text{MATCH}}$ pin will require that the user provide an open-drain device during debugging operations to avoid any conflicts. A maximum of 100 picofarads load is allowed on the $\overline{\text{RESET}}$/$\overline{\text{MATCH}}$ pin when in the debug mode.

C.6 ELECTRICAL SPECIFICATIONS

Information contained in **SECTION 9 ELECTRICAL SPECIFICATIONS** of this document applies to the MC68HC805C4 MCU device except for the areas described in the following paragraphs.

Estimated operating (run) current at 5.0 Vdc ± 10% is typically 2 milliamperes greater than MC68HC05C4. The Wait mode increase (from MC68HC05C4 to MC68HC805C4) is typically 200-300 microamperes. Maximum supply current specifications for the MC68HC805C4 are to be determined.

$\overline{\text{RESET}}$/$\overline{\text{MATCH}}$ pin output levels are equivalent to the output levels of por

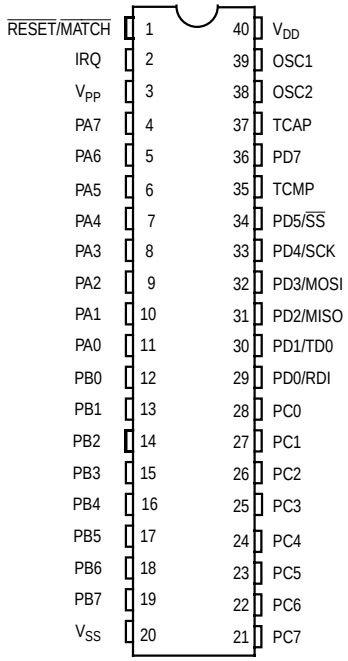
C.7 ORDERING INFORMATION

Refer to **SECTION 10 ORDERING INFORMATION** of this document for MCU ordering form information.

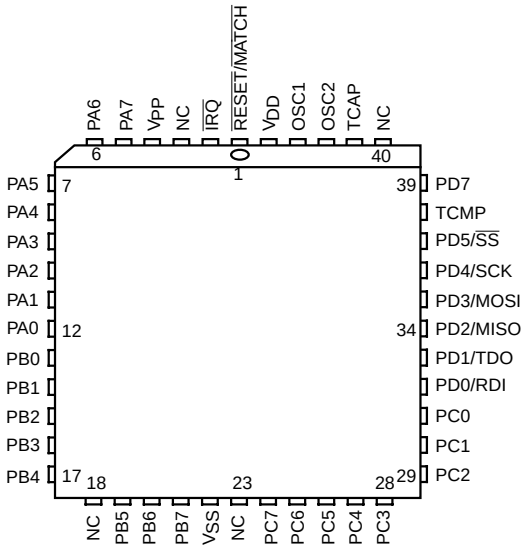
C.8 MECHANICAL DATA

Information contained in **SECTION 11 MECHANICAL DATA** of this document applies to the MC68HC805C4 MCU device except for the pin assignments which are identified below.

40-PIN DUAL IN-LINE PACKAGE



44-LEAD PLCC PACKAGE



NOTE: BULK SUBSTRATE TIED TO V_{SS}.

APPENDIX D
MC68HC05C4 EMULATION

D.1 INTRODUCTION

The EEPROM feature of the MC68HC805C4 MCU enables the user to emulate the MC68HC05C4 MCU device. The following paragraphs describe the multi-byte EEPROM programming technique used to program the MC68HC805C4 MCU internal EEPROM to emulate the MC68HC05C4 MCU device. The multi-byte EEPROM programming technique (introduced in **APPENDIX C MC68HC805C4**) uses a bootstrap program contained in ROM to program the MC68HC805C4 MCU internal EEPROM. Figure D-1 illustrates typical MC68HC805C4 MCU EEPROM programming board/circuitry used in conjunction with the multi-byte EEPROM programming technique.

D.2 MULTI-BYTE PROGRAMMING

The multi-byte EEPROM programming technique is used to load a user program into the MC68HC805C4 MCU EEPROM in order to emulate the MC68HC05C4 device. This type of multi-byte programming is accomplished via a bootstrap mode of operation. The user program contained in EPROM is copied into the internal EEPROM of the MC68HC805C4 device.

The MC68HC805C4 device is inserted into the programming board/circuitry as illustrated in Figure D-1. Programming routine is selected via mode switches S1 through S4, and +5 volt power is applied to the programming circuitry. The MCU is removed from the reset state and placed in the run mode of operation via switch S5, and MCU control is transferred to the bootstrap ROM. The selected programming routine is then executed.

EEPROM programming sequence of events are as follows:

1. Place switch S5 to RESET position.
2. Select programming routine via switches S1–S4.
3. Apply +5 volt power to programming circuitry.
4. Apply external V_{PP} to programming circuitry.
5. Place switch S5 in RUN position.
6. Programming routine is executed.
7. Place switch S5 to RESET position.
8. Remove external V_{PP} from programming circuitry.
9. Remove +5 volt power, or select and run new routine.

Once the bootstrap mode is entered, mode switch settings are scanned to establish the routine to be executed. The routines are as follows:

- Program and Verify EEPROM
- Bulk Erase and Verify EEPROM
- Load Program in RAM and Execute
- Verify EEPROM Contents
- Dump EEPROM Contents
- Execute Program in RAM

D.2.1 Program and Verify EEPROM

In the program and verify EEPROM routine, the contents of an external 8K EPROM are copied into the EEPROM areas of the MC68HC805C4 device. There is a direct correspondence of addresses between the two devices. Non-EEPROM addresses are ignored so data contained in those areas are not accessed. Unprogrammed EPROM address locations should contain $FF to speed up the programming operation. During the programming routine the PROGRAMMING LED DS2 is illuminated. At the end of the programming routine, DS2 is turned off, and the verification routine is entered. If the contents of the EEPROM and external ROM exactly match, then the VERIFIED LED DS1 is illuminated. The verification routine stops if a discrepancy has been detected and the error address location will be placed on the external memory address bus.

Devices from the A65G mask set do not automatically verify at the end of the programming routine. When the programming LED DS2 turns off, reset the MC68HC805C4 and follow the procedure described in **D.2.4 Verify EEPROM Contents**.

D.2.2 Bulk Erase and Verify EEPROM

In the bulk erase and verify EEPROM routine, all EEPROM locations are returned to the unprogrammed ($FF) state. Upon completion of this erasing operation, every EEPROM location is verified for $FF. When every location is erased and verified, the VERIFIED LED DS1 is illuminated. If a location did not erase, the error address location will be placed on the external memory address bus. If required, this routine can be reexecuted until all EEPROM locations are erased and verified.

During the erase verification routine external memory is disabled, the data port is switched to output data, and $FF data value is written into the output register. All locations are compared to the erased byte state ($FF). The verification routine stops if a discrepancy has been detected and the error address location will be placed on the external memory address bus.

D.2.3 Load Program in RAM and Execute

In the load program in RAM and execute routine, user programs are loaded into MCU RAM via the serial communications interface (SCI) port, and then executed. Data is loaded sequentially, starting at RAM location $0050, until the last byte is loaded. Program control is then transferred to the RAM program starting at location $0051. The first byte loaded is the count of the total number of bytes in the program plus the count byte. The program starts at the second byte in RAM. During the firmware initialization stage the SCI is configured for the NRZ data format (idle line, start bit, eight data bits, and stop bit). The baud rate is 4800 with a 2 MHz crystal.

If immediate execution is not desired after loading the RAM program, it is possible to hold off execution. This is accomplished by the setting of the byte count to a value that is greater than the overall length of the loaded data. When the last byte is loaded, the firmware will halt operations expecting additional data to arrive. At this point, switch S5 is placed in the RESET position which will reset the MCU but keep the RAM program intact. All other routines (modes) can now be entered from this state, including the one which will execute the program in RAM, once switch S5 is placed in the RUN position. At the end of the RAM load routine, ports A and C are configured as outputs.

D.2.4 Verify EEPROM Contents

The verify EEPROM contents routine is normally entered automatically after the EEPROM is programmed or erased. Direct entry of this mode will cause the EEPROM contents to be compared to external memory contents residing at the same address locations. Both DS1 and DS2 LEDs are turned off at this time until verification is completed. Upon completion of the verification routine (every location verified) the VERIFIED LED DS1 is illuminated. If DS1 does not illuminate, a discrepancy has been detected and the error address location will be placed on the external memory address bus.

D.2.5 Dump EEPROM Contents

In the dump EEPROM contents routine, entire EEPROM contents are dumped sequentially to the SCI output. The first location transmitted will be $0020 and the last one will be $1FFF. Unused locations will be bypassed so that no gaps will appear in the data stream. The external memory address lines will always indicate the current location being transmitted. The data is sent out in exactly the same NRZ format described in the load program in RAM routine.

D.2.6 Execute Program in RAM

Using this routine, the MCU will transfer control to a program that has been previously loaded into RAM. This program will be executed once the bootstrap mode has been entered, if mode switch S4 is activated. No firmware initializations will take place. The program must start at RAM location $0051 to be compatible with the load program in RAM routine.

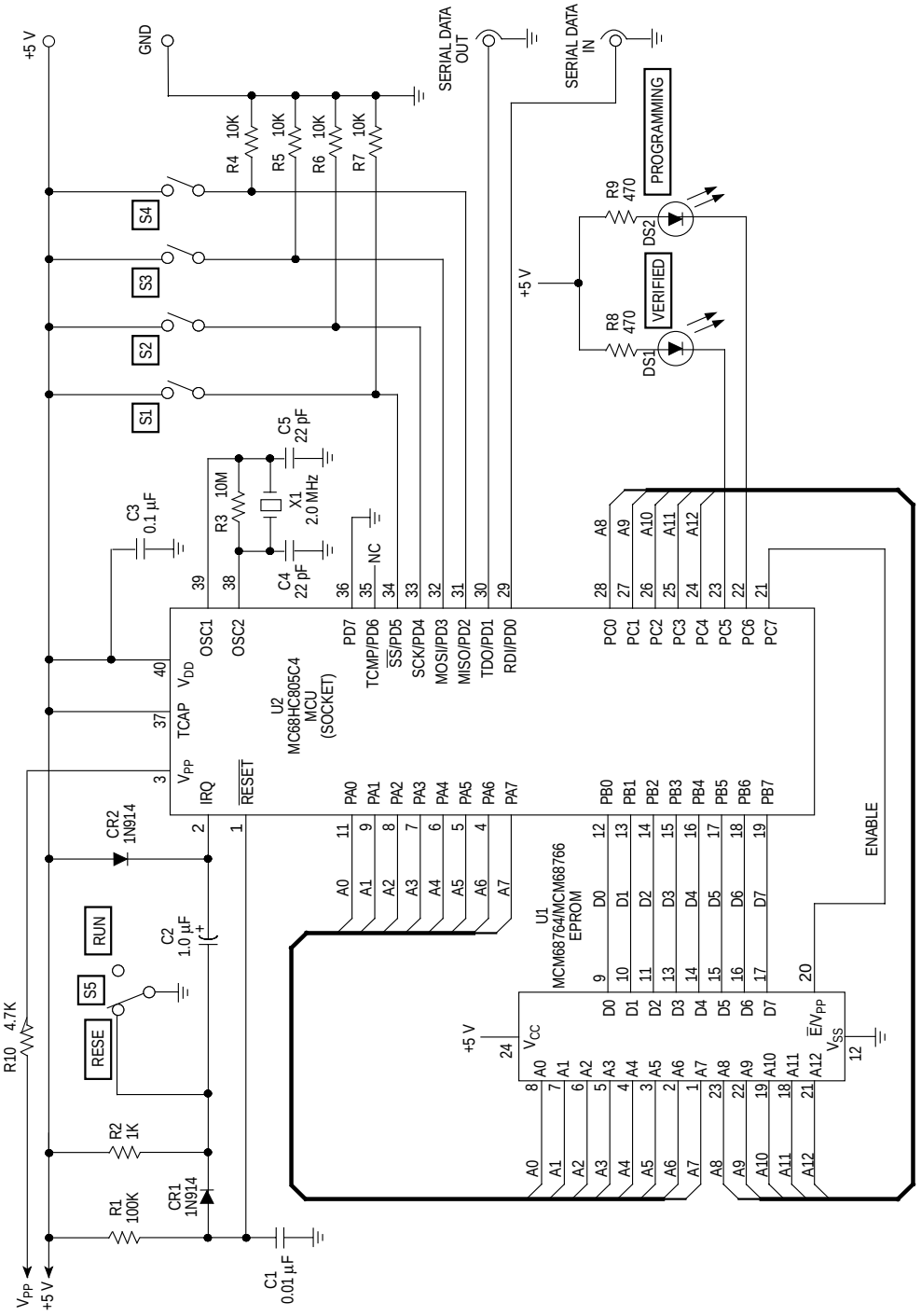


Figure D-1. MC68HC805C4 MCU EEPROM Programming Board/Circuitry

APPENDIX E
MC68HCL05C4

The MC68HCL05C4 microcomputer unit (MCU) device is a low power version of the MC68HC05C4 MCU device. The entire data sheet of the MC68HC05C4 applies to the MC68HCL05C4 with the exception of the following DC electrical characteristics provided in this appendix.

Low Power Output Voltage (V_{DD} = 1.8–2.3 Vdc)

Characteristic	Symbol	Min	Typ	Max	Unit
Output High Voltage (I_{LOAD} = –0.1 mA) PA7–PA0, PB7–PB0, PC7–PC0, TCMP (I_{LOAD} = –0.2 mA) PD4-PD1	V_{OH}	V_{DD}–0.3 V_{DD}–0.3	—	—	V
Output Low Voltage (I_{LOAD} = 0.2 mA) PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1	V_{OL}	—		0.3	V

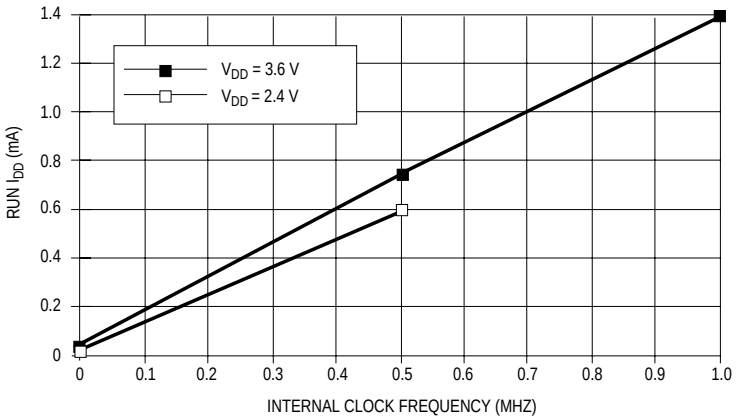
Low Power Output Voltage (V_{DD} = 2.4–3.6 Vdc)

Characteristic	Symbol	Min	Typ	Max	Unit
Output High Voltage (I_{LOAD} = –0.2 mA) PA7–PA0, PB7–PB0, PC6–PC0, TCMP (I_{LOAD} = –0.4 mA) PD4–PD1	V_{OH}	V_{DD}–0.3 V_{DD}–0.3	—	—	V
Output Low Voltage (I_{LOAD} = 0.4 mA) PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1	V_{OL}	—		0.3	V

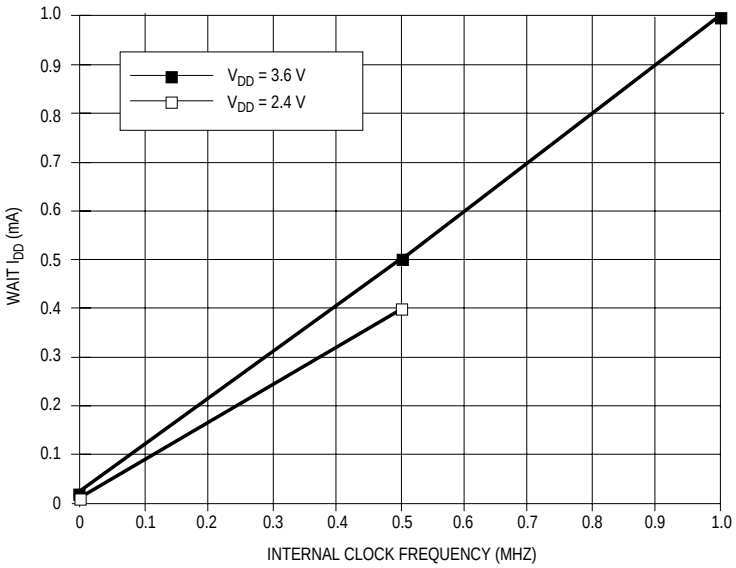
Low Power Supply Current

Characteristic	Symbol	Min	Typ(1)	Max	Unit
Supply Current (V_{DD} = 4.5–5.5 Vdc, f_{OP} = 2.1 MHz)					
Run(2)	I_{DD}	—	3.50	4.25	mA
WAIT(3)		—	1.60	2.25	mA
STOP(4)					
25 °C		—	1	15	µA
0 °C to 70 °C (Standard)		—	—	25	µA
Supply Current (V_{DD} = 2.5–3.6 Vdc f_{OP} = 1.0 MHz)					
Run(2)	I_{DD}	—	1.00	1.4	mA
WAIT(3)		—	0.70	1.0	µA
STOP(4)					
25 °C		—	1	5	µA
0 °C to 70 °C (Standard)		—	—	10	µA
Supply Current (V_{DD} = 2.5–3.6 Vdc f_{OP} = 500 kHz)	I_{DD}				
Run(2)		—	400	750	µA
WAIT(3)		—	300	500	µA
STOP(4)					
25 °C		—	1	5	µA
0 °C to 70 °C (Standard)		—	—	10	µA
Supply Current (V_{DD} = 1.8–2.4 Vdc f_{OP} = 500 kHz)					
Run(2)	I_{DD}	—	300	600	µA
WAIT(3)		—	250	400	µA
STOP(4)					
25 °C		—	1	2	µA
0 °C to 70 °C (Standard)		—	—	5	µA

1. Typical values reflect average measurements at midpoint of voltage range at 25 °C.
2. Run (operating) I_{DD} measured using external square wave clock source wilth all inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.
3. WAIT I_{DD} measured using external square wave clock source wilth all inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. V_{IL} = 0.2 V, V_{IH} = V_{DD} –0.2V. OSC2 capacitance linearly affects WAIT I_{DD}.
4. STOP I_{DD} measured with OSC1 = V_{DD}. All ports configured as inputs. V_{IL} = 0.2 V, V_{IH} = V_{DD} –0.2 V.



Maximum Run Mode I_{DD} vs Frequency



Maximum WAIT Mode I_{DD} vs Frequency

MC Order Numbers

Package Type	Temperature Range	Order Number
40-Pin Dual In-Line Package (DIP)	0 °C to 70 °C	MC68HCL05C4P
44-Lead Plastic-Leaded Chip Carrier (PLCC)	0 °C to 70 °C	MC68HCL05C4FN
42-Pin Shrink Dual In-Line Package (SDIP)	0 °C to 70 °C	MC68HCL05C4B
44-Pin Quad Flat Pack (QFP)	0 °C to 70 °C	MC68HCL05C4FB
40-Pin Ceramic Dual In-Line (CERDIP)	0 °C to 70 °C	MC68HCL05C4S

MC68HC05C4AD/D
Rev. 4.3

APPENDIX F
MC68HCL05C8

The MC68HCL05C8 microcomputer unit (MCU) device is a low power version of the MC68HC05C4 MCU device. The entire data sheet of the MC68HC05C4 applies to the MC68HCL05C8 with the exceptions provided in this appendix.

The MC68HCL05C8 incorporates 3584 additional bytes of user ROM for a total of 7744 bytes of on-chip user ROM. Figure F-1 illustrates the MC68HCL05C8 memory map.

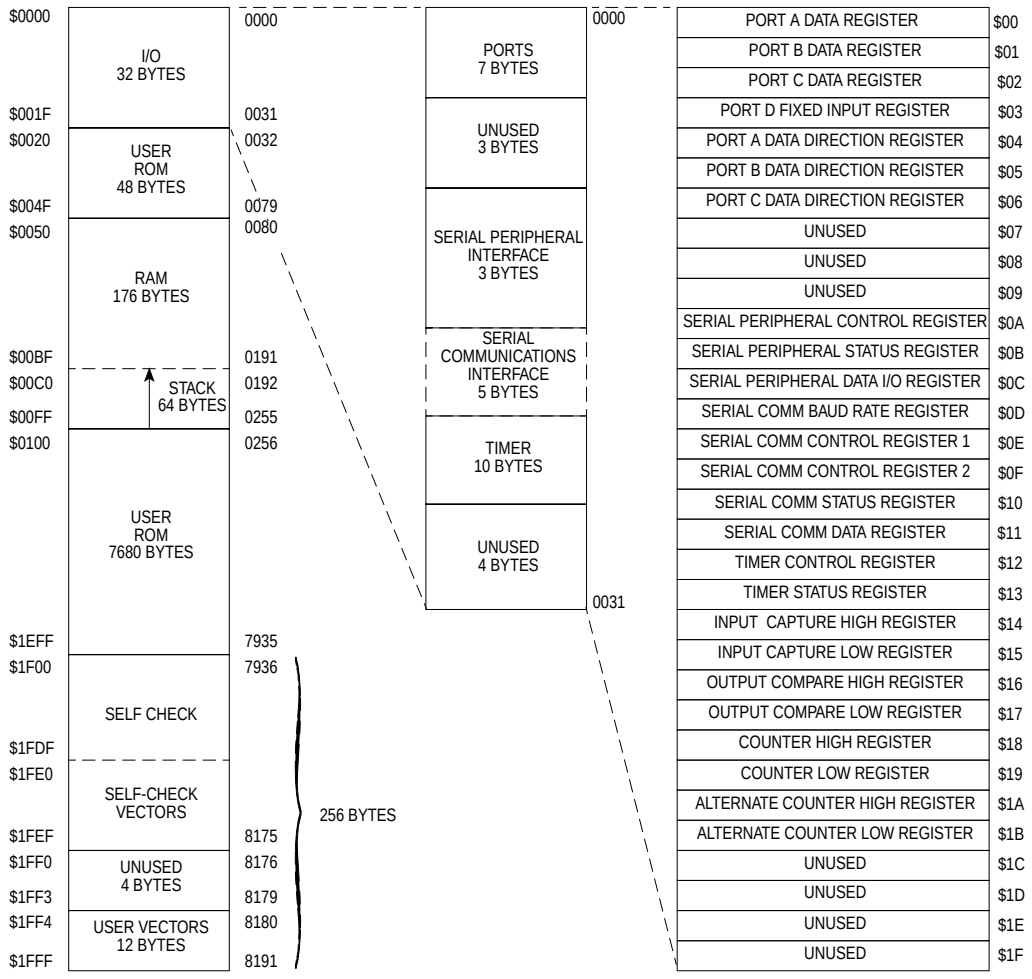


Figure F-1. MC68HCL05C8 Memory Map

The MC68HCL05C8 DC electrical characteristics are as follows:

Low Power Output Voltage (V_{DD} = 1.8–2.3 Vdc)

Characteristic	Symbol	Min	Typ	Max	Unit
Output High Voltage (I_{LOAD} = –0.1 mA) PA7–PA0, PB7–PB0, PC6–PC0, TCMP (I_{LOAD} = –0.2 mA) PD4–PD1	V_{OH}	V_{DD}–0.3 V_{DD}–0.3	—	—	V
Output Low Voltage (I_{LOAD} = 0.2 mA) PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1	V_{OL}	—		0.3	V

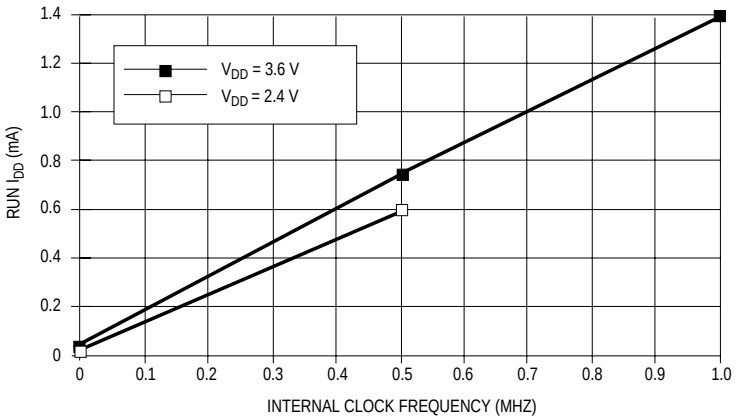
Low Power Output Voltage (V_{DD} = 2.4–3.6 Vdc)

Characteristic	Symbol	Min	Typ	Max	Unit
Output High Voltage (I_{LOAD} = –0.2 mA) PA7–PA0, PB7–PB0, PC6–PC0, TCMP (I_{LOAD} = –0.4 mA) PD4–PD1	V_{OH}	V_{DD}–0.3 V_{DD}–0.3	—	—	V
Output Low Voltage (I_{LOAD} = 0.4 mA) PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1	V_{OL}	—		0.3	V

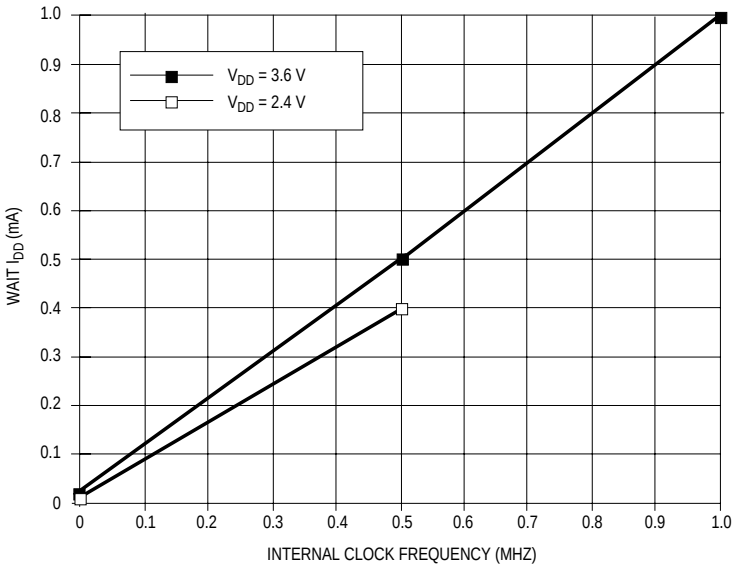
Low Power Supply Current

Characteristic	Symbol	Min	Typ(1)	Max	Unit
Supply Current (V_{DD} = 4.5–5.5 Vdc, f_{OP} = 2.1 MHz)					
Run(2)	I_{DD}	—	3.50	4.25	mA
WAIT(3)		—	1.60	2.25	mA
STOP(4)					
25 °C		—	1	15	µA
0 °C to 70 °C (Standard)		—	—	25	µA
Supply Current (V_{DD} = 2.5–3.6 Vdc f_{OP} =1.0 MHz)					
Run(2)	I_{DD}	—	1.00	1.4	mA
WAIT(3)		—	0.70	1.0	mA
STOP(4)					
25 °C		—	1	5	µA
0 °C to 70 °C (Standard)		—	—	10	µA
Supply Current (V_{DD} = 2.5–3.6 Vdc f_{OP} = 500 kHz)	I_{DD}				
Run(2)		—	400	750	µA
WAIT(3)		—	300	500	µA
STOP(4)					
25 °C		—	1	5	µA
0 °C to 70 °C (Standard)		—	—	10	µA
Supply Current (V_{DD} = 1.8–2.4 Vdc f_{OP} = 500 kHz)					
Run(2)	I_{DD}	—	300	600	µA
WAIT(3)		—	250	400	µA
STOP(4)					
25 °C		—	1	2	µA
0 °C to 70 °C (Standard)		—	—	5	µA

1. Typical values reflect average measurements at midpoint of voltage range at 25 °C.
2. Run (operating) I_{DD} measured using external square wave clock source wilth all inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.
3. WAIT I_{DD} measured using external square wave clock source wilth all inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2. All ports configured as inputs. V_{IL} = 0.2 V, V_{IH} = V_{DD} –0.2 V. OSC2 capacitance linearly affects WAIT I_{DD}.
4. STOP I_{DD} measured with OSC1 = V_{DD}. All ports configured as inputs. V_{IL} = 0.2 V, V_{IH} = V_{DD} –0.2 V.



Maximum Run Mode I_{DD} vs Frequency



Maximum WAIT Mode I_{DD} vs Frequency

MC Order Numbers

Package Type	Temperature Range	Order Number
40-Pin Dual In-Line Package (DIP)	0 °C to 70 °C	MC68HCL05C8P
44-Lead Plastic-Leaded Chip Carrier (PLCC)	0 °C to 70 °C	MC68HCL05C8FN
42-Pin Shrink Dual In-Line Package (SDIP)	0 °C to 70 °C	MC68HCL05C8B
44-Pin Quad Flat Pack (QFP)	0 °C to 70 °C	MC68HCL05C8FB
40-Pin Ceramic Dual In-Line Package (CERDIP)	0 °C to 70 °C	MC68HCL058S

MC68HC05C4AD/D
Rev. 4.3

APPENDIX G
MC68HSC05C8

The MC68HSC05C8 microcomputer unit (MCU) device is a high speed version of the MC68HC05C4 MCU device. The entire data sheet of the MC68HC05C4 applies to the MC68HSC05C8 with the exceptions provided in this appendix.

The MC68HSC05C8 incorporates 3584 additional bytes of user ROM for a total of 7744 bytes of on-chip user ROM. Figure G-1 illustrates the MC68HSC05C8 memory map.

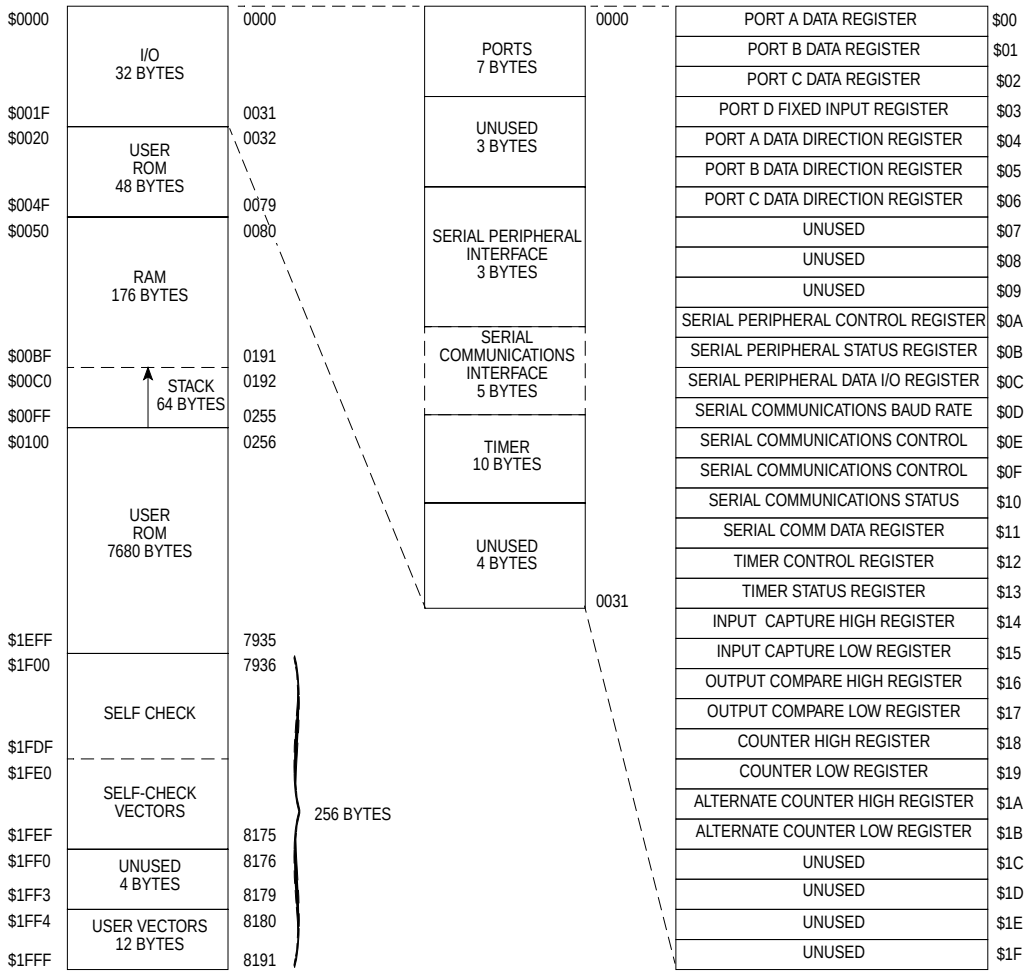


Figure G-1. MC68HSC05C8 Memory Map

The MC68HSC05C8 DC electrical characteristics are as follows:

G.1 DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = 0° to 70 °C)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage, $I_{Load} \leq 10.0$ µA	V_{OL} V_{OH}	— V_{DD} - 0.1	— —	0.1 —	V V
Output High Voltage (I_{Load} = 0.8 mA) PA0-PA7, PB0-PB7, PC0-PC7, TCMP (See Figure 9-2) (I_{Load} = 1.6 mA) PD1-PD4 (See Figure 9-3)	 V_{OH} V_{OH}	 V_{DD} - 0.8 V_{DD} - 0.8	 — —	 — —	 V V
Output Low Voltage (See Figure 9-4) (I_{Load} =1.6 mA) PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD4, TCMP	V_{OL}	—	—	0.4	V
Input High Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input Low Voltage PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD5, PD7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Data Retention Mode (0° to 70 °C)	V_{RM}	2.0	—	—	V
Supply Current (See Notes) Run (See Figures 9-5 and 9-6) Wait (See Figures 9-5 and 9-6) Stop (See Figure 9-6) 25 °C 0° to 70 °C (Standard)	 I_{DD} I_{DD} I_{DD} I_{DD}	 — — — —	 6.7 3.0 2.0 —	 13.3 7.6 50 140	 mA mA µA µA
I/O Ports Hi-Z Leakage Current PA0-PA7, PB0-PB7, PC0-PC7, PD1-PD4	I_{IL}	—	—	± 10	µA
Input Current $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0, PD5, PD7	I_{in}	—	—	± 1	µA
Capacitance Ports (as Input or Output) $\overline{RESET}$, $\overline{IRQ}$, TCAP, OSC1, PD0-PD5, PD7	 C_{out} C_{in}	 — —	 — —	 12 8	 pF pF

NOTES:

1. All values shown reflect average measurements.
2. Typical values at midpoint of voltage range, 25 °C only.
3. Wait I_{DD}: Only timer system active (SPE = TE = RE = 0). If SPI, SCI active (SPE = TE = RE = 1) add 10% current draw.
4. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square wave clock source (f_{osc} = 8.0 MHz), all inputs 0.2 V from rail, no DC loads, less than 50 pF on all outputs, C_L = 20 pF on OSC2.
5. Wait, Stop, I_{DD}: All ports configured as inputs, V_{IL} = 0.2 V, V_{IH} = V_{DD} –0.2 V.
6. Stop I_{DD} measured with OSC1 = V_{SS}.
7. Standard temperature range is 0° to 70 °C. 25 °C only version is available.
8. Wait I_{DD} is affected linearly by the OSC2 capacitance.
9. Figures 9-5 and 9-6 reflect supply currents up to 2.0 MHz internal operating frequency. There is a linear relationship between supply current and operating frequency for frequencies beyond 2.0 MHz for the MC68HSC05C4 device.

G.2 CONTROL TIMING

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = 0° to 70 °C)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Crystal Option External Clock Option	 f_{osc} f_{osc}	 — dc	 8.0 8.0	 MHz MHz
Internal Operating Frequency Crystal (f_{osc} ÷ 2) External Clock (f_{osc} ÷ 2)	 f_{op} f_{op}	 — dc	 4.0 4.0	 MHz MHz
Cycle Time (See Figure 3-1)	t_{cyc}	250	—	ns
Crystal Oscillator Startup Time (See Figure 3-1)	t_{OXOV}	—	100	ms
Stop Recovery Startup Time (Crystal Oscillator) (See Figure 9-8)	t_{ILCH}	—	100	ms
$\overline{\text{RESET}}$ Pulse Width (See Figure 3-1)	t_{RL}	1.5	—	t_{cyc}
Timer Resolution** Input Capture Pulse Width (See Figure 9-9) Input Capture Pulse Period (See figure 9-9)	 t_{RESL} t_{TH}, t_{TL} t_{TLTL}	 4.0 63 ***	 — — —	 t_{cyc} ns t_{cyc}
Interrupt Pulse Width Low (Edge-Triggered) (See Figure 3-4)	t_{ILIH}	63	—	ns
Interrupt Pulse Period (See Figure 3-4)	t_{ILIL}	*	—	t_{cyc}
OSC1 Pulse Width	t_{OH}, t_{OL}	45	—	ns

* The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

** Since a 2-bit prescaler in the timer must count four internal cycles (t_{cyc}), this is the limiting minimum factor in determining the timer resolution.

*** The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{cyc}.

MC68HC05C4AD/D
Rev. 4.3

Home Page:
www.freescale.com
email:
support@freescale.com
USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130
support@freescale.com
Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com
Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
support.japan@freescale.com
Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com
For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
(800) 441-2447
303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

RoHS-compliant and/or Pb- free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb- free counterparts. For further information, see http://www.freescale.com or contact your Freescale sales representative.

For information on Freescale.s Environmental Products program, go to http://www.freescale.com/epp.

freescale™
semiconductor