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MC68HC05F12/D

HC05

MC68HC05F12

TECHNICAL
DATA

MC68HC05F12

High-density complementary metal oxide semiconductor (HCMOS) microcontroller unit

Conventions

Where abbreviations are used in the text, an explanation can be found in the glossary, at the back of this manual. Register and bit mnemonics are defined in the paragraphs describing them.

An overbar is used to designate an active-low signal, eg: $\overline{\text{RESET}}$.

Unless otherwise stated, shaded cells in a register diagram indicate that the bit is either unused or reserved; ‘u’ is used to indicate an undefined state (on reset).

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SECTION 4 PARALLEL INPUT/OUTPUT PORTS	❑	❑	❑	❑	❑
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SECTION 7 DTMF/MELODY GENERATOR	❑	❑	❑	❑	❑
SECTION 8 LIQUID CRYSTAL DISPLAY DRIVER MODULE	❑	❑	❑	❑	❑
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SECTION 12 MECHANICAL DATA	❑	❑	❑	❑	❑
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1
INTRODUCTION

The MC68HC05F12 is a member of the M68HC05 family of HCMOS microcomputers. Its memory configuration comprises 12K bytes of ROM, 384 bytes of RAM and 256 bytes of EEPROM. The on-board features of this device make it particularly suitable for use in highly integrated telephone handsets; the timer and DTMF generator allow for both pulse and tone dialling and, in addition to telephone set-up parameters and features such as last number redial, the EEPROM can typically store up to 12 telephone numbers of 20 digits, even after power has been removed from the circuit. Other features of the MC68HC05F12 include the LCD circuit which can drive up to 128 segments of an LCD display. A high level of integration has been achieved on the MC68HC05F12, and careful attention has been paid to its low-power and low-voltage performance, a major consideration in many telecommunications applications.

Features

- Fully static design featuring the industry-standard M68HC05 CPU core
- 12144 bytes of user ROM, plus 16 bytes for vectors
- 128 bytes of bootloader ROM
- 384 bytes of RAM plus 16 bytes of LCD RAM
- 256 bytes of user EEPROM
- DTMF/Melody generator
- 16-bit programmable timer with three input captures and three output compares (the output of one of the output compares is used internally and does not have an external connection)
- 15 stage multipurpose core timer with timer overflow, real time interrupt and COP watchdog
- LCD driver with 4 backplanes and 32 frontplanes
- Power saving STOP and WAIT modes
- I/O lines
  - 100 QFP configuration – total of 50 I/O pins configured as:
    37 dedicated bidirectional I/O
    13 shared with peripherals

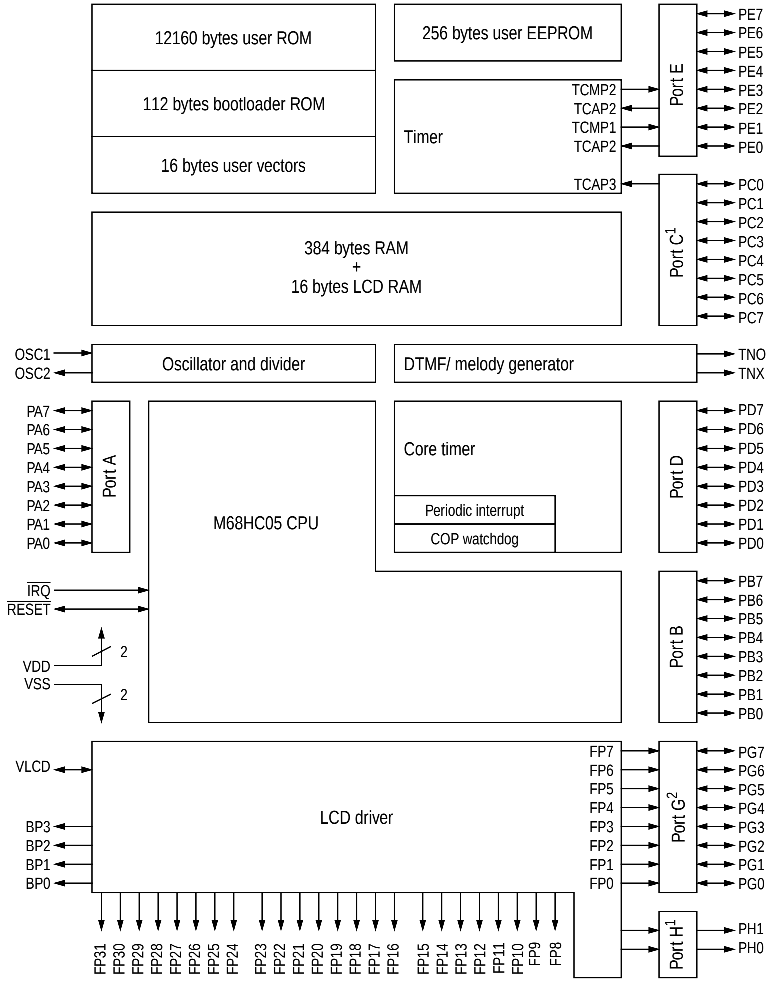
- – 80 QFP configuration – total of 43 I/O pins configured as:
  30 dedicated bidirectional I/O
  13 shared with peripherals

- Hardware interrupt with edge or edge-and-level sensitive interrupt trigger
- On-chip oscillator
- Power-on and power-off resets; low voltage detection circuitry (EEPROM)
- Available in 100-pin QFP and a reduced I/O 80-pin QFP

Note: In the 80-pin package, there is no port H, and in port C, only pins PC0, PC4 and PC5 are available.

1.1 Mask options for the MC68HC05F12

There are three mask options available on the MC68HC05F12: STOP instruction (enable/disable), COP watchdog timer (enable/disable) and low voltage reset (LVR – enable/disable). These options are programmed during fabrication and must be specified by the customer at the time of ordering.



1. In the 80-pin package, there is no port H, and in port C only pins PC0, PC4 and PC5 are available.
2. When not being used to output eight LCD frontplanes, port G pins are input only

Figure 1-1 MC68HC05F12 block diagram

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2
MODES OF OPERATION AND PIN DESCRIPTIONS

The normal operating mode of the MC68HC05F12 is single chip mode. There is also a bootloader mode, primarily for factory test purposes. In addition to these modes, there are three low power modes which may be entered and exited at will from user mode: STOP, WAIT and data retention.

2.1 Single-chip mode

This is the normal user operating mode, in which the device functions as a self-contained microcomputer unit, with all on-board peripherals and I/O ports available to the user. All address and data activity occurs within the MCU.

2.2 Low power modes

2.2.1 STOP mode

The STOP instruction places the MCU in its lowest power consumption mode. In STOP mode, the internal oscillator is turned off, halting all internal processing, including timer (and COP watchdog timer) operation.

During STOP mode, the core timer interrupt flags (CTOF and RTIF) and interrupt enable bits (TOFE and RTIE) in the CTCSR as well as the 16-bit timer flags in register TSR and interrupt enable bits in register TCR are cleared by internal hardware. The I-bit in the CCR is cleared to enable external interrupts. All other registers, the remaining bits in the CTCSR, and memory contents remain unaltered. All input/output lines remain unchanged. The processor can be brought out of STOP mode only by an interrupt ($\overline{\text{IRQ}}$, keyboard, LVI), if enabled or $\overline{\text{RESET}}$ (external reset or low voltage reset – LVR). See Figure 2-1.

The STOP instruction can be disables by a mask option. When disabled, the STOP instruction is executed as a NOP.

2.2.2 WAIT mode

The WAIT instruction places the MCU in a low power consumption mode, though it consumes more power than in STOP mode. All CPU action is suspended, but the Core timer and the 16-bit timer remain active. An interrupt from the core timer, 16-bit timer, $\overline{\text{IRQ}}$, keyboard, or LVI, if enabled, will cause the MCU to exit the WAIT mode. An external reset, or LVR, causes the MCU to exit the wait mode.

During WAIT mode, the I-bit in CCR is cleared to enable interrupts. All other registers, memory and input/output lines remain in their previous state. The DMG is still active during WAIT mode.

2.2.3 Data retention mode

The contents of the RAM and CPU registers are retained at supply voltages as low as 2.0Vdc. This is called the data retention mode, in which data is maintained but the device is not guaranteed to operate. If the voltage drops below V_{ROFF} the low voltage reset circuit generates a reset.

For lowest power consumption in data retention mode the device should be put into STOP mode before reducing the supply voltage, to ensure that all the clocks are stopped. If the device is not in STOP mode then it is recommended that $\overline{\text{RESET}}$ be held low whilst the power supply is outwith the normal operating range, to ensure that processing is suspended in an orderly manner.

Recovery from data retention mode, after the power supply has been restored, is by an external interrupt, or by pulling the $\overline{\text{RESET}}$ line high.

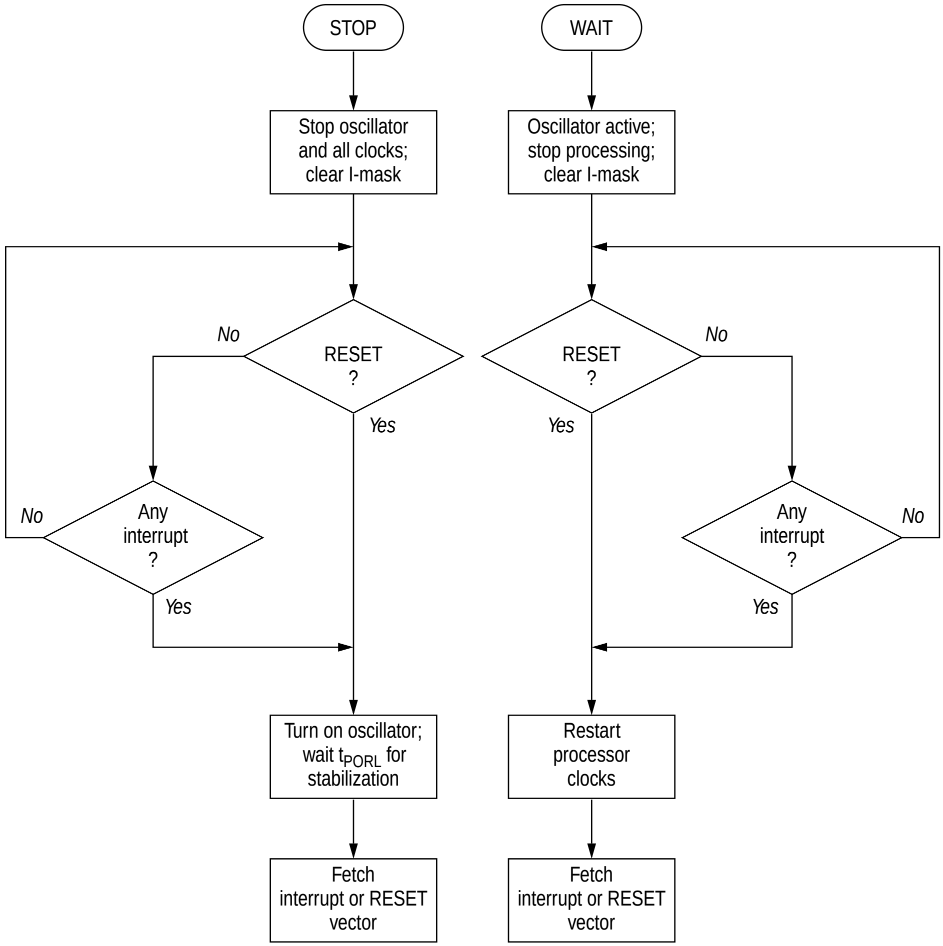


Figure 2-1 STOP and WAIT flowcharts

2.3 System options register (SOR)

The MC68HC05F12 MCU contains a system option register which is located at address $4D. This register is used to control the LVI and the clock system.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
System options register	$003D	LVIF	LVIE	LVION	SC	IRQ	0	KEYCLR	PUEN	0000 0000

LVIF, LVIE, LVION — Low voltage interrupt bits

The LVIF flag is set by the low voltage detection circuit, if the LVI is enabled and power supply VDD falls below V_{lvi}.

The low voltage interrupt must be enabled by first setting bit LVION Low Voltage Interrupt On and after that setting bit LVIE Low Voltage Interrupt Enable. After power on reset the LVI circuit is disabled.

SC — System clock option

After power on reset the internal bus frequency is f=3.58Mhz/2. If the bit SC System Clock is set the system speed is reduced to f=3.58Mhz/4, with the exception of the DTMF generator (Oscillator Frequency 3.58Mhz).

IRQ — Interrupt sensitivity

IRQ edge or level sensitivity

1 (set) – IRQ input edge and level sensitive

0 (clear) – IRQ input edge sensitive

KEYCLR — Keyboard interrupt clear

The keyboard wake-up interrupt status flag (Bit 7, $1B) is cleared by writing a ‘1’ to bit KEYCLR. A read access to this bit always returns ‘0’.

PUEN — PORTC pull-up enable

After power on reset the pull-up resistors in port C are disabled. If bit PUEN is set, the pull-up resistors in port C are enabled. Writing a ‘0’ to PUEN disables the pull-up function.

2

2.4 Pin descriptions

2.4.1 VDD and VSS

Power is supplied to the microcomputer via these two pins. VDD is the positive supply pin and VSS is the ground pin.

It is in the nature of CMOS designs that very fast signal transitions occur on the MCU pins. These short rise and fall times place very high short-duration current demands on the power supply. To prevent noise problems, special care must be taken to provide good power supply bypassing at the MCU. Bypass capacitors should have good high-frequency characteristics and be as close to the MCU as possible. Bypassing requirements vary, depending on how heavily the MCU pins are loaded.

2.4.2 $\overline{\text{IRQ}}$

This is an input-only pin for external interrupt sources. Interrupt triggering is selected using the IRQ bit in the SOR register, to be one of two options: either edge and level sensitive or edge sensitive only.

The $\overline{\text{IRQ}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity.

2.4.3 $\overline{\text{RESET}}$

This active low I/O pin is used to reset the MCU. Applying a logic zero to this pin forces the device to a known start-up state. An external RC-circuit can be connected to this pin to generate a power-on reset (POR) if required. In this case, the time constant must be great enough (at least 100ms) to allow the oscillator circuit to stabilise. This input has an internal Schmitt trigger to improve noise immunity. When a low voltage reset condition occurs internally, the $\overline{\text{RESET}}$ pin provides an active-low open drain output signal that may be used to reset external hardware. Other internal reset conditions are not visible at the $\overline{\text{RESET}}$ pin.

2.4.4 PA7–PA0/keyboard interrupt, PB7–PB0

These 16 I/O lines comprise the two 8-bit ports A and B. The state of any pin is software programmable, and on reset, the port pins are configured as inputs, with internal pull-up resistors. The eight I/O lines of port A are shared with the keyboard interrupt function.

2.4.5 PC7–PC1, PC0/TCAP3

During reset, these eight lines of port C are configured as inputs and each has an internal pull-up resistor. Port pin PC0 is shared with the timer input capture TCAP3.

2.4.6 PD7–PD0

During reset, the eight lines of port D are configured as inputs. As all port D pins are open drain outputs, an external pull-up resistor is needed when a pin is used as an output.

2.4.7 PE7–PE4, PE3/TCMP2, PE2/TCMP1, PE1/TCAP2, PE0/TCAP1

The eight pins of port E are general purpose I/O lines. These pins are all open drain, therefore an external pull-up resistor is needed when a pin is used as an output. Four of the pins, PE3–PE0, are shared with the timer system when the corresponding port E control register bits are set. PE0 and PE1 are shared with TCAP1 and TCAP2, PE2 and PE3 are shared with TCMP1 and TCMP2.

2.4.8 BP3–BP0, PF23–FP0

The LCD driver subsystem has a maximum of four frontplanes and 32 backplanes configured under software control. The four lines BP3–BP0 provide the backplane drive signals and the output lines FP23–FP0 provide the frontplane drive signals to the LCD unit. The remaining eight frontplanes are shared with port G.

2.4.9 PH1–PH0

Port H is a 2-bit output only port.

2.4.10 PG7–PG0/FP31–FP24

The eight pins of port G are shared with the frontplanes FP31–FP24. These lines are configured by default as input only, however when the corresponding bits are set in the port G control register, the lines are then connected to the LCD frontplane driver.

2.4.11 VLCD

The analogue part of the LCD controller can be supplied with an external voltage, V_{LCD}, using the VLCD pin. The value of V_{LCD} may not exceed the positive power supply voltage V_{DD}. When the INTVLCD bit in the LCD control register is set to 1, an internal voltage generator (approx. 3V, if V_{DD}>3V) is activated as the source of the analogue LCD supply voltage.

2.4.12 TNO and TNX

The TNO output provides dual tone DTMF or melody under program control. TNO is an open-drain output, and therefore requires an external pull-up resistor. The TNX output provides pacifier tones under program control.

2.4.13 OSC1 and OSC2

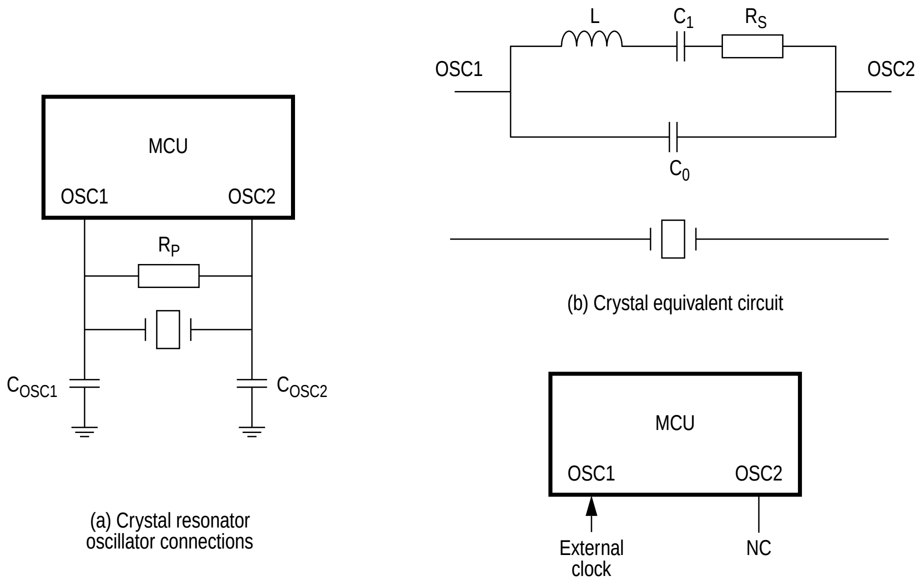
These pins provide control input for an on-chip oscillator circuit. A crystal or external clock signal connected to these pins supplies the oscillator clock. The oscillator frequency of 3.579 MHz provides the time base for the real-time clock and the DTMF/melody generator.

2.4.13.1 Crystal

The circuit shown in Figure 2-2(a) is recommended when using either a crystal or a ceramic resonator. Figure 2-2(d) provides the recommended capacitance and feedback resistance values. The internal oscillator is designed to interface with an AT-cut parallel-resonant quartz crystal resonator in the frequency range specified for f_{OSC} (see Section 11.4). Use of an external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and associated components should be mounted as close as possible to the input pins to minimize output distortion and start-up stabilization time. The manufacturer of the particular crystal being considered should be consulted for specific information.

2.4.13.2 External clock

An external clock should be applied to the OSC1 input, with the OSC2 pin left unconnected, as shown in Figure 2-2(c). The t_{OXOV} specification (see Section 11.4) does not apply when using an external clock input. The equivalent specification of the external clock source should be used in lieu of t_{OXOV}.



(a) Crystal resonator oscillator connections

(b) Crystal equivalent circuit

(c) External clock source connections

Crystal

	2MHz	4MHz	Unit
R_S(max)	400	75	Ω
C_0	5	7	pF
C_1	8	12	*f*F
C_{OSC1}	15 – 40	15 – 30	pF
C_{OSC2}	15 – 30	15 – 25	pF
R_P	10	10	MΩ
Q	30 000	40 000	—

(d) Crystal resonator parameters

Figure 2-2 Oscillator connections

3
MEMORY AND REGISTERS

The MC68HC05F12 has a 64K byte memory map consisting of registers (for I/O, control and status), user RAM, user ROM, EEPROM, bootloader ROM and reset and interrupt vectors as shown in Figure 3-1.

3.1 Registers

All the I/O, control and status registers of the MC68HC05F12 are contained within the first 64 byte block of the memory map, as detailed in Table 3-1.

3.2 RAM

The user RAM consists of 384 bytes of memory, from $0050 to $01CF. This is shared with a 64 byte stack area. The stack begins at $00FF, and may extend down to $00C0.

Note: Using the stack area for data storage or temporary work locations requires care to prevent the data from being overwritten due to stacking from an interrupt or subroutine call.

3.3 ROM

The user ROM occupies 12160 bytes of memory, from $5000 to $7F7F. In addition, there are 16 bytes of user vectors, from $7FF0 to $7FFF.

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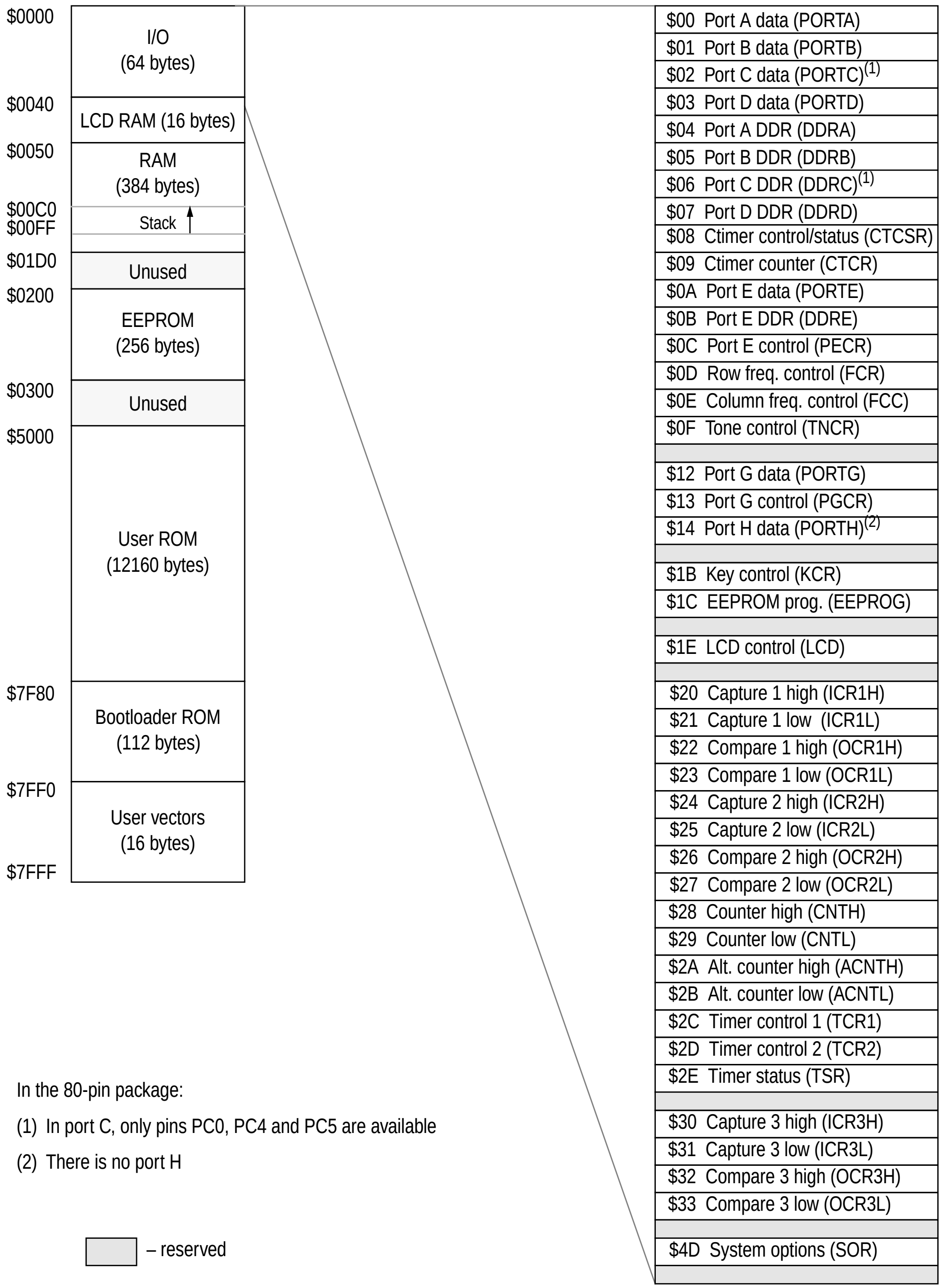


Figure 3-1 MC68HC05F12 memory map

Table 3-1 Register outline

Register Name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	undefined
Key interrupt status (KISR)	$0000									0000 0000
Port B data (PORTB)	$0001	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	undefined
Port C data (PORTC)	$0002	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	undefined
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
Port D data direction ((DDRD)	$0007									0000 0000
Core timer control/status (CTCSR)	$0008	TOF	RTIF	TOFE	RTIE	RTOF	RRTIF	RT1	RT0	0000 0011
Core timer counter (CTCR)	$0009									0000 0000
Port E data (PORTE)	$000A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	undefined
Port E data direction (DDRE)	$000B									0000 0000
Port E control (PECR)	$000C						0		0	0000 0000
DTMF row freq. control (FCR)	$000D	0	0	0	FCR4	FCR3	FCR2	FCR1	FCR0	undefined
DTMF column freq. control (FCC)	$000E	0	0	0	FCC4	FCC3	FCC2	FCC1	FCC0	undefined
DTMF tone control (TNCR)	$000F	MS1	MS0	TGER	TGEC	TNOE	0	0	0	0000 0000
Port G data (PORTG)	$0012	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	undefined
Port G control (PGCR)	$0013									0000 0000
Port H data (PORTH)	$0014	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	0000 0000
Key control (KCR)	$001B	KF	KIE	EDG5	EDG4	EDG3	EDG2	EDG1	EDG0	0000 0000
EEPROM prog. (EEPROG)	$001C	0	CPEN	0	ER1	ER0	LATCH	EERC	EEPGM	0000 0000
LCD control (LCD)	$001E	WTLCDO	FSEL1	FSEL0	INTVLCD	FDISP	MUX4	MUX3	EXTVON	0000 0000
Capture 1 high (ICR1H)	$0020	(bit 15)							(bit 8)	undefined
Capture 1 low (ICR1L)	$0021									undefined
Compare 1 high (OCR1H)	$0022	(bit 15)							(bit 8)	undefined
Compare 1 low (OCR1L)	$0023									undefined
Capture 2 high (ICR2H)	$0024	(bit 15)							(bit 8)	undefined
Capture 2 low (ICR2L)	$0025									undefined

Table 3-1 Register outline

Register Name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Compare 2 high (OCR2H)	$0026	(bit 15)							(bit 8)	undefind
Compare 2 low (OCR2L)	$0027									undefined
Counter high (CNTH)	$0028	(bit 15)							(bit 8)	1111 1111
Counter low (CNTL)	$0029									1111 1100
Alternate counter high (ACNTH)	$002A	(bit 15)							(bit 8)	1111 1111
Alternate counter low (ACNT)	$002B									1111 1100
Timer control 1 (TCR1)	$002C	ICI1E	ICI2E	OCI1E	TOIE	CO1E	IEDG1	IEDG2	OLVL1	0000 0uu0
Timer control 2 (TCR2)	$002D	0	0	OCI2E	0	CO2E	0	0	OLVL2	0000 0000
Timer status (TSR)	$002E	IC1F	IC2F	OC1F	TOF	TCAP1	TCAP2	OC2F	0	uuuu uuu0
Capture 3 high (ICR3H)	$0030	(bit 15)							(bit 8)	undefined
Capture 3 low (ICR3L)	$0031									undefined
Compare 3 high (OCR3H)	$0032	(bit 15)							(bit 8)	undefined
Compare 3 low (OCR3L)	$0033									undefined
System options (SOR)	$003D	LVIF	LVIE	LVION	SC	IRQ	KEYMUX	KEYCLR	PUEN	0000 0000

u = undefined

Note: For compatibility, unused and reserved bits (shaded) should always be cleared, when writing to them

3

3.4 Bootloader ROM

The MC68HC05F12 has 112 bytes of bootloader ROM, from $7F80 to $7FEF. These are included primarily for factory test purposes.

3.5 EEPROM

256 bytes of user EEPROM reside at addresses $0400 to $04FF.

Programming or erasing the EEPROM can be done by the user on a single byte basis; erasing may also be performed on a block or bulk basis. All programming or erasing is accomplished by manipulating the programming register (EEPROG), located at address $001C.

Note: The erased state of an EEPROM byte is '$FF'. This means that a write forces zeros to the bits specified, whilst bits defined as ones are unchanged by a write operation.

3.5.1 EEPROM programming register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
EEPROM programming (EEPROG)	$001C	0	CPEN	0	ER1	ER0	LATCH	EERC	EEPGM	0000 0000

CPEN — Charge pump enable

1 (set) – Charge pump enabled.

0 (clear) – Charge pump disabled.

When set, CPEN enables the charge pump which produces the internal programming voltage. This bit should be set at the same time as the LATCH bit. The programming voltage will not be available until EEPGM is set. The charge pump should be disabled when not in use. CPEN is readable and writable and is cleared by reset.

ER1, ER0 — Erase select bits

ER1 and ER0 are used to select either single byte programming or one of three erase modes: byte, block, or bulk. Table 3-2 shows the mode selected for each bit configuration. These bits are readable and writable and are cleared by reset.

– In byte erase mode, only the selected byte is erased.

– In block erase mode, a 32-byte block of EEPROM is erased. The EEPROM memory space is divided into four 64-byte blocks ($0400 – $043F, $0440 –

Table 3-2 Erase modes

ER1	ER0	Mode
0	0	Program
0	1	Byte erase
1	0	Block erase
1	1	Bulk erase

$047F, $0480 – $04BF and $04C0 – $04FF) and performing a block erase on any address within a block will erase the entire block.

– In bulk erase mode, the entire 256 bytes of EEPROM are erased.

LATCH — EEPROM latch bit

1 (set) – EEPROM address and data buses are configured for programming.

0 (clear) – EEPROM address and data buses are configured for normal operation.

When set, the LATCH bit configures the EEPROM address and data buses for programming. In addition, writes to the EEPROM array cause the address and data buses to be latched. This bit is readable and writable, but reads from the EEPROM array are inhibited if the LATCH bit is set and a write to the EEPROM space has taken place. When this bit is clear, address and data buses are configured for normal operation. Reset clears this bit.

EERC — EEPROM RC oscillator control

1 (set) – Use internal RC oscillator for EEPROM.

0 (clear) – Use CPU clock for EEPROM.

When this bit is set, the EEPROM memory array uses the internal RC oscillator instead of the CPU clock. After setting the EERC bit, the user should wait a time t_{RCON} to allow the RC oscillator to stabilize. This bit is readable and writable and should be set by the user when the internal bus frequency falls below 1.5MHz. Reset clears this bit.

EEPGM — EEPROM programming power enable

1 (set) – Programming power connected to the EEPROM array.

0 (clear) – Programming power switched off.

EEPGM must be set to enable the EEPGM function. When set, EEPGM turns on the charge pump and enables the programming (or erasing) power to the EEPROM array. When clear, this power is switched off. This will enable pulsing of the programming voltage to be controlled internally. This bit can be read at any time, but can only be written to if LATCH = 1, i.e. if LATCH is not set, then EEPGM cannot be set. Reset clears this bit.

3.5.2 Programming and erasing procedures

To program a byte of EEPROM, set LATCH = CPEN = 1, set ER1 = ER0 = 0, write data to the desired address and then set EEPGM for a time t_{EPGM}.

There are three possibilities for erasing data from the EEPROM array, depending on how much data is affected.

- To erase a byte of EEPROM, set LATCH = CPEN = 1, set ER1 = 0 and ER0 = 1, write data to the desired address and then set EEPGM for a time t_{EBYTE}.
- To erase a block of EEPROM, set LATCH = CPEN = 1, set ER1 = 1 and ER0 = 0, write data to any address in the block and then set EEPGM for a time t_{EBLOCK}.
- To bulk erase the EEPROM, set LATCH = CPEN = 1, set ER1 = ER0 = 1, write data to any address in the array and then set EEPGM for a time t_{EBULK}.

To terminate the programming or erase sequence, clear EEPGM, wait for a time t_{FPV} to allow the programming voltage to fall, and then clear LATCH and CPEN to release the buses. Following each erase or programming sequence, clear all programming control bits.

3.5.3 Sample EEPROM programming sequence

The following program is an example of the EEPROM programming sequence, using the timer to implement the required delay and assuming a 1 MHz bus frequency.

```
TCSR   EQU   $0008        TIMER CONTROL AND STATUS REGISTER
TCNT   EQU   $0009        TIMER COUNTER REGISTER
TOF    EQU   7            TOF BIT OF TCSR
PROG   EQU   $001C        EEPROM PROGRAM REGISTER
CPEN   EQU   6            CHARGE PUMP ENABLE BIT
ER1    EQU   4            ERASE SELECT BIT 1
ER0    EQU   3            ERASE SELECT BIT 0
LATCH  EQU   2            LATCH BIT
EERC   EQU   1            RC/OSC SELECTOR BIT
EEPGM  EQU   0            EEPROM PROGRAM BIT
EESTARTEQU   $0400        START ADDRESS OF EEPROM
SUMPIN EQU   $FF          DUMMY DATA

ORG          $0680
START  EQU   *
       BSET  EERC, PROG   SELECT RC OSCILLATOR
       BSR   DELAY        RC OSCILLATOR STABILIZATION
       BSET  CPEN, PROG   TURN ON CHARGE PUMP
       BSET  LATCH, PROG  ENABLE LATCH BIT
       BCLR  ER1, PROG    SELECT PROGRAM (NOT ERASE)
       BCLR  ER0, PROG    SELECT PROGRAM (NOT ERASE)

       LDA   #SUMPIN      GET DATA
       STA   EESTART
       BSET  EEPGM, PROG  ENABLE PROGRAMMING POWER
       JSR   DELAY        WAIT FOR PROGRAMMING TIME
       BCLR  EEPGM, PROG  CLEAR EEPGM

       JSR   DELAY        WAIT FOR PROG VOLTAGE TO FALL
       BCLR  LATCH, PROG  CLEAR LATCH
       BCLR  CPEN, PROG   DISABLE CHARGE PUMP
       CMP   EESTART      VERIFY
       BNE   OUT1
       CLC                CLEAR CARRY BIT IF NO ERROR

OUT    RTS

OUT1   SEC                FLAG AN ERROR
       RTS

*THIS ROUTINE GIVES A 15MS (+/-1MS) DELAY AT 1 MHZ BUS. THE SAME DELAY
* ROUTINE IS USED IN THIS EXAMPLE FOR SIMPLICITY, USING THE LONGEST DELAY
* TIME. USERS WILL WANT TO WRITE SHORTER DELAY ROUTINES FOR APPLICATIONS
*IN WHICH SPEED IS IMPORTANT.

DELAY  EQU   *
       LDX   #15          COUNT OF 15
TIMLP  BCLR  TOF, TCSR    CLEAR TOF
       BRCLR TOF, TCSR    WAIT FOR TOF FLAG
       DECX
       BNE   TIMLP        COUNT DOWN TO 0
       RTS
```

4
PARALLEL INPUT/OUTPUT PORTS

4

The MC68HC05F12 has a total of 50 I/O lines, arranged as six 8-bit ports and one 2-bit port. The I/O lines are individually programmable as either input or output, under the software control of the data direction registers. Port A can also be configured to respond to keyboard interrupts.

To avoid glitches on the output pins, data should be written to the I/O port data register before writing ones to the corresponding data direction register bits to set the pins in output mode.

4.1 Input/output programming

The bidirectional port lines may be programmed as inputs or outputs under software control. The direction of each pin is determined by the state of the corresponding bit in the port data direction register (DDR). Each I/O port has an associated DDR. Any I/O port pin is configured as an output if its corresponding DDR bit is set to a logic one. A pin is configured as an input if its corresponding DDR bit is cleared.

At power-on or reset, all DDRs are cleared, thus configuring all port pins as inputs. The data direction registers can be written to or read by the MCU. During the programmed output state, a read of the data register actually reads the value of the output data latch and not the I/O pin. The operation of the standard port hardware is shown schematically in Figure 4-2.

This is further summarized in Table 4-1, which shows the effect of reading from, or writing to an I/O pin in various circumstances. Note that the read/write signal shown is internal and not available to the user.

4

4.2 Port A

Port A is an 8-bit bidirectional port which is equipped with a keyboard interrupt. All eight lines have internal pull-up resistors, which are required when the port is in input mode. On reset, this port is configured as a standard I/O port comprising a data register and a data direction register.

Reset does not affect the state of the data register, but clears the data direction register, thereby returning all ports pins to input mode. Writing a 1 to any DDR bit sets the corresponding port pin to output mode. As every pin configured as an input contributes to the keyboard interrupt, it is possible to disable a single pin by configuring it as an output.

4.2.1 Keyboard interrupt

Provided that the interrupt mask bit of the condition code register is cleared, the keyboard interrupt facility is enabled by setting the keyboard interrupt bit (KIE) in the Key Control register.

On detection of a high-to-low transition, the interrupt inputs PA6 and PA7 are triggered. The trigger edges of the interrupt lines, PA0–PA5, can be programmed using the EDG0–EDG5 bits in the Key Control register. If one of these bits is cleared, after reset the corresponding interrupt is falling-edge sensitive. If, however, one of them is set, after reset the corresponding interrupt is rising-edge sensitive. The internal pull-up resistors of input lines, PA7–PA0, are disabled, if rising-edge sensitivity is selected.

When a correct transition is detected, on any of this port’s pins, a keyboard interrupt request is generated, and the corresponding interrupt status flag of the interrupt status register, IRSTATE, is set. The interrupt status register is an 8-bit register which has the same address as PORTA, $0000. This register can be read if the KEYMUX bit in the system option register is set. If KIE is set, a keyboard interrupt is generated and the keyboard status flag, KF, is set by generating the logical OR of the eight interrupt state register outputs.

The 8 interrupt state register flags can be reset in three ways:

1) Completely, if the chip is reset.
2) Completely, if a 1 is written to KEYCLR, in the system option register.
3) Individually, if a 1 is written to the corresponding bit position of the interrupt state register ($00 with KEYMUX = 1, in the system option register).

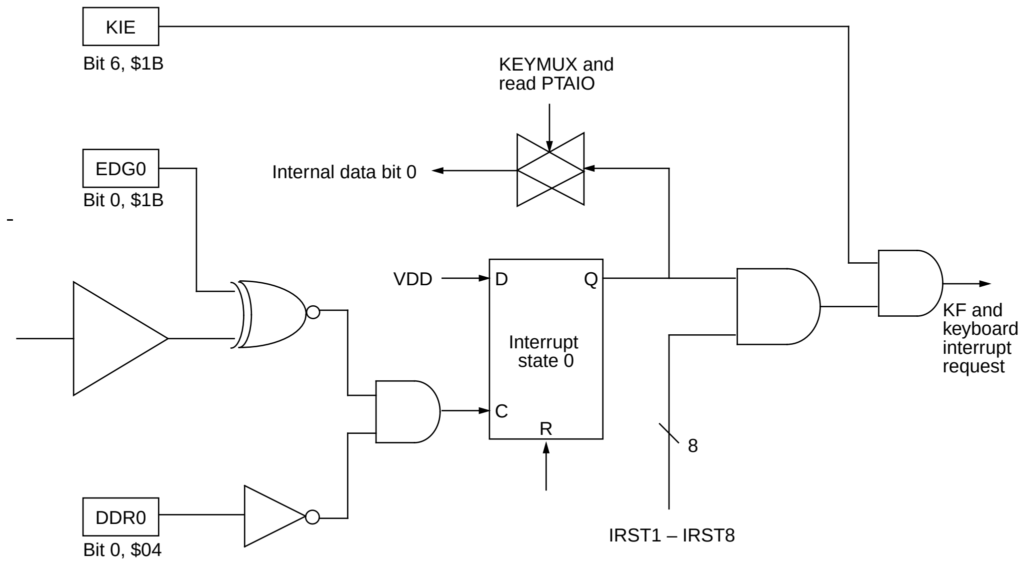


Figure 4-1 Structure of port with keyboard interrupt

4.2.1.1 Key control register (KCR)

This register contains eight bits, two of which are used to control the keyboard interrupt facility, the others determine the keyboard interrupt edges.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Key control register (KCR)	$001B	KF	KIE	0	0	0	0	0	0	0000 0000

KF — Keyboard interrupt status flag

1 (set) – A valid transition has occurred on one of the port pins.

0 (clear) – No valid transition has occurred on any of the port pins.

This bit is set when a valid transition is detected on any of the port A pins; a keyboard interrupt request will be generated, if keyboard interrupts are enabled (only if KIE is set). The KF flag is cleared by resetting the IRSTATE register, or by setting KEYCLR = 1 in the system option register.

KIE — keyboard interrupt enable

1 (set) – Keyboard interrupt enabled.

0 (clear) – Keyboard interrupt disabled.

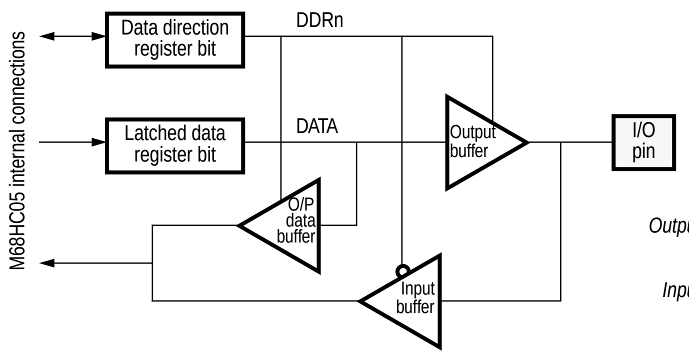
An interrupt can only be generated if KIE and KF are both set and the I-bit in the CCR is clear.

Note: Bits 0–5 are reserved for future use and should be cleared when writing to this register.

4.3 Port B

This port is a standard M68HC05 bidirectional I/O port, comprising a data register and a data direction register.

Reset does not affect the state of the data register, but clears the data direction register, thereby returning all port pins to input mode. Writing a ‘1’ to any DDR bit sets the corresponding port pin to output mode. The port B lines have internal pull-up resistors.



	DDRn	DATA	I/O
Output	1	0	0
	1	1	1
Input	0	0	tristate
	0	1	tristate

Figure 4-2 Standard I/O port structure

Table 4-1 I/O pin states

R/W	DDRn	Action of MCU write to/read of data bit
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch, and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in output mode. The output data latch is read.

4.4 Port C

Port C is an 8-bit bidirectional port. Port pin 0 is shared with TCAP3. This line must be configured as an input by resetting the DDR, thus enabling the TCAP function. All eight lines have internal, programmable pull-up resistors. If the PUEN bit in the system options register is cleared, the pull-ups are disabled after reset. However, setting the PUEN bit enables all the pull-up resistors.

4.5 Port D

Port D is an 8-bit bidirectional port which does not share any of its pins with other subsystems. Port D has open drain outputs which means when a pin is being used an output, an external pull-up resistor is required.

Reset does not affect the data register, but it clears the data direction register and the control register. The default setting of the register control bits is 0, making the pins general purpose I/O lines. The direction of the pins is then determined by their corresponding bits in DDR (0 - input, 1 - output). Write access to DDR or the I/O register is blocked to reduce digital noise. Read access to DDR or the I/O register returns 0. Port D has open-drain outputs, it therefore requires external pull-up resistors for each pin when they are used as outputs.

4.6 Port E

Port E is an 8-bit bidirectional port which shares four of its pins with the timer system. The default state of the port E control bits is logic zero, the ports are then general I/O ports. The direction of the pins is determined by their corresponding bits in the data direction register. Setting a bit in this register makes the port pin an output, clearing a bit makes the corresponding port pin an input. When bit 1 or bit 3 in the port E control register is set, the pin is connected to the timer system (TCMP1, 2). In this case the bit in DDR has no meaning. Pins E0 and E1 are always connected to the timer system (TCAP1, 2). These two lines must be inputs, by resetting the DDR, to enable correct TCAP function.

Note: As the voltage at port D or port E is driven above V_{DD}, the protection device will begin to conduct and tend to clamp the input voltage to protect the input buffer. The voltage at which this occurs varies significantly from lot to lot and over the operating temperature range. At room temperature, the pin typically does not draw any current until approximately 18V.

4.7 Port H

Port H is a 2-bit output only port.

4.8 Port G

The eight port lines of port G are shared with the frontplanes FP31–FP24. The default setting of the port G control bits is zero, making all the pins input only. When the corresponding control bit is set, the pin is connected to the LCD frontplane driver.

4.9 Port registers

The following sections explain in detail the individual bits in the data and control registers associated with the ports.

4.9.1 Port data registers (Ports A, B, C, D, E, G and H)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data (PORTA)	$0000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	undefined
Port B data (PORTB)	$0001	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	undefined
Port C data (PORTC)	$0002	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	undefined
Port D data (PORTD)	$0003	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	undefined
Port E data (PORTE)	$000A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	undefined
Port G data (PORTG)	$0012	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	undefined
Port H data (PORTH)	$0014	0	0	0	0	0	0	PH1	PH0	0000 0000

Each bit of port A – port E can be configured as input or output via the corresponding data direction bit in the port data direction register (DDRx).

Reset does not affect the state of the port A – port G data registers. However, the port H data register is reset to 0.

4.9.2 Data direction registers (DDRA, DDRB, DDRC, DDRD and DDRE)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A data direction (DDRA)	$0004									0000 0000
Port B data direction (DDRB)	$0005									0000 0000
Port C data direction (DDRC)	$0006									0000 0000
Port D data direction (DDRD)	$0007									0000 0000
Port E data direction (DDRE)	$000B									0000 0000

Writing a ‘1’ to any bit configures the corresponding port pin as an output; conversely, writing any bit to ‘0’ configures the corresponding port pin as an input.

Reset clears these registers, thus configuring all port pins as inputs.

4.9.3 Port control registers

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset$
Port D control	$001A									0000 0000
Port E control	$000C									0000 0000
Port G control	$0013									0000 0000
Port H control	$0015									0000 0000

Writing a 1 to any bit configures the corresponding port pin as a special function port (timer, A/D, LCD, PWM, refresh clock). However, clearing any bit to 0, configures the corresponding port pin in port D and port E as general purpose I/O, port G as input, and port H as output.

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5
CORE TIMER

The MC68HC05F12 has a 15-stage ripple counter called the core timer (CTIMER). Features of this timer are: timer overflow, power-on reset (POR), real time interrupt (RTI) with four selectable interrupt rates and a computer operating properly (COP) watchdog timer.

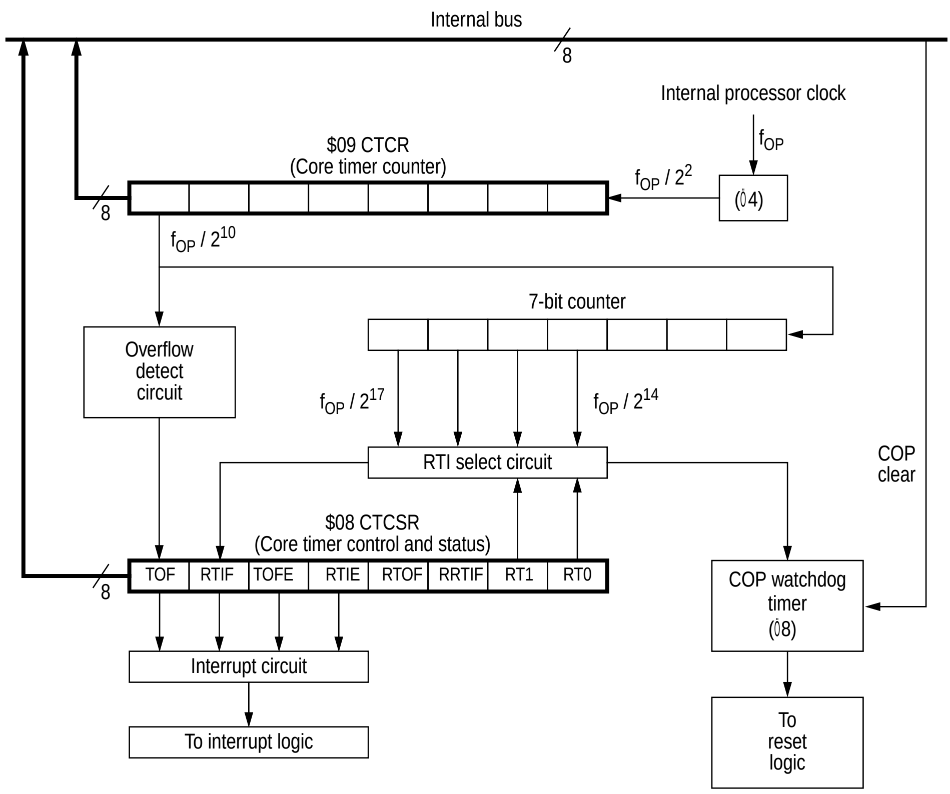

Figure 5-1 Core timer block diagram

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As shown in Figure 5-1, the timer is driven by the internal bus clock divided by four with a fixed prescaler. This signal drives an 8-bit ripple counter. The value of this 8-bit ripple counter can be read by the CPU at any time, by accessing the CTIMER counter register (CTCR) at address $09. A timer overflow function is implemented on the last stage of this counter, giving a possible interrupt at the rate of $f_{OP}/1024$. (The POR signal (t_{PORL}) is also derived from this register, at $f_{OP}/4064$.) The counter register circuit is followed by four more stages, with the resulting clock ($f_{OP}/16384$) driving the real time interrupt circuit. The RTI circuit consists of three divider stages with a 1-of-4 selector. The output of the RTI circuit is further divided by 8 to drive the COP watchdog timer circuit. The RTI rate selector bits, and the RTI and CTIMER overflow enable bits and flags, are located in the CTIMER control and status register (CTCSR) at location $08.

CTOF (core timer overflow flag) is a clearable, read-only status bit and is set when the 8-bit ripple counter rolls over from $FF to $00. A CPU interrupt request will be generated if CTOFE is set. Clearing the CTOF is done by writing a ‘0’ to it. Writing a ‘1’ to CTOF has no effect on the bit’s value. Reset clears CTOF.

When CTOFE (core timer overflow enable) is set, a CPU interrupt request is generated when the CTOF bit is set. Reset clears CTOFE.

The core timer counter register (CTCR) is a read-only register that contains the current value of the 8-bit ripple counter at the beginning of the timer chain. This counter is clocked at $f_{OP}/4$ and can be used for various functions including a software input capture. Extended time periods can be attained using the CTIMER overflow function to increment a temporary RAM storage location thereby simulating a 16-bit (or more) counter.

The power-on cycle clears the entire counter chain and begins clocking the counter. After t_{PORL} cycles, the power-on reset circuit is released, which again clears the counter chain and allows the device to come out of reset. At this point, if $\overline{\text{RESET}}$ is not asserted, the timer will start counting up from zero and normal device operation will begin. When $\overline{\text{RESET}}$ is asserted at any time during operation (other than POR), the counter chain will be cleared.

5.1 Real time interrupts (RTI)

The real time interrupt circuit consists of a three stage divider and a 1-of-4 selector. The clock frequency that drives the RTI circuit is $f_{OP}/2^{14}$ (or $f_{OP}/16384$), with three additional divider stages, giving a maximum interrupt period of 4 seconds at a bus frequency (f_{OP}) of 32kHz. Register details are given in Section 5.2.

5.2 Core timer registers

5.2.1 Core timer control and status register (CTCSR)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Core timer control/status (CTCSR)	$0008	CTOF	RTIF	CTOFE	RTIE	RTOF	RRTIF	RT1	RT0	0000 0011

5

CTOF — Core timer overflow

1 (set) – Core timer overflow has occurred.

0 (clear) – No core timer overflow interrupt has been generated.

CTOF is a read-only status bit and is set when the core timer counter register rolls over from $FF to $00; an interrupt request will be generated if CTOFE is set. When set, CTOF may be cleared by writing a ‘1’ to RTOF.

RTIF — Real time interrupt flag

1 (set) – A real time interrupt has occurred.

0 (clear) – No real time interrupt has been generated.

RTIF is a read-only status bit and is set when the output of the chosen stage becomes active; an interrupt request will be generated if RTIE is set. When set, the bit may be cleared by writing a ‘1’ to RRTIF. Reset also clears this bit.

CTOFE — Core timer overflow enable

1 (set) – Core timer overflow interrupt is enabled.

0 (clear) – Core timer overflow interrupt is disabled.

Setting this bit enables the core timer overflow Interrupt. A CPU interrupt request will then be generated whenever the CTOF bit becomes set and the I-bit in the CCR is clear. Clearing this bit disables the core timer overflow interrupt capability.

RTIE — Real time interrupt enable

1 (set) – Real time interrupt is enabled.

0 (clear) – Real time interrupt is disabled.

Setting this bit enables the real time interrupt. A CPU interrupt request will then be generated whenever the RTIF bit becomes set and the I-bit in the CCR is clear. Clearing this bit disables the real time interrupt capability.

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RT1, RT0 — Real time interrupt rate select

These two bits select one of four taps from the real time interrupt circuitry. Reset sets both RT0 and RT1 to one, selecting the lowest periodic rate and therefore the maximum time in which to alter them if necessary. The COP reset times are also determined by these two bits. Care should be taken when altering RT0 and RT1 if a timeout is imminent, or the timeout period is uncertain. If the selected tap is modified during a cycle in which the counter is switching, an RTIF could be missed or an additional one could be generated. To avoid problems, the COP should be cleared before changing the RTI taps. See Table 5-1 for some example RTI periods.

Table 5-1 Example RTI periods

			RTI Rates at f_{OP} Frequency Specified			
RT1	**RT0**	**Division ratio**	**16.384 kHz**	**447 kHz**	**895 kHz**	**1.789 MHz**
0	0	2^{14}	1 s	36.7 ms	18.35 ms	9.17 ms
0	1	2^{15}	2 s	73.4 ms	36.7 ms	18.35 ms
1	0	2^{16}	4 s	146.8 ms	73.4 ms	36.7 ms
1	1	2^{17}	8 s	293.6 ms	146.8 ms	73.4 ms

5.2.2 Core timer counter register (CTCR)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Core timer counter (CTCR)	$0009									0000 0000

The core timer counter register is a read-only register, which contains the current value of the 8-bit ripple counter at the beginning of the timer chain. Reset clears this register.

5.3 Computer operating properly (COP) watchdog timer

The COP watchdog timer function is implemented by taking the output of the RTI circuit and further dividing it by eight, as shown in Figure 5-1. Note that the minimum COP timeout period is seven times the RTI period. This is because the COP will be cleared asynchronously with respect to the value in the core timer counter register/RTI divider, hence the actual COP timeout period will vary between 7x and 8x the RTI period. The minimum COP reset rates are shown in Table 5-2.

The COP function is a mask option, enabled or disabled during device manufacture.

If the COP circuit times out, an internal reset is generated and the normal reset vector is fetched. A COP timeout is prevented by writing a '0' to bit 0 of address $0FF0. When the COP is cleared, only the final divide-by-eight stage is cleared (see Figure 5-1).

Table 5-2 Minimum COP reset times

		Minimum COP reset at f_{OP} frequency specified				
RT1	**RT0**	**16.384 kHz**	**447 kHz**	**895 kHz**	**1.789 MHz**	f_{OP}
0	0	7 s	256.9 ms	128.45 ms	64.19 ms	7 x RTI rate
0	1	14 s	513.8 ms	256.9 ms	128.45 ms	7 x RTI rate
1	0	28 s	1.03 s	513.8 s	256.9 ms	7 x RTI rate
1	1	56 s	2.06 s	1.03 s	513.8 ms	7 x RTI rate

5.4 Core timer during WAIT

The CPU clock halts during the WAIT mode, but the timer remains active. If the CTIMER interrupts are enabled, then a CTIMER interrupt will cause the processor to exit the WAIT mode.

5.5 Core timer during STOP

The timer is cleared when going into STOP mode. When STOP is exited by an external interrupt or an external reset, the internal oscillator will restart, followed by an internal processor stabilization delay (t_{PORL}). The timer is then cleared and operation resumes.

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6
16-BIT PROGRAMMABLE TIMER

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The MC68HC05F12 has a single 16-bit programmable timer consisting of a 16-bit, free running counter driven by a fixed divide-by-four prescaler.

The timer consists of a 16-bit read-only free-running counter, with a fixed divide-by-four prescaler, plus the input capture/output compare circuitry. The timer can be used for many purposes including measuring pulse length of two input signals and generating two output signals. Pulse lengths for both input and output signals can vary from several microseconds to many seconds. The timer is also capable of generating periodic interrupts or indicating passage of an arbitrary multiple of four CPU cycles. A block diagram is shown in Figure 6-1, and timing diagrams are shown in Figure 6-1, Figure 6-2, Figure 6-3 and Figure 6-4.

The timer has a 16-bit architecture, hence each specific functional segment is represented by two 8-bit registers. These registers contain the high and low byte of that functional segment. Accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

The 16-bit programmable timer is monitored and controlled by a group of fifteen registers, full details of which are contained in this section.

Note: A problem may arise if an interrupt occurs in the time between the high and low bytes being accessed. To prevent this, the I-bit in the condition code register (CCR) should be set while manipulating both the high and low byte register of a specific timer function, ensuring that an interrupt does not occur.

6.1 Counter

The key element in the programmable timer is a 16-bit, free-running counter or counter register, preceded by a prescaler that divides the internal processor clock by four. The prescaler gives the timer a resolution of 2µs if the internal bus clock is 2 MHz. The counter is incremented during the low portion of the internal bus clock. Software can read the counter at any time without affecting its value.

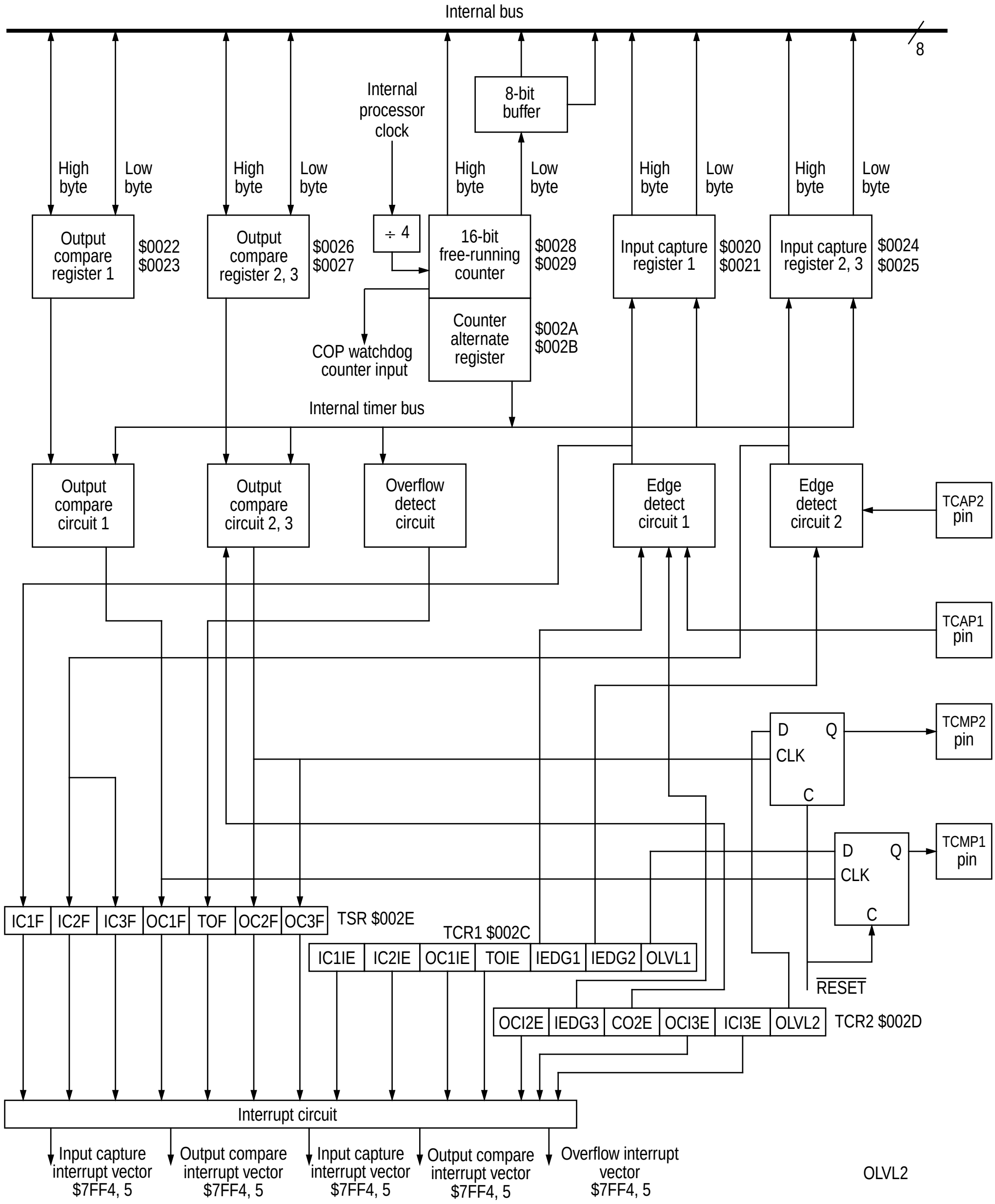

Figure 0-1 16-bit programmable timer block diagram

6.1.1 Counter register and alternate counter register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Timer counter high (CNTH)	$0028									1111 1111
Timer counter low (CNTL)	$0029									1111 1100

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Alternate counter high (ACNTH)	$002A									1111 1111
Alternate counter low (ACNTL)	$002B									1111 1100

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The double-byte, free-running counter can be read from either of two locations, $0028 – $0029 (counter register) or $002A – $002B (counter alternate register). A read from only the less significant byte (LSB) of the free-running counter ($0029 or $002B) receives the count value at the time of the read. If a read of the free-running counter or alternate counter register first addresses the more significant byte (MSB) ($0028 or $002A), the LSB is transferred to a buffer. This buffer value remains fixed after the first MSB read, even if the user reads the MSB several times. This buffer is accessed when reading the free-running counter or alternate counter register LSB and thus completes a read sequence of the total counter value. In reading either the free-running counter or alternate counter register, if the MSB is read, the LSB must also be read to complete the sequence. If the timer overflow flag (TOF) is set when the counter register LSB is read then a read of the timer status register (TSR) will clear the flag.

The counter alternate register differs from the counter register only in that a read of the LSB does not clear TOF. Therefore, where it is critical to avoid the possibility of missing timer overflow interrupts due to clearing of TOF, the alternate counter register should be used.

The free-running counter is set to $FFFC during power-on and external reset and is always a read-only register. During a power-on reset, the counter begins running after the oscillator start-up delay. Because the free-running counter is 16 bits preceded by a fixed divide-by-4 prescaler, the value in the free-running counter repeats every 262,144 internal bus clock cycles. TOF is set when the counter overflows (from $FFFF to $0000); this will cause an interrupt if TOIE is set.

The divide-by-4 prescaler is also reset and the counter resumes normal counting operation. All of the flags and enable bits remain unaltered by this operation. If access has previously been made to the high byte of the free-running counter ($0028 or $002A), then the reset counter operation terminates the access sequence.

Caution: This operation may affect the function of the watchdog system (see Section 5.3).

6.2 Timer control and status

The various functions of the timer are monitored and controlled using the timer control and status registers described below.

6.2.1 Timer control registers 1 and 2 (TCR1 and TCR2)

6

The two timer control registers TCR1 and TCR2 ($002C and $002D) are used to enable the input captures (IC1IE, IC2IE and IC3IE), output compares (OC1IE, OC2IE and OC3IE), and timer overflow (TOIE) functions as well as enabling the compare outputs (CO1E, CO2E and CO3E), selecting input edge sensitivity (IEDG1 and IEDG2) and levels of output polarity (OLVL1 and OLVL2).

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Timer control 1 (TCR1)	$002C	IC1IE	IC2IE	OC1IE	TOIE	CO1E	IEDG1	IEDG2	OLVL1	0000 0uu0

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Timer control 2 (TCR2)	$002D	CO3E	OLVL3	OC2IE	IEDG3	CO2E	OC3IE	IC3IE	OLVL2	000u 0000

IC1IE — Input capture 1 interrupt enable

If this bit is set, a timer interrupt is enabled whenever the IC1F status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

IC2IE — Input capture 2 interrupt enable

If this bit is set, a timer interrupt is enabled whenever the IC2F status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

OC1IE — Output compare 1 interrupt enable

If this bit is set, a timer interrupt is enabled whenever the OC1F status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

TOIE — Timer overflow interrupt enable

If this bit is set, a timer interrupt is enabled whenever the TOF status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

CO1E — Timer compare 1 output enable

If this bit is set, the output from timer output compare 1 is enabled.

1 (set) – Output compare 1 enabled.

0 (clear) – Output compare 1 disabled.

IEDG1 — Input edge 1

When IEDG1 is set, a positive-going edge on the TCAP1 pin will trigger a transfer of the free-running counter value to the input capture register 1. When clear, a negative-going edge triggers the transfer.

1 (set) – TCAP1 is positive-going edge sensitive.

0 (clear) – TCAP1 is negative-going edge sensitive.

6

IEDG2 — Input edge 2

When IEDG2 is set, a positive-going edge on the TCAP2 pin will trigger a transfer of the free-running counter value to the input capture register 2. When clear, a negative-going edge triggers the transfer.

1 (set) – TCAP2 is positive-going edge sensitive.

0 (clear) – TCAP2 is negative-going edge sensitive.

OLVL1 — Output level 1

When OLV1 is set a high output level will be clocked into the output level register by the next successful output compare, and will appear on the TCMP1 pin. When clear, it will be a low level which will appear on the TCMP1 pin.

1 (set) – A high output level will appear on the TCMP1 pin.

0 (clear) – A low output level will appear on the TCMP1 pin.

OC2IE — Output compare 2 interrupt enable

If this bit is set, a timer interrupt is enabled whenever the OC2F status flag (in the timer status register) is set.

1 (set) – Interrupt enabled.

0 (clear) – Interrupt disabled.

IEDG3 — Input edge 3

When IEDG3 is set, a positive-going edge on the TCAP3 pin will trigger a transfer of the free-running counter value to the input capture register 3. When clear, a negative-going edge triggers the transfer.

1 (set) – TACP3 is positive-going edge sensitive

0 (clear) – TCAP3 is negative-going edge sensitive

CO2E — Timer compare 2 output enable

If this bit is set, the output from timer output compare 2 is enabled.

1 (set) – Output compare 2 enabled.

0 (clear) – Output compare 2 disabled.

OC3IE — Output compare 3 interrupt enable

If this bit is set, a timer interrupt is enabled whenever the OC3F status flag (in the timer status register) is set.

1 (set) – interrupt enabled

0 (clear) – interrupt disabled

IC3IE — Input capture 3 interrupt enable

If this bit is set, a timer interrupt is enabled whenever the IC3F status flag (in the timer status register) is set.

1 (set) – interrupt enabled

0 (clear) – interrupt disabled

OLVL2 — Output level 2

When OLV2 is set a high output level will be clocked into the output level register by the next successful output compare, and will appear on the TCMP2 pin. When clear, it will be a low level which will appear on the TCMP2 pin.

1 (set) – A high output level will appear on the TCMP2 pin.

0 (clear) – A low output level will appear on the TCMP2 pin.

CO3E, OLVL3

These bits have no effect and should be cleared to zero when writing to TCR2.

6.2.2 Timer status register (TSR)

The timer status register ($002E) contains the status bits corresponding to the timer interrupt conditions – IC1F, IC2F, OC1F, TOF, TCAP1, TCAP2 and OC2F.

Accessing the timer status register satisfies the first condition required to clear the status bits. The remaining step is to access the register corresponding to the status bit.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Timer status (TSR)	$002E	IC1F	IC2F	OC1F	TOF	TCAP1	TCAP2	OC2F	0	Undefined

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IC1F — Input capture 1 flag

This bit is set when the selected polarity of edge is detected by the input capture edge detector 1 at TCAP1; an input capture interrupt will be generated, if IC1IE is set. IC1F is cleared by reading the TSR and then the input capture 1 low register ($0021).

1 (set) – A valid input capture has occurred.

0 (clear) – No input capture has occurred.

IC2F — Input capture 2 flag

This bit is set when the selected polarity of edge is detected by the input capture edge detector 2 at TCAP2; an input capture interrupt will be generated if IC2IE is set. IC2F is cleared by reading the TSR and then the input capture 2 low register ($0025).

1 (set) – A valid input capture has occurred.

0 (clear) – No input capture has occurred.

OC1F — Output compare 1 flag

This bit is set when the output compare register 1 contents match those of the free-running counter; an output compare interrupt will be generated if OC1IE is set. OC1F is cleared by reading the TSR and then the output compare 1 low register ($0023).

1 (set) – A valid output compare has occurred.

0 (clear) – No output compare has occurred.

TOF — Timer overflow status flag

This bit is set when the free-running counter overflows from $FFFF to $0000; a timer overflow interrupt will occur if TOIE is set. TOF is cleared by reading the TSR and the counter low register ($0029).

1 (set) – Timer overflow has occurred.

0 (clear) – No timer overflow has occurred.

When using the timer overflow function and reading the free-running counter at random times to measure an elapsed time, a problem may occur whereby the timer overflow flag is unintentionally cleared if:

1. The timer status register is read or written when TOF is set, and
2. The LSB of the free-running counter is read, but not for the purpose of servicing the flag.

Reading the alternate counter register instead of the counter register will avoid this potential problem.

IC3F — Input capture 3 flag

This bit is set when the selected polarity of edge is detected by the input capture edge detector 3 at TCAP3; an input capture interrupt will be generated if IC3IE is set. IC3F is cleared by reading the TSR and then the input capture 3 low register ($0031).

1 (set) – A valid output compare has occurred.

0 (clear) – No output compare has occurred.

OC3F — Output compare 3 flag

This bit is set when the output compare register 3 contents match those of the free-running counter; an output compare interrupt will be generated if OC3IE is set. OC3F is cleared by reading the TSR and then the output compare 3 low register ($0033).

1 (set) – A valid output compare has occurred.

0 (clear) – No output compare has occurred.

OC2F — Output compare 2 flag

This bit is set when the output compare register 2 contents match those of the free-running counter; an output compare interrupt will be generated if OC2IE is set. OC2F is cleared by reading the TSR and then the output compare 2 low register ($0027).

1 (set) – A valid output compare has occurred.

0 (clear) – No output compare has occurred.

6.3 Input capture

'Input capture' is a technique whereby an external signal is used to trigger a read of the free running counter. In this way it is possible to relate the timing of an external signal to the internal counter value, and hence to elapsed time.

There are two input capture registers: input capture register 1 (ICR1) and input capture register 2 (ICR2).

There are two input capture interrupt enable bits (IC1IE and IC2IE).

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6.3.1 Input capture register 1 (ICR1)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Input capture 1 high (ICR1H)	$0020									Undefined
Input capture 1 low (ICR1L)	$0021									Undefined

The two 8-bit registers that make up the 16-bit input capture register 1 are read-only, and are used to latch the value of the free-running counter after the input capture edge detector circuit 1 senses a valid transition at TCAP1. The level transition that triggers the counter transfer is defined by the input edge bit (IEDG1). When an input capture 1 occurs, the corresponding flag IC1F in TSR is set. An interrupt can also accompany an input capture 1 provided the IC1IE bit in TCR1 is set. The 8 most significant bits are stored in the input capture register 1 high at $0020, the 8 least significant bits in the input capture register 1 low at $0021.

The result obtained from an input capture will be one greater than the value of the free-running counter on the rising edge of the internal bus clock preceding the external transition. This delay is required for internal synchronization. Resolution is one count of the free-running counter, which is four internal bus clock cycles. The free-running counter contents are transferred to the input capture register 1 on each valid signal transition whether the input capture 1 flag (IC1F) is set or clear. The input capture register 1 always contains the free-running counter value that corresponds to the most recent input capture 1. After a read of the input capture register 1 MSB ($0020), the counter transfer is inhibited until the LSB ($0021) is also read. This characteristic causes the time used in the input capture software routine and its interaction with the main program to determine the minimum pulse period. A read of the input capture register 1 LSB ($0021) does not inhibit the free-running counter transfer since the two actions occur on opposite edges of the internal bus clock.

Reset does not affect the contents of the input capture register 1, except when exiting STOP mode (see Section 6.5).

6.3.2 Input capture register 2 (ICR2)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Input capture 2 high (ICR2H)	$0024									Undefined
Input capture 2 low (ICR2L)	$0025									Undefined

The two 8-bit registers that make up the 16-bit input capture register 2 are read-only, and are used to latch the value of the free-running counter after the input capture edge detector circuit 2 senses a valid transition at pin TCAP2. When an input capture 2 occurs, the corresponding flag IC2F in TSR is set. An interrupt can also accompany an input capture 2 provided the IC2IE bit in TCR1 is set. The 8 most significant bits are stored in the input capture 2 high register at $0024, the 8 least significant bits in the input capture 2 low register at $0025.

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The result obtained from an input capture will be one greater than the value of the free-running counter on the rising edge of the internal bus clock preceding the external transition. This delay is required for internal synchronization. Resolution is one count of the free-running counter, which is four internal bus clock cycles. The free-running counter contents are transferred to the input capture register 2 on each valid signal transition whether the input capture 2 flag (IC2F) is set or clear. The input capture register 2 always contains the free-running counter value that corresponds to the most recent input capture 2. After a read of the input capture register 2 MSB ($0024), the counter transfer is inhibited until the LSB ($0025) is also read. This characteristic causes the time used in the input capture software routine and its interaction with the main program to determine the minimum pulse period. A read of the input capture register 2 LSB ($0024) does not inhibit the free-running counter transfer since the two actions occur on opposite edges of the internal bus clock.

Reset does not affect the contents of the input capture register 2, except when exiting STOP mode (see Section 6.5).

6.3.3 Input capture register 3 (ICR3)

Input capture register 3 is identical to input capture registers 1 and 2; it is located at $0030 (MSB) and $0031 (LSB).

6.4 Output compare

'Output compare' is a technique which may be used, for example, to generate an output waveform, or to signal when a specific time period has elapsed, by presetting the output compare register to the appropriate value.

There are two output compare registers: output compare register 1 (OCR1) and output compare register 2 (OCR2).

There are two output compare interrupt enable bits (OC1IE and OC2IE).

6.4.1 Output compare register 1 (OCR1)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Output compare 1 high (OCR1H)	$0022									Undefined
Output compare 1 low (OCR1L)	$0023									Undefined

The 16-bit output compare register 1 is made up of two 8-bit registers at locations $0022 (MSB) and $0023 (LSB). The contents of the output compare register 1 are compared with the contents of the free-running counter continually and, if a match is found, the corresponding output compare flag (OC1F) in the timer status register is set. If the timer compare output enable bit (CO1E) is set, the output level (OLVL1) is transferred to pin TCMP1. The output compare register 1 values and the output level bit should be changed after each successful comparison to establish a new elapsed timeout. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit (OC1IE) is set. (The free-running counter is updated every four internal bus clock cycles.)

After a processor write cycle to the output compare register 1 containing the MSB ($0022), the output compare function is inhibited until the LSB ($0023) is also written. The user must write both bytes (locations) if the MSB is written first. A write made only to the LSB ($0023) will not inhibit the compare 1 function. The processor can write to either byte of the output compare register 1 without affecting the other byte. The output level (OLVL1) bit is clocked to the output level register and hence to the TCMP1 pin whether the output compare flag 1 (OC1F) is set or clear. The minimum time required to update the output compare register 1 is a function of the program rather than the internal hardware. Because the output compare flag 1 and the output compare register 1 are not defined at power on, and not affected by reset, care must be taken when initializing output compare functions with software. The following procedure is recommended:

- Write to output compare 1 high to inhibit further compares;
- Read the timer status register to clear OC1F (if set);
- Write to output compare 1 low to enable the output compare 1 function.

The purpose of this procedure is to prevent the OC1F bit from being set between the time it is read and the write to the corresponding output compare register.

All bits of the output compare register are readable and writable and are not altered by the timer hardware or reset. If the compare function is not needed, the two bytes of the output compare register can be used as storage locations.

6.4.2 Output compare register 2 (OCR2)

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Output compare 2 high (OCR2H)	$0026									Undefined
Output compare 2 low (OCR2L)	$0027									Undefined

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The 16-bit output compare register 2 is made up of two 8-bit registers at locations $0026 (MSB) and $0027 (LSB). The contents of the output compare register 2 are compared with the contents of the free-running counter continually and, if a match is found, the corresponding output compare flag (OC2F) in the timer status register is set. If the timer compare 2 output enable bit (CO2E) is set, the output level (OLVL2) is transferred to pin TCMP2. The output compare register 2 values and the output level bit should be changed after each successful comparison to establish a new elapsed timeout. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit (OC2IE) is set. (The free-running counter is updated every four internal bus clock cycles.)

After a processor write cycle to the output compare register 2 containing the MSB ($0026), the output compare function is inhibited until the LSB ($0027) is also written. The user must write both bytes (locations) if the MSB is written first. A write made only to the LSB ($0027) will not inhibit the compare 2 function. The processor can write to either byte of the output compare register 2 without affecting the other byte. The output level (OLVL2) bit is clocked to the output level register and hence to the TCMP2 pin whether the output compare 2 flag (OC2F) is set or clear. The minimum time required to update the output compare register 2 is a function of the program rather than the internal hardware. Because the output compare 2 flag and the output compare register 2 are not defined at power on, and not affected by reset, care must be taken when initializing output compare functions with software. The following procedure is recommended:

– Write to output compare 2 high to inhibit further compares;
– Read the timer status register to clear OC2F (if set);
– Write to output compare 2 low to enable the output compare 2 function.

The purpose of this procedure is to prevent the OC2F bit from being set between the time it is read and the write to the corresponding output compare register.

All bits of the output compare register are readable and writable and are not altered by the timer hardware or reset. If the compare function is not needed, the two bytes of the output compare register can be used as storage locations.

6.4.3 Output compare register 3 (OCR3)

The 16-bit output compare register 3 is made up of two 8-bit registers at locations $0032 (MSB) and $0033 (LSB). This register has no external output; it is used for generating precision time intervals and interrupts only. The OLVL3 bit and the CO3E bit have no effect

6.5 Timer during STOP mode

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When the MCU enters STOP mode, the timer counter stops counting and remains at that particular count value until STOP mode is exited by an interrupt. If STOP mode is exited by power-on or external reset, the counter is forced to $FFFC but if it is exited by external interrupt ($\overline{\text{IRQ}}$) then the counter resumes from its stopped value.

Another feature of the programmable timer is that if at least one valid input capture edge occurs at one of the TCAP pins while in STOP mode, the corresponding input capture detect circuitry is armed. This action does not wake the MCU or set any timer flags, but when the MCU does wake-up there will be an active input capture flag (and data) from that first valid edge which occurred during STOP mode.

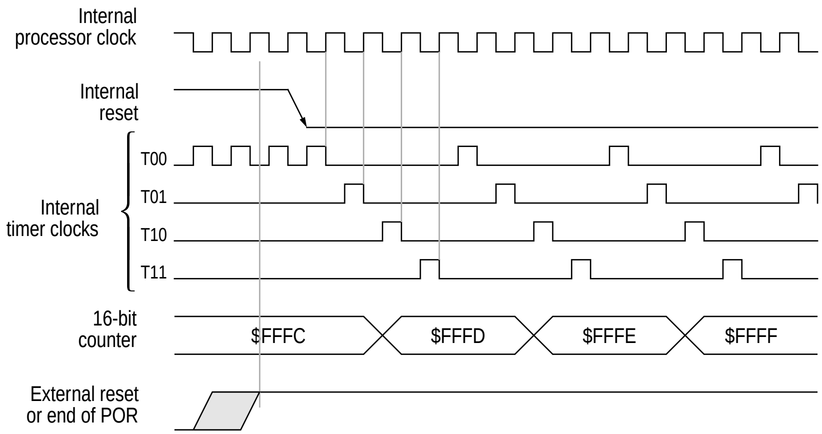
If STOP mode is exited by an external reset then no such input capture flag or data action takes place even if there was a valid input capture edge (at one of the TCAP pins) during STOP mode.

6.6 Timer during WAIT mode

During WAIT mode, the CPU clock halts but the timer keeps running. If a reset is used to exit WAIT mode, the counters are forced to $FFFC. If interrupts are enabled, a timer interrupt will cause the processor to exit WAIT mode.

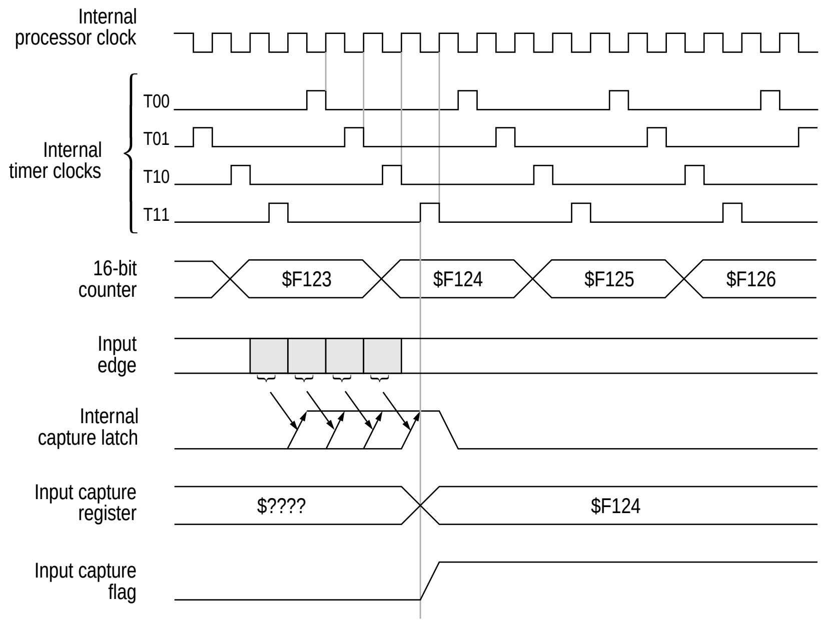
6.7 Timer state diagrams

The relationships between the internal clock signals, the counter contents and the status of the flag bits are shown in the following figures. It should be noted that the signals labelled ‘internal’ (processor clock, timer clocks and reset) are not available to the user.



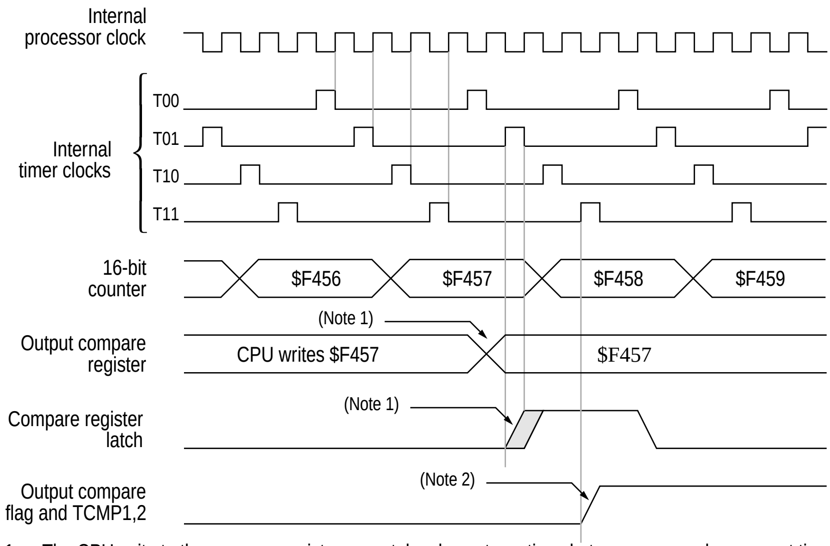
Note: The counter and timer control registers are the only ones affected by power-on or external reset.

Figure 6-1 Timer state timing diagram for reset



Note: If the input edge occurs in the shaded area from one timer state T10 to the next timer state T10, then the input capture flag will be set during the next T11 state.

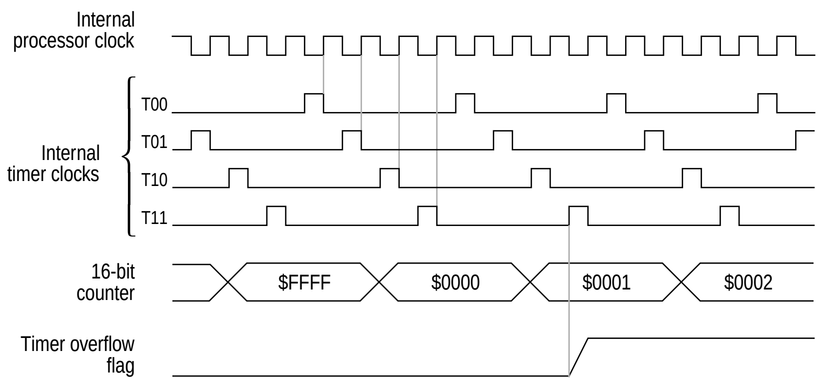
Figure 6-2 Timer state timing diagram for input capture



Note: 1 The CPU write to the compare registers may take place at any time, but a compare only occurs at timer state T01. Thus a four cycle difference may exist between the write to the compare register and the actual compare.

2 The output compare flag is set at the timer state T11 that follows the comparison match ($F457 in this example).

Figure 6-3 Timer state timing diagram for output compare



Note: The timer overflow flag is set at timer state T11 (transition of counter from $FFFF to $0000). It is cleared by a read of the timer status register during the internal processor clock high time, followed by a read of the counter low register.

Figure 6-4 Timer state timing diagram for timer overflow

7

DTMF/MELODY GENERATOR

7.1 Introduction

The DTMF/melody generator (DMG) is a multi-functional tone generator built into the MC68HC05F12 MCU which supports DTMF dialling, melody-on-hold and pacifier tone functions.

7.1.1 Features

- 4 row and 4 column frequencies for DTMF dialling
- 24 row and 24 column frequencies for dual tone melody
- 28 frequencies for pacifier tone to acknowledge button pressed for pulse dialling
- Power saving mechanism for output disable condition
- 3.579MHz/2 operation
- 6-bit D/A converter and 28 time steps for sine wave generation
- Sine wave or square wave selectable output for melody (or DTMF)
- Single or dual tone capability for melody (or DTMF)

7.2 Functional description

As shown in Figure 7-1, the DMG consists of 2 tone generation paths (the column and row paths). One path generates the row tone and the other the column tone, whose frequencies are determined by the values in the frequency control registers FCR and FCC respectively. The tones allowed at the TNO output are single/dual sine/square wave tones of DTMF and melody frequencies, whereas at the TNX output, only single square wave tones are allowed. The method of tone generation for the two paths is almost the same, and is described as follows.

To generate a sine wave tone with programmable frequency in a path, the internal clock (i.e. the 3.58MHz/2) is first divided by a frequency divider according to a number on the register (FCR or FCC). The output of the divider is a periodic pulse train whose frequency is the sampling rate of the desired 'staircase sine wave'. This pulse train, in turn, clocks a divide-by-28 binary counter (PLA scanner) whose 28 decoded outputs scan sequentially 28 memory locations of a 28x6 sine wave generator (PLA) in 28 time steps (M). The six resulting digital sine wave bits are then fed separately to a 6-bit resistor ladder to produce a current signal.

The method for generating a square wave tone in a path is similar to that of a sine wave tone except that only the most significant bit of a sine wave PLA is fed to the 6-bit resistor ladder to produce a current signal (the other 5 least significant bits are masked by the sine/square wave select). Using this method, a square wave tone can be produced which has exactly the same frequency and phase as a sine wave tone, and uses the same frequency control register value.

After obtaining the current signals from the row and column paths, the row current signal is first attenuated by 2dB. It is then summed with the column current signal, and is finally fed to an active 7 KHz low pass filter to reduce harmonic distortion (note that square wave tones are also passed through this filter). The resulting DTMF or melody signal is output through the TNO pin which is normally connected to a speech circuit.

The generator provides not only DTMF and melody but also a square wave pacifier tone (ToneX). This signal is also extracted from the most significant bit of the sine wave PLA of the row path, but is not passed through the filter. The ToneX signal is output through the TNX pin which is normally connected to a loudspeaker.

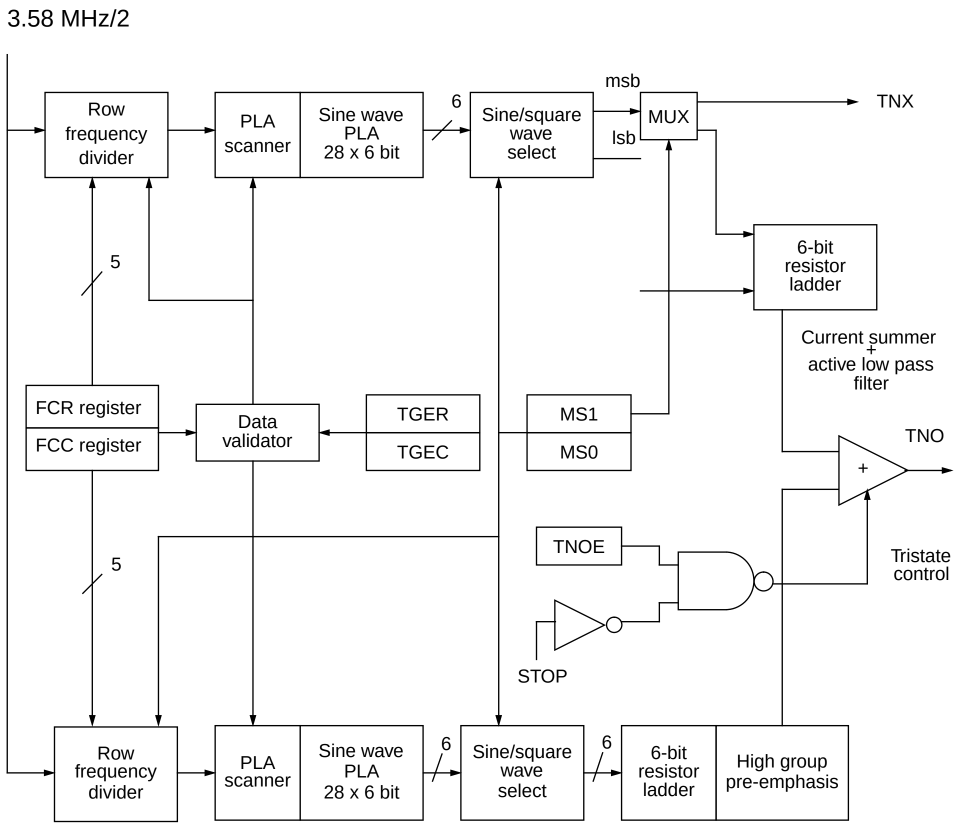


Figure 7-1 DTMF/melody generator (DMG) block diagram

7.3 DMG registers

The DMG has two registers (row frequency control register and column frequency control register) for row and column frequency selection respectively, and one register (tone control register) for tone output control and mode selection.

7.3.1 Row and column frequency control registers

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Row frequency control register (FCR)	$000D	0	0	0	FCR4	FCR3	FCR2	FCR1	FCR0	undefined

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	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Column frequency control register (FCC)	$000E	0	0	0	FCC4	FCC3	FCC2	FCC1	FCC0	undefined

FCR4–FCR0 and FCC4–FCC0 control the frequency of the tone signals on the row and the column paths respectively. The row and column paths are not exactly identical owing to the presence of the high group pre-emphasis in the column path. In order to avoid the entry of the row DTMF tone values to the column, and vice versa, the above cases are treated as illegal. The data validator will disable all outputs when an illegal value is detected. The bit description for DTMF and melody tone generation are shown in Table 7-1 and Table 7-2 respectively. It is the user's responsibility to ensure good programming practice by initialising all registers to contain legal values for the desired function.

7.3.2 Tone control register (TNCR)

This register controls the internal configuration and tone output timing of the DTMF/melody generator.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Tone control register (TNCR)	$000F	MS1	MS0	TGER	TGEC	TNOE	0	0	0	0000 0000

MS1, MS0 — Melody select for operation

The MS0 and MS1 bits control the mode of operation of the DTMF/melody generator. There are sine wave, square wave 1, square wave 2 and square wave 3 modes. They are specified as shown in Table 7-3.

When square wave 2 or square wave 3 mode is selected, the TNX pin is activated. The idle state for TNX is a logic high. The final state of the TNX pin is still dependant on the values of TGER, TGEC (see Table 7-4), FCR and FCC bits (when illegal values are input).

The state of the TNO pin depends on the value of the TNOE bit. After a RESET, the TNOE is cleared and the TNO pin is tristate. When TNOE is set, the TNO output is activated. If the TGER and TGEC bits are held low and TNOE is set, the dc offset of $V_{DD}/2$ appears at TNO pin. In STOP mode, the TNX pin is high and the TNO pin is tristate.

When both MS1 and MS0 are set (square wave 3), the generator can generate both single tone melody at the column path, and ToneX at the row path simultaneously.

TGER — Tone generator enable row path

1 (set) – Row path on

0 (clear) – Row path off

TGEC — Tone generator enable column path

1 (set) – Column path on

0 (clear) – Column path off

TNOE — Tone output enable

1 (set) – TNO on

0 (clear) – TNO off

Table 7-1 Bit description for DTMF generation

FCR register	FCC register	Tone	Standard frequency (Hz)	Tone output frequency (Hz)	Frequency deviation
$00		f_{R1}	697.0	694.8	–0.32
$01		f_{R2}	770.0	770.1	0.02
$02		f_{R3}	852.0	854.2	0.03
$03		f_{R4}	941.0	940.0	–0.11
	$10	f_{C1}	1209.0	1206.0	–0.244
	$11	f_{C2}	1336.0	1331.7	–0.324
	$12	f_{C3}	1477.0	1486.5	0.645
	$13	f_{C4}	1633.0	1639.0	0.367

Note: The legal values in the FCR register column are illegal to the FCC register, and vice versa. An input of illegal values to these registers will produce a high at TNX output and $V_{DD}/2$ at TNO output (TNOE = 1)

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Table 7-2 Bit description for melody generator

FCR/FCC register	Tone	Standard frequency (Hz)	Tone output frequency (Hz)	Frequency deviation (%)
$04	D#5	622.3	620.6	–0.28
$05	E5	659.3	659.0	–0.05
$06	F5	698.5	694.8	–0.53
$07	F#5	740.0	743.3	0.44
$08	G5	784.0	779.5	–0.57
$09	G#5	830.6	830.1	–0.06
$0A	A5	880.0	875.6	–0.50
$0B	A#5	932.0	926.4	–0.64
$0C	B5	987.8	983.4	–0.45
$0D	C6	1046.5	1047.9	0.13
$0E	C#6	1108.7	1102.1	–0.60
$0F	D6	1174.7	1183.7	0.77
$14	D#6	1244.5	1253.3	0.71
$15	E6	1318.5	1331.7	1.00
$16	F6	1396.9	1389.6	–0.52
$17	F#6	1480.0	1486.5	0.44
$18	G6	1568.0	1559.0	–0.57
$19	G#6	1661.2	1682.1	1.26
$1A	A6	1760.0	1775.6	0.89
$1B	A#6	1864.7	1880.0	0.82
$1C	B6	1975.5	1997.5	1.11
$1D	C7	2093.0	2062.0	–1.49
$1E	C#7	2217.5	2204.2	–0.60
$1F	D7	2349.3	2367.4	0.771

Table 7-3 Mode of operation for DMG

MS1	MS0	Mode	TNX output	TNO output
0	0	sine wave	high	sine wave row and column frequency
0	1	square wave 1	high	square wave row and column frequency
1	0	square wave 2	row frequency	square wave row and column frequency
1	1	square wave 3	row frequency	square wave column frequency

TGER, TGEC — Tone generation enable for row and column paths

When both bits are held low, the DMG is disabled by forcing the two frequency counters and the two PLA scanning counters to their reset states. The DMG should then consume zero dynamic power, if the TNOE bit is also cleared.

When a TGE bit for a path is held high (provided that the value in the frequency control register for that path is legal), the generator is enabled. All the counters associated with that path are then run from their reset states.

The reset state of a frequency counter defines the time=0 state of the time step, whereas at their reset state, the PLA scanning counters, scanning the memory location, contain the dc values of the staircase sine wave.

In DTMF dialling, the row and column tone values are first entered to the FCR and FCC registers. The TGER and TGEC bits are then set or reset simultaneously to achieve dual tone multiple frequency. Similarly, in melody generation, one path is chosen as the high part, and the other as the low part. The TGER and TGEC bits are then set and reset according to the rhythm required by the musical piece. One can exhibit only single tone melody by disabling either TGER or TGEC permanently. The DTMF column and row frequency tones can also be output separately for testing by enabling just the one path.

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Table 7-4 Effect of tone generation on DMG

TGER	TGEC	Row Path	Column Path
0	0	off	off
0	1	off	active
1	0	active	off
1	1	active	active

7.4 Operation of the DMG

The DMG is recommended to be operated using the following procedures:

To operate melody generation, the choice of sine wave or square wave output mode is totally up to the user’s taste. The sine wave melody has a sound like a flute, whereas the square wave melody possesses much richer harmonics. The required tones are selected through the FCR and FCC registers. The selected tone is output when the corresponding TGER or TGEC bit and TNOE bit are set. The FCR register should contain the value representing the tone output frequency and the FCC register should contain a value of $03 or greater to ensure the output is not blocked by the data validator.

7.5 DMG during WAIT mode

The DMG is still active during the WAIT mode.

7.6 DMG during STOP mode

In STOP mode the oscillator is stopped causing the DMG to cease function.

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8

LIQUID CRYSTAL DISPLAY DRIVER MODULE

The LCD driver module on the MC68HC05F12 supports 32 frontplanes and 4 backplanes, allowing a maximum of 128 LCD segments. Each segment is controlled by a corresponding bit in the LCD RAM. The mode of operation is determined by the values set in the LCD control register at $1E.

After reset and on leaving standby, the drivers are configured in the default duplex mode, 1/2 bias with 2 backplanes. At power-up or after reset, the ON/OFF control bits for the internal and external V_{LCD} voltage (INTVLCD and EXTVON) are cleared, disabling the LCD drivers. Figure 8-1 shows a block diagram of the LCD system. At power-up or after reset the LCD port's control bits are cleared, which disables the LCD frontplane drivers.

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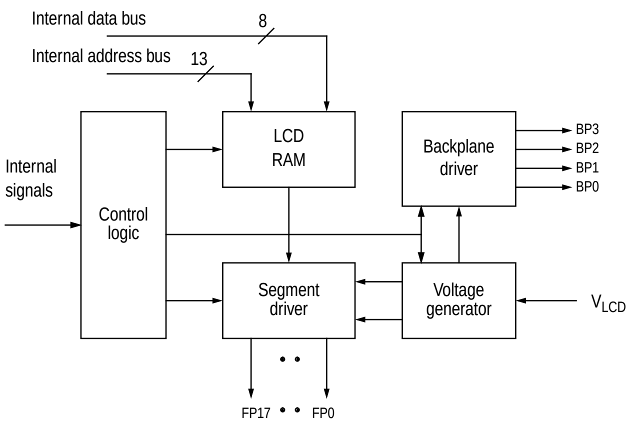

Figure 8-1 LCD system block diagram

8.1 LCD RAM

Data to be displayed on the LCD must be written into the LCD RAM. The LCD RAM is comprised of 16 bytes of RAM (in the MC68HC05F12's memory map) at $0040 – $004F. The 128 bits in the LCD RAM correspond to the 128 segments that can be driven by the frontplane/backplane drivers. Table 8-1 shows how the LCD RAM is organized. Writing a '1' to a given location will result in the corresponding display segment being activated when the EXTVON or INTVLCD bit is set. The LCD RAM is a dual port RAM that interfaces with the internal address and data buses of the MCU. It is possible to read from LCD RAM locations for scrolling purposes.

Table 8-1 LCD RAM organization

LCD RAM	Data							
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$40	FP1-BP3	FP1-BP2	FP1-BP1	FP1-BP0	FP0-BP3	FP0-BP2	FP0-BP1	FP0-BP0
$41	FP3-BP3	FP3-BP2	FP3-BP1	FP3-BP0	FP2-BP3	FP2-BP2	FP2-BP1	FP2-BP0
$42	FP5-BP3	FP5-BP2	FP5-BP1	FP5-BP0	FP4-BP3	FP4-BP2	FP4-BP1	FP4-BP0
$43	FP7-BP3	FP7-BP2	FP7-BP1	FP7-BP0	FP6-BP3	FP6-BP2	FP6-BP1	FP6-BP0
$44	FP9-BP3	FP9-BP2	FP9-BP1	FP9-BP0	FP8-BP3	FP8-BP2	FP8-BP1	FP8-BP0
$45	FP11-BP3	FP11-BP2	FP11-BP1	FP11-BP0	FP10-BP3	FP10-BP2	FP10-BP1	FP10-BP0
$46	FP13-BP3	FP13-BP2	FP13-BP1	FP13-BP0	FP12-BP3	FP12-BP2	FP12-BP1	FP12-BP0
$47	FP15-BP3	FP15-BP2	FP15-BP1	FP15-BP0	FP14-BP3	FP14-BP2	FP14-BP1	FP14-BP0
$48	FP17-BP3	FP17-BP2	FP17-BP1	FP17-BP0	FP16-BP3	FP16-BP2	FP16-BP1	FP16-BP0
$49	FP19-BP3	FP19-BP2	FP19-BP1	FP19-BP0	FP18-BP3	FP18-BP2	FP18-BP1	FP18-BP0
$4A	FP21-BP3	FP21-BP2	FP21-BP1	FP21-BP0	FP20-BP3	FP20-BP2	FP20-BP1	FP20-BP0
$4B	FP23-BP3	FP23-BP2	FP23-BP1	FP23-BP0	FP22-BP3	FP22-BP2	FP22-BP1	FP22-BP0
$4C	FP25-BP3	FP25-BP2	FP25-BP1	FP25-BP0	FP24-BP3	FP24-BP2	FP24-BP1	FP24-BP0
$4D	FP27-BP3	FP27-BP2	FP27-BP1	FP27-BP0	FP26-BP3	FP26-BP2	FP26-BP1	FP26-BP0
$4E	FP29-BP3	FP29-BP2	FP29-BP1	FP29-BP0	FP28-BP3	FP28-BP2	FP28-BP1	FP28-BP0
$4F	FP31-BP3	FP31-BP2	FP31-BP1	FP31-BP0	FP30-BP3	FP30-BP2	FP30-BP1	FP30-BP0

8.2 LCD operation

The LCD driver module can operate in four modes providing different multiplex ratios and number of backplanes as follows:

- 1/2 bias, 2 backplanes
- 1/3 bias, 2 backplanes
- 1/3 bias, 3 backplanes
- 1/4 bias, 4 backplanes

The operating mode is selected at power on using the multiplex ratio bits (MUX3 and MUX4) in the LCD control register as shown in Table 8-3.

It is recommended that the EXTVON and INTVLCD bits in the LCD register are not set (display is disabled) until the multiplex rate is selected. The voltage levels required for the different multiplex rates are generated internally by a resistive divider chain between V_{LCD} and V_{SS}.

The 2-way multiplex with 1/3 bias and the three and four-way multiplex options require four voltage levels, whereas the two-way multiplex with 1/2 bias needs only three levels. Resistors R1, R2 and R3 are valued at 20kΩ ±40%. Figure 8-2 shows the resistive divider chain network that is used to produce the various LCD waveforms outlined in Section 8.3.

The LCD drivers can operate with an external V_{LCD} supply when EXTVON = 1, or with an internally generated LCD voltage when INTVLCD = 1. The EXTVON option is useful when a display with particular thresholds is being used. The LCD controller is enabled if the EXTVON bit or the INTVLCD bit is set. Table 8-2 shows the different modes of operation depending on the bits EXTVON and INTVLCD of the LCD control register.

Table 8-2 LCD controller operating modes

EXTVON	INTVLCD	LCD controller	Internal voltage generator	Resistor chain connected with
0	0	off	off	—
0	1	on	on	internal V_{LCD}
1	0	on	off	VLCD pin
1	1	on	on	both (for test)

Note: The external voltage V_{LCD} may not exceed the positive power supply voltage, V_{DD}.

Note: If both bits INTVLCD and EXTVON are set, an externally applied voltage source can cause damage to the LCD drivers.

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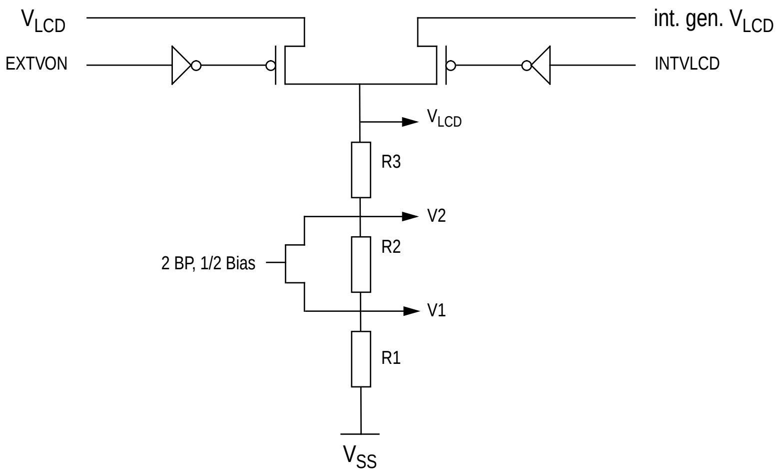


Figure 8-2 Voltage level selection

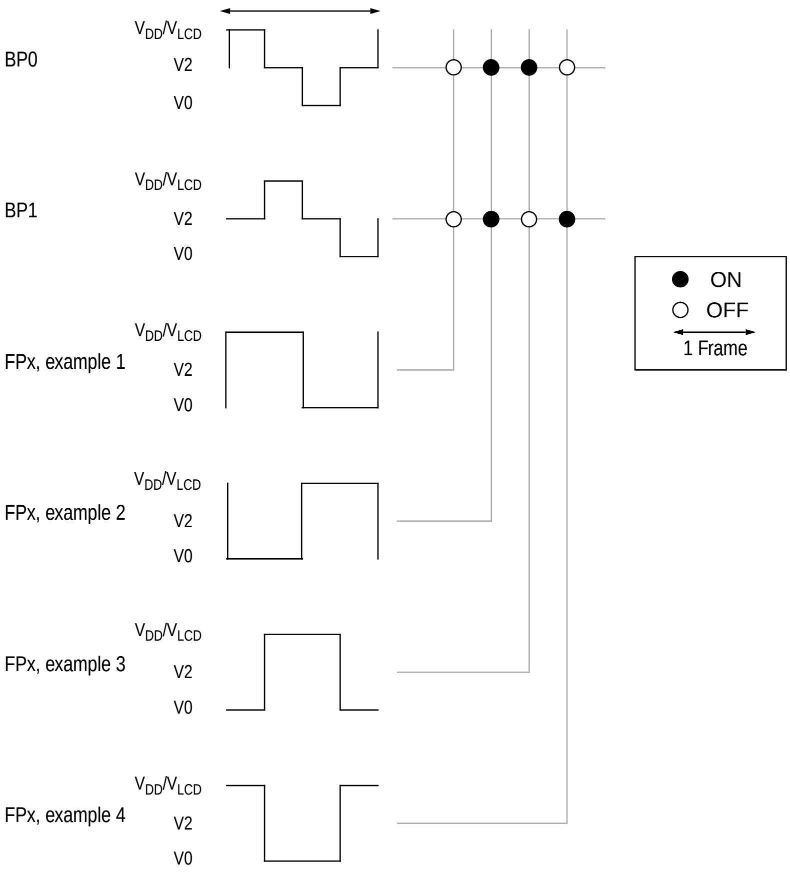
8.3 Timing signals and LCD voltage waveforms

The LCD timing signals are all derived from the main system clock. The frame rate will be $f_{OSC}/2^{16}$, therefore, if f_{OSC} = 3.579 MHz, the frame rate will be 54.6 Hz for two and four-way multiplexing and 72.8 Hz for three-way multiplexing (see Table 8-3). An extra divide-by-two stage can be included in the LCD clock generator by setting FDISP in the LCD register. This will result in the frame rate being halved. For example, when three-way multiplexing is used, a frame rate of 36.4 Hz instead of 72.8 Hz can be obtained. See Section 8.4.

Figure 8-3 to Figure 8-6 show the backplane waveforms and some examples of frontplane waveforms for each of the operating modes.

The backplane waveforms are continuous and repetitive (every frame); they are fixed within each operating mode and are not affected by the data in the LCD RAM.

The frontplane waveforms are dependent on the LCD segments to be driven as defined in the LCD RAM. Each ‘on’ segment must have a differential driving voltage (BP–FP) applied to it once in each frame; the LCD driver module hardware uses the data in the LCD RAM to construct the frontplane waveform to meet this criterion.



Note: In this mode V1=V2

Figure 8-3 LCD waveform with 2 backplanes, 1/2 bias

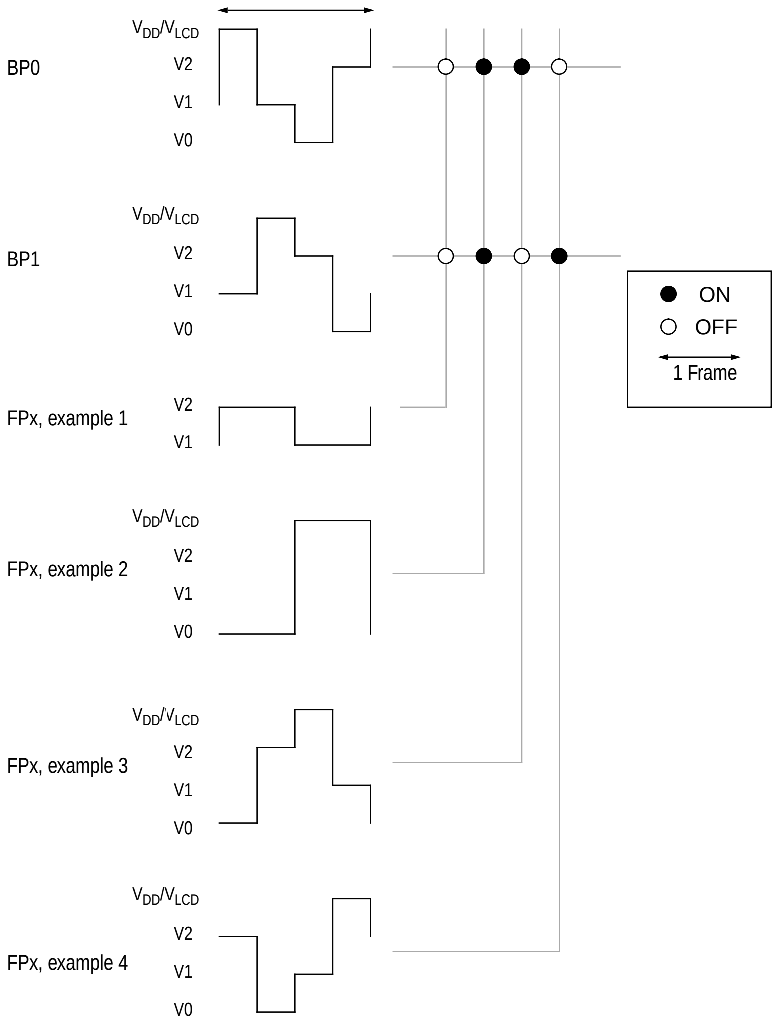


Figure 8-4 LCD waveform with 2 backplanes, 1/3 bias

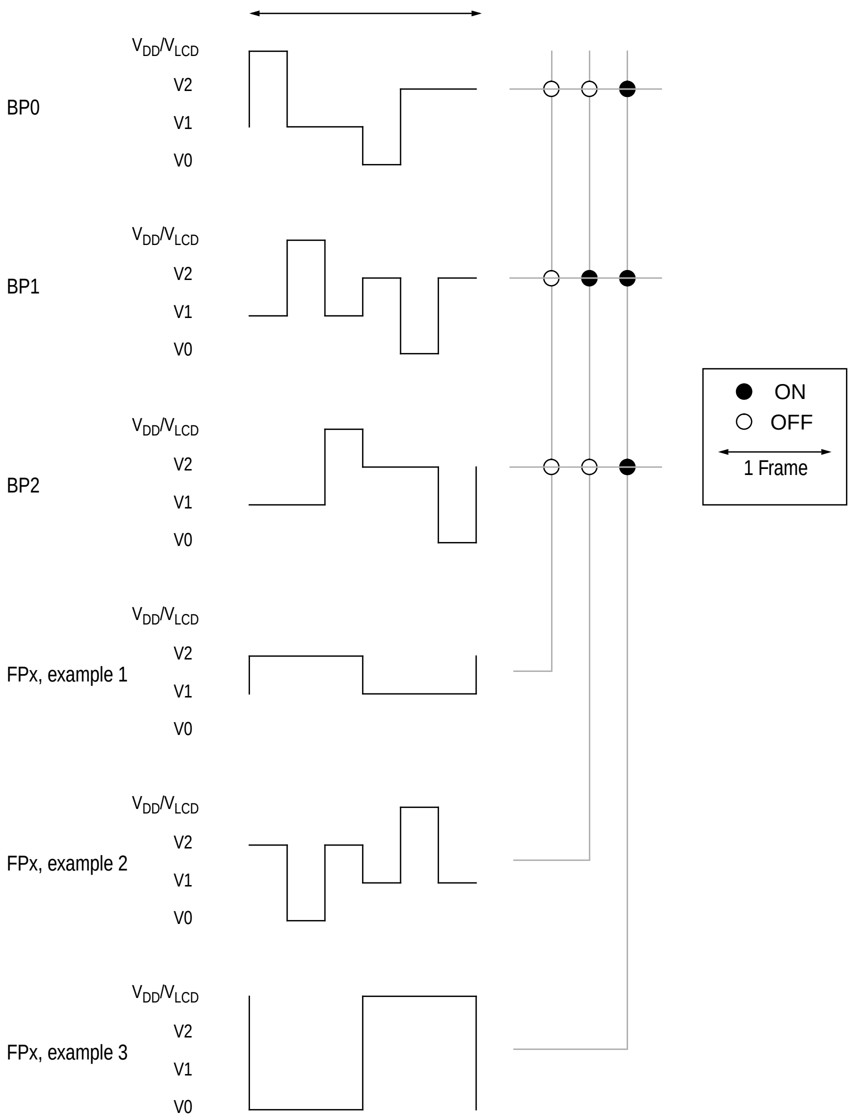


Figure 8-5 LCD waveform with 3 backplanes

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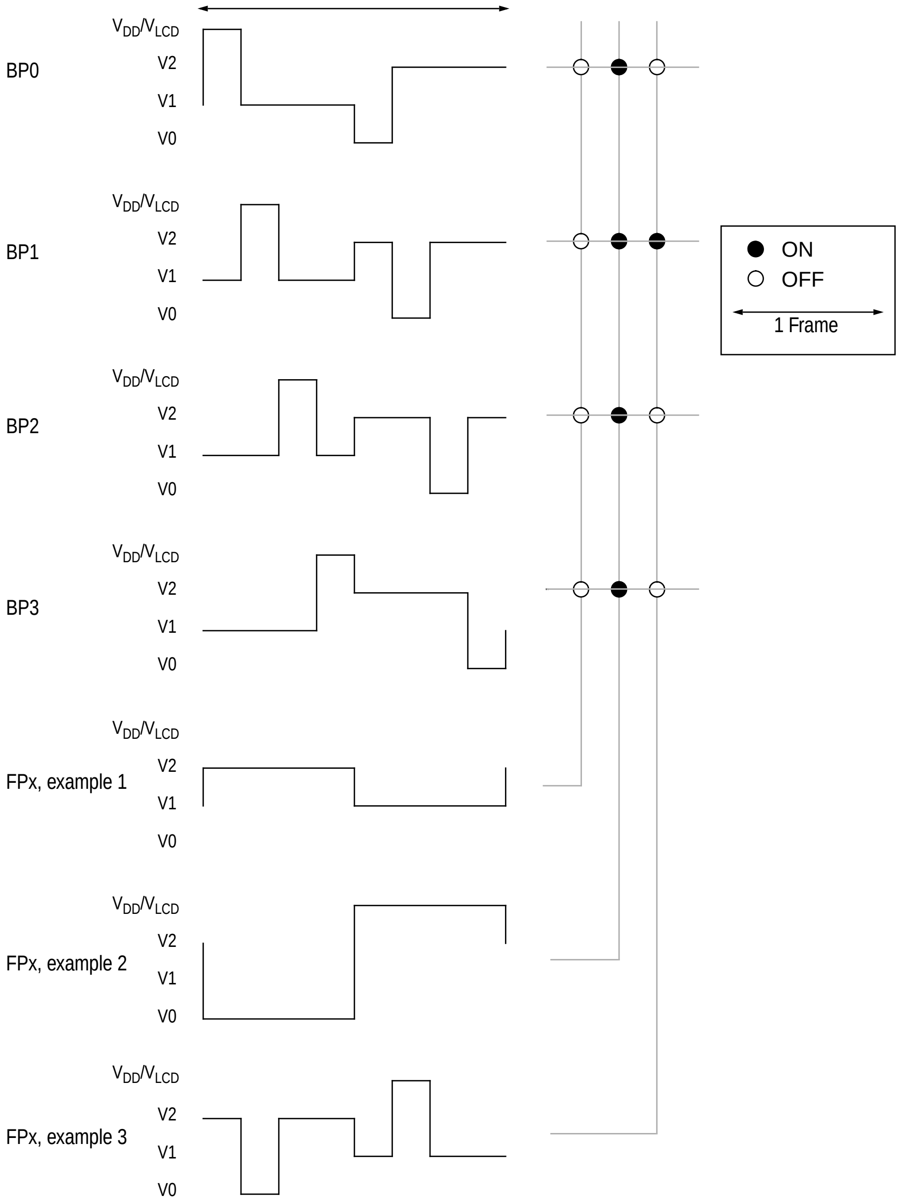

Figure 8-6 LCD waveform with 4 backplanes

8.4 LCD control register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
LCD control register (LCD)	$001E	0	0	0	INTVLCD	FDISP	MUX4	MUX3	EXTVON	0000 0000

Bits 5, 6 and 7

These bits are reserved for future use and must be cleared to zero when writing to this register.

INTVLCD — Internal voltage generator ON/OFF

1 (set) – The display is on and an internal voltage generator is activated.

0 (clear) – The internal voltage generator is turned off.

When the INTVLCD bit is set, the display controller is on and an internal voltage generator is activated and connected to the resistor chain (V_{LCD} = 3V approx., if V_{DD} > 3V). See Table 8-2.

FDISP — Display frequency

1 (set) – Extra divide by two stage is included in the LCD clock generator when this bit is set, giving a reduced frame rate.

0 (clear) – Default frame rate is used.

For example, in the 3-way multiplexing mode, a frame rate of 36.8 Hz instead of 72.8 Hz can be achieved.

MUX4, MUX3 — Multiplex ratio

These two bits select the multiplex ratio to be 2, 3 or 4 backplanes. See Table 8-3.

Table 8-3 Multiplex ratio/backplane selection

MUX4	MUX3	Backplanes	Bias	Frequency
0	0	2	1/2	54.6 Hz
0	1	3	1/3	72.8 Hz
1	0	4	1/3	54.6 Hz
1	1	2	1/3	54.6 Hz

EXTVON — External LCD voltage ON/OFF

1 (set) – External LCD voltage is connected.

0 (clear) – External LCD voltage is disconnected.

Clearing this bit disconnects the voltage generator resistor chain from the external V_{LCD}. See Table 8-2.

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8.5 LCD during WAIT mode

The LCD drivers function normally during WAIT mode and will keep the display active if the EXTVON bit or the INTVLCD bit is set.

8.6 LCD during STOP mode

During STOP mode the LCD controller is disabled. The driver outputs are discharged by the resistor chain.

9
RESETS AND INTERRUPTS

9.1 Resets

The MC68HC05F12 can be reset in five ways: by the initial power-on reset function, by an active low input to the $\overline{\text{RESET}}$ pin, by an on-chip low voltage reset, by an opcode fetch from an illegal address, and by a COP watchdog timer reset. Any of these resets will cause the program to return to its starting address, specified by the contents of memory locations $7FFE and $7FFF, and cause the interrupt mask of the CCR to be set.

9.1.1 Power-on reset

A power-on reset occurs when a positive transition is detected on VDD. The power-on reset function is strictly for power turn-on conditions and should not be used to detect drops in the power supply voltage. The power-on circuitry provides a stabilization delay (t_{PORL}) from when the oscillator becomes active. If the external $\overline{\text{RESET}}$ pin is low at the end of this delay then the processor remains in the reset state until $\overline{\text{RESET}}$ goes high.

9.1.2 $\overline{\text{RESET}}$ pin

When the oscillator is running in a stable state, the MCU is reset when a logic zero is applied to the $\overline{\text{RESET}}$ input for a minimum period of 1.5 machine cycles (t_{CYC}). This pin contains an internal Schmitt trigger as part of its input to improve noise immunity. When the reset pin goes high, the MCU will resume operation on the following cycle. The $\overline{\text{RESET}}$ pin is also an output device for the internal low voltage reset.

9.1.3 Illegal address reset

When an opcode fetch occurs from an address which is not part of the RAM ($0050 – $01CF) or of the ROM ($4F00 – $7FFF) or EEPROM ($0200 – $02FF), the device is automatically reset.

Note: No RTS or RTI instruction should be placed at the end of a memory block since this could result in an illegal address reset.

9.1.4 Computer operating properly (COP) reset

The MCU contains a watchdog timer that automatically times out if not reset (cleared) within a specific time by a program reset sequence.

If the COP watchdog timer is allowed to timeout, an internal reset is generated to reset the MCU. Because the internal reset signal is used, the MCU comes out of a COP reset in the same operating mode it was in when the COP timeout was generated.

The COP function is a mask option, enabled or disabled during device manufacture. See Section 1.1.

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Refer to Section 5.3 for more information on the COP watchdog timer.

9.1.5 Low voltage reset

The MCU contains a low voltage detection circuit which drives the external reset.

For a positive transition of supply voltage v_{DD}, the low voltage reset occurs as long as V_{DD} is below the V_{RON} level. In this case the external reset pin is pulled down. If the supply voltage drops off above the V_{RON} level, the reset is released. If the supply voltage falls off below the V_{ROFF} level, the $\overline{RESET}$ pin is pulled down.

9.2 Interrupts

The MCU can be interrupted by six different sources, five maskable hardware interrupts and one nonmaskable software interrupt:

- External signal on the $\overline{\text{IRQ}}$ pin
- Keyboard interrupt
- Core timer interrupt
- 16-bit programmable timer interrupt
- Low voltage interrupt (LVI) – EEPROM
- Software interrupt instruction (SWI)

Interrupts cause the processor to save the register contents on the stack and to set the interrupt mask (I-bit) to prevent additional interrupts. The RTI instruction (return from interrupt) causes the register contents to be recovered from the stack and normal processing to resume. While executing the RTI instruction, the interrupt mask bit (I-bit) will be cleared providing the corresponding enable bit stored on the stack is zero, i.e. the interrupt is disabled.

Unlike reset, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction is complete. The current instruction is the one already fetched and being operated on. When the current instruction is complete, the processor checks all pending hardware interrupts. If interrupts are not masked (CCR I-bit clear) and the corresponding interrupt enable bit is set, the processor proceeds with interrupt processing; otherwise, the next instruction is fetched and executed. Figure 9-1 shows the interrupt processing flow.

Note: Power-on or external reset clears all interrupt enable bits thus preventing interrupts during the reset sequence.

9.2.1 Interrupt priorities

Each potential interrupt source is assigned a priority which means that if more than one interrupt is pending at the same time, the processor will service the one with the highest priority first. For example, if both an external interrupt and a timer interrupt are pending after an instruction execution, the external interrupt is serviced first.

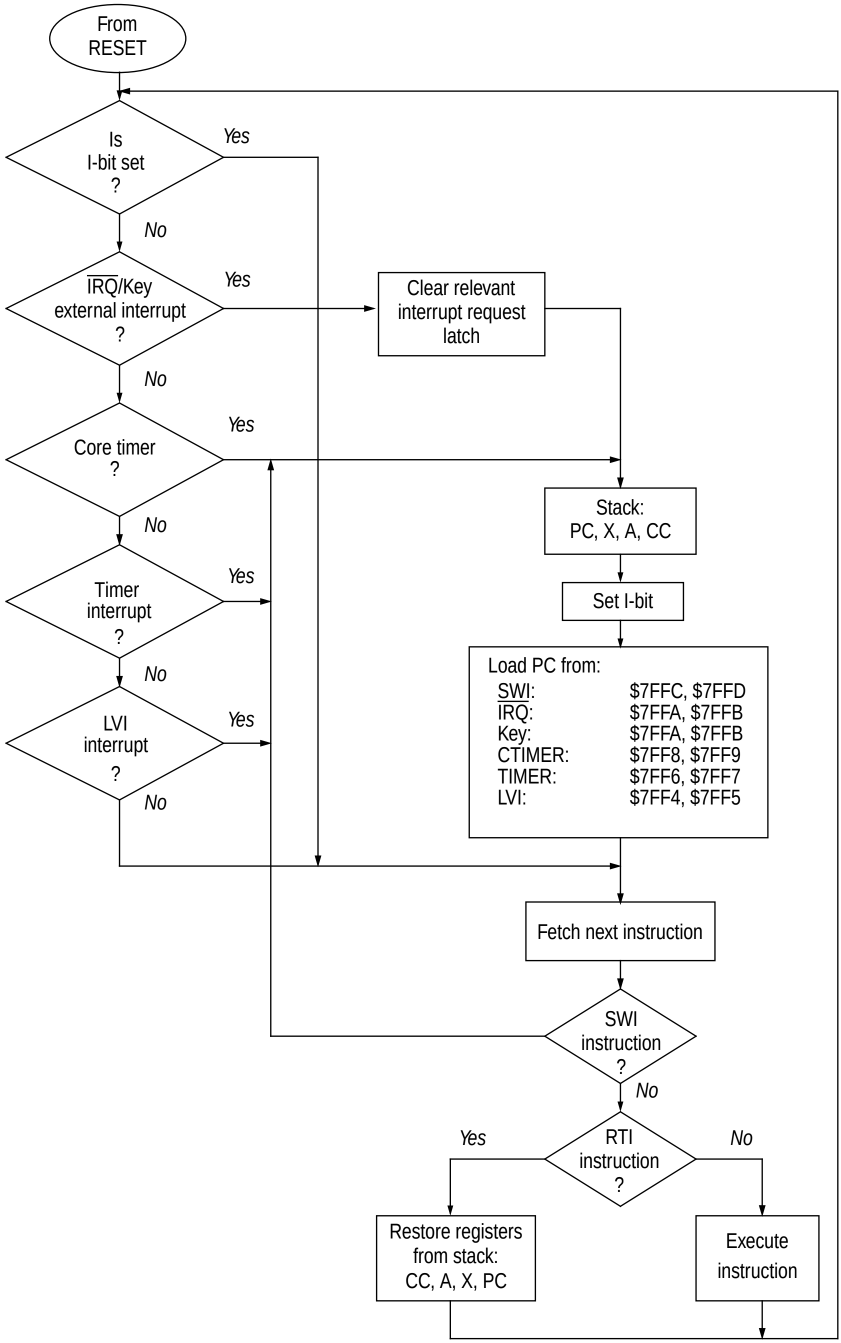

Figure 9-1 Interrupt flowchart

Table 9-1 Vector address for interrupts and reset

Register	Flag name	Interrupts	CPU interrupt	Vector address
—	—	Reset	$\overline{\text{RESET}}$	$7FFE–$7FFF
—	—	Software interrupt	SWI	$7FFC–$7FFD
—	—	External interrupt	$\overline{\text{IRQ}}$	$7FFA–$7FFB
CTCSR	CTOF	Core timer overflow	CTIMER	$7FF8–$7FF9
CTCSR	RTIF	Real time interrupt	CTIMER	$7FF8–$7FF9
TSR	ICF1	Timer input capture1	TIMER	$7FF6–$7FF7
TSR	OCF1	Timer output compare1	TIMER	$7FF6–$7FF7
TSR	ICF2	Timer input capture2	TIMER	$7FF6–$7FF7
TSR	OCF2	Timer output compare2	TIMER	$7FF6–$7FF7
TSR2	ICF3	Timer input capture3	TIMER	$7FF6–$7FF7
TSR2	OCF3	Timer output compare3	TIMER	$7FF6–$7FF7
TSR	TOF	Timer overflow	TIMER	$7FF6–$7FF7
KEY	KSF	Keyboard interrupt	KEYF	$7FFA–$7FFB
SOR	LVI	Low voltage interrupt	LVI	$7FF4–$7FF5

9.2.2 Non-maskable software interrupt (SWI)

The software interrupt (SWI) is an executable instruction and a nonmaskable interrupt: it is executed regardless of the state of the I-bit in the CCR. If the I-bit is zero (interrupts enabled), SWI is executed after interrupts that were pending when the SWI was fetched, but before interrupts generated after the SWI was fetched. The SWI interrupt service routine address is specified by the contents of memory locations $7FFC and $7FFD.

9.2.3 Maskable hardware interrupts

If the interrupt mask bit (I-bit) of the CCR is set, all maskable interrupts (internal and external) are masked. Clearing the I-bit allows interrupt processing to occur. $\overline{\text{IRQ}}$ is software selectable as either edge or edge-and-level sensitive (bit 3 of the system option register).

Note: The internal interrupt latch is cleared in the first part of the interrupt service routine; therefore, one external interrupt pulse could be latched and serviced as soon as the I-bit is cleared.

9.2.3.1 Real time and core timer (CTIMER) interrupts

There are two different core timer interrupt flags that cause a CTIMER interrupt whenever an interrupt is enabled and its flag becomes set, namely RTIF and CTOF. The interrupt flags and enable bits are located in the CTIMER control and status register (CTCSR). These interrupts will vector to the same interrupt service routine, whose start address is contained in memory locations $7FF8 and $7FF9 (see Section 5.2.1 and Figure 5-1).

To make use of the real time interrupt the RTIE bit must first be set. The RTIF bit will then be set after the specified number of counts.

To make use of the core timer overflow interrupt, the CTOFE bit must first be set. The CTOF bit will then be set when the core timer counter register overflows from $FF to $00.

9.2.3.2 Programmable 16-bit timer interrupt

There are seven different timer interrupt flags that cause a timer interrupt whenever they are set and enabled. The timer interrupt enable bits are located in the timer control register (TCR) and the timer interrupt flags are located in the timer status register (TSR). Either of these interrupts will vector to the same service routine, whose start address is contained in memory locations $7FF6 and $7FF7.

9.2.3.3 Keyboard interrupt

When configured as input pins, all eight port A lines provide a wired-OR keyboard interrupt facility and will generate an interrupt, provided that the keyboard interrupt enable bit (KIE) in the keyboard/timer register (KEY/TIM) is set. The address of the interrupt service routine is specified by the contents of memory locations $0FFA and $0FFB. Since this interrupt vector is shared with the IRQ external interrupt function the interrupt service routine should check KSF to determine the interrupt source. KSF should be cleared by software in the interrupt service routine. Care must be taken to allow adequate time for switch debounce before clearing the flag.

9.2.3.4 Low voltage interrupt

There is a low voltage interrupt flag that causes an interrupt whenever it is set and enabled. The low voltage interrupt enable bit and the interrupt flag are located in the system option register (SOR). This interrupt will vector to the service routine, located at the address specified by the contents of memory locations $7FF4 and $7FF5.

9.2.4 Hardware controlled interrupt sequence

The following three functions (RESET, STOP, and WAIT) are not in the strictest sense interrupts. However, they are acted upon in a similar manner. Flowcharts for STOP and WAIT are shown in Figure 2-1.

RESET: A reset condition causes the program to vector to its starting address, which is contained in memory locations $7FFE (MSB) and $7FFF (LSB). The I-bit in the condition code register is also set, to disable interrupts.

STOP: The STOP instruction causes the oscillator to be turned off and the processor to ‘sleep’ until an external interrupt ($\overline{IRQ}$), a low voltage interrupt (LVI), or a keyboard interrupt occurs, or the device is reset.

WAIT: The WAIT instruction causes all processor clocks to stop, but leaves the timer clocks running. This ‘rest’ state of the processor can be cleared by reset, an external interrupt ($\overline{IRQ}$), a keyboard interrupt, a timer interrupt (core or 16-bit), or a LVI interrupt. There are no special WAIT vectors for these interrupts.

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10
CPU CORE AND INSTRUCTION SET

This section provides a description of the CPU core registers, the instruction set and the addressing modes of the MC68HC05F12.

10.1 Registers

The MCU contains five registers, as shown in the programming model of Figure 10-1. The interrupt stacking order is shown in Figure 10-2.

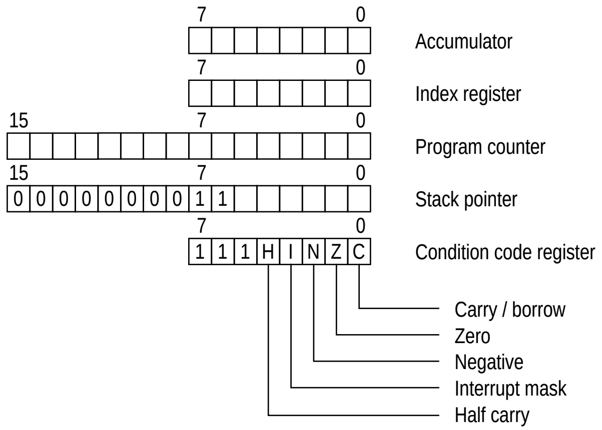

Figure 10-1 Programming model

10.1.1 Accumulator (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

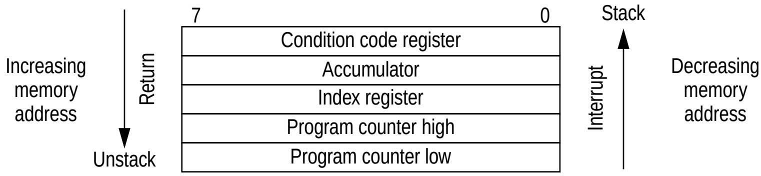

Figure 10-2 Stacking order

10.1.2 Index register (X)

The index register is an 8-bit register, which can contain the indexed addressing value used to create an effective address. The index register may also be used as a temporary storage area.

10.1.3 Program counter (PC)

The program counter is a 16-bit register, which contains the address of the next byte to be fetched.

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10.1.4 Stack pointer (SP)

The stack pointer is a 16-bit register, which contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location \$00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the ten most significant bits are permanently set to 0000000011. These ten bits are appended to the six least significant register bits to produce an address within the range of \$00C0 to \$00FF. Subroutines and interrupts may use up to 64 (decimal) locations. If 64 locations are exceeded, the stack pointer wraps around and overwrites the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.

10.1.5 Condition code register (CCR)

The CCR is a 5-bit register in which four bits are used to indicate the results of the instruction just executed, and the fifth bit indicates whether interrupts are masked. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.

Half carry (H)

This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

Interrupt (I)

When this bit is set, all maskable interrupts are masked. If an interrupt occurs while this bit is set, the interrupt is latched and remains pending until the interrupt bit is cleared.

Negative (N)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative.

Zero (Z)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

Carry/borrow (C)

When set, this bit indicates that a carry or borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions and during shifts and rotates.

10.2 Instruction set

The MCU has a set of 62 basic instructions. They can be grouped into five different types as follows:

- Register/memory
- Read/modify/write
- Branch
- Bit manipulation
- Control

The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

This MCU uses all the instructions available in the M146805 CMOS family plus one more: the unsigned multiply (MUL) instruction. This instruction allows unsigned multiplication of the contents of the accumulator (A) and the index register (X). The high-order product is then stored in the index register and the low-order product is stored in the accumulator. A detailed definition of the MUL instruction is shown in Table 10-1.

10.2.1 Register/memory Instructions

Most of these instructions use two operands. The first operand is either the accumulator or the index register. The second operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 10-2 for a complete list of register/memory instructions.

10.2.2 Branch instructions

These instructions cause the program to branch if a particular condition is met; otherwise, no operation is performed. Branch instructions are two-byte instructions. Refer to Table 10-3.

10.2.3 Bit manipulation instructions

The MCU can set or clear any writable bit that resides in the first 256 bytes of the memory space (page 0). All port data and data direction registers, timer and serial interface registers, control/status registers and a portion of the on-chip RAM reside in page 0. An additional feature allows the software to test and branch on the state of any bit within these locations. The bit set, bit clear, bit test and branch functions are all implemented with single instructions. For the test and branch instructions, the value of the bit tested is also placed in the carry bit of the condition code register. Refer to Table 10-4.

10.2.4 Read/modify/write instructions

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to this sequence of reading, modifying and writing, since it does not modify the value. Refer to Table 10-5 for a complete list of read/modify/write instructions.

10.2.5 Control instructions

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 10-6 for a complete list of control instructions.

10.2.6 Tables

Tables for all the instruction types listed above follow. In addition there is a complete alphabetical listing of all the instructions (see Table 10-7), and an opcode map for the instruction set of the M68HC05 MCU family (see Table 10-8).

Table 10-1 MUL instruction

Operation	**X:A ← X*A**			
Description	Multiplies the eight bits in the index register by the eight bits in the accumulator and places the 16-bit result in the concatenated accumulator and index register.			
Condition codes	H : Cleared I : Not affected N : Not affected Z : Not affected C : Cleared			
Source	MUL			
Form	Addressing mode	Cycles	Bytes	Opcode
	Inherent	11	1	$42

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10.3 Addressing modes

Ten different addressing modes provide programmers with the flexibility to optimize their code for all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions; the longest instructions (three bytes) enable access to tables throughout memory. Short absolute (direct) and long absolute (extended) addressing are also included. One or two byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory locations.

The term 'effective address' (EA) is used in describing the various addressing modes. The effective address is defined as the address from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate 'contents of' the location or register referred to. For example, (PC) indicates the contents of the location pointed to by the PC (program counter). An arrow indicates 'is replaced by' and a colon indicates concatenation of two bytes. For additional details and graphical illustrations, refer to the ***M6805 HMOS/M146805 CMOS Family Microcomputer/ Microprocessor User's Manual*** or to the ***M68HC05 Applications Guide***.

Table 10-2 Register/memory instructions

Function	Mnemonic	Addressing modes																	
		Immediate			Direct			Extended			Indexed (no offset)			Indexed (8-bit offset)			Indexed (16-bit offset)		
		Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles
Load A from memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in memory	STA				B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in memory	STX				BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add memory and carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract memory from A with borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND memory with A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic compare A with memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic compare X with memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit test memory with A (logical compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump unconditional	JMP				BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to subroutine	JSR				BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

10.3.1 Inherent

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, as well as the control instruction, with no other arguments are included in this mode. These instructions are one byte long.

10.3.2 Immediate

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants that do not change during program execution (e.g. a constant used to initialize a loop counter).

$$EA = PC+1; PC \leftarrow PC+2$$

Table 10-3 Branch instructions

Function	Mnemonic	Relative addressing mode		
		Opcode	# Bytes	# Cycles
Branch always	BRA	20	2	3
Branch never	BRN	21	2	3
Branch if higher	BHI	22	2	3
Branch if lower or same	BLS	23	2	3
Branch if carry clear	BCC	24	2	3
(Branch if higher or same)	(BHS)	24	2	3
Branch if carry set	BCS	25	2	3
(Branch if lower)	(BLO)	25	2	3
Branch if not equal	BNE	26	2	3
Branch if equal	BEQ	27	2	3
Branch if half carry clear	BHCC	28	2	3
Branch if half carry set	BHCS	29	2	3
Branch if plus	BPL	2A	2	3
Branch if minus	BMI	2B	2	3
Branch if interrupt mask bit is clear	BMC	2C	2	3
Branch if interrupt mask bit is set	BMS	2D	2	3
Branch if interrupt line is low	BIL	2E	2	3
Branch if interrupt line is high	BIH	2F	2	3
Branch to subroutine	BSR	AD	2	6

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Table 10-4 Bit manipulation instructions

Function	Mnemonic	Addressing modes					
		Bit set/clear			Bit test and branch		
		Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles
Branch if bit n is set	BRSET n (n=0–7)				2•n	3	5
Branch if bit n is clear	BRCLR n (n=0–7)				01+2•n	3	5
Set bit n	BSET n (n=0–7)	10+2•n	2	5			
Clear bit n	BCLR n (n=0–7)	11+2•n	2	5			

10.3.3 Direct

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two-byte instruction.

$$EA = (PC+1); PC \leftarrow PC+2$$
$$\text{Address bus high} \leftarrow 0; \text{Address bus low} \leftarrow (PC+1)$$

Table 10-5 Read/modify/write instructions

Function	Mnemonic	Inherent (A)			Inherent (X)			Direct			Indexed (no offset)			Indexed (8-bit offset)		
		Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (two's complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate left through carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate right through carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical shift left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical shift right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic shift right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for negative or zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5
Multiply	MUL	42	1	11												

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Table 10-6 Control instructions

Function	Mnemonic	Inherent addressing mode		
		Opcode	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set carry bit	SEC	99	1	2
Clear carry bit	CLC	98	1	2
Set interrupt mask bit	SEI	9B	1	2
Clear interrupt mask bit	CLI	9A	1	2
Software interrupt	SWI	83	1	10
Return from subroutine	RTS	81	1	6
Return from interrupt	RTI	80	1	9
Reset stack pointer	RSP	9C	1	2
No-operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

Table 10-7 Instruction set

Mnemonic	Addressing modes										Condition codes				
	INH	IMM	DIR	EXT	REL	IX	IX1	IX2	BSC	BTB	H	I	N	Z	C
ADC											x	•	x	x	x
ADD											x	•	x	x	x
AND											•	•	x	x	•
ASL											•	•	x	x	x
ASR											•	•	x	x	x
BCC											•	•	•	•	•
BCLR											•	•	•	•	•
BCS											•	•	•	•	•
BEQ											•	•	•	•	•
BHCC											•	•	•	•	•
BHCS											•	•	•	•	•
BHI											•	•	•	•	•
BHS											•	•	•	•	•
BIH											•	•	•	•	•
BIL											•	•	•	•	•
BIT											•	•	x	x	•
BLO											•	•	•	•	•
BLS											•	•	•	•	•
BMC											•	•	•	•	•
BMI											•	•	•	•	•
BMS											•	•	•	•	•
BNE											•	•	•	•	•
BPL											•	•	•	•	•
BRA											•	•	•	•	•
BRN											•	•	•	•	•
BRCLR											•	•	•	•	x
BRSET											•	•	•	•	x
BSET											•	•	•	•	•
BSR											•	•	•	•	•
CLC											•	•	•	•	0
CLI											•	0	•	•	•
CLR											•	•	0	1	•
CMP											•	•	x	x	x

Address mode abbreviations

BSC	Bit set/clear	IMM	Immediate
BTB	Bit test & branch	IX	Indexed (no offset)
DIR	Direct	IX1	Indexed, 1 byte offset
EXT	Extended	IX2	Indexed, 2 byte offset
INH	Inherent	REL	Relative

(shaded) Not implemented

Condition code symbols

H	Half carry (from bit 3)	x	Tested and set if true, cleared otherwise
I	Interrupt mask	•	Not affected
N	Negate (sign bit)	?	Load CCR from stack
Z	Zero	0	Cleared
C	Carry/borrow	1	Set

Table 10-7 Instruction set (Continued)

Mnemonic	Addressing modes										Condition codes				
	INH	IMM	DIR	EXT	REL	IX	IX1	IX2	BSC	BTB	H	I	N	Z	C
COM											•	•	x	x	1
CPX											•	•	x	x	x
DEC											•	•	x	x	•
EOR											•	•	x	x	•
INC											•	•	x	x	•
JMP											•	•	•	•	•
JSR											•	•	•	•	•
LDA											•	•	x	x	•
LDX											•	•	x	x	•
LSL											•	•	x	x	x
LSR											•	•	0	x	x
MUL											0	•	•	•	0
NEG											•	•	x	x	x
NOP											•	•	•	•	•
ORA											•	•	x	x	•
ROL											•	•	x	x	x
ROR											•	•	x	x	x
RSP											•	•	•	•	•
RTI											?	?	?	?	?
RTS											•	•	•	•	•
SBC											•	•	x	x	x
SEC											•	•	•	•	1
SEI											•	1	•	•	•
STA											•	•	x	x	•
STOP											•	0	•	•	•
STX											•	•	x	x	•
SUB											•	•	x	x	x
SWI											•	1	•	•	•
TAX											•	•	•	•	•
TST											•	•	x	x	•
TXA											•	•	•	•	•
WAIT											•	0	•	•	•

Address mode abbreviations

BSC	Bit set/clear	IMM	Immediate
BTB	Bit test & branch	IX	Indexed (no offset)
DIR	Direct	IX1	Indexed, 1 byte offset
EXT	Extended	IX2	Indexed, 2 byte offset
INH	Inherent	REL	Relative

(shaded box) Not implemented

Condition code symbols

H	Half carry (from bit 3)	x	Tested and set if true, cleared otherwise
I	Interrupt mask	•	Not affected
N	Negate (sign bit)	?	Load CCR from stack
Z	Zero	0	Cleared
C	Carry/borrow	1	Set

Table 10-8 M68HC05 opcode map

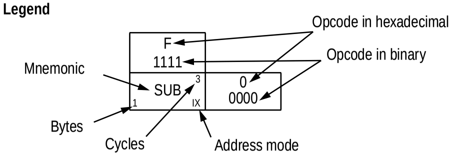
	Bit manipulation		Branch	Read/modify/write					Control		Register/memory						
	BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
Low \ High	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	High / Low
0 0000	BRSET0 5 / 3 BTB	BSET0 5 / 2 BSC	BRA 3 / 2 REL	NEG 5 / 2 DIR	NEGA 3 / 1 INH	NEGX 3 / 1 INH	NEG 6 / 2 IX1	NEG 5 / 1 IX	RTI 9 / 1 INH		SUB 2 / 2 IMM	SUB 3 / 2 DIR	SUB 4 / 3 EXT	SUB 5 / 3 IX2	SUB 4 / 2 IX1	SUB 3 / 1 IX	0 0000
1 0001	BRCLR0 5 / 3 BTB	BCLR0 5 / 2 BSC	BRN 3 / 2 REL						RTS 6 / 1 INH		CMP 2 / 2 IMM	CMP 3 / 2 DIR	CMP 4 / 3 EXT	CMP 5 / 3 IX2	CMP 4 / 2 IX1	CMP 3 / 1 IX	1 0001
2 0010	BRSET1 5 / 3 BTB	BSET1 5 / 2 BSC	BHI 3 / 2 REL		MUL 11 / 1 INH						SBC 2 / 2 IMM	SBC 3 / 2 DIR	SBC 4 / 3 EXT	SBC 5 / 3 IX2	SBC 4 / 2 IX1	SBC 3 / 1 IX	2 0010
3 0011	BRCLR1 5 / 3 BTB	BCLR1 5 / 2 BSC	BLS 3 / 2 REL	COM 5 / 2 DIR	COMA 3 / 1 INH	COMX 3 / 1 INH	COM 6 / 2 IX1	COM 5 / 1 IX	SWI 10 / 1 INH		CPX 2 / 2 IMM	CPX 3 / 2 DIR	CPX 4 / 3 EXT	CPX 5 / 3 IX2	CPX 4 / 2 IX1	CPX 3 / 1 IX	3 0011
4 0100	BRSET2 5 / 3 BTB	BSET2 5 / 2 BSC	BCC 3 / 2 REL	LSR 5 / 2 DIR	LSRA 3 / 1 INH	LSRX 3 / 1 INH	LSR 6 / 2 IX1	LSR 5 / 1 IX			AND 2 / 2 IMM	AND 3 / 2 DIR	AND 4 / 3 EXT	AND 5 / 3 IX2	AND 4 / 2 IX1	AND 3 / 1 IX	4 0100
5 0101	BRCLR2 5 / 3 BTB	BCLR2 5 / 2 BSC	BCS 3 / 2 REL								BIT 2 / 2 IMM	BIT 3 / 2 DIR	BIT 4 / 3 EXT	BIT 5 / 3 IX2	BIT 4 / 2 IX1	BIT 3 / 1 IX	5 0101
6 0110	BRSET3 5 / 3 BTB	BSET3 5 / 2 BSC	BNE 3 / 2 REL	ROR 5 / 2 DIR	RORA 3 / 1 INH	RORX 3 / 1 INH	ROR 6 / 2 IX1	ROR 5 / 1 IX			LDA 2 / 2 IMM	LDA 3 / 2 DIR	LDA 4 / 3 EXT	LDA 5 / 3 IX2	LDA 4 / 2 IX1	LDA 3 / 1 IX	6 0110
7 0111	BRCLR3 5 / 3 BTB	BCLR3 5 / 2 BSC	BEQ 3 / 2 REL	ASR 5 / 2 DIR	ASRA 3 / 1 INH	ASRX 3 / 1 INH	ASR 6 / 2 IX1	ASR 5 / 1 IX		TAX 2 / 1 INH		STA 4 / 2 DIR	STA 5 / 3 EXT	STA 6 / 3 IX2	STA 5 / 2 IX1	STA 4 / 1 IX	7 0111
8 1000	BRSET4 5 / 3 BTB	BSET4 5 / 2 BSC	BHCC 3 / 2 REL	LSL 5 / 2 DIR	LSLA 3 / 1 INH	LSLX 3 / 1 INH	LSL 6 / 2 IX1	LSL 5 / 1 IX		CLC 2 / 1 INH	EOR 2 / 2 IMM	EOR 3 / 2 DIR	EOR 4 / 3 EXT	EOR 5 / 3 IX2	EOR 4 / 2 IX1	EOR 3 / 1 IX	8 1000
9 1001	BRCLR4 5 / 3 BTB	BCLR4 5 / 2 BSC	BHCS 3 / 2 REL	ROL 5 / 2 DIR	ROLA 3 / 1 INH	ROLX 3 / 1 INH	ROL 6 / 2 IX1	ROL 5 / 1 IX		SEC 2 / 1 INH	ADC 2 / 2 IMM	ADC 3 / 2 DIR	ADC 4 / 3 EXT	ADC 5 / 3 IX2	ADC 4 / 2 IX1	ADC 3 / 1 IX	9 1001
A 1010	BRSET5 5 / 3 BTB	BSET5 5 / 2 BSC	BPL 3 / 2 REL	DEC 5 / 2 DIR	DECA 3 / 1 INH	DECX 3 / 1 INH	DEC 6 / 2 IX1	DEC 5 / 1 IX		CLI 2 / 1 INH	ORA 2 / 2 IMM	ORA 3 / 2 DIR	ORA 4 / 3 EXT	ORA 5 / 3 IX2	ORA 4 / 2 IX1	ORA 3 / 1 IX	A 1010
B 1011	BRCLR5 5 / 3 BTB	BCLR5 5 / 2 BSC	BMI 3 / 2 REL							SEI 2 / 1 INH	ADD 2 / 2 IMM	ADD 3 / 2 DIR	ADD 4 / 3 EXT	ADD 5 / 3 IX2	ADD 4 / 2 IX1	ADD 3 / 1 IX	B 1011
C 1100	BRSET6 5 / 3 BTB	BSET6 5 / 2 BSC	BMC 3 / 2 REL	INC 5 / 2 DIR	INCA 3 / 1 INH	INCX 3 / 1 INH	INC 6 / 2 IX1	INC 5 / 1 IX		RSP 2 / 1 INH		JMP 2 / 2 DIR	JMP 3 / 3 EXT	JMP 4 / 3 IX2	JMP 3 / 2 IX1	JMP 2 / 1 IX	C 1100
D 1101	BRCLR6 5 / 3 BTB	BCLR6 5 / 2 BSC	BMS 3 / 2 REL	TST 4 / 2 DIR	TSTA 3 / 1 INH	TSTX 3 / 1 INH	TST 5 / 2 IX1	TST 4 / 1 IX		NOP 2 / 1 INH	BSR 6 / 2 REL	JSR 5 / 2 DIR	JSR 6 / 3 EXT	JSR 7 / 3 IX2	JSR 6 / 2 IX1	JSR 5 / 1 IX	D 1101
E 1110	BRSET7 5 / 3 BTB	BSET7 5 / 2 BSC	BIL 3 / 2 REL						STOP 2 / 1 INH		LDX 2 / 2 IMM	LDX 3 / 2 DIR	LDX 4 / 3 EXT	LDX 5 / 3 IX2	LDX 4 / 2 IX1	LDX 3 / 1 IX	E 1110
F 1111	BRCLR7 5 / 3 BTB	BCLR7 5 / 2 BSC	BIH 3 / 2 REL	CLR 5 / 2 DIR	CLRA 3 / 1 INH	CLRX 3 / 1 INH	CLR 6 / 2 IX1	CLR 5 / 1 IX	WAIT 2 / 1 INH	TXA 2 / 1 INH		STX 4 / 2 DIR	STX 5 / 3 EXT	STX 6 / 3 IX2	STX 5 / 2 IX1	STX 4 / 1 IX	F 1111

Abbreviations for address modes and registers

BSC	Bit set/clear	IX	Indexed (no offset)
BTB	Bit test and branch	IX1	Indexed, 1 byte (8-bit) offset
DIR	Direct	IX2	Indexed, 2 byte (16-bit) offset
EXT	Extended	REL	Relative
INH	Inherent	A	Accumulator
IMM	Immediate	X	Index register

(shaded) Not implemented

Legend



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10.3.4 Extended

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode byte. Instructions with extended addressing mode are capable of referencing arguments anywhere in memory with a single three-byte instruction. When using the Freescale assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the short form of the instruction.

EA = (PC+1):(PC+2); PC ← PC+3
Address bus high ← (PC+1); Address bus low ← (PC+2)

10.3.5 Indexed, no offset

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. This addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

EA = X; PC ← PC+1
Address bus high ← 0; Address bus low ← X

10.3.6 Indexed, 8-bit offset

In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. Therefore the operand can be located anywhere within the lowest 511 memory locations. This addressing mode is useful for selecting the mth element in an n element table.

EA = X+(PC+1); PC ← PC+2
Address bus high ← K; Address bus low ← X+(PC+1)
where K = the carry from the addition of X and (PC+1)

10.3.7 Indexed, 16-bit offset

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This address mode can be used in a manner similar to indexed, 8-bit offset except that this three-byte instruction allows tables to be anywhere in memory. As with direct and extended addressing, the Freescale assembler determines the shortest form of indexed addressing.

EA = X+[(PC+1):(PC+2)]; PC ← PC+3
Address bus high ← (PC+1)+K; Address bus low ← X+(PC+2)
where K = the carry from the addition of X and (PC+2)

10.3.8 Relative

The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte (the offset) following the opcode are added to the PC if, and only if, the branch conditions are true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from –126 to +129 from the opcode address. The programmer need not calculate the offset when using the Freescale assembler, since it calculates the proper offset and checks to see that it is within the span of the branch.

EA = PC+2+(PC+1); PC ← EA if branch taken;
otherwise EA = PC ← PC+2

10.3.9 Bit set/clear

In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode. The byte following the opcode specifies the address of the byte in which the specified bit is to be set or cleared. Any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single two-byte instruction.

EA = (PC+1); PC ← PC+2
Address bus high ← 0; Address bus low ← (PC+1)

10.3.10 Bit test and branch

The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit to be tested and its condition (set or clear) is included in the opcode. The address of the byte to be tested is in the single byte immediately following the opcode byte (EA1). The signed relative 8-bit offset in the third byte (EA2) is added to the PC if the specified bit is set or cleared in the specified memory location. This single three-byte instruction allows the program to branch based on the condition of any readable bit in the first 256 locations of memory. The span of branch is from –125 to +130 from the opcode address. The state of the tested bit is also transferred to the carry bit of the condition code register.

EA1 = (PC+1); PC ← PC+2
Address bus high ← 0; Address bus low ← (PC+1)
EA2 = PC+3+(PC+2); PC ← EA2 if branch taken;
otherwise PC ← PC+3

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11
ELECTRICAL SPECIFICATIONS

This section contains the electrical specifications and associated timing information for the MC68HC05F12.

11.1 Maximum ratings

Table 11-1 Maximum ratings

Rating[1]	Symbol	Value	Unit
Supply voltage	V_{DD}	– 0.3 to + 0.7	V
Input voltage	V_{IN}	V_{SS} – 0.3 to V_{SS} + 0.3	V
Bootloader mode ($\overline{IRQ}$ pin only)	V_{IN}	V_{SS} – 0.3 to 2 x V_{DD} + 0.3	V
Current drain per pin[2] — excluding VDD and VSS	I	25	mA
Operating temperature range — standard —extended	T_A	T_L to T_H 0 to + 70 –40 to +85	°C
Storage temperature range	T_{STG}	– 65 to + 150	°C

(1) All voltages are with respect to V_{SS}.

(2) Maximum current drain per pin is for one pin at a time, limited by an external resistor.

Note: This device contains circuitry designed to protect against damage due to high electrostatic voltages or electric fields. However, it is recommended that normal precautions be taken to avoid the application of any voltages higher than those given in the Maximum Ratings table to this high impedance circuit. For maximum reliability all unused inputs should be tied to either V_{SS} or V_{DD}.

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11.2 Thermal characteristics and power considerations

Table 11-2 Package thermal characteristics

Characteristics	Symbol	Value	Unit
Thermal resistance — 100-pin QFP package — 80-pin QFP package	θ_{JA}	55	°C/W

The average chip junction temperature, T_J, in degrees Celsius can be obtained from the following equation:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where:

T_A = Ambient Temperature (°C)

θ_{JA} = Package Thermal Resistance,

Junction-to-ambient (°C/W)

$P_D = P_{INT} + P_{I/O}$ (W)

P_{INT} = Internal Chip Power = $I_{DD} \bullet V_{DD}$ (W)

$P_{I/O}$ = Power Dissipation on Input and Output pins (User determined)

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An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{T_J + 273}$$

Solving equations [1] and [2] for K gives:

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2$$

where K is a constant for a particular part. K can be determined by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained for any value of T_A by solving the above equations. The package thermal characteristics are shown in Table 11-2.

11.3 DC electrical characteristics

Table 11-3 DC electrical characteristics (V_{DD} = 5.0 V)

(V_{DD} = 5.0V_{DC} ± 10%, V_{SS} = 0 V_{DC}, T_A = –40 to +85°C, unless otherwise stated**)**

Characteristic	Symbol	Min.	Typ.[(1)]	Max.	Unit
Output voltage					
I_{LOAD} = –10 µA	V_{OH}	V_{DD} – 0.1	—	—	V
I_{LOAD} = +10 µA	V_{OL}	—	—	0.1	V
Output high voltage (I_{LOAD} = –0.8 mA) Ports (PA0–7, PB0–7, PC0–7, PH0–1)	V_{OH}	V_{DD} – 0.8	—	—	V
Output low voltage (I_{LOAD} = +1.6 mA) Ports(PA0–7, PB0–7, PC0–7, PH0–1)	V_{OL}	—	—	0.4	V
Input high voltage Ports (PD0–7, PE0–7)	V_{IH}	0.7V_{DD}	—	15.0	V
Input high voltage Ports (PA0–7, PB0–7, PC0–7, PG0–7) $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$,OSC1	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input low voltage Ports (PA0–7, PB0–7, PC0–7, PD0–7, PE0–7, PG0–7), $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, OSC1	V_{IL}	—	—	0.2V_{DD}	V
Supply Current[(2)]	I_{DD}				
RUN		—	2.5	5	mA
WAIT (DTMF disabled)		—	0.4	1.2	mA
WAIT (DTMF enabled)			0.8	1.2	mA
STOP		—	—	80	µA
I/O ports hi-Z leakage current Ports (PA0–7, PB0–7, PC0–7, PD0–7, PE0–7)	I_{OZ}	—	—	10	µA
Input current $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, OSC1	I_{IN}	—	—	1	µA
Capacitance					
Ports (as input or output)	C_{OUT}	—	—	12	pF
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$	C_{IN}	—	—	8	pF
Input current low Ports (PA0–7, PB0–7, PC0–7), $\overline{\text{RESET}}$	I_{IL}	–30	–90	–170	µA
LCD step down resistor	R_{LCDSD}	—	20	—	kΩ

(1) Typical values are at midpoint of voltage range and at 25 °C only.

(2) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs. RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 3.58 MHz); all inputs0.2V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2). WAIT I_{DD}: only the timer system active; current varies linearly with the OSC2 capacitance. STOP and WAIT I_{DD}: all ports configured as inputs, V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V. STOP I_{DD}: measured with OSC1 = V_{SS}.

Table 11-4 DC electrical characteristics (V_{DD} = 2.7 V)

(V_{DD} = 2.7 V_{DC}, V_{SS} = 0 V_{DC}, T_A = –40 to +85°C)

Characteristic	Symbol	Min.	Typ.[(1)]	Max.	Unit
Output Voltage I_{LOAD} = –10 µA I_{LOAD} = +10 µA	 V_{OH} V_{OL}	 V_{DD} – 0.1 —	 — —	 — 0.1	 V V
Output High Voltage (I_{LOAD} = –0.2 mA) Ports (PA0–7, PB0–7, PC0–7, PH0–7, PI0–7)	V_{OH}	V_{DD} – 0.3	—	—	V
Output Low Voltage (I_{LOAD} = +0.4 mA) Ports(PA0–7, PB0–7, PC0–7, PD0–7, PE0–7, PH0–1)	V_{OL}	—	—	0.3	V
Input high voltage Ports (PD0–7, PE0–7)	V_{IH}	0.7V_{DD}	—	15.0	V
Input high voltage Ports (PA0–7, PB0–7, PC0–7, PG0–7) $\overline{\mathrm{IRQ}}$, $\overline{\mathrm{RESET}}$,OSC1	V_{IH}	0.7V_{DD}	—	V_{DD}	V
Input Low Voltage Ports (PA0–7, PB0–7, PC0–7, PD0–7, PE0–7, PG0–7) OSC1, $\overline{\mathrm{IRQ}}$, $\overline{\mathrm{RESET}}$	V_{IL}	—	—	0.2V_{DD}	V
Supply Current[(2)]: f_{OSC} = 3.579 MHz, f_{OP} = 1.789 MHz RUN WAIT (DTMF disabled) WAIT (DTMF enabled) STOP	I_{DD}	 — — — —	 1.5 0.2 0.5 —	 3.0 1.0 1.0 40	 mA mA µA µA
I/O ports hi-Z leakage current Ports (PA0–7, PB0–7, PC0–7, PD0–7, PE0–7)	I_{OZ}	—	—	10	µA
Input current $\overline{\mathrm{RESET}}$, $\overline{\mathrm{IRQ}}$, OSC1	I_{IN}	—	—	1	µA
Capacitance Ports (as input or output) $\overline{\mathrm{RESET}}$, $\overline{\mathrm{IRQ}}$	 C_{OUT} C_{IN}	 — —	 — —	 12 8	 pF pF
Input current low Ports (PA0–7, PB0–7, PC0–7), $\overline{\mathrm{RESET}}$	I_{IL}	–5	–15	–40	µA
LCD step down resistor	R_{LCDSD}	—	20	—	kΩ

(1) Typical values are at midpoint of voltage range and at 25 °C only.

(2) All I_{DD} measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs. RUN and WAIT I_{DD}: measured using an external square-wave clock source (f_{OSC} = 3.58 MHz); all inputs0.2V from rail; no DC loads; maximum load on outputs 50pF (20pF on OSC2). WAIT I_{DD}: only the timer system active; current varies linearly with the OSC2 capacitance. STOP and WAIT I_{DD}: all ports configured as inputs, V_{IL} = 0.2 V, V_{IH} = V_{DD} – 0.2 V. STOP I_{DD}: measured with OSC1 = V_{SS}.

11.4 Control timing

Table 11-5 Control timing (V_{DD} = 5V)

(V_{DD} = 5.0 V_{DC} ± 10%, V_{SS} = 0 V_{DC}, T_A = T_L to T_H)

Characteristic	Symbol	Min.	Max.	Unit
Frequency of operation: Crystal External clock	f_{OSC}	— DC	3.579 3.579	MHz
Internal operating frequency: Crystal External clock	f_{OP}	— DC	1.789 1.789	MHz
Processor cycle time	t_{CYC}	550.0	—	ns
Stop recovery start-up time	t_{ILCH}	—	20	ms
Crystal oscillator start-up time	t_{OXOV}	—	20.0	ms
$\overline{\text{RESET}}$ pulse width	t_{RL}	1.5	—	t_{CYC}
Interrupt pulse width low (edge-triggered)	t_{ILIH}	250.0	—	ns
Interrupt pulse period	t_{ILIL}	(1)	—	t_{CYC}
OSC1 pulse width	t_{OH}, t_{OL}	100.0	—	ns
EEPROM byte programming time	t_{EPGM}	—	15.0	ms
EEPROM byte erase time	t_{EBYTE}	—	15.0	ms
EEPROM block erase time	t_{EBLOCK}	—	100.0	ms
EEPROM bulk erase time	t_{EBULK}	—	300.0	ms
EEPROM programming voltage fall time	t_{FPV}	—	10.0	µs
EEPROM minimum programming voltage	V_{CCMIN}	2.7		V

(1) The minimum period T_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

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Table 11-6 Control timing (V_{DD} = 2.7V)

(V_{DD} = 2.7 V_{DC}, V_{SS} = 0 V_{DC}, T_A = T_L to T_H)

Characteristic	Symbol	Min.	Max.	Unit
Frequency of operation: Crystal External clock	 f_{OSC} f_{OSC}	 — DC	 3.579 3.579	 MHz MHz
Internal operating frequency: Crystal External clock	 f_{OP} f_{OP}	 — DC	 1.789 1.789	 MHz MHz
Processor cycle time	t_{CYC}	550.0	—	ns
Crystal oscillator start-up time	t_{OXOV}	—	20.0	ms
Stop recovery start-up time	t_{ILCH}	—	20	ms
$\overline{\text{RESET}}$ pulse width	t_{RL}	1.5	—	TCYC
Interrupt pulse width low (edge-triggered)	t_{ILIH}	250.0	—	ns
Interrupt pulse period	t_{ILIL}	(1)	—	t_{CYC}
OSC1 pulse width	TOH, TOL	100.0	—	ns
EEPROM Byte Programming time	t_{EPGM}	—	15.0	ms
EEPROM Byte Erase time	t_{EBYTE}	—	15.0	ms
EEPROM Block Erase time	t_{EBLOCK}	—	100.0	ms
EEPROM Bulk Erase time	t_{EBULK}	—	300.0	ms
EEPROM Programming Voltage fall time	t_{FPV}	—	10.0	µs
EEPROM minimum programming voltage	V_{CCMIN}	2.7		V

(1) The minimum period T_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

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11.5 DC levels for low voltage $\overline{RESET}$ and LVI

Table 11-7 DC levels for low voltage reset and LVI

(TA = 0C to 70°C, unless otherwise stated)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Power-on reset voltage	V_{RON}	2.55	2.8	3.05	V
Power-off reset voltage	V_{ROFF}	2.45	2.7	2.95	V
Low voltage interrupt	V_{LVI}	2.75	3.0	3.25	V

11.6 Electrical specifications for DTMF/melody generator

Table 11-8 Sine wave tones at TNO

Characteristic	Min.	Typ.	Max.	Unit
Operating voltage	2.7	—	5.5	V
Tone output level: Low group – row High group – column	 0.120 0.160	 0.160 0.205	 0.210 0.280	 V_{rms} V_{rms}
Frequency deviation (DTMF)	– 0.65		+ 0.65	%
Frequency deviation (Melody)	– 1.5		+ 1.5	%
Tone output DC level	0.45	0.50	0.55	Vdd
High group pre-emphasis	1	2.15	3	dB
Total harmonic distortion	—	–25	—	dB

Table 11-9 Square wave tones at TNO

Characteristic	Min.	Typ.	Max.	Unit
Operating voltage	2.7	—	5.5	V
Tone output level: Low group – row High group – column	 — —	 0.270 0.360		 V_{p-p} V_{p-p}
Frequency deviation (Melody)	– 1.5		+ 1.5	%
Tone output DC level (+ 1/2 V_{p-p} value)	0.45	0.50	0.55	Vdd

Table 11-10 TONEX at TNX output

Characteristic	Min.	Typ.	Max.	Unit
Operating voltage	2.7	—	5.5	V
Tone output level (square wave)		V_{DD}		V_{p-p}
Frequency deviation	– 1.5		+ 1.5	%

11.7 EEPROM additional information

Table 11-11 EEPROM additional information

Temperature	Read/write cycles	Remarks
0 °C – 85 °C	10 000	The value is regularly tested and monitored
50 °C	35 000	This value is predicted from the tested ones
25 °C	100 000	This value is predicted from the tested ones

11

12
MECHANICAL DATA

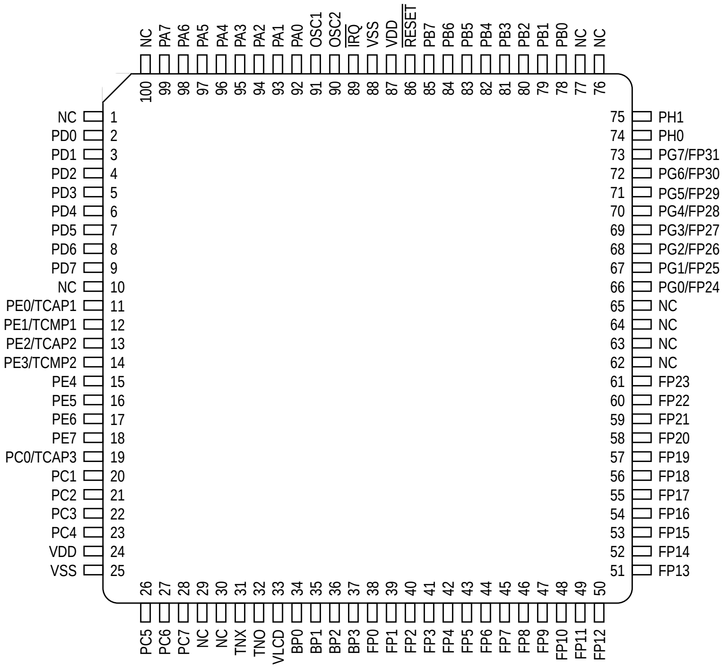
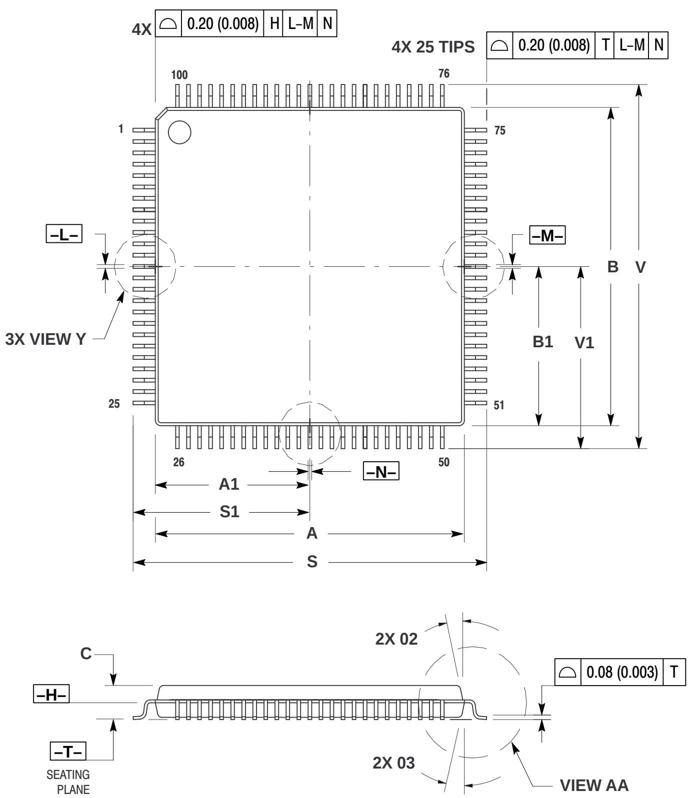


Figure 12-1 100-pin QFP pinout for the MC68HC05F12

12

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.100) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350 (0.014). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.070 (0.003).



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00 BSC		0.551 BSC	
A1	7.00 BSC		0.276 BSC	
B	14.00 BSC		0.551 BSC	
B1	7.00 BSC		0.276 BSC	
C	—	1.60	—	0.063
C1	0.05	0.15	0.002	0.006
C2	1.35	1.45	0.053	0.057
D	0.17	0.27	0.007	0.011
E	0.45	0.75	0.018	0.030
F	0.17	0.23	0.007	0.009
G	0.50 BSC		0.20 BSC	
J	0.09	0.20	0.004	0.008
K	0.50 REF		0.020 REF	
R1	0.10	0.20	0.004	0.008
S	16.00 BSC		0.630 BSC	
S1	8.00 BSC		0.315 BSC	
U	0.09	0.16	0.004	0.006
V	16.00 BSC		0.630 BSC	
V1	8.00 BSC		0.315 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12°		12°	
θ3	5°	13°	5°	13°

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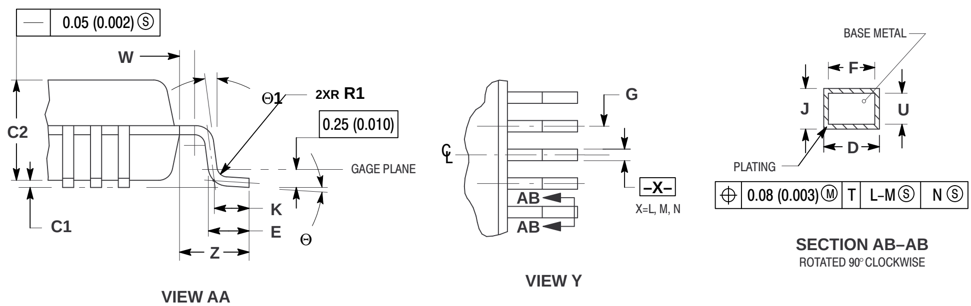

CASE 983-01

Figure 12-2 100-pin QFP mechanical dimensions

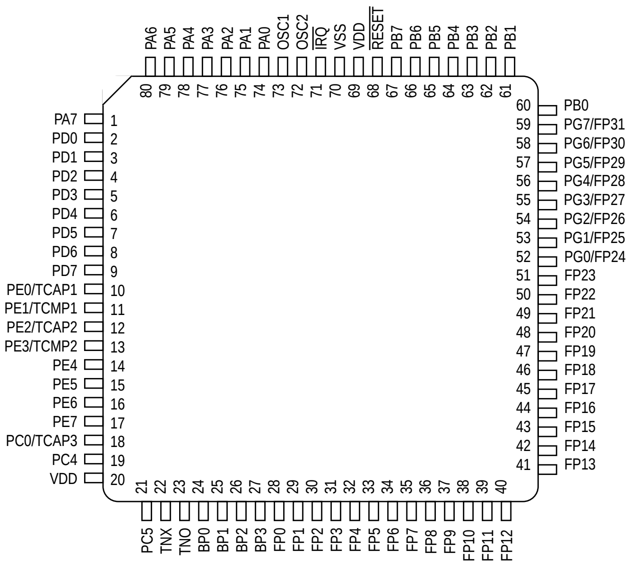

Figure 12-3 80-pin QFP pinout

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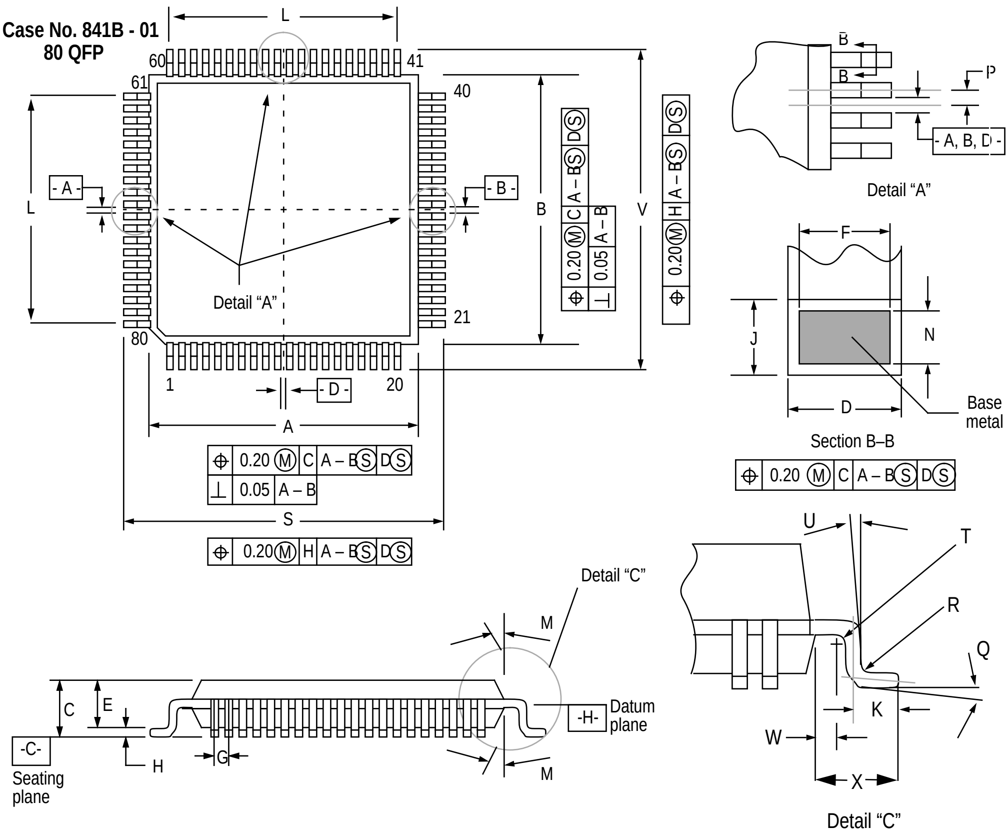

Dim.	Min.	Max.
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	—	0.250
J	0.130	0.230
K	0.65	0.95
L	12.35 REF	

Notes

1. Datum plane –H– is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
2. Datums A–B and –D to be determined at datum plane –H–.
3. Dimensions S and V to be determined at seating plane –C–.
4. Dimensions A and B do not include mould protrusion. Allowable mould protrusion is 0.25 mm per side. Dimensions A and B do include mould mismatch and are determined at datum plane –H–.
5. Dimension D does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 total in excess of the D dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
6. Dimensions and tolerancing per ANSI Y 14.5M, 1982.
7. All dimensions in mm.

Dim.	Min.	Max.
M	5	10
N	0.130	0.170
Q	0	7
R	0.13	0.30
S	16.95	17.45
T	0.13	—
U	0	—
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure 12-4 80-pin QFP mechanical dimensions

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ORDERING INFORMATION

This section describes the information needed to order the MC68HC05F12.

To initiate a ROM pattern for the MCU, it is necessary to first contact your local field service office, local sales person or Freescale representative. Please note that you will need to supply details such as: mask option selections; temperature range; oscillator frequency; package type; electrical test requirements; and device marking details so that an order can be processed, and a customer specific part number allocated. Refer to Table 13-1 for appropriate part numbers.

Table 13-1 MC order numbers

Device title	Package type	Temperature	Part number
MC68HC05F12	100-pin QFP	0 to 70 C	MC68HC05F12PU
	80-pin QFP		MC68HC05F12FU

13.1 EPROMs

For the MC68HC05F12, a 32K byte EPROM programmed with the customer's software (positive logic for address and data) should be submitted for pattern generation. All unused bytes should be programmed to $00.

The EPROM should be clearly labelled, placed in a conductive IC carrier and securely packed.

13.2 Verification media

All original pattern media (EPROMs) are filed for contractual purposes and are not returned. A computer listing of the ROM code will be generated and returned with a listing verification form. The listing should be thoroughly checked and the verification form completed, signed and returned to Freescale. The signed verification form constitutes the contractual agreement for creation of the custom mask. If desired, Freescale will program blank EPROMs (supplied by the customer) from the data file used to create the custom mask, to aid in the verification process.

13.3 ROM verification units(RVU)

Ten MCUs containing the customer's ROM pattern will be provided for program verification. These units will have been made using the custom mask but are for ROM verification only. For expediency, they are usually unmarked and are tested only at room temperature (25 C) and at 5 Volts. These RVUs are included in the mask charge and are not production parts. They are neither backed nor guaranteed by Freescale Quality Assurance.

INDEX

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SECTION 3 MEMORY AND REGISTERS	☐	☐	☐	☐	☐
SECTION 4 PARALLEL INPUT/OUTPUT PORTS	☐	☐	☐	☐	☐
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SECTION 6 16-BIT PROGRAMMABLE TIMER	☐	☐	☐	☐	☐
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