MC68HC05T16

HC05

TECHNICAL DATA

MC68HC05T16
MC68HC705T16

TECHNICAL
DATA

MOTOROLA

MOTOROLA

MC68HC05T16
MC68HC705T16

High-density complementary metal oxide semiconductor (HCMOS) microcontroller unit

All Trade Marks recognized. This document contains information on new products. Specifications and information herein are subject to change without notice.

Conventions

Register and bit mnemonics are defined in the paragraphs describing them.

An overbar is used to designate an active-low signal, eg: $\overline{\text{RESET}}$.

Unless otherwise stated, blank cells in a register diagram indicate that the bit is either unused or reserved; shaded cells indicate that the bit is not described in the following paragraphs; ‘u’ is used to indicate an undefined state (on reset).

CUSTOMER FEEDBACK QUESTIONNAIRE (MC68HC05T16D/H)

Motorola wishes to continue to improve the quality of its documentation. We would welcome your feedback on the publication you have just received. Having used the document, please complete this card (or a photocopy of it, if you prefer).

1. How would you rate the quality of the document? Check one box in each category.

	Excellent			Poor		Excellent			Poor
Organization	☐	☐	☐	☐	Tables	☐	☐	☐	☐
Readability	☐	☐	☐	☐	Table of contents	☐	☐	☐	☐
Understandability	☐	☐	☐	☐	Index	☐	☐	☐	☐
Accuracy	☐	☐	☐	☐	Page size/binding	☐	☐	☐	☐
Illustrations	☐	☐	☐	☐	Overall impression	☐	☐	☐	☐

Comments: _____

2. What is your intended use for this document? If more than one option applies, please rank them (1, 2, 3).

Selection of device for new application ☐
System design ☐
Training purposes ☐
Other ☐ Please specify: _____

3. How well does this manual enable you to perform the task(s) outlined in question 2?

Completely ☐ ☐ ☐ ☐ Not at all

Comments: _____

4. How easy is it to find the information you are looking for?

Easy ☐ ☐ ☐ ☐ Difficult

Comments: _____

5. Is the level of technical detail in the following sections sufficient to allow you to understand how the device functions?

		Too little detail				Too much detail
SECTION 1	GENERAL DESCRIPTION	☐	☐	☐	☐	☐
SECTION 2	PIN DESCRIPTIONS AND INPUT/OUTPUT PORTS	☐	☐	☐	☐	☐
SECTION 3	MEMORY AND REGISTERS	☐	☐	☐	☐	☐
SECTION 4	RESETS AND INTERRUPTS	☐	☐	☐	☐	☐
SECTION 5	TIMERS	☐	☐	☐	☐	☐
SECTION 6	M-BUS SERIAL INTERFACE	☐	☐	☐	☐	☐
SECTION 7	PULSE ACCUMULATIOR	☐	☐	☐	☐	☐
SECTION 8	PULSE WIDTH MODULATION	☐	☐	☐	☐	☐
SECTION 9	ON-SCREEN DISPLAY	☐	☐	☐	☐	☐
SECTION 10	ANALOG TO DIGITAL CONVERTER	☐	☐	☐	☐	☐
SECTION 11	CPU CORE AND INSTRUCTION SET	☐	☐	☐	☐	☐
SECTION 12	LOW POWER MODES	☐	☐	☐	☐	☐
SECTION 13	OPERATING MODES	☐	☐	☐	☐	☐
SECTION 14	ELECTRICAL SPECIFICATIONS	☐	☐	☐	☐	☐
SECTION 15	MECHANICAL SPECIFICATIONS	☐	☐	☐	☐	☐

Comments: _____

6. Have you found any errors? If so, please comment: _____

7. From your point of view, is anything missing from the document? If so, please say what: _____

– *Cut along this line to remove* –

8. How could we improve this document? _____

_____

_____

9. How would you rate Motorola's documentation?

	Excellent			Poor
– In general	☐	☐	☐	☐
– Against other semiconductor suppliers	☐	☐	☐	☐

10. Which semiconductor manufacturer provides the best technical documentation? _____

11. Which company (in any field) provides the best technical documentation? _____

12. How many years have you worked with microprocessors?

Less than 1 year ☐ 1–3 years ☐ 3–5 years ☐ More than 5 years ☐

– Second fold back along this line –

By air mail
Par avion

FIX STAMP HERE

– First fold back along this line –

– Cut along this line to remove –

Motorola Semiconductors H.K. Ltd.,
13/F, Prosperity Centre,
77-81 Container Port Road,
Kwai Chung, N.T.,
HONG KONG.

F.A.O. HKG CSIC Technical Publications
(re: MC68HC05T16D/H)

FAX: (852) 2485-0548

MOTOROLA
Semiconductor Products Sector
Asia Pacific Group

– Third fold back along this line –

13. Currently there is some discussion in the semiconductor industry regarding a move towards providing data sheets in electronic form. If you have any opinion on this subject, please comment. _____

_____

14. We would be grateful if you would supply the following information (at your discretion), or attach your card.

Name: _____ Phone No: _____

Position: _____ FAX No: _____

Department: _____

Company: _____

Address: _____

_____

Thank you for helping us improve our documentation,
HKG CSIC Technical Publications , Motorola Semiconductors H.K. Ltd., Hong Kong.

– Finally, tuck this edge into opposite flap –

TABLE OF CONTENTS

5
TIMERS

6
M-BUS SERIAL INTERFACE

7
PULSE ACCUMULATOR

8
PULSE WIDTH MODULATOR

9
ON-SCREEN DISPLAY

10
ANALOG TO DIGITAL CONVERTER

11
CPU CORE AND INSTRUCTION SET

12
LOW POWER MODES

13
OPERATING MODES

14
ELECTRICAL SPECIFICATIONS

15
MECHANICAL SPECIFICATIONS

THIS PAGE LEFT BLANK INTENTIONALLY

LIST OF FIGURES

THIS PAGE LEFT BLANK INTENTIONALLY

LIST OF TABLES

THIS PAGE LEFT BLANK INTENTIONALLY

1
GENERAL DESCRIPTION

The MC68HC05T16 HCMOS microcontroller is a member of the M68HC05 Family of low-cost single-chip microcontrollers. This 8-bit microcontroller unit (MCU) contains on-chip oscillator, CPU, RAM, ROM, OSD, M-Bus, PWM, PAC, Timer, A/D converter, I/O and Watchdog Timer.

The MC68HC705T16 is an EPROM version of the MC68HC05T16; it is available in windowed and OTP 56-pin SDIP packages. All references to the MC68HC05T16 apply equally to the MC68HC705T16, unless otherwise stated. *References specific to the MC68HC705T16 are italicized in the text.*

1.1 Features

- 8-bit architecture
- Power saving Stop, Wait modes
- 320 bytes of on-chip RAM (64 bytes for stack)
- 24064 bytes of on-chip ROM/*EPROM*
- PLL-based, 4-row-buffer On Screen Display (OSD)
- 128-character (4K bytes) OSD ROM/*EPROM*
- 16-character (512 bytes) dual ported OSD RAM; both readable and writable by CPU
- 40 bidirectional I/O lines: 24 dedicated and 16 multiplexed I/O lines; 12 of the 24 dedicated I/Os and 10 of the 16 multiplexed I/Os are of +12V open-drain type
- Multi-master M-Bus (I^2C†) interface system
- Timer with TCAP input pin and 2 output compare functions
- Pulse Accumulator (PAC)
- 9 channel 7-bit PWM, and single channel 14-bit PWM
- 2 channel 5-bit Analog to Digital Converter
- COP watchdog system
- Available in 56-pin SDIP package

† I^2C-bus is a proprietary Philips interface bus

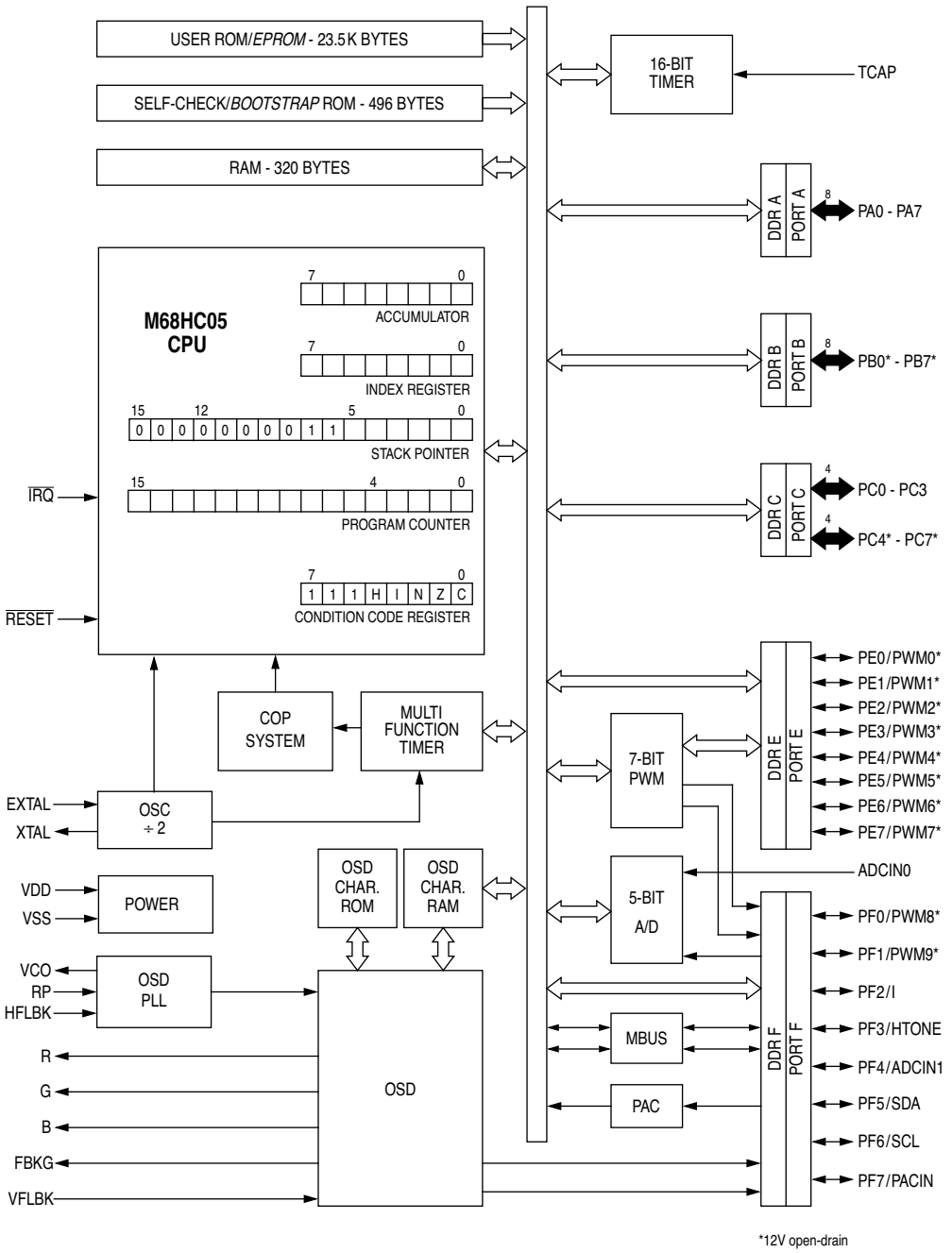


Figure 1-1 MC68HC05T16/*MC68HC705T16* Block Diagram

2
PIN DESCRIPTIONS AND INPUT/OUTPUT PORTS

This section provides a description of the functional pins and I/O programming of the MC68HC05T16/*MC68HC705T16* microcontroller.

2.1 PIN DESCRIPTIONS

PIN NAME	56-pin SDIP PIN No.	DESCRIPTION
VDD, VSS	41, 44	Power is supplied to the MCU using these two pins. VDD is power and VSS is ground.
$\overline{IRQ}$/VPP	38	In the user mode this pin is an external hardware interrupt $\overline{IRQ}$. It is software programmable to provide two choices of interrupt triggering sensitivity. These options are: 1) negative edge-sensitive triggering only, or 2) both negative edge-sensitive and level sensitive triggering. *In the bootstrap mode on the MC68HC705T16, this is the EPROM programming voltage input pin.*
$\overline{RESET}$	53	The active low $\overline{RESET}$ input is not required for start-up, but can be used to reset the MCU internal state and provide an orderly software start-up procedure.
TCAP	15	The TCAP input controls the input capture feature for the on-chip programmable free-running timer.
EXTAL, XTAL	51, 52	These pins provide connections to the on-chip oscillator. The maximum crystal frequency is 4.2 MHz. EXTAL may be driven by an external oscillator if an external crystal circuit is not used.
PA0-PA7	31-24	These eight I/O lines comprise port A. The state of any pin is software programmable. All port A lines are configured as input during power on or external reset.
PB0-PB7	16-23	These eight I/O lines comprise port B. The state of any pin is software programmable. All port B lines are configured as input during power on or external reset. These pins are +12V open-drain pins.

PIN NAME	56-pin SDIP PIN No.	DESCRIPTION
PC0-PC7	40, 39, 37-32	These eight I/O lines comprise port C. The state of any pin is software programmable. All port C lines are configured as input during power on or external reset. PC0-3 are push-pull type pins, and PC4-7 are +12V open-drain pins.
PE0/PWM0 to PE7/PWM7	54, 55,56, 1 2, 3, 4, 5	These eight I/O lines comprise port E. The state of any pin is software programmable. All port E lines are configured as input during power on or external reset. These pins become PWM outputs by setting the appropriate bits in the port E Configuration register ($0C). See Section 2.2.2.
PF0-PF7	6-13	These eight I/O lines comprise port F. The state of any pin is software programmable. All port F lines are configured as input during power on or external reset. Other functions are also shared with these pins, and is selected by setting the appropriate bits in the port F Configuration register ($0D). See Section 2.2.2.
PWM8, PWM9	6, 7	PWM channels. These pins are shared with port pins PF0 and PF1, and are selected by setting port F Configuration register ($0D) bits 0 and 1 respectively.
I, TONE	8. 9	The I pin of the OSD module expands the color selection range by providing an intensity bit. The HTONE pin is mainly used for creating transparent background effect when the background of a character window overlaps the original TV picture display. These pins are shared with port pins PF2 and PF3.Selection is by the port F Configuration register ($0D) bits 2 and 3 respectively.
ADCIN0, ADCIN1	14, 10	These are the two input channels to the analog to digital converter. ADCIN1 pin is shared with port PF4, and is selected by setting the port F Configuration register ($0D) bit 4.
SDA, SCL	11, 12	These two pins are the M-Bus interface pins. SDA is the data line, and SCL is the clock line. These pins are shared with port pins PF5 and PF6 respectively. Selection is by the port F Configuration register ($0D) bits 5 and 6.
PACIN	13	This is the clock/control input to the pulse accumulator. This pin is shared with port pin PF7. Selection is by the port F Configuration register ($0D) bit 7.
R, G, B	50, 49, 48	These are the output pins for OSD R, G, and B videos.
FBKG	47	This is the OSD output pin for blanking out the original TV picture display so that OSD data can be displayed on the TV screen.
HFBLK, VFBLK	45, 46	These are the OSD input pins for horizontal and vertical flyback signals from the TV set chassis. They are used for synchronizing OSD signals with TV display.
VCO	43	This OSD pin is the phase detector output pin. With a low-pass filter this pin controls the frequency of the internal OSD VCO.
RP	42	This is an input pin for biasing the internal OSD VCO.

2.1.1 Pin Assignments

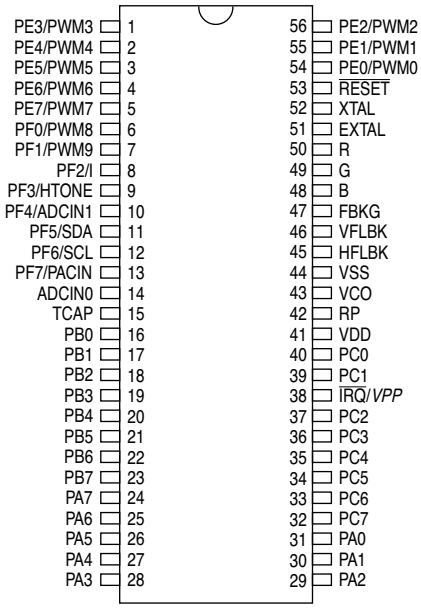


Figure 2-1 Pin Assignments for 56-pin SDIP package

2.2 INPUT/OUTPUT PORTS

2.2.1 Input/Output Programming

Port A, B, C, E, and F may be programmed as an input or an output under software control. The direction of the pins is determined by the state of corresponding bit in the port data direction register (DDR). Each 8-bit port has an associated 8-bit data direction register. Any port A, B, C, E, or F pin is configured as an output if its corresponding DDR bit is set to a logic one. A pin is configured as an input if its corresponding DDR bit is cleared to a logic zero. At power-on or reset, all DDRs are cleared, which configure all port A, B, C, E and F pins as inputs. The data direction registers are capable of being written to or read by the processor. Refer to Figure 2-2 and Table 2-1. During the programmed output state, a read of the data register actually reads the value of the output data latch and not the I/O pin.

Table 2-1 I/O Pin Functions

R/$\overline{W}$	DDR	I/O Pin Function
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

2.2.2 Port E and F Configuration Registers

Port E and F are shared with PWM, PAC, OSD, MBUS, and ADC. The configuration registers, at $0C and $0D, are used to configure these I/O pins. The default state after a reset or POR is zero. Setting the corresponding bits will enable the corresponding functions. For example, setting the SDA and SCL bits will configure PF5 and PF6 as MBUS interface pins, regardless of the settings in the port F Data Direction register.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port E Configuration Register	$0C	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0	0000 0000

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port F Configuration Register	$0D	PAC	SCL	SDA	ADC1	HTONE	I	PWM9	PWM8	0000 0000

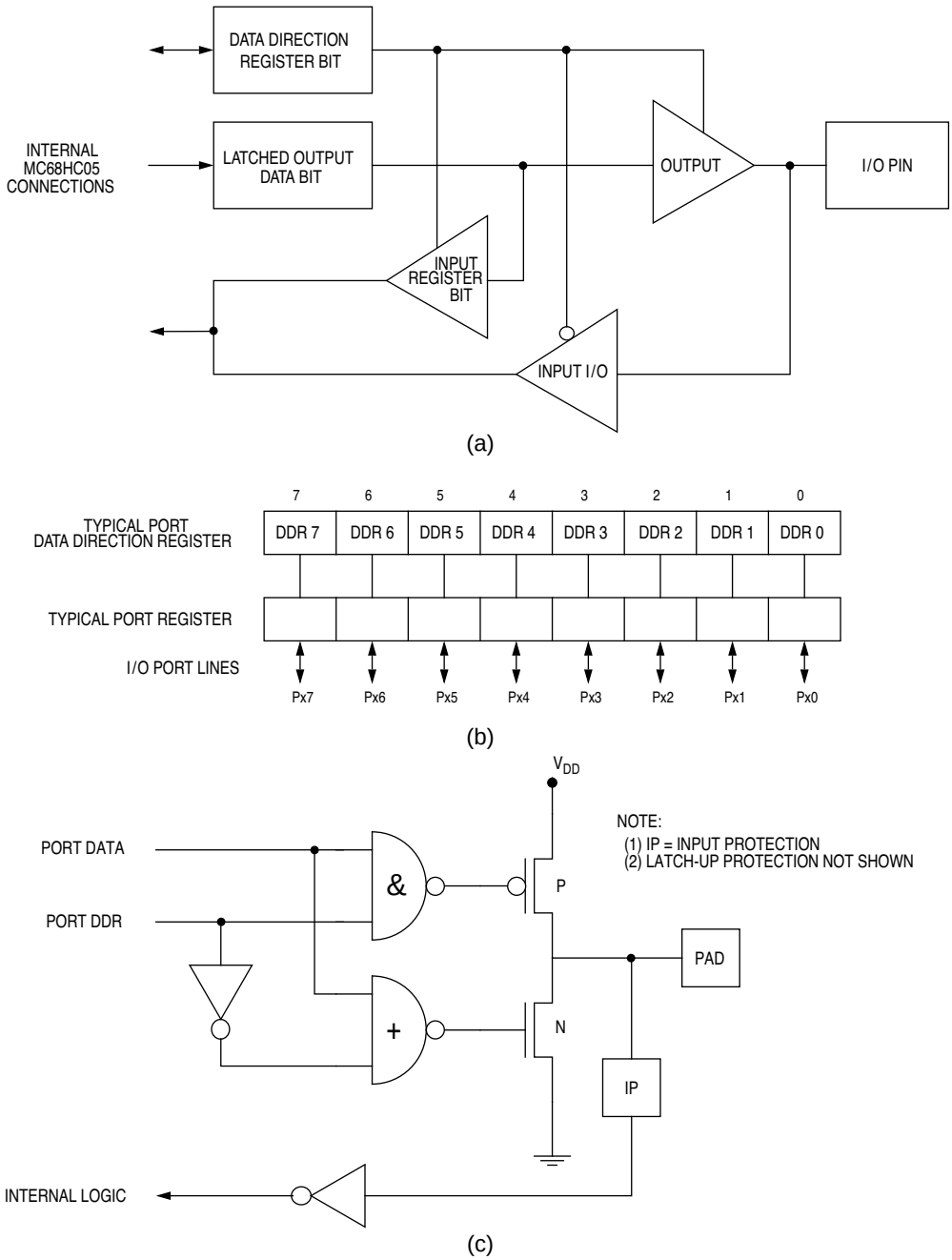


Figure 2-2 Parallel Port I/O Circuitry

THIS PAGE LEFT BLANK INTENTIONALLY

3
MEMORY AND REGISTERS

This section describes the organization of the on-chip memory.

3.1 Memory Map

The CPU can address 64K-bytes of memory space. The ROM portion of memory holds the program instructions, fixed data, user-defined vectors, and interrupt service routines. The RAM portion of memory holds variable data. I/O registers are memory-mapped so that the CPU can access their locations in the same way that it accesses all other memory locations. Figure 3-1 shows the Memory Map for the MC68HC05T16/*MC68HC705T16*.

3.2 Input/Output Section

The first 64 addresses of memory space, $0000-$003F, are the I/O section. These are the addresses of the I/O control registers, status registers, and data registers. Table 3-1 shows these registers and their respective bits.

3.3 RAM

The 320 addresses from $0050-$018F are RAM locations. The CPU uses the 64 RAM addresses, $00C0-$00FF, as the stack. Before processing an interrupt, the CPU uses five bytes of the stack to save the contents of the CPU registers. During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements during pushes and increments during pulls.

Note: Be careful when using nested subroutines or multiple interrupt levels. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation. Once the stack pointer passes $00C0, it wraps round back to $00FF.

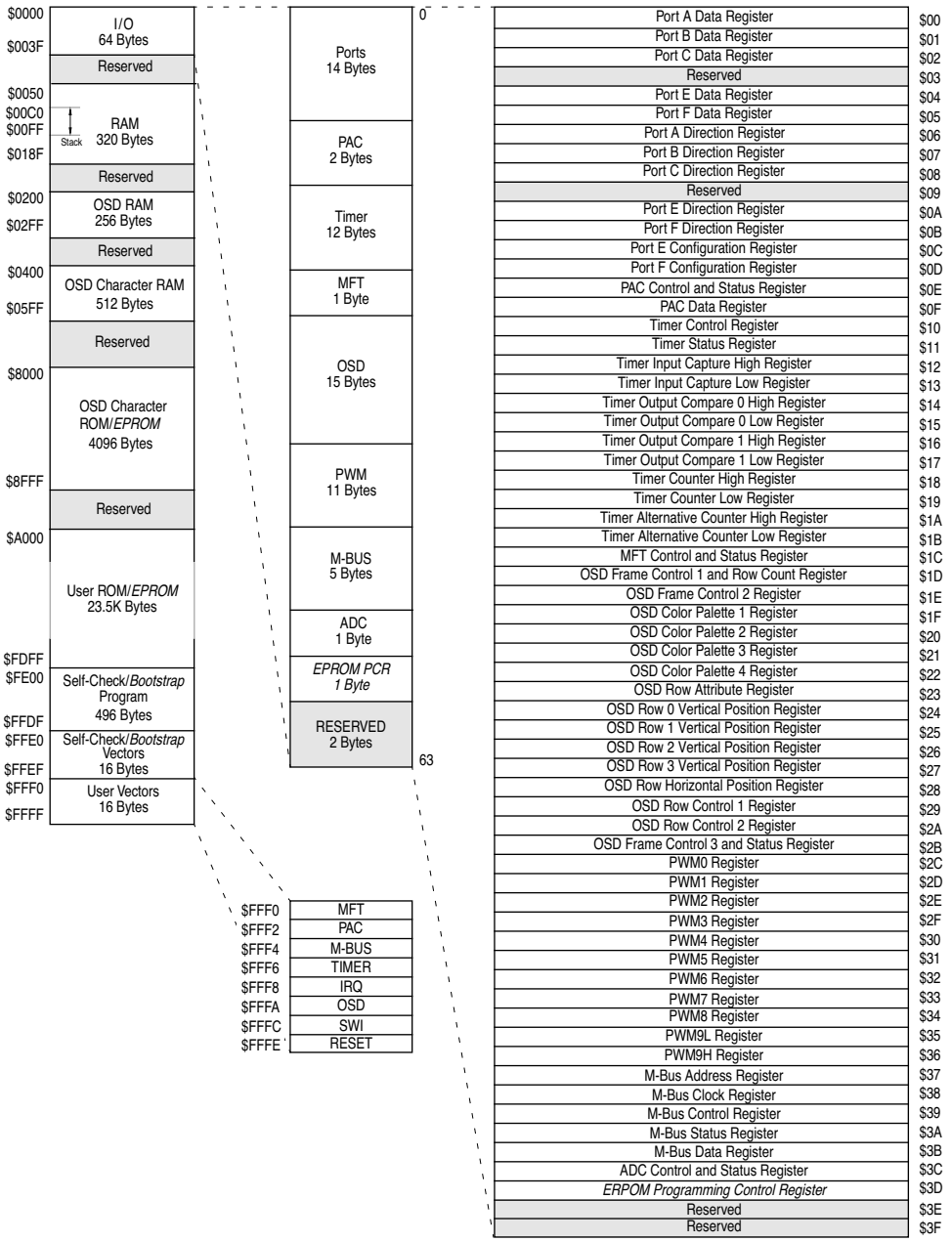


Figure 3-1 MC68HC05T16/*MC68HC705T16* Memory Map

Table 3-1 MC68HC05T16/*MC68HC705T16* Registers

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00	Port A data	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$01	Part B data	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$02	Port C data	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$03	Reserved								
$04	Port E data	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$05	Port F data	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$06	Port A data direction	DDR7	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0
$07	Port B data direction	DDR7	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0
$08	Port C data direction	DDR7	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0
$09	Reserved								
$0A	Port E data direction	DDR7	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0
$0B	Port F data direction	DDR7	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0
$0C	Port E configuration	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
$0D	Port F configuration	PAC	SCL	SDA	ADC1	HTONE	I	PWM9	PWM8
$0E	PAC control and status	PAOF	PAEN	PAMOD	PAIE				
$0F	PAC data	PAD7	PAD6	PAD5	PAD4	PAD3	PAD2	PAD1	PAD0
$10	Timer control	ICIE	OC0IE	OC1IE	TOVFIE			IEDG	
$11	Timer status	ICF	OC0F	OC1F	TOF	TCAPS			
$12	Timer input capture high	CAP7H	CAP6H	CAP5H	CAP4H	CAP3H	CAP2H	CAP1H	CAP0H
$13	Timer input capture low	CAP7L	CAP6L	CAP5L	CAP4L	CAP3L	CAP2L	CAP1L	CAP0L
$14	Timer output compare 0 high	0CMP7H	0CMP6H	0CMP5H	0CMP4H	0CMP3H	0CMP2H	0CMP1H	0CMP0H
$15	Timer output compare 0 low	0CMP7L	0CMP6L	0CMP5L	0CMP4L	0CMP3L	0CMP2L	0CMP1L	0CMP0L
$16	Timer output compare 1 high	1CMP7H	1CMP6H	1CMP5H	1CMP4H	1CMP3H	1CMP2H	1CMP1H	1CMP0H
$17	Timer output compare 1 low	1CMP7L	1CMP6L	1CMP5L	1CMP4L	1CMP3L	1CMP2L	1CMP1L	1CMP0L
$18	Timer counter high	CNT7H	CNT6H	CNT5H	CNT4H	CNT3H	CNT2H	CNT1H	CNT0H
$19	Timer counter low	CNT7L	CNT6L	CNT5L	CNT4L	CNT3L	CNT2L	CNT1L	CNT0L
$1A	Timer alternate counter high	ACNT7H	ACNT6H	ACNT5H	ACNT4H	ACNT3H	ACNT2H	ACNT1H	ACNT0H
$1B	Timer alternate counter low	ACNT7L	ACNT6L	ACNT5L	ACNT4L	ACNT3L	ACNT2L	ACNT1L	ACNT0L
$1C	MFT control and status	TOF	RTIF	TOFIE	RTIE	IRQN	WDOG	RT1	RT0
$1D	OSD frame control 1 and row count	PLLEN	DSCAN	FADE	ON/OFF	CDRC3	CDRC2	CDRC1	CDRC0
$1E	OSD frame control 2	BR1	BR0	VFPOL	HFPOL	HTPOL	FBPOL	RGBPOL	IPOL
$1F	OSD color palette 1	I1	R1	G1	B1	I0	R0	G0	B0

Table 3-1 MC68HC05T16/*MC68HC705T16* Registers

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$20	OSD color palette 2	I3	R3	G3	B3	I2	R2	G2	B2
$21	OSD color palette 3	I5	R5	G5	B5	I4	R4	G4	B4
$22	OSD color palette 4	I7	R7	G7	B7	I6	R6	G6	B6
$23	OSD row attribute	MTRX3	MTRX2	MTRX1	MTRX0	R3BE	R2BE	R1BE	R0BE
$24	OSD row 0 vertical position	FBKGC0	R0VP6	R0VP5	R0VP4	R0VP3	R0VP2	R0VP1	R0VP0
$25	OSD row 1 vertical position	FBKGC1	R1VP6	R1VP5	R1VP4	R1VP3	R1VP2	R1VP1	R1VP0
$26	OSD row 2 vertical position	FBKGC2	R2VP6	R2VP5	R2VP4	R2VP3	R2VP2	R2VP1	R2VP0
$27	OSD row 3 vertical position	FBKGC3	R3VP6	R3VP5	R3VP4	R3VP3	R3VP2	R3VP1	R3VP0
$28	OSD row horizontal position	SHDW	HP6	HP5	HP4	HP3	HP2	HP1	HP0
$29	OSD row control 1	R3INTE	R2INTE	R1INTE	R0INTE	R3EN	R2EN	R1EN	R0EN
$2A	OSD row control 2	R3CHS1	R3CHS0	R2CHS1	R2CHS0	R1CHS1	R1CHS0	R0CHS1	R0CHS0
$2B	OSD frame control 3 and status	VFINTE	MUTE1	MUTE0	VFLB	R3CF	R2CF	R1CF	R0CF
$2C	PWM0		0PWM6	0PWM5	0PWM4	0PWM3	0PWM2	0PWM1	0PWM0
$2D	PWM1		1PWM6	1PWM5	1PWM4	1PWM3	1PWM2	1PWM1	1PWM0
$2E	PWM2		2PWM6	2PWM5	2PWM4	2PWM3	2PWM2	2PWM1	2PWM0
$2F	PWM3		3PWM6	3PWM5	3PWM4	3PWM3	3PWM2	3PWM1	3PWM0
$30	PWM4		4PWM6	4PWM5	4PWM4	4PWM3	4PWM2	4PWM1	4PWM0
$31	PWM5		5PWM6	5PWM5	5PWM4	5PWM3	5PWM2	5PWM1	5PWM0
$32	PWM6		6PWM6	6PWM5	6PWM4	6PWM3	6PWM2	6PWM1	6PWM0
$33	PWM7		7PWM6	7PWM5	7PWM4	7PWM3	7PWM2	7PWM1	7PWM0
$34	PWM8		8PWM6	8PWM5	8PWM4	8PWM3	8PWM2	8PWM1	8PWM0
$35	PWM9L			9PWM5	9PWM4	9PWM3	9PWM2	9PWM1	9PWM0
$36	PWM9H	9PWM13	9PWM12	9PWM11	9PWM10	9PWM9	9PWM8	9PWM7	9PWM6
$37	MB address	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	
$38	MB clock				MBC4	MBC3	MBC2	MBC1	MBC0
$39	MB control	MEM	MIEM	MSTR	XMT	ACKEB			
$3A	MB status	MCF	SELTED	BBSY	ALOST		SRW	MIF	RXACKB
$3B	MB data	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0
$3C	ADC control and status	RESULT		CHNL	AD4	AD3	AD2	AD1	AD0
$3D	*EPROM programming control*							ELAT	PGM
$3E	Reserved								
$3F	Reserved								

4
RESETS AND INTERRUPTS

4.1 RESETS

The MC68HC05T16 can be reset in three ways: by the initial power-on reset function, by an active low input to the $\overline{\text{RESET}}$ pin, and by a COP watchdog timer reset (if enabled). Any of these resets will cause the program to go to its starting address, specified by the contents of memory locations $FFFE and $FFFF, and cause the interrupt mask of the Condition Code register to be set.

4.1.1 Power-On Reset (POR)

The power-on reset occurs when a positive transition is detected on the supply voltage, V_{DD}. The power-on reset is used strictly for power-up conditions, and should not be used to detect any drops in the power supply voltage. There is no provision for a power-down reset. The power-on circuitry provides for a 4064 tcyc delay from the time that the oscillator becomes active. If the external $\overline{\text{RESET}}$ pin is low at the end of the 4064 tcyc time out, the processor remains in the reset condition until $\overline{\text{RESET}}$ goes high. The user must ensure that V_{DD} has risen to a point where the MCU can operate properly prior to the time the 4064 POR cycles have elapsed. If there is doubt, the external $\overline{\text{RESET}}$ pin should remain low until such time that V_{DD} has risen to the minimum operating voltage specified.

4.1.2 $\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ input pin is used to reset the MCU to provide an orderly software start-up procedure. When using the external reset, the $\overline{\text{RESET}}$ pin must stay low for a minimum of 1.5tcyc. The $\overline{\text{RESET}}$ pin contains an internal Schmitt Trigger as part of its input to improve noise immunity.

4.1.3 Computer Operating Properly (COP) Reset

The MCU contains a watchdog timer that automatically times out if not reset (cleared) within a specific amount of time by a program reset sequence.

Note: COP time-out is prevented by periodically writing a '0' to bit 0 of address $FFF0.

4

If the watchdog timer is allowed to time-out, an internal reset is generated to reset the MCU. Because the internal reset signal is used, the MCU comes out of a COP reset in the same operating mode it was in when the COP time-out was generated.

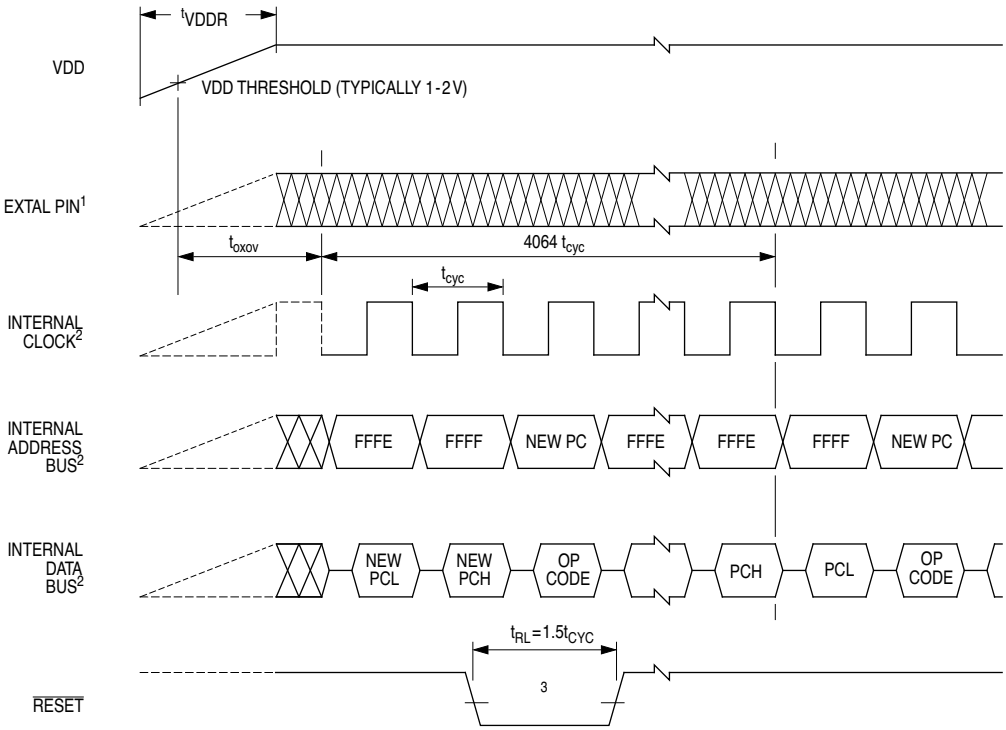
The watchdog timer is initially disabled after a reset, it is enabled by setting the WDOG bit in the Multi-Function Timer register (writing a '1' to bit 2 of address $1C); see Section 5.2 for more details. Once enabled, it cannot be disabled by software.

Table 4-1 shows the internal circuit actions on reset, but not necessary in order of occurrence.

Table 4-1 Reset Action on Internal Circuit

	DEFAULT CONDITIONS AFTER RESET
1	Timer prescaler reset to zero state
2	Timer counter configures to $FFFC
3	All timer interrupt enable bits cleared (ICIE, OC0IE, OC1IE, and TOVFIE) to disable timer interrupt
4	All data direction registers cleared to zero (default to inputs)
5	Port E and port F configured as general purpose I/O ports
6	Configure stack pointer to $00FF
7	Force internal address bus to the address of reset vector ($FFFE)
8	Set interrupt mask bit (I bit) in condition code register to logic one
9	Clear Stop latch
10	Clear Wait latch
11	Clear all interrupt enable bits
12	COP watchdog timer reset
13	COP watchdog disabled
14	Initialize M-Bus registers
15	Initialize PWM registers
16	Initialize PAC registers
17	OSD disabled, all registers initialized to default values

Listed numbers do not represent order of occurrence.



NOTES:
1. EXTAL is not meant to represent frequency. It is only used to represent time.
2. Internal clock, internal address bus, and internal data bus signals are not available externally.
3. Next rising edge of internal clock after rising edge of $\overline{\text{RESET}}$ initiates reset sequence.

Figure 4-1 Power-On Reset and $\overline{\text{RESET}}$ Timing

4.2 INTERRUPTS

The MC68HC05T16 is capable of handling eight types of interrupt, seven hardware and one software. The interrupt mask bit (“I” bit in the Condition Code register), if set, masks all interrupts except the software interrupt, SWI. Interrupts such as Timer, M-Bus, OSD, and MFT have several flags which will cause the interrupt. Interrupt flags are found in “read only” status registers, while their enables are in associated control registers. They are never mixed in the same register. If the enable bit is “0”, it masks the interrupt from occurring but does not inhibit the flag from being set. A reset clears all enable bits. The general sequence for clearing an interrupt is a software sequence of reading the status register while the flag is set followed by a read or write of an associated register. When any of these interrupts occur, and if enabled, normal processing is suspended at the end of the current instruction execution. The state of the machine is pushed onto the stack (see Figure 4-2 for stacking order) and the appropriate vector points to the starting address of the interrupt service routine (see Table 4-2). Also, the interrupt mask bit in the condition code register is set. This masks further interrupts. At the completion of the service routine, the software normally contains an RTI instruction which, when executed, restores the machine state and continues executing the interrupted program. Interrupt priority is based on interrupt vector addresses. The higher the vector addresses, the higher the priority. For example, OSD interrupts have a higher priority than $\overline{\text{IRQ}}$, TIMER, M-BUS, PAC, and MFT interrupts; but lower priority than SWI and $\overline{\text{RESET}}$.

Note: The interrupt mask bit (I bit) will be cleared if and only if the corresponding bit stored on the stack is zero.

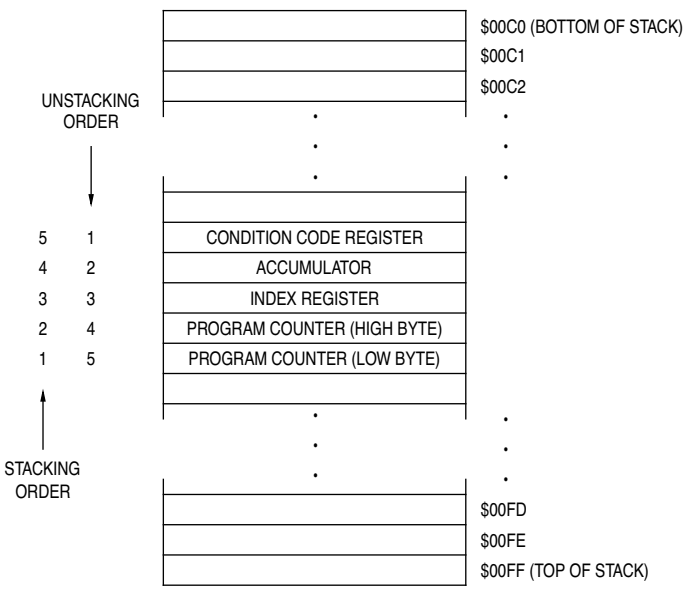


Figure 4-2 Interrupt Stacking Order

Table 4-2 Reset/Interrupt Vector Addresses

Register	Flag Name	Interrupt	CPU Interrupt	Vector Address
–	–	Reset	$\overline{\text{RESET}}$	$FFFE-$FFFF
–	–	Software	SWI	$FFFC-$FFFD
OSD Status	VFLB	Vertical Flyback	OSD	$FFFA-$FFFB
	R3CF/R2CF/ R1CF/R0CF	OSD Row Completion		
–	–	External Interrupt	$\overline{\text{IRQ}}$	$FFF8-$FFF9
Timer Status	ICF	Input Capture	TIMER	$FFF6-$FFF7
	OC0F/OC1F	Output Compare		
	TOF	Timer Overflow		
M-Bus Status	ALOST	Arbitration Loss	M-BUS	$FFF4-$FFF5
	SELTED	Addressed as Slave		
	MCF	Transfer Complete		
PAC Control	PAOF	Pulse Accumulator Overflow	PAC	$FFF2-$FFF3
Multi-Function Timer	RTIF	Real Time Interrupt	MFT	$FFF0-$FFF1
	TOF	Timer Overflow		

4.2.1 Hardware Controlled Sequences

The following three functions are not strictly interrupts, however, they are tied very closely to the interrupts. These functions are $\overline{\text{RESET}}$, STOP, WAIT.

1) $\overline{\text{RESET}}$ The $\overline{\text{RESET}}$ input pin causes the program to go to its starting address. This address is specified by the contents of memory locations $FFFE and $FFFF. The interrupt mask of the condition code register is also set. Most parts of the MCU is configured to some known state as described in Table 4-1.

2) STOP The STOP instruction causes the oscillator to be turned off and the processor “sleeps” until an external interrupt ($\overline{\text{IRQ}}$) or $\overline{\text{RESET}}$ occurs. See section 12 on Low Power Modes.

3) WAIT The WAIT instruction causes all processor clocks to stop, but leaves the Timer and PAC clocks running. This “rest” state of the processor can be exited by $\overline{\text{RESET}}$, an external interrupt ($\overline{\text{IRQ}}$), or any of the interrupts described above. There are no special wait vectors for these individual interrupts. See section 12 on Low Power Modes.

4.2.2 Software Interrupt (SWI)

The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask in the condition code register. The service routine address is specified by the contents of memory location $FFFC and $FFFD.

4.2.3 External Interrupt ($\overline{\text{IRQ}}$)

The external interrupt $\overline{\text{IRQ}}$ can be software configured for “negative-edge” or “negative-edge and level” sensitive triggering by the IRQN bit in the Multi-Function Timer register.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Multi-Function Timer Register	$1C	TOF	RTIF	TOFIE	RTIE	IRQN	WDOG	RT1	RT0	0000 0011

IRQN

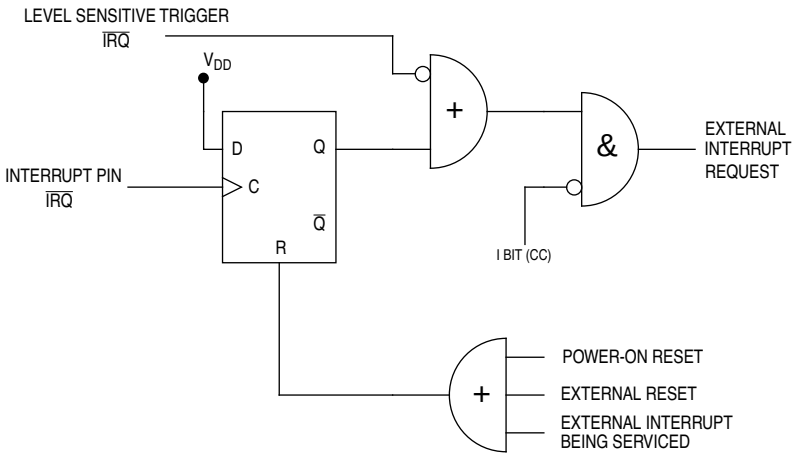
1 (set) – Negative edge triggering for $\overline{\text{IRQ}}$ only.

0 (clear) – Level and negative edge triggering for $\overline{\text{IRQ}}$.

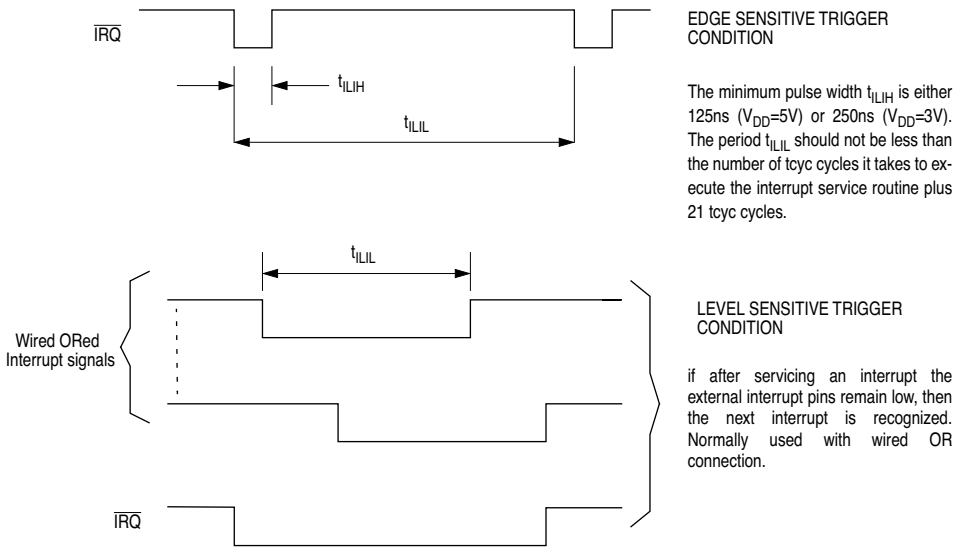
When the signal of the external interrupt pin, $\overline{\text{IRQ}}$, satisfies the condition selected, an external interrupt occurs. The actual processor interrupt is generated only if the interrupt mask bit of the condition code register is also cleared. When the interrupt is recognized, the current state of the processor is pushed onto the stack and the interrupt mask bit in the condition code register is set. This masks further interrupts until the present one is serviced. The service routine address is specified by the contents of $FFF8 & $FFF9.

The interrupt logic recognizes negative edge transitions and pulses (special case of negative edges) on the external interrupt line. Figure 4-3 shows both a block diagram and timing for the interrupt line ($\overline{\text{IRQ}}$) to the processor. The first method is used if pulses on the interrupt line are spaced far enough apart to be serviced. The minimum time between pulses is equal to the number of cycles required to execute the interrupt service routine plus 21 cycles. Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an RTI occurs). The second configuration shows several interrupt lines wired-OR to perform the interrupt at the processor. Thus, if the interrupt lines remain low after servicing one interrupt, the next interrupt is recognized.

Note: The internal interrupt latch is cleared in the first part of the service routine; therefore, one (and only one) external interrupt pulse could be latched during t_{ILIL} and serviced as soon as the I bit is cleared.



(a) Interrupt Function Diagram



(b) Interrupt Mode Diagram

Figure 4-3 External Interrupt Circuit and Timing

4.2.4 Programmable Timer Interrupt

Four timer interrupt flags are found in the top nibble of the Timer Status register (TSR) at location $11. All four interrupts will vector to the same address at location $FFF6-$FFF7.

Each flag bit is defined as follows:

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Timer Status Register	$11	ICF	OC0F	OC1F	TOF	TCAPS	0	0	0	0000 u000

TOF - Timer Overflow Flag

TOF is set during the counter transition of $FFFF to $0000. It is cleared by reading the TSR (with TOF set) followed by reading the counter least significant byte ($19).

OC0F, OC1F - Output Compare Flag 1 and Output Compare 2

The appropriate OCF is set when the corresponding Output Compare register matches the Counter register. It is cleared by reading the TSR (with OCF set) and then accessing the corresponding Output Compare register least significant byte ($15 or $17).

ICF - Input Capture Flag

ICF is set when a proper edge has been sensed by the input capture edge detector. It is cleared by an CPU read of the TSR (with ICF set) followed by accessing the Input Capture register least significant byte ($13).

All four timer interrupt flags have corresponding enable bits (ICIE, OC0IE, OC1IE, and TOIE) found in the Timer Control register (TCR) at location $10. Reset clears all enable bits preventing an interrupt from occurring. The actual processor interrupt is generated only if the interrupt mask bit of the condition code register is also cleared. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the interrupt mask bit in the condition code register is set. This masks further interrupts until the present one is serviced. The service routine address is specified by the contents of $FFF6 and $FFF7.

Refer to section 5.1 for detailed description of Programmable Timer.

4.2.5 M-Bus Interrupts

M-Bus interrupt is enabled when the M-Bus Interrupt Enable bit, MIEN of M-Bus Control register is set, provided the interrupt mask bit of the condition code register is cleared. There are three causes of M-Bus interrupt:

1) An arbitration lost which is signified by the Arbitration Lost flag, ALOST of M-Bus Status Register.
2) Addressed as slave which is indicated by the master addressed as slave flag, SELTED of M-Bus Status Register.
3) Completed transmission or reception of one byte of data. It depends on the original mode of the M-Bus interface which is determined by the Transmit/Receive flag, XMT of M-Bus Control Register.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
M-Bus Status Register	$3A	MCF	SELTED	BBSY	ALOST		SRW	MIF	RXACKB	1000 0001

MCF - Data Transfer Complete Flag

1 (set) – A byte transfer has been completed.

0 (clear) – A byte is being transfer.

SELTED - Addressed as Slave

1 (set) – Currently addressed as a slave.

0 (clear) – Currently not addressed.

When its own specific address (M-Bus Address register) matches the calling address, this bit is set. An interrupt is generated if the MIEN bit is set. Then CPU needs to check the SRW bit and set its XMT bit accordingly. Writing to the M-Bus Control register clears this bit.

ALOST - Arbitration Lost

This arbitration lost bit is set by hardware when the M-bus master loses arbitration during a master transmission mode. This bit must be cleared by software.

On entering the interrupt service routine, the M-Bus interrupt flag, MIF of M-Bus Status Register must be cleared by software.

The interrupt service routine address is specified by the contents of memory location $FFF4 and $FFF5. Reset disables the whole M-Bus block by clearing the M-Bus Control Register.

Refer to Section 6 for detailed description of M-Bus.

4.2.6 PAC Interrupt

Pulse Accumulator interrupt is enabled when the enable bit, PAIE of PAC Control register is set. The interrupt service routine address for PAC is specified by the contents of memory location $FFF2 and $FFF3.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
PACTL	$0E	PAOF	PAEN	PAMOD	PAIE					0000 0000

PAOF - PAC Overflow Interrupt Flag Bit.

1 (set) – A PAC overflow from $FF to $00 has occurred.

0 (clear) – No PAC overflow has occurred.

It is set when the count in the pulse accumulator rolls over from $FF to $00. PAOF is cleared by writing a “0” to the bit. An interrupt to the CPU is generated if the PAIE bit is set.

PAIE - PAC Interrupt Enable Bit

1 (set) – PAC overflow Interrupt enabled.

0 (clear) – PAC overflow Interrupt disabled.

Refer to section 7 for detailed description of Pulse Accumulator.

4.2.7 OSD Interrupts

There are five OSD interrupt sources, VFLBK bit and R0/1/2/3CF bits of OSD Status register, in the OSD module. VFLB bit will be set whenever the leading edge of vertical flyback pin, VFLBK, has been detected. An interrupt will occur if the corresponding interrupt enable bit, VFINTE, is set. Whenever each row terminates its display, RiCF bit will be set and an interrupt will be generated provided that the corresponding interrupt enable bit, RiINTE is set. The interrupt service routine address is specified by the contents of memory location $FFFA and $FFFB.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Frame Control 3 and Status	$2B	VFINTE	MUTE1	MUTE0	VFLB	R3CF	R2CF	R1CF	R0CF	0000 0000

VFINTE - VFLBK interrupt enable

1 (set) – Vertical flyback interrupt enabled.

0 (clear) – Vertical flyback interrupt disabled.

VFLB - VFLBK status

1 (set) – Vertical flyback (leading edge) signal detected.

0 (clear) – No Vertical flyback signal detected.

RiCF - Row i display status

1 (set) – Row i display has been terminated.

0 (clear) – Row i display has been not terminated.

Whenever a row display has been terminated, the corresponding RiCF flag will be set along with update of CDRC3-CDRC0 field.

Refer to section 9 for detailed description of On-Screen Display.

4.2.8 Multi-Function Timer Interrupts

There are two different interrupting sources, TOF and RTIF bits of Multi-Function Timer Register, in this module. The interrupt service routine address is specified by the contents of memory location $FFF0 and $FFF1.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Multi-Function Timer	$1C	TOF	RTIF	TOFIE	RTIE	IRQN	WDOG	RT1	RT0	0000 0011

TOF - Timer Overflow

1 (set) – 8-bit ripple timer overflow has occurred.

0 (clear) – No 8-bit ripple timer overflow has occurred.

This bit is set when the 8-bit ripple counter overflows from $FF to $00; a timer overflow interrupt will occur, if TOFIE (bit 5) is set. TOF is cleared by writing a ‘0’ to the bit.

RTIF - Real Time Interrupt Flag

1 (set) – A real time interrupt has occurred.

0 (clear) – A real time interrupt has not occurred.

A RTIF indicates when the output of the RTI circuit goes active. The clock frequency that drives the RTI circuit is E/16384 giving a maximum interrupt period of 3.9ms at a bus rate of 4.2MHz. A CPU interrupt request will be generated if RTIE is set. RTIE is cleared by writing a ‘0’ to the bit.

TOFIE - Timer Overflow Interrupt Enable

1 (set) – TOF interrupt is enabled.

0 (clear) – TOF interrupt is disabled.

RTIE - Real Time Interrupt Enable

1 (set) – Real time interrupt circuit is active.

0 (clear) – Real time interrupt circuit is inactive.

Refer to section 5.2 for detailed description of Multi-Function Timer.

5
TIMERS

5.1 PROGRAMMABLE TIMER

The timer consists of a 16-bit free-running counter driven by a fixed divide-by-four prescaler. This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from several microseconds to many seconds. Figure 5-1 shows a block diagram for the Programmable Timer.

Because the timer has a 16-bit architecture, the I/O registers for the input capture and output compare functions are pairs of 8-bit registers (high byte and low byte). Generally, assessing the low byte of a specific timer function allows full control of that function. However, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

Note: The I bit in the condition code register should be set while manipulating both the high and low byte register of a specific timer function to ensure that an interrupt does not occur.

Twelve 8-bit registers are associated with the programmable timer.

- Timer Control Register (TCR) $10
- Timer Status Register (TSR) $11
- Input Capture Register High byte - $12, Low byte - $13
- Output Compare 0 Register High byte - $14, Low byte - $15
- Output Compare 1 Register High byte - $16, Low byte - $17
- Counter Register High byte - $18, Low byte - $19
- Alternate Counter Register High byte - $1A, Low byte - $1B

A description of each register is provided in the following paragraphs.

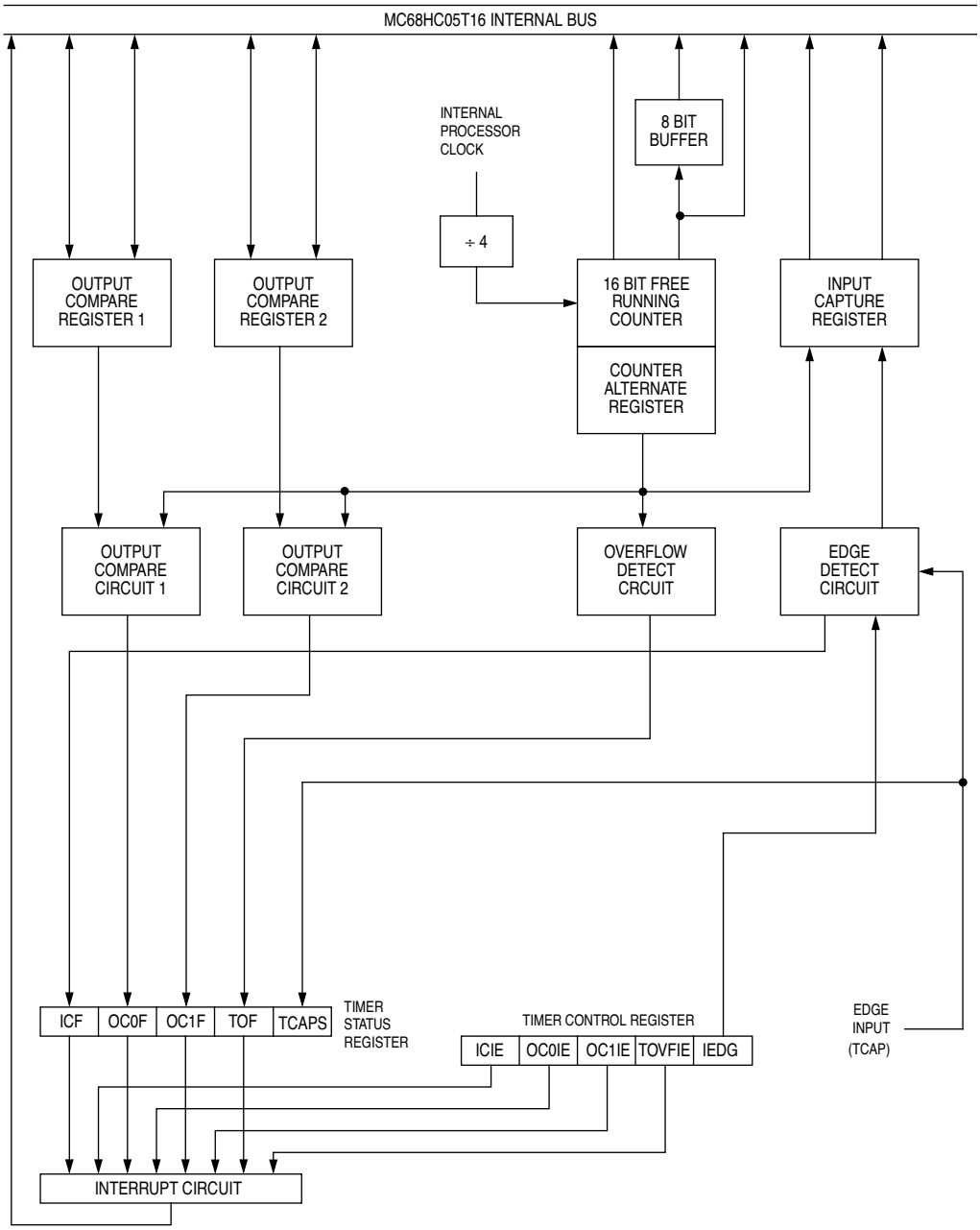


Figure 5-1 Programmable Timer Block Diagram

5.1.1 Counter

- Counter Register location — High byte - $18, Low byte - $19
- Alternate Counter Register — High byte - $1A, Low byte - $1B

The key element in the programmable timer is a 16-bit, free-running counter or counter register, preceded by a prescaler that divides the internal processor clock by four. The prescaler gives the timer a resolution of 0.95µs if the internal bus clock is 4.2MHz. The counter is incremented during the low portion of the internal bus clock. Software can read the counter at any time without affecting its value.

The double-byte, free-running counter can be read from either of two locations, $18 and $19 (counter register) or $1A and $1B (counter alternate register). Reading only the least significant byte (LSB) of the free-running counter ($19 or $1B) receives the count value at the time of the read. If the most significant byte (MSB) ($18 or $1A) is read first, the LSB ($19 or $1B) is transferred to a buffer. This buffer value remains fixed after the first MSB read, even if the MSB is read several times. This buffer is accessed when the LSB ($19 or $1B) is read, and thus, completes a read sequence of the complete counter value.

Reading the Timer Counter register low byte after reading the timer Status Register clears the timer overflow flag (TOF), but reading the Counter Alternate register does not affect TOF. Therefore, the counter alternate register can be read any time without risk of missing timer overflow interrupts due to a cleared TOF.

The free-running counter is preset to $FFFC during reset and is always a read-only register. During a power-on reset, the counter is also preset to $FFFC and begins running after the oscillator start-up delay. The value in the free-running counter repeats every 262144 internal bus clock cycles. TOF is set when the counter overflows (from $FFFF to $0000); this will cause an interrupt if TOVFIE (bit 4 of Timer Control register) is set.

In some timing control applications it may be desirable to reset the counter under software control. When the low byte of the counter ($19 or $1B) is written to, the counter is set to its reset value of $FFFC. The divide-by-4 prescaler is also reset and the counter resumes normal counting operation. All of the flags and enable bits remain unaltered by this operation. If access has previously been made to the high byte of the free-running counter ($18 or $1A), then the reset counter operation terminates the access sequence.

5.1.2 Output Compare Registers

There are two 16-bit Output Compare registers:

- Output Compare 0 Register — High byte - $14, Low byte - $15
- Output Compare 1 Register — High byte - $16, Low byte - $17

Each 16-bit Output Compare register is made up of two 8-bit registers. These Output Compare registers are used for several purposes, such as indicating when a period of time has elapsed. All

bits are readable and writable and are not affected by the timer hardware or reset. If the compare function is not needed, the Output Compare registers can be used as storage locations.

The contents of the Output Compare registers are continually compared with the contents of the free-running counter and, if a match is found, the corresponding output compare flag (OC0F or OC1F) in the Timer Status register is set. The Output Compare registers' value should be changed after each successful comparison to establish a new elapsed time-out. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit (OC0IE or OC1IE) is set. (The free-running counter is updated every four internal bus clock cycles.)

After a processor write cycle to the Output Compare registers containing the MSB ($14 or $16), the output compare function is inhibited until the LSB ($15 or $17) is also written. The user must write both bytes (locations) if the MSB is written first. A write made only to the LSB ($15 or $17) will not inhibit the compare function. The processor can write to either byte of an Output Compare register without affecting the other byte. The minimum time required to update the Output Compare registers is a function of the program rather than the internal hardware. Because the output compare flags and Output Compare registers are not defined at power on, and not affected by reset, care must be taken when initializing output compare functions with software. The following procedure is recommended:

1) write to Output Compare register 0 and/or 1 High-byte to inhibit further compares;
2) read the Timer Status register to initialize clearing of OC0F or/and OC1F;
3) write to Output Compare register 0 or/and 1 Low-byte to enable the output compare function.

5.1.3 Input Capture Registers

– Input Capture Register High byte - $12, Low byte - $13

'Input Capture' is a technique whereby an external signal (connected to TCAP pin) is used to trigger a read of the free-running counter. In this way it is possible to relate the timing of an external signal to the internal counter value, and hence to elapsed time.

The two 8-bit registers that make up the 16-bit input capture register, are read-only, and are used to latch the value of the free-running counter after the corresponding input capture edge detector senses a valid transition. The level transition that triggers the counter transfer is defined by the corresponding input edge bit (IEDG). Reset does not affect the contents of the input capture register.

The result obtained from an input capture will be one greater than the value of the free-running counter on the rising edge of the internal bus clock preceding the external transition. This delay is required for internal synchronization. Resolution is one count of the free-running counter, which is four internal bus clock cycles.

The free-running counter contents are transferred to the input capture register on each valid signal transition whether the input capture flag (ICF) is set or clear. The input capture register always

contains the free-running counter value that corresponds to the most recent input capture.After a read of the input capture register MSB ($12), the counter transfer is inhibited until the LSB ($13) is also read. This characteristic causes the time used in the input capture software routine and its interaction with the main program to determine the minimum pulse period. A read of the input capture register LSB ($13) does not inhibit the free-running counter transfer since they occur on opposite edges of the internal bus clock.

5.1.4 Timer Control Register (TCR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$10	ICIE	OC0IE	OC1IE	TOVFIE			IEDG		0000 0000

The TCR is a read/write register containing five control bits. Four bits control interrupts associated with each of the four flag bits found in the Timer Status register. The other bit controls which edge is significant to the input capture edge detector. The Timer Control register and the free-running counter are the only sections of the timer affected by reset.

Definition of each bit is as follows:

ICIE - Input Capture Interrupt Enable

1 (set) – Input Capture interrupt enabled.

0 (clear) – Input Capture interrupt disabled.

OC0IE - Output Compare Interrupt Enable

1 (set) – Output Compare 0 interrupt enabled.

0 (clear) – Output Compare 0 interrupt disabled.

OC1IE - Output Compare Interrupt Enable

1 (set) – Output Compare 1 interrupt enabled.

0 (clear) – Output Compare 1 interrupt disabled.

TOVFIE - Timer Overflow Interrupt Enable

1 (set) – Timer Overflow interrupt enabled.

0 (clear) – Timer Overflow interrupt disabled.

IEDG - Input Edge

1 (set) – TCAP is positive-going edge sensitive.

0 (clear) – TCAP is negative-going edge sensitive.

When IEDG is set, a positive-going edge on the TCAP pin will trigger a transfer of the free-running counter value to the input capture registers. When clear, a negative-going edge triggers the transfer.

5.1.5 Timer Status Register (TSR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$11	ICF	OC0F	OC1F	TOF	TCAPS				0000 u000

The Timer Status register contains the status bits for the above four interrupt conditions - ICF, OC0F, OC1F, TOF.

Accessing the timer status register satisfies the first condition required to clear the status bits. The remaining step is to access the register corresponding to the status bit.

ICF - Input Capture Flag

1 (set) – A valid input capture has occurred.

0 (clear) – No input capture has occurred.

This bit is set when the selected polarity of edge is detected by the input capture edge detector; an input capture interrupt will be generated, if ICIE is set, ICF is cleared by reading the TSR and then the Input Capture Low register ($13)

OC0F - Output Compare 0 Flag

1 (set) – A valid output compare has occurred on output compare 0 register.

0 (clear) – No output compare has occurred on output compare 0 register.

OC0F will be set when its output compare 0 register contents match that of the free-running counter; an output compare interrupt will be generated, if OC0IE is set. OC0F is cleared by reading the TSR and then the Output Compare 0 Low register ($15).

OC1F - Output Compare 1 Flag

1 (set) – A valid output compare has occurred on output compare 1 register.

0 (clear) – No output compare has occurred on output compare 1 register.

OC0F will be set when its output compare 1 register contents match that of the free-running counter; an output compare interrupt will be generated, if OC1IE is set. OC1F is cleared by reading the TSR and then the Output Compare 1 Low register ($17).

TOF - Timer Overflow Flag

1 (set) – Timer Overflow has occurred.

0 (clear) – No timer overflow has occurred.

This bit is set when the free-running counter overflows from $FFFF to $0000; a timer overflow interrupt will occur, if TOIE (bit 5 in Timer Control register $10) is set. TOF is cleared by reading the TSR and the counter low register ($19).

When using the timer overflow function and reading the free-running counter at random times to measure an elapsed time, a problem may occur whereby the timer overflow flag is unintentionally cleared if:

1) the timer status register is read or written when the TOF is set, and
2) the LSB of the free-running counter is read, but not for the purpose of servicing the flag.

Reading the alternate counter register instead of the counter register will avoid this potential problem.

TCAPS - Timer Capture State

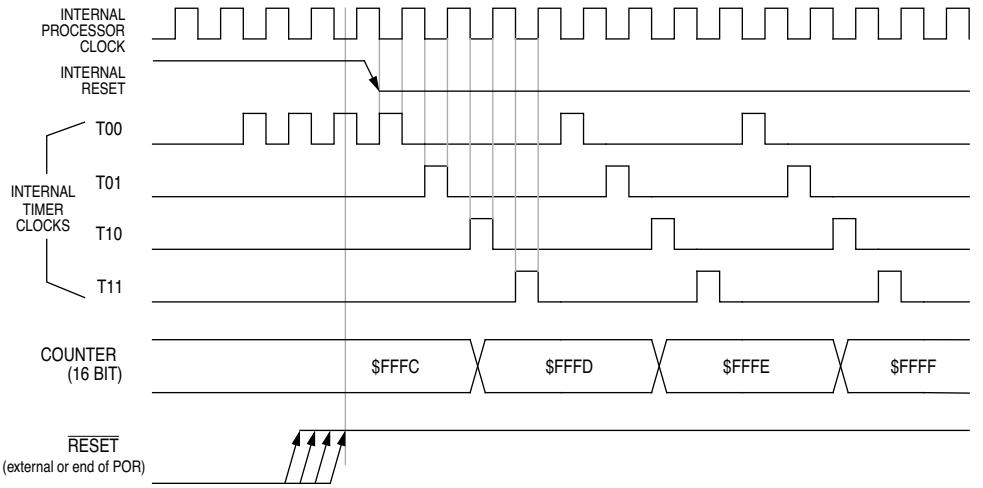
1 (set) – TCAP pin is a logic high.

0 (clear) – TCAP pin is a logic low.

This bit reflects the logic level at the TCAP pin.

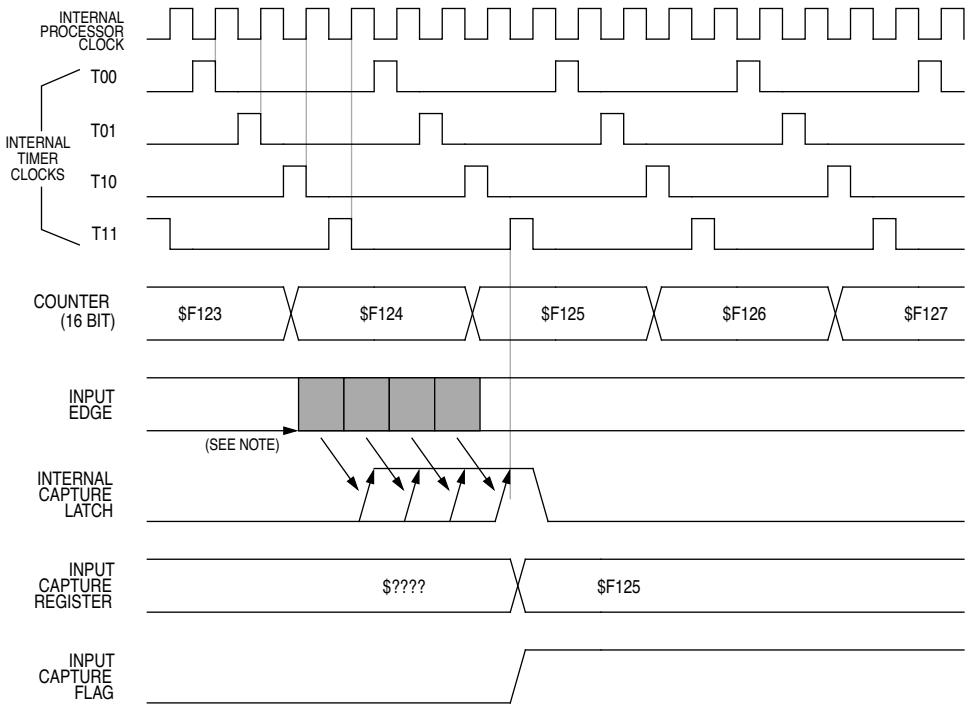
5.1.6 Programmable Timer Timing Diagrams

The relationships between the internal clock signals, the counter contents and the status of the flag bits are shown in the following diagrams. It should be noted that the signals labelled ‘internal’ (processor clock, timer clocks and Reset) are not available to the user.



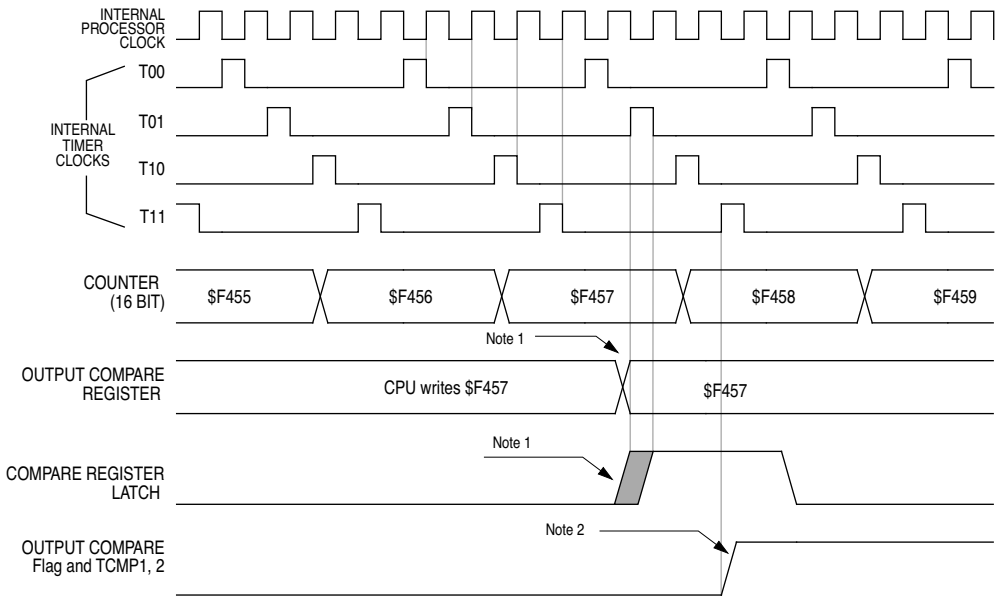
Notes: RESET affects only the Counter register and Timer Control register.

Figure 5-2 Timer State Timing Diagram for Reset



Note: If the input edge occurs in the shaded area from one timer state T10 to the other timer state T10 the input capture flag is set during the next state T11.

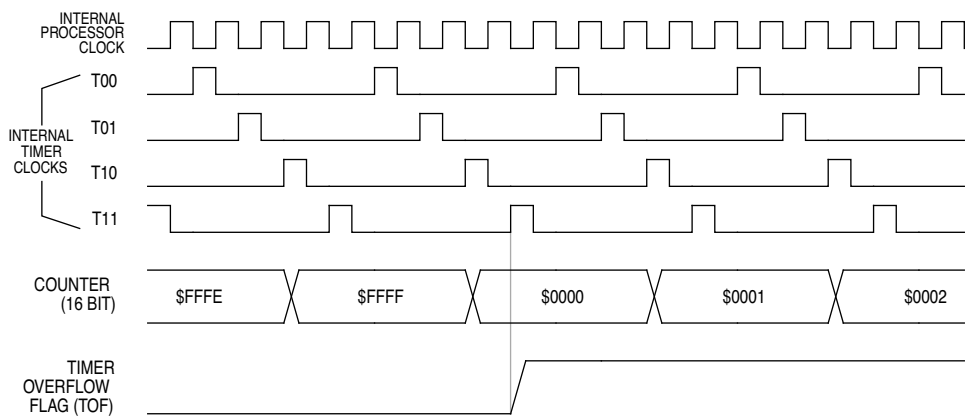
Figure 5-3 Timer State Timing Diagram for Input Capture



Note: 1. The CPU write to the compare registers may take place at any time, but a compare only occurs at the timer state T01. Thus a 4-cycle difference may exist between the write to the compare register and the actual compare.

2. The output compare flag is set at the timer state T11 that follows the comparison match ($F547 in this example).

Figure 5-4 Timer State Timing Diagram for Output Compare



Note: The TOF bit is set at timer state T11 (transition of counter from $FFFF to $0000). It is cleared by a read of the timer status register during the internal processor clock high time followed by a read of the counter low register.

Figure 5-5 Timer State Diagram for Timer Overflow

5.2 MULTI-FUNCTION TIMER

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Multi-Function Timer Register	$1C	TOF	RTIF	TOFIE	RTIE	IRQN	WDOG	RT1	RT0	0000 0011

The MFT provides miscellaneous function to the MC68HC05T16 MCU. It includes a timer overflow function, real-time interrupt, and COP watchdog. The external interrupt ($\overline{IRQ}$) triggering option is also set by this Multi-Function Timer register.

The clock base for this module is derived from the bus clock divided by four. For a 4.2 MHz E (CPU) clock, the clock base is 1.05 MHz. This clock base is then divided by an 8-stage ripple counter to generate the timer overflow. Timer overflow rate is thus E/1024. The output of this 8-stage ripple counter then drives a 4-stage divider to generate real time interrupt. Hence, the clock base for real time interrupt is E/16384. Real time interrupt rate is selected by RT0 and RT1 bits of Multi-Function Timer register. The interrupt rates are E/16384, (E/16384)/2, (E/16384)/4, and (E/16384)/8. The selected real time interrupt rate is then divided by 8 to generate COP reset.

Register bit definitions:

TOF - Timer Overflow

1 (set) – 8-bit ripple timer overflow has occurred.

0 (clear) – No 8-bit ripple timer overflow has occurred.

This bit is set when the 8-bit ripple counter overflows from $FF to $00; a timer overflow interrupt will occur, if TOFIE (bit 5) is set. TOF is cleared by writing a ‘0’ to the bit.

RTIF - Real Time Interrupt Flag

1 (set) – A real time interrupt has occurred.

0 (clear) – A real time interrupt has not occurred.

When RTIF is set, a CPU interrupt request is generated if RITE is set. The clock frequency that drives the RTI circuit is E/16384 giving a maximum interrupt period of 3.9 ms at a bus rate of 4.2 MHz. RTIF is cleared by writing a “0” to the bit.

TOFIE - Timer Overflow Interrupt Enable

1 (set) – TOF interrupt is enabled.

0 (clear) – TOF interrupt is disabled.

RTIE - Real Time Interrupt Enable

1 (set) – Real time interrupt is enabled.

0 (clear) – Real time interrupt is disabled.

IRQN - $\overline{\text{IRQ}}$ Pin Trigger Option

1 (set) – Negative edge triggering for $\overline{\text{IRQ}}$ only.

0 (clear) – Level and negative edge triggering for $\overline{\text{IRQ}}$.

WDOG - COP Watchdog Enable

1 (set) – COP watchdog circuit enabled.

0 (clear) – COP watchdog circuit disabled.

See Section 5.2.1 on COP watchdog reset.

RT1, RT0 - Rate Select for COP watchdog and RTI

See Section 5.2.1 on watchdog reset.

5.2.1 COP Watchdog Reset

The COP (Computer Operating Properly) watchdog timer function is implemented by using the output of the Multi-Function Timer counter. The minimum COP reset rates are controlled by RT0 and RT1 of Multi-Function Timer register. If the COP circuit times out, an internal reset is generated and the reset vector is fetched (at $FFFE & $FFFF). Preventing a COP time-out is achieved by writing a '0' to bit 0 of address $FFF0. The COP counter has to be cleared periodically by software with a period less than COP reset rate.

Watchdog timer function will stop counting in Wait and Stop modes. Counting continues when it wakes up from Wait mode, and a 4064 cycle delay after waking up from Stop mode.

The watchdog counter system is controlled by the WDOG bit in the Multi-Function Timer register (bit 2 of address $1C). After power-on or external reset the watchdog system is disabled. Writing a "1" to the WDOG bit will enable the watchdog system and the counter starts counting. Once enabled, the watchdog system cannot be disabled by software. Writing a "0" to bit 0 of address $FFF0 will reset watchdog counter to prevent a watchdog time-out.

Table 5-1 COP Reset and RTI Rates

RT1	RT0	Minimum COP reset period E clock = 4.2MHz	RTI period E clock = 4.2MHz
0	0	27.3ms	3.9ms
0	1	54.6ms	7.8ms
1	0	109.27ms	15.6ms
1	1	218.4ms	31.2ms
RT0 and RT1 should only be changed immediately after COP watchdog timer has been reset.			

5

THIS PAGE LEFT BLANK INTENTIONALLY

6
M-BUS SERIAL INTERFACE

M-Bus (Motorola Bus) is a two-wire, bidirectional serial bus which provides a simple, efficient way for data exchange between devices. It is fully compatible with the I^2C bus standard. This two-wire bus minimizes the interconnection between devices and eliminates the need for address decoders; resulting in less PCB traces and economic hardware structure. This bus is suitable for applications requiring communications in a short distance among a number of devices. The maximum data rate is 100 Kbit/s. The maximum communication length and number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.

The M-Bus system is a true multi-master bus, including arbitration to prevent data collision if two or more masters intend to control the bus simultaneously. It may be used for rapid testing and alignment of end products via external connections to an assembly-line computer.

6.1 M-Bus Interface Features

- Compatible with I^2C bus standard
- Multi-master operation
- 32 software programmable serial clock frequencies
- Software selectable acknowledge bit
- Interrupt driven byte-by-byte data transfer
- Arbitration lost driven interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Generate/detect the start, stop and acknowledge signals
- Repeated START signal generation
- Bus busy detection

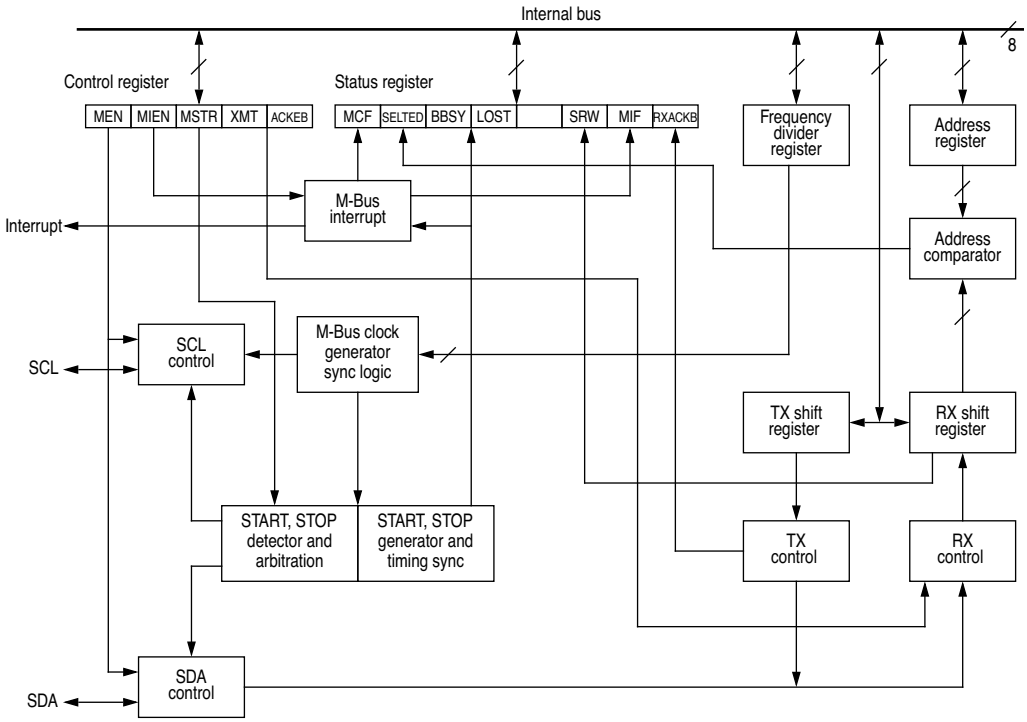


Figure 6-1 M-Bus Interface Block Diagram

6.2 M-Bus Protocol

Normally, a standard communication is composed of four parts,

1) START signal,
2) slave address transmission,
3) data transfer, and
4) STOP signal.

They are described briefly in the following sections and illustrated in Figure 6-2.

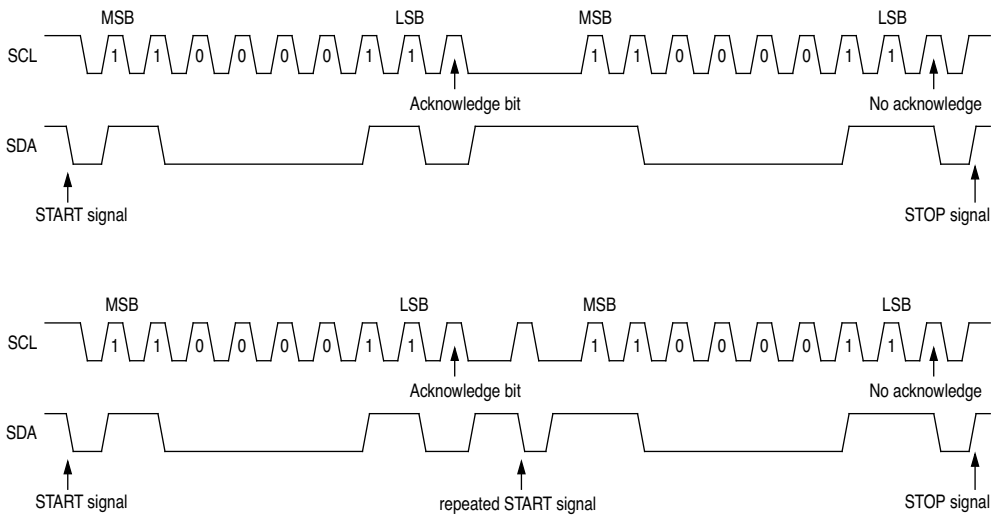


Figure 6-2 M-Bus Transmission Signal Diagram

6.2.1 START Signal

When the bus is free, i.e., no master device is occupying the bus (both SCL and SDA lines are at logic high), a master may initiate communication by sending a START signal. As shown in Figure 6-2, a START signal is defined as a high to low transition of SDA while SCL is high. This signal denotes the beginning of a new data transfer (each data transfer may contain several bytes of data) and wakes up all slaves.

6.2.2 Slave Address Transmission

The first byte of data transfer immediately following the START signal is the slave address transmitted by the master. This is a seven bits long calling address followed by a R/$\overline{W}$ bit. The R/$\overline{W}$ bit dictates the slave of the desired direction of data transfer.

Only the slave with matched address will respond by sending back an acknowledge bit by pulling the SDA low at the 9th clock; see Figure 6-2.

6.2.3 Data Transfer

Once a successful slave addressing is achieved, the data transfer can proceed byte by byte in a direction specified by the R/$\overline{W}$ bit sent by the calling master.

Each data byte is 8 bits long. Data can be changed only when SCL is low and must be held stable when SCL is high as shown in Figure 6-2. One clock pulse is for one bit of data transfer, MSB is transferred first. Each data byte has to be followed by an acknowledge bit. Hence, one complete data byte transfer requires 9 clock pulses.

If the slave receiver does not acknowledge the master, the SDA line should be left high by the slave, the master can then generate a STOP signal to abort the data transfer or a START signal (repeated START) to commence a new calling.

If the master receiver does not acknowledge the slave transmitter after one byte transmission, it means an “end of data” to the slave. The slave shall release the SDA line for the master to generate STOP or START signal.

6.2.4 Repeated START Signal

As shown in Figure 6-2, a repeated START signal is to generate a START signal without first generating a STOP signal to terminate the communication. This is used by the master to communicate with another slave or with the same slave in a different mode (transmit/receive mode) without releasing the bus.

6.2.5 STOP Signal

The master can terminate the communication by generating a STOP signal to free the bus. However, the master may generate a START signal followed by a calling command without generating a STOP signal first. This is called repeat START. A STOP signal is defined as a low to high transition of SDA while SCL is at a logical high; See Figure 6-2.

6.2.6 Arbitration Procedure

This interface circuit is a true multi-master system which allows more than one master to be connected. If two or more masters try to control the bus at the same time, a clock synchronization procedure determines the bus clock. The clock low period is equal to the longest clock low period among the masters; and the clock high period is the shortest among the masters. A data arbitration procedure determines the priority. A master will lose arbitration if it transmits a logic “1” while the others transmit logic “0”, the losing master will immediately switch over to slave receive mode and stops its data and clock outputs. The transition from master to slave mode will not generate a STOP condition. Meanwhile, a software bit will be set by hardware to indicate loss of arbitration.

6.2.7 Clock Synchronization

Since wire-AND logic is performed on the SCL line, a high to low transition on SCL line will affect the devices connected to the bus. The devices start counting their low period and once a device's clock has gone low, it will hold the SCL line low until the clock high state is reached. However, the change of low to high in this device clock may not change the state of the SCL line, if another device clock is still in its low period. Therefore synchronized clock SCL will be held low by the device which releases SCL to a logic high in the last place. Devices with shorter low periods enter a high wait state during this time (See Figure 6-3). When all devices concerned have counted off their low period, the synchronized clock SCL line will be released and go high. All of them will start counting their high periods. The first device to complete its high period will again pull the SCL line low.

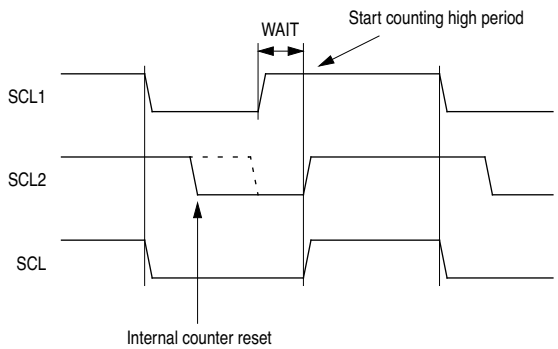


Figure 6-3 Clock Synchronization

6.2.8 Handshaking

The clock synchronization mechanism can be used as a handshake in data transfer. Slave device may hold the SCL low after completion of one byte transfer (9 bits). In such case, it will halt the bus clock and force the master clock in a wait state until the slave releases the SCL line.

6.3 M-Bus Registers

There are five registers used in the M-Bus interface, these are discussed in the following paragraphs.

6.3.1 M-Bus Address Register (MADR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$37	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1		0000 0000

ADR1-ADR7 are the slave address bits of the M-Bus module.

6.3.2 M-Bus Clock Register (MCKR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$38				MBC4	MBC3	MBC2	MBC1	MBC0	0000 0000

MBC0-MBC4 are used for clock rate selection. The serial bit clock frequency is equal to the CPU clock divided by the divider shown in Table 6-1.

Table 6-1 M-Bus Prescaler

MBC4	MBC3	MBC2	MBC1	MBC0	DIVIDER	MBC4	MBC3	MBC2	MBC1	MBC0	DIVIDER
0	0	0	0	0	22	1	0	0	0	0	352
0	0	0	0	1	24	1	0	0	0	1	384
0	0	0	1	0	28	1	0	0	1	0	448
0	0	0	1	1	34	1	0	0	1	1	544
0	0	1	0	0	44	1	0	1	0	0	704
0	0	1	0	1	48	1	0	1	0	1	768
0	0	1	1	0	56	1	0	1	1	0	896
0	0	1	1	1	68	1	0	1	1	1	1088
0	1	0	0	0	88	1	1	0	0	0	1408
0	1	0	0	1	96	1	1	0	0	1	1536
0	1	0	1	0	112	1	1	0	1	0	1792
0	1	0	1	1	136	1	1	0	1	1	2176
0	1	1	0	0	176	1	1	1	0	0	2816
0	1	1	0	1	192	1	1	1	0	1	3072
0	1	1	1	0	224	1	1	1	1	0	3584
0	1	1	1	1	272	1	1	1	1	1	4352

For a 4.2 MHz external crystal operation (2.1 MHz internal operating frequency), the serial bit clock frequency of M-Bus ranges from 483 Hz to 95,455 Hz.

6.3.3 M-Bus Control Register (MCR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$39	MEN	MIEN	MSTR	XMT	ACKEB				0000 0000

Register bit definitions:

MEN - M-Bus Enable

1 (set) – M-Bus interface system enabled.

0 (clear) – M-Bus interface system disabled.

MIEN - M-Bus Interrupt Enable

1 (set) – M-Bus interrupt enabled.

0 (clear) – M-Bus interrupt disabled.

This bit enables the MIF (in MSR) for M-Bus interrupts.

MSTR - Master/Slave Select Bit

1 (set) – M-Bus is set for master mode operation.

0 (clear) – M-Bus is set for slave mode operation.

Upon reset, this bit is cleared. When this bit is changed from 0 to 1, a START signal is generated on the bus, and the master mode is selected. When this bit is changed from 1 to 0, a STOP signal is generated and the operation mode changes from master to slave. In master mode, a bit clear immediately followed by a bit set of this bit generates a repeated START signal without generating a STOP signal.

XMT - Transmit/Receive Mode Select Bit

1 (set) – M-Bus is set for transmit mode.

0 (clear) – M-Bus is set for receive mode.

ACKEB - Acknowledge Enable Bit

1 (set) – Do not send acknowledge signal.

0 (clear) – Send acknowledge signal at 9th clock bit.

If cleared, an acknowledge signal will be sent out to the bus at the 9th clock bit after receiving one byte of data. If set, no acknowledge signal response. This is an active low control bit.

6.3.4 M-Bus Status Register (MSR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$3A	MCF	SELTED	BBSY	ALOST		SRW	MIF	RXACKB	1000 0001

The MIF and ALOST bits are software clearable; while the other bits are read only.

MCF - Data Transfer Complete Flag

1 (set) – A byte transfer has been completed.

0 (clear) – A byte is being transfer.

When MCF is set, the MIF (M-bus interrupt) bit is also set. An M-bus interrupt is generated if the MIEN bit is set.

SELTED - Addressed as Slave Bit

1 (set) – Currently addressed as a slave.

0 (clear) – Not currently addressed.

This SELTED bit is set when its own specific address (M-Bus Address register) matches the calling address. When SELTED is set, the MIF (M-bus interrupt) bit is also set. An interrupt is generated if the MIEN bit is set. Then CPU needs to check the SRW bit and set its XMT bit accordingly. Writing to the M-Bus Control register clears this bit.

BBSY - Bus Busy Bit

1 (set) – M-Bus busy.

0 (clear) – M-Bus idle.

This bit indicates the status of the bus. When a START signal is detected, BBSY is set. If a STOP signal is detected, it is cleared.

ALOST - Arbitration Lost Flag

1 (set) – Lost arbitration in master mode.

0 (clear) – No arbitration lost.

This arbitration lost flag is set when the M-bus master loses arbitration during a master transmission mode. When ALOST is set, the MIF (M-bus interrupt) bit is also set. This bit must be cleared by software.

SRW - Slave R/W Select

1 (set) – Read from slave, from calling master.

0 (clear) – Write to slave from calling master.

When SELTED is set, the R/W command bit of the calling address sent from the master is latched into this SRW bit. By checking this bit, the CPU can then select slave transmit/receive mode by configuring XMT bit of the M-Bus Control register.

MIF - M-Bus Interrupt Flag

1 (set) – A M-Bus interrupt has occurred.

0 (clear) – A M-Bus interrupt has not occurred.

When this bit is set, an interrupt is generated to the CPU if MIEN is set. This bit is set when one of the following events occurs:

1) Completion of one byte of data transfer. It is set at the falling edge of the 9th clock - MCF set.
2) A match of the calling address with its own specific address in slave receive mode - SELTED set.
3) A loss of bus arbitration - ALOST set.

This bit must be cleared by software in the interrupt routine.

RXACKB - Receive Acknowledge Bit

1 (set) – No acknowledgment signal detected.

0 (clear) – Acknowledgment signal detected after 8 bits data transmitted.

If cleared, it indicates an acknowledge signal has been received after the completion of 8 bits data transmission on the bus. If set, no acknowledge signal has been detected at the 9th clock. This is an active low status flag.

6.3.5 M-Bus Data I/O Register (MDR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$3B	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	uuuu uuuu

In master transmit mode, data written into this register is sent to the bus automatically, with the most significant bit out first. In master receive mode, reading of this register initiates receiving of the next byte data. In slave mode, the same function applies after it has been addressed.

6

THIS PAGE LEFT BLANK INTENTIONALLY

7
PULSE ACCUMULATOR

The Pulse Accumulator is an 8-bit counter that can operate in either of two modes; event counting mode and the gated time accumulation mode. The operating mode is selected by a control bit in the Pulse Accumulator Control register.

In the event counting mode, the 8-bit counter is clocked by the signal on the PACIN pin. The maximum clocking rate for the external counting mode is E (CPU) clock divided by two.

In the gated time accumulation mode, the 8-bit counter is driven by E clock divided by 64. The counter will increment when PACIN pin is high and halt when PACIN is low.

7.1 Pulse Accumulator Registers

Two registers are associated with the Pulse Accumulator; they are described below.

7.1.1 PAC Control and Status Register (PACTL)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$0E	PAOF	PAEN	PAMOD	PAIE					0000 0000

Register bit definitions:

PAOF - PAC Overflow Interrupt Flag Bit.

1 (set) – A PAC overflow from $FF to $00 has occurred.

0 (clear) – No PAC overflow has occurred.

It is set when the count in the pulse accumulator rolls over from $FF to $00. PAOF is cleared by writing a “0” to the bit. An interrupt to the CPU is generated if the PAIE bit is set.

PAEN - PAC Enable Bit

1 (set) – Pulse Accumulator enabled.

0 (clear) – Pulse Accumulator disabled. PAC counter register is also cleared.

PAMOD - Pulse Accumulator Mode Bit

1 (set) – Gated time accumulation mode.

0 (clear) – External event counting mode.

PAIE - PAC Interrupt Enable Bit

1 (set) – PAC overflow Interrupt enabled.

0 (clear) – PAC overflow Interrupt disabled.

This PAIE bit enables interrupt caused by the PAOF bit.

7.1.2 PAC Counter Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$0F	PAD7	PAD6	PAD5	PAD4	PAD3	PAD2	PAD1	PAD0	0000 0000

When PAC is disabled (PAEN=0), the counter will be cleared to zero. This ensures the Counter starts from zero every time it is disabled and enabled.

The Pulse Accumulator Counter is read only and resets to zero a write operation.

8
PULSE WIDTH MODULATOR

The MC68HC05T16 has 10 PWM channels, with output pins shared with port E and port F pins. Nine 7-bit channels are driven by the Timer clock, the other single 14-bit channel is driven by the CPU clock. All PWM outputs are +12V open-drain type; therefore a pull-up resistor is required at each PWM pin.

8.1 7-Bit PWM Channels

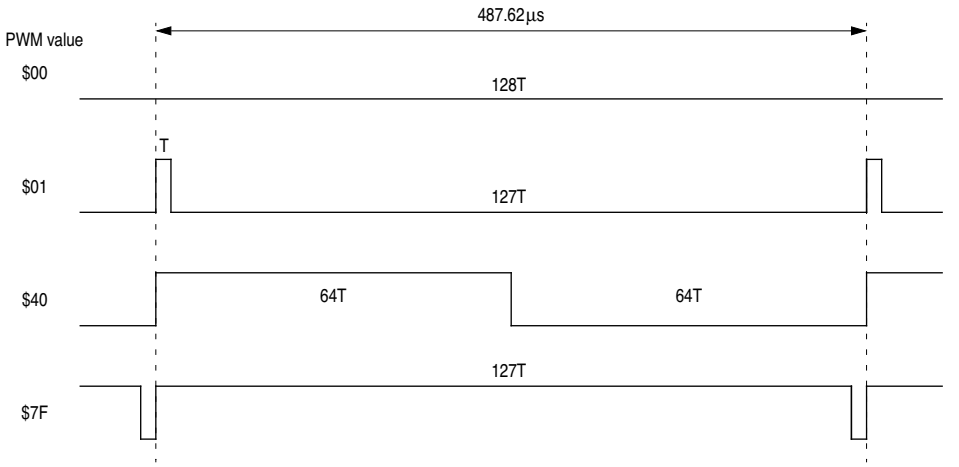
The 7-bit PWM system works in conjunction with the 16-bit free running timer to implement nine channels of conversion. A PWM register is allocated for each PWM channel. Channels PWM0 to PWM8, located at $2C to $34 respectively. Each 7-bit PWM data register has the same bit structure as shown below:

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
PWM0	$2C		0PWM6	0PWM5	0PWM4	0PWM3	0PWM2	0PWM1	0PWM0	0000 0000
:						:				
PWM8	$34		8PWM6	8PWM5	8PWM4	8PWM3	8PWM2	8PWM1	8PWM0	0000 0000

The driving clock for the 7-bit PWM channels is the 16-bit free-running timer clock divide by 2. For a 2.1MHz CPU clock, PWM clock = 2.1MHz/4/2 = 262500Hz. The PWM pulse period is 128 x 1/262500Hz = 487.62µs, i.e. a repetition frequency of 2050.8Hz. The duty cycle is proportional to the value in the corresponding PWM data register. A value of $00 loaded into these registers results in a continuously low output on the corresponding PWM output pin with external pull-up resistor connected. A value of $40 results in a 50% duty cycle output. The maximum value of $7F results in a 127/128 duty cycle output.

Changes to the value in the PWM registers will only become effective after the end of the current PWM cycle. This prevents erroneous PWM output during value update.

In Stop mode, the oscillator is stopped asynchronously with PWM operation. As a consequence, the PWM output will remain at the state at the moment when the oscillator is stopped. The PWM output might be at its high or low state at that moment, and it remains at that state until Stop mode



T = PWM clock period = 2 Timer clock periods = 8 CPU clock periods =3.81µs if MCU runs at 2.1MHz

Figure 8-1 7-Bit PWM Output Waveform

is exited. After Stop mode is exited, the PWM output resumes its unfinished portion of the stopped cycle. In Wait mode, the oscillator is running even though the CPU clock is not present, the PWM outputs are not affected.

Note: Since the 7-bit PWM module uses the 16-bit free-running timer counter, PWM outputs will be affected when the counter is being reset.

8.2 14-Bit PWM Channel

The output waveform of the 14-bit PWM channel is controlled by an 8-bit and a 6-bit register. Each register can be viewed as configuring its own waveform; the final PWM output waveform is a combination of the two waveforms (waveforms are ORed). The driving clock for the 14-bit PWM channels is CPU clock.

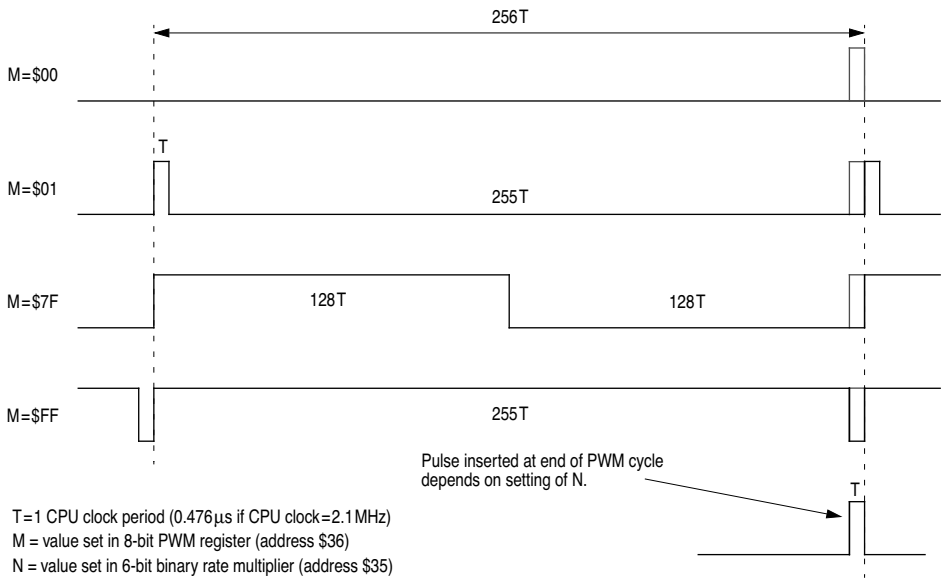
	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
BRM	$35			9PWM5	9PWM4	9PWM3	9PWM2	9PWM1	9PWM0	0000 0000
PWM	$36	9PWM13	9PWM12	9PWM11	9PWM10	9PWM9	9PWM7	9PWM7	9PWM6	0000 0000

The 8-bit register works in the same way as the 7-bit PWMs. That is, the value set in this 8-bit register determines the basic duty cycle of the waveform. A value of $00 results in a continuously

low cycle. A value of $7F results in a 50% duty cycle. The maximum value of $FF results in a 255/256 duty cycle. The 14-bit PWM period is 256x0.476µs=121.9µs for a CPU clock of 2.1MHz.

The 6-bit register acts as a binary rate multiplier (BRM). The value set in this register (powers of 2) equals the number of pulses (pulse width equals to the PWM driving clock cycle) equally distributed in a 64-PWM-cycle. A maximum value of $2x will have 32 pulses equally distributed in 64 PWM cycles (64 cycles has a period of 64x121.9µs=7.8ms).

Combining the 8-bit PWM together with the 6-bit BRM, the total average duty cycle at the output will be (M+N/64)/256, where M is the content of the 8-bit high-order register, and N is the content of the 6-bit low-order register. Using this mechanism, a true 14-bit resolution PWM is achieved. Figure 8-2 shows the waveform for the 14-bit PWM channel. Note that the resulting waveform is periodic on every 64 PWM cycles.



N	PWM cycles where pulses are inserted in a 64-cycle frame	Number of inserted pulses in a 64-cycle
--xxxxx1	32	1
--xxxx1x	16, 48	2
--xxx1xx	8, 24, 40, 56	4
--xx1xxx	4, 12, 20, 28, 36, 44, 52, 60	8
--x1xxxx	2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62	16
--1xxxxx	1, 3, 5, 7, ...61, 63	32

Figure 8-2 14-Bit PWM Output Waveform

In order to prevent transient noise at the output during MCU write to the 8-bit PWM and 6-bit BRM registers, double buffering is used. Programming of the 2 registers must follow the sequence as shown below:

```
LDA BRM_value
STA $35      ;Data put in 6-bit BRM buffer
LDA PWM_value
STA $36      ;Load 6-bit BRM and 8-bit PWM register
```

The instruction STA $35 simply puts the 6-bit BRM data in a buffer. Output is not affected at this time. The instruction STA $36, then, puts the total 14-bit data to BRM and PWM register at the same time. Output waveform will change accordingly starting from the beginning of the next PWM cycle.

9
ON-SCREEN DISPLAY

9.1 Introduction

The PLL-based On-Screen Display module displays programmable number of rows of symbols, be them characters or graphic symbols, either in a 16x16 dot matrix or in a 12x16 dot matrix over a full TV screen. It supports double scan mode for TV broadcast systems which implement non-interlaced scan broadcast. In double scan mode, each horizontal line in the character dot matrix will be displayed twice. Users have to determine if the target TV system is an interlaced or non-interlaced TV system. Auto TV system detection is not implemented.

The essence of this OSD module consists of four row buffers for displaying screen characters; with each row buffer having its own vertical position registers. Row buffers are refreshed if more than four rows of display are required. The PLL enables the OSD to adapt to any shift or change in the incoming horizontal flyback frequency. Frame display fade-in and fade-out features are supported for smooth display appearance and disappearance.

Besides the 128-character ROM/EPROM for fixed character patterns, there is a 16-character RAM for user defined patterns. This character RAM can be written and read by the CPU, but read-only by the OSD hardware. Since the contents of this character RAM can be changed during run-time, the user can have a large number of character sets stored in internal ROM, or in external ROM/EPROM/EEPROMs and have them load in via the M-bus.

The character dot matrix can be programmed to be either 12x16 or 16x16. Mixture of character dot matrices is not permissible on a row. There is no space between adjacent character dot matrices. The 12x16 dot matrix is mainly used for English-type characters; whereas the 16x16 dot matrix is mainly used for character sets requiring bigger dot matrix to create legible fonts, such as Korean, Chinese, and Kanji. Each row buffer can display 32 characters for a 12x16 configuration, and 24 characters for a 16x16 configuration.

Character blinking, black-edge (bordering or shadowing), and background color features are supported. Background and blinking features are on per character basis; whereas bordering feature is on per row basis. Users have to be careful while designing their character fonts so that bordering effect is not nullified between adjacent characters in the same row or in two consecutive rows.

The video mute function, when enabled, blocks off all TV video signals; but OSD signals remain. This feature can be used when, for example, the selected channel does not have any valid broadcast signals. Rather than displaying snow flakes on the screen, the OSD mute function can be activated to cover up the snow flakes and replace them by one of three color selections: black, green or blue. Video mute can be synchronized with vertical flyback signal so that muting always occurs on vertical flyback boundary to avoid inconsistent display in the same display field, be it even or odd. To facilitate this, OSD interrupt activated by the leading edge of vertical flyback is implemented. Whenever the video mute function is activated, fast blanking signal will be constantly activated until video mute function is deactivated. As a result, half tone feature is disabled while video mute is activated.

Ten pins are used for the OSD module; HFLBK, VFLBK, VCO, RP, FBKG, R, G, B, I, and HTONE. The I and HTONE pins are shared with port PF2 and PF3 respectively. HTONE (half tone) is used to create transparent background effect on the screen.

OSD registers are divided into four groups; with characters register group defining individual character features, frame register group defining frame features, row register group defining individual row features, and finally status register carrying the status of the whole OSD module.

9.2 Features

Frame/Row Features

- PLL-based clock source
- Four display row buffers
- Programmable R/G/B, I, fast blanking, and half tone output polarity and H/V sync input polarity
- Programmable row V and frame H start positions
- 12x16 or 16x16 character dot matrix selection on per row basis
- 32 (12x16 dot matrix) or 24 (16x16 dot matrix) symbols per row
- 8 common color palettes for both symbol color and background color
- 16 color selections per palette
- Frame fade in and fade out feature for smooth display appearance and disappearance
- Four row character size selections: 1Hx1V, 2Hx2V, 3Hx3V, and 4Hx4V
- Row character black-edge features: bordering or shadowing
- Double scan mode support for non-interlaced scan TV system
- Half tone capability for creating transparent background effect
- Video mute. Three color selections for video mute: black, green, and blue

- Interrupt on the leading edge of vertical flyback signal

Character Features

- 128-character ROM/EPROM plus 16-character RAM. Character RAM is dual ported
- Character attribute is on per character basis
- Individually controllable character background
- Character blinking with four blinking rates

9.3 Characters

Characters are stored in a 128-character ROM and a 16-character RAM. The 128 pairs of character registers are equally allocated for the 4 row buffers, each have 32 pairs. Each pair of character registers consists of the Character Code register and the Character Attribute register. The Character Code register selects the particular character from the character ROM/EPROM/RAM. The Character Attribute register selects the color, background, and blinking features for that selected character.

9.3.1 Character RAM

OSD character RAM is a dual ported RAM, consisting of 16x(16x16)/8=512 bytes of RAM; located from $0400 to $05FF. Upon reset, the content of character RAM is random. Every entry of this 16-entry character RAM occupies 32 consecutive memory bytes, always starting at even addresses. Users can read and write any byte at any time. OSD can only read the character RAM. Figure 9-1 shows the memory map of one entry of the 16-entry OSD character RAM.

If 12x16 character dot matrix is selected, bit 3 to bit 0 of all low order bytes at the right-hand side of Figure 9-1 will not be used for display.

9.3.2 Character ROM/EPROM

The memory arrangement of OSD character ROM/EPROM is the same as that of character RAM. Character ROM/EPROM is not readable to the CPU in user mode. OSD character ROM is located from $8000 to $8FFF. Three characters in the Character ROM are fixed, and cannot be changed. They are shown in Figure 9-2.

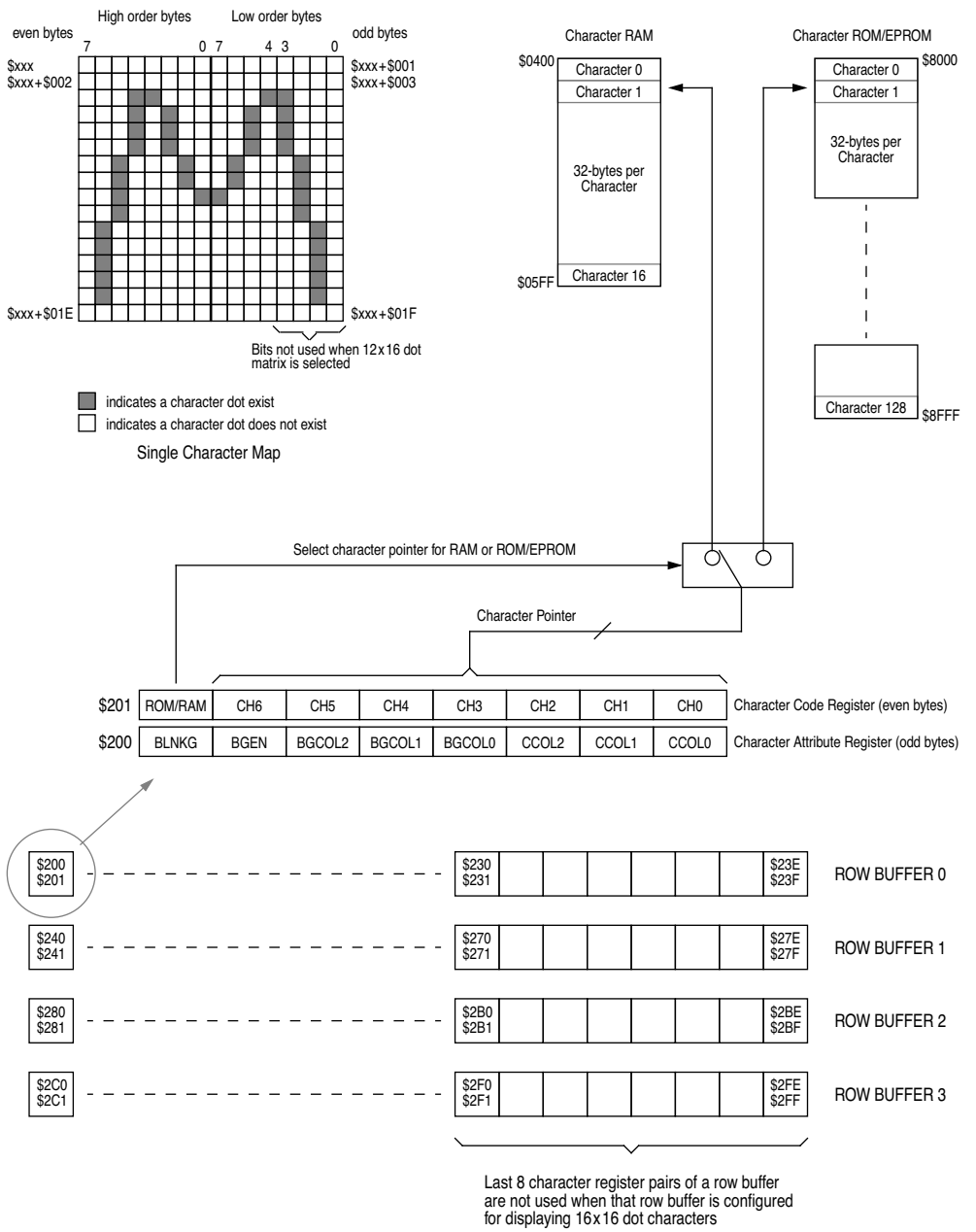


Figure 9-1 OSD Character and Row Structure

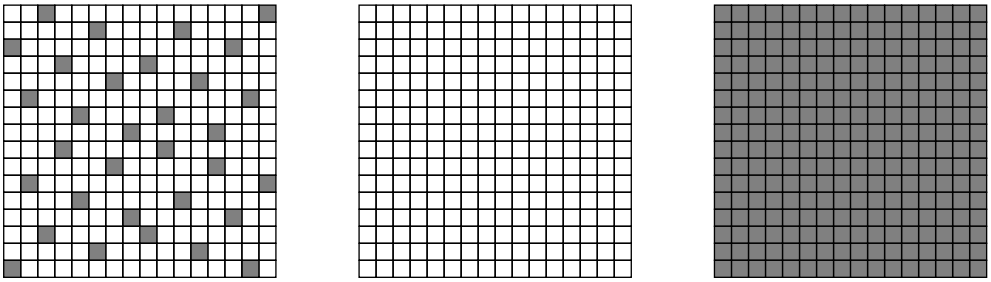


Figure 9-2 Reserved Character ROM Codes

9.3.3 Character Registers

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Character Code reg. 1	$200	ROM/RAM	CH6	CH5	CH4	CH3	CH2	CH1	CH0	uuuu uuuu
Character Attribute reg. 1	$201	BLNKG	BGEN	BGCOL2	BGCOL1	BGCOL0	CCOL2	CCOL1	CCOL0	uuuu uuuu
						:				
						:				
Character Code reg. 128	$2FE	ROM/RAM	CH6	CH5	CH4	CH3	CH2	CH1	CH0	uuuu uuuu
Character Attribute reg. 128	$2FF	BLNKG	BGEN	BGCOL2	BGCOL1	BGCOL0	CCOL2	CCOL1	CCOL0	uuuu uuuu

There are a total of 128 character code registers, 32 characters per row for four rows.

Character Codes:

ROM/RAM - ROM/RAM mapping select

1 (set) – CH6-CH0 is mapped to the 16 RAM codes.

0 (clear) – CH6-CH0 is mapped to the 128 ROM/EPROM codes.

CH6-CH0

0 to 127 = ROM/EPROM codes.

0 to 15 = RAM codes. Codes 16 and higher are invalid.

Character attributes:

BLNKG - Character blinking on/off

1 (set) – Character blinking enabled.

0 (clear) – Character blinking disabled.

The blinking speed is controlled by BR1 and BR0 in Frame Control register 2.

BGEN - Character background display on/off

1 (set) – Character background display enabled.

0 (clear) – Character background display disabled.

BGCOL2, BGCOL1, BGCOL0 - Character background color select

Selects a color from the color palette. See Section 9.3.4.

CCOL2, CCOL1, CCOL0 - Character color select

Selects a color from the color palette. See Section 9.3.4.

9.3.4 Color Palette Registers

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$1F	I1	R1	G1	B1	I0	R0	G0	B0	0000 0000
$20	I3	R3	G3	B3	I2	R2	G2	B2	0000 0000
$21	I5	R5	G5	B5	I4	R4	G4	B4	0000 0000
$22	I7	R7	G7	B7	I6	R6	G6	B6	0000 0000

Ii, Ri, Gi, and Bi bits select the color for color palette i, where i=0, 1, 2,..., 7. I bit is the intensity bit. There are 8 color palettes; each color palette is one of 16 colors. Figure 9-3 shows the color palette organization and Table 9-1 shows the RGB color map.

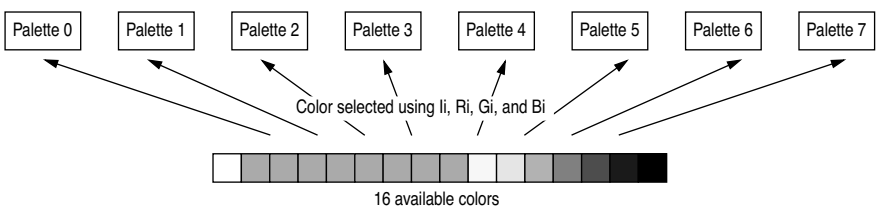


Figure 9-3 Color Palette Organization

Table 9-1 RGB Color Map

Ii	Ri	Gi	Bi	Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Yellow
0	1	1	1	White
1	0	0	0	Dark Grey
1	0	0	1	Dark Blue
1	0	1	0	Dark Green
1	0	1	1	Dark Cyan
1	1	0	0	Dark Red
1	1	0	1	Dark Magenta
1	1	1	0	Dark Yellow
1	1	1	1	Light Grey

Bit definitions may be reversed, depending on the chroma unit in the TV

9.4 Row

The OSD module has 4 row buffers for displaying on-screen characters; row 0, 1, 2 and 3. Each row buffer consists of 32 pairs of Character register pairs (See Section 9.3). There are 5 registers which affects the position and attributes of the display rows.

9.4.1 Row Attribute Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$23	MTRX3	MTRX2	MTRX1	MTRX0	R3BE	R2BE	R1BE	R0BE	0000 0000

MTRXi - Character dot matrix select for row i

1 (set) – 12x16 character dot matrix selected for row i.

0 (clear) – 16x16 character dot matrix selected for row i.

If 12x16 matrix is selected, a maximum of 32 characters may be displayed for that row. Rows selected for 16x16 matrix characters, the maximum is 24 characters per row; the remaining 8

Character register pairs are not used. See Figure 9-1. Unused Character register pairs may be used as general purpose RAM.

RiBE - Black-edge for row i enable

1 (set) – Black-edge (bordering or shadowing) for row i enabled.

0 (clear) – Black-edge (bordering or shadowing) for row i disabled.

This bit is the enable bit for the shadowing and bordering option selected by the SHDW bit in the OSD Row Horizontal Position register (bit 7 of address $28).

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Horizontal Position Register	$28	SHDW	HP6	HP5	HP4	HP3	HP2	HP1	HP0	0000 0000

SHDW - Shadow/border select

1 (set) – Shadow feature is selected if RiBE is enabled.

0 (clear) – Border feature is selected if RiBE is enabled.

This bit does not have any effect if RiBE bit is disabled.

9.4.2 Row Vertical Position Registers

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Row 0 Vertical Position Register	$24	FBKGC0	R0VP6	R0VP5	R0VP4	R0VP3	R0VP2	R0VP1	R0VP0	0000 0000
Row 1 Vertical Position Register	$25	FBKGC1	R1VP6	R1VP5	R1VP4	R1VP3	R1VP2	R1VP1	R1VP0	0000 0000
Row 2 Vertical Position Register	$26	FBKGC2	R2VP6	R2VP5	R2VP4	R2VP3	R2VP2	R2VP1	R2VP0	0000 0000
Row 3 Vertical Position Register	$27	FBKGC3	R3VP6	R3VP5	R3VP4	R3VP3	R3VP2	R3VP1	R3VP0	0000 0000

FBKGCi - FBKG (Fast Blanking) pin active select

1 (set) – FBKG pin is active during row i character dots only.

0 (clear) – FBKG pin is active during both row i character and row i background dots.

FBKGCi bit controls the FBKG output pin of the OSD during row i display. If FBKGCi is clear, FBKG output pin is active during both character dots and background dots of row i. If FBKGCi is set, FBKG output pin is active only where character dots exist in the character dot matrix (including bordering or shadowing dots). The FBKG and HTONE pins may be used to create transparent background effects for OSD displays.

Figure 9-4 and Figure 9-5 illustrate the timing signals of R, G, B, I, FBKG, and HTONE as a function of control bits BGEN, RiBE, and FBKGCi, using the 5th line (line 4) of a 12x16 dot matrix as an example. All output signals assume positive polarity.

Figure 9-4 illustrates the timing of output signals for characters with and without bordering effect. Figure 9-5 illustrates the output signal timing for characters with background enabled, yet with opposite FBKGCi bit setting. Note that both RiBE and FBKGCi are row features. Hence, the two adjacent dot matrices in both figures are drawn for demonstration purposes only, they do not imply that users can configure OSD display in such a manner that one character has FBKGCi bit set and the next character in the same row has FBKGCi bit cleared. Note that 'HTONE' has exactly the same waveform as 'Background R,G,B, or I'. Output signal timing diagram similar to Figure 9-5 for the case where character bordering is enabled can be derived in very similar fashion. The only difference is that 'FBKG' will be on and 'HTONE' will be off where a bordering dot exists. Other output signal timings remain the same.

RiVP6 to RiVP0 - Row i Vertical Position

For single scan mode: Vertical position = RiVPx setting x 4

For double scan mode: Vertical position = RiVPx setting x 4 x 2

Each RiVP6-RiVP0 step shifts the vertical position of row i by 4 horizontal display lines. For single scan mode, the shift is (RiVP6-RiVP0)x4 horizontal lines. For double scan mode, the shift is ((RiVP6-RiVP0)x4) x 2 horizontal lines. The calculation of shift is a function of scan mode, not character size selection. Hence, care should be taken when choosing vertical position for a particular row that locates after a row which has character size other than the basic 12x16 or 16x16 setting. For example, assuming single scan mode, if row X has 4Hx4V character size and vertical position of $40 while row Y has basic character size of 1Hx1V and vertical position of $48, then row X will be displayed from the 256th (64x4) line to the 287th line, which covers only the first 32 lines of the supposed 64-line row X display, and row Y will be displayed from the 288th (72x4) line to 303th line without any missing lines.

The reference point of shift is the leading edge of vertical flyback input signal, VFLBK. As a result of this vertical start position granularity, there are a total of 262.5/4 row positions in a full screen.

In Figure 9-6(a), row (i+1) and row i partially overlaps. Since the vertical position of row (i+1) is lower than row i, row (i+1) will be partially covered by row i. New symbols may be generated when rows are partially overlapped.

In Figure 9-6(b), row (j+1) is completely covered by row j. As result, only row j is visible.

Note that in cases where the character size of the blocked row is bigger than that of the blocking row, once the blocked row has been blocked, it will never be displayed again even after the blocking row display has been terminated. For example, assume the character size of row (i+1) is 4Hx4V and that of row i is 1Hx1V, and the difference in vertical position between them is 4 horizontal lines only. After the first four lines of row (i+1) have been displayed, row i display will commence and continue for the next sixteen lines, blocking off row (i+1) display for these sixteen lines. After row i display has been terminated, there are still (64-4-16)=44 lines of row (i+1) display

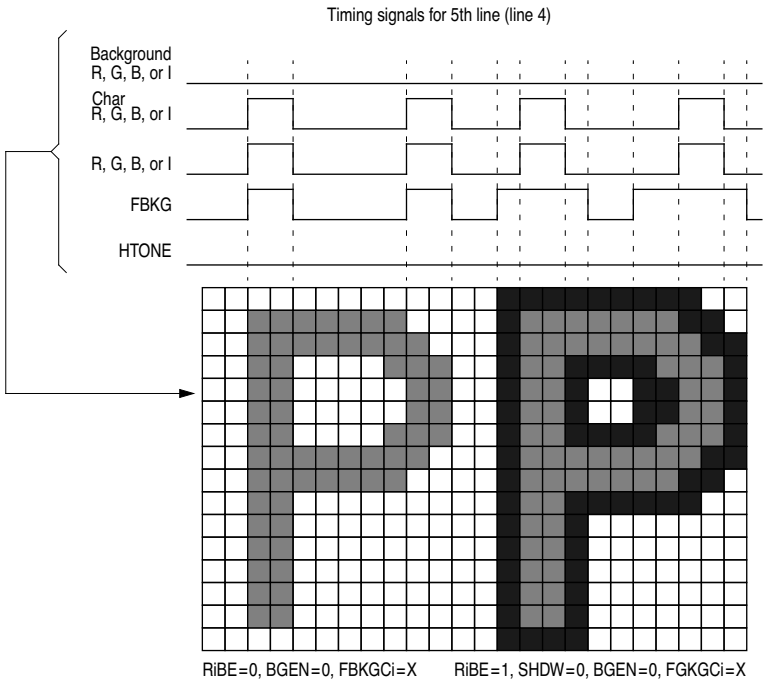


Figure 9-4 Output Signal Timing Diagram - Without Background

that could have been displayed, the OSD is so designed that these remaining lines will not be displayed. The same result applies to the complete overlap situation with different character sizes.

A row display is terminated if:

1) the part of the row display which is not overridden by other overlapping rows has been completed, or
2) it completely overlaps a row or rows with higher priority, or
3) the part of the row display which does not overlap vertical retrace period has been completed. (This applies to rows immediately before vertical retrace)

Note that the judgement of overlap is totally based on the vertical position of rows, it has nothing to do with character size of rows. RiCF bit of Frame Control 3 and Status register will also be set when a row display is terminated.

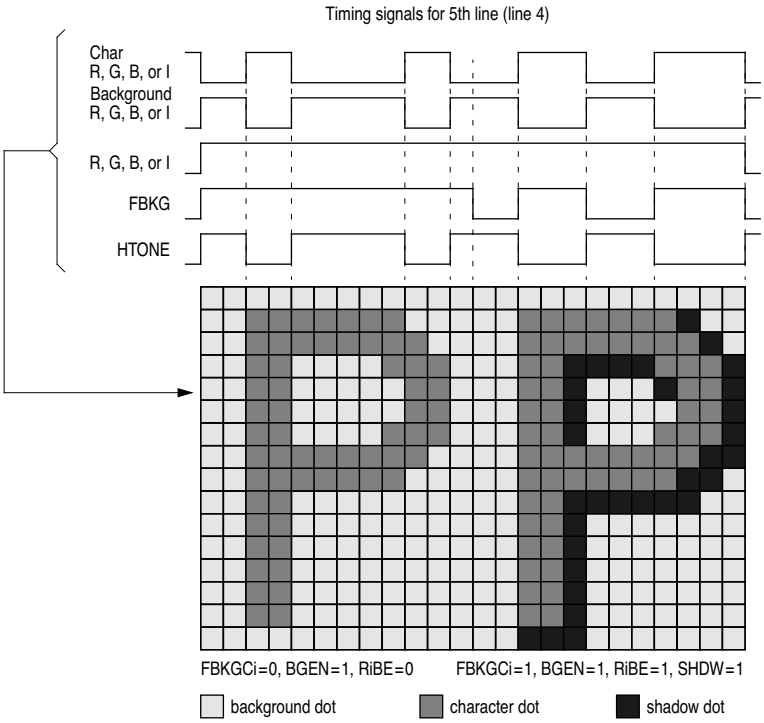


Figure 9-5 Output Signal Timing Diagram - With Background

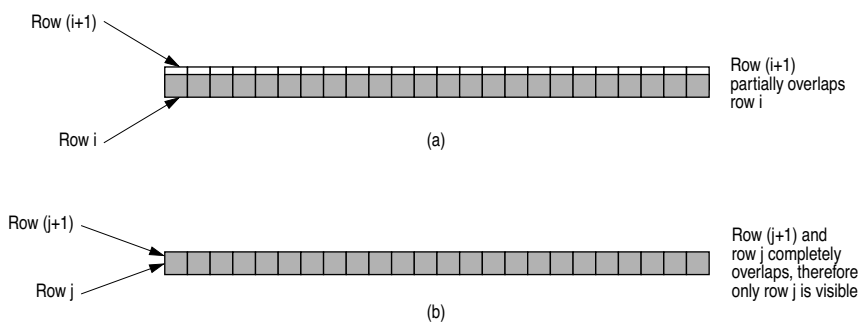


Figure 9-6 Resolution of Overlap among Rows

9.4.3 Row Horizontal Position Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$28	SHDW	HP6	HP5	HP4	HP3	HP2	HP1	HP0	0000 0000

SHDW - Shadow/border select

1 (set) – Shadow feature is selected if RiBE is enabled. See Section 9.4.1.

0 (clear) – Border feature is selected if RiBE is disabled. See Section 9.4.1.

HP6 to HP0 - Horizontal Position

Each (HP6-HP0) step shifts the horizontal position of all four rows by 4 dots. The reference point of shift is the leading edge of horizontal flyback signal. Note that there is only one Row Horizontal Position register for all 4 row buffers, therefore all rows will have the same horizontal start point.

If (HP6-HP0) is so programmed that part of the row display goes beyond the beginning of a horizontal flyback signal, display wrap-around occurs. That is, all lines of the row display will have all dots before the nth horizontal flyback displayed on one line and all remaining dots after the nth horizontal flyback, along with all dots of next line before the (n+1)th horizontal flyback displayed on the next line.

9.4.4 Row Control Register 1

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$29	R3INTE	R2INTE	R1INTE	R0INTE	R3EN	R2EN	R1EN	R0EN	0000 0000

RiINTE - Row interrupt

1 (set) – Row interrupt enabled.

0 (clear) – Row interrupt disabled.

Enable/disable interrupt of row i if one of the following conditions occur:

1) the part of the row i display which is not overridden by other overlapping rows has been completed, or
2) the part of the row i display which does not overlap vertical retrace period has been completed.

Note that for the case where row i is completely overlapped by other rows, row i display has never really happened, that is, terminated upon its commencement, row i interrupt will never occur.

RiEN - Row i display enable

1 (set) – Row i display enabled.

0 (clear) – Row i display disabled.

If RiEN bit is set while the horizontal line currently being displayed has already passed the vertical start position of this recently enabled row, this recently enabled row will not be displayed in this frame. It will then be displayed in the next frame. That is, RiEN bit has to be set before current horizontal display line reaches ((RiVP6-RiVP0)x4) for single scan mode or ((RiVP6-RiVP0)x4)x2 for double scan mode to enable display of row i in current frame.

Note that clearing RiEN bit does not clear the corresponding RiCF bit. Hence, care must be taken before enabling RiINTE and RiEN to avoid interrupt caused by uncleared RiCF before the setting of RiINTE and RiEN.

9.4.5 Row Control Register 2

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$2A	R3CHS1	R3CHS0	R2CHS1	R2CHS0	R1CHS1	R1CHS0	R0CHS1	R0CHS0	0000 0000

RiCHS1, RiCHS0 - Row i character size

RiCHS1	RiCHS0	Character size of row i
0	0	basic - 1Hx1V
0	1	Single expanded - 2Hx2V
1	0	Double expanded - 3Hx3V
1	1	Triple expanded - 4Hx4V

There are two predefined numbers of total dots that can be displayed on a horizontal line. The number of dots per line is a function of character size selection and the size of character dot matrix. For the special case of 3Hx3V and 12x16 dot matrix, the number of total dots per line is 396; whereas for other combinations of character size and dot matrix, the number is 384 dots per line. Users can avoid filling the unused bytes in a row since these bytes will not be displayed. Table 9-2 lists the number of valid character bytes per row.

9.5 Frame

The following registers affect the frame of an OSD displays.

Table 9-2 Number of Visible Characters Per Row

char size \ dot matrix	16x16	12x16
1H x 1V	24	32
2H x 2V	12	16
3H x 3V	8	11
4H x 4V	6	8

9.5.1 Frame Control 1 and Row Count Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$1D	PLLEN	DSCAN	FADE	ON/OFF	CDRC3	CDRC2	CDRC1	CDRC0	0000 0000

Bits 7 to 4 are control bits and, bits 3 to 0 are status bits.

PLLEN - PLL enable bit

1 (set) – PLL enabled for OSD clock source.

0 (clear) – PLL disabled.

DSCAN - Double/Single scan mode select

1 (set) – Double scan mode.

0 (clear) – Single scan mode.

DSCAN (double scan) bit is for the control of OSD logic so that the OSD can accommodate non-interlaced scan TV system by adjusting dot matrix scan output. Users have to determine if the target TV broadcast system is a double scan system. If DSCAN is set, all horizontal lines in the character dot matrix will be displayed twice in the same frame. The other feature associated with horizontal lines that will also be doubled is the RiVP6-RiVP0 field of Row Vertical Position Registers.

FADE - Display fade enable

1 (set) – Display fade function enabled.

0 (clear) – Display fade function disabled.

The FADE bit controls the sequence of frame display appearance and disappearance. When FADE bit is set, frame display will gradually appear (fade in) if ON/OFF is set, and gradually disappear (fade out) if ON/OFF is clear. If FADE bit is clear, OSD display will be turned on or off instantly.

ON/OFF - OSD display on/off

1 (set) – OSD display on.

0 (clear) – OSD display off.

For the fading feature, the whole screen is divided into several 16-horizontal-line segments. Notice that a row might not fit into the 16-horizontal-line segments. It might cross two segments, depending on the vertical position of a row. The way that fade-in feature works is that one line in all 16-line segments will appear in the first fading sequence; two lines, including the one line in the first fading sequence, will appear in the second fading sequence; four lines, including the two lines in the second fading sequence, will appear in the third fading sequence; eight lines, including the four lines in the third fading sequence, will appear in the fourth fading sequence; and finally, all sixteen lines, including the eight lines in the fourth fading sequence, will appear in the fifth fading sequence. Fade-out feature works in the opposite manner, that is, the number of display lines to be disappeared are 8 lines, 12 lines, 14 lines, 15 lines, and all 16 lines in each disappearance sequence, respectively. Fade out sequence for a character in a row fitting right into the 16-horizontal-line segment is illustrated in Figure 9-7. Fading rate is fixed at 32 frames per sequence. Therefore, it takes 160 frames to execute the fade function. At 60 Hz vertical frequency, this will take five plus seconds. Note that when display disappears, all output pins are not tri-stated, rather they remain in their deserted states.

CDRC3 to CDRC0 - Terminated display rows

These status bits reflect the number of row displays that have been terminated. These bits are reset only by vertical flyback and incremented by one every time a row display has been terminated.

9.5.2 Frame Control Register 2

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$1E	BR1	BR0	VFPOL	HFPOL	HTPOL	FBPOL	RGBPOL	IPOL	0000 0000

BR1, BR0 - Blink rate select

These bits control the blinking rate of all symbols on the TV screen. The on/off ratio of blinking is always 3/1.

VFPOL - VFLBK input polarity select

1 (set) – Vertical flyback signal at VFLBK is active low.

0 (clear) – Vertical flyback signal at VFLBK is active high.

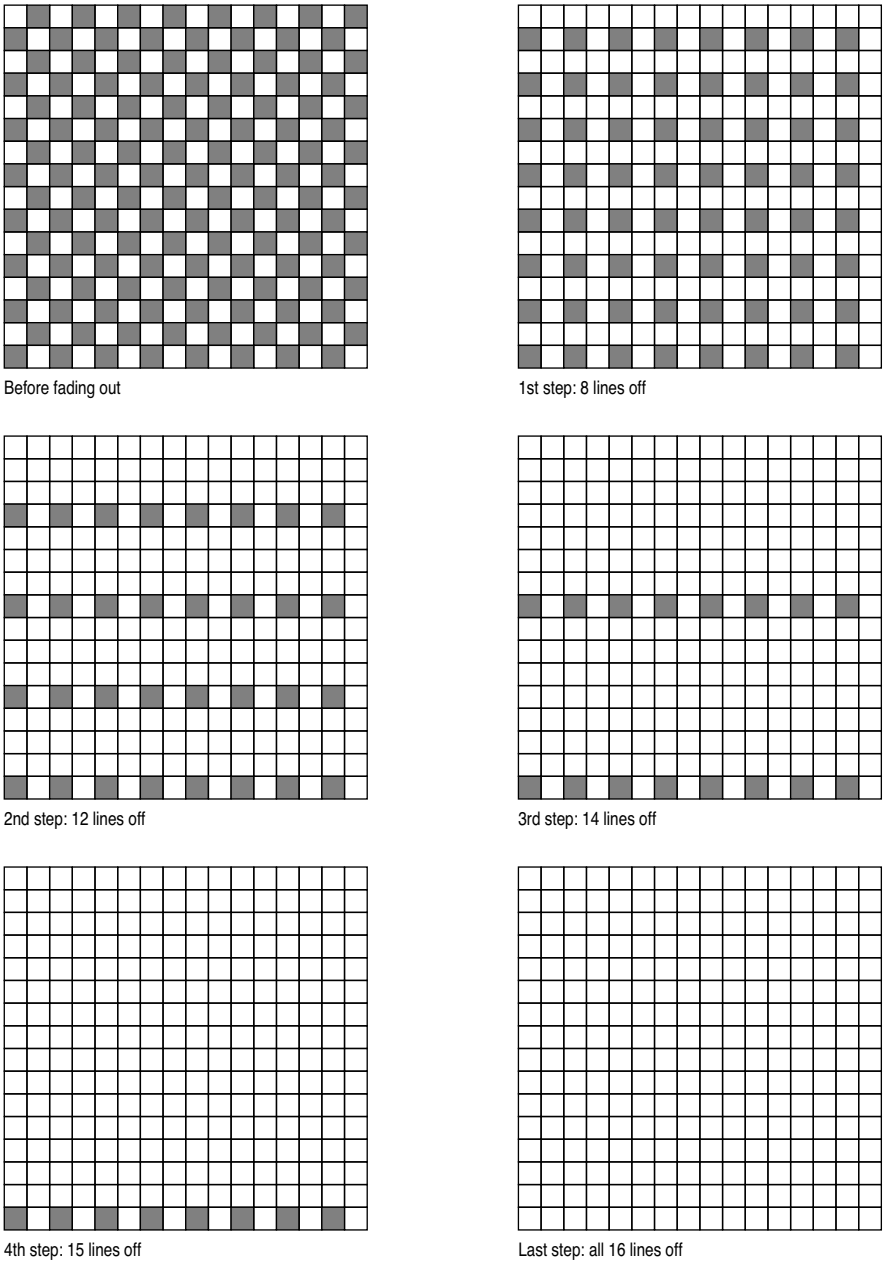


Figure 9-7 Fading Out Sequence

BR1	BR0	On-Time (frames)	Off-Time (frames)
0	0	24	8
0	1	48	16
1	0	96	32
1	1	192	64

HFPOL - HFLBK input polarity select

1 (set) – Horizontal flyback signal at HFLBK is active low.

0 (clear) – Horizontal flyback signal at HFLBK is active high.

HTPOL - FBKG output polarity select

1 (set) – HTONE (half tone) output pin is active low.

0 (clear) – HTONE (half tone) output pin is active high.

The HTONE output pin is shared with port pin PF3. If HTONE is disabled, HTPOL will have no effect.

FBPOL - FBKG output polarity select

1 (set) – FBKG (fast blanking) output pin is active low.

0 (clear) – FBKG (fast blanking) output pin is active high.

RGBPOL - RGB output polarity select

1 (set) – RBG output pins are active low.

0 (clear) – RGB output pins are active high.

IPOL - I output polarity select

1 (set) – I (intensity) output pin is active low.

0 (clear) – I (intensity) output pin is active high.

9.5.3 Frame Control 3 and Status Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$2B	VFINTE	MUTE1	MUTE0	VFLB	R3CF	R2CF	R1CF	R0CF	0000 0000

Bits 7 to 5 are control bits whereas bits 4 to 0 are status bits associated with interrupt. A status bit is cleared by writing a 0 to that bit. Care must be taken while clearing a status bit: make sure the

status bit to be cleared is indeed one before writing a zero, and do not write a 0 to a status bit which is not 1. Otherwise, status bits which are becoming ones will be inadvertently cleared.

VFINTE - VFLBK interrupt enable

1 (set) – Vertical flyback interrupt enabled.

0 (clear) – Vertical flyback interrupt disabled.

MUTE1, MUTE0 - Video mute enable

MUTE1	MUTE0	Function
0	0	No video mute
0	1	Mute with black color
1	0	Mute with G color
1	1	Mute with B color

VFLB - VFLBK status

1 (set) – Vertical flyback (leading edge) signal detected.

0 (clear) – No Vertical flyback signal detected.

RiCF - Row i display status

1 (set) – Row i display has been terminated.

0 (clear) – Row i display has been not terminated.

Whenever a row display has been terminated, the corresponding RiCF flag will be set along with update of CDRC3-CDRC0 field.

10
ANALOG TO DIGITAL CONVERTER

The Analog-to-Digital Converter (ADC) system consists of two analog input channels and a single 5-bit D/A Converter and Comparator, with continuous conversion. A result flag indicates if the comparator output is above or below the analog Input. ADC is disabled by setting AD4 to AD0 bits of ADC Control/Status register to all 1's. This disable function is mainly for low power applications.

Figure 10-1 shows a block diagram of the ADC module.

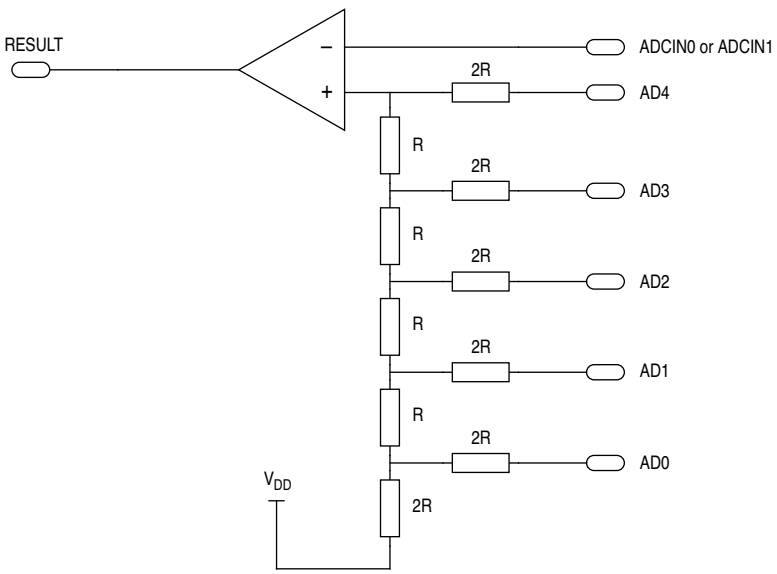


Figure 10-1 ADC Block Diagram

10.1 ADC Inputs

The ADC has two input channels: one dedicated input pin at ADCIN0 and one shared pin at PF4/ADCIN1.

10.1.1 PF4/ADCIN1

ADCIN1 multiplexes with PF4 at this pin. When the ADC1 bit of Port F Configuration register is cleared, PF4/ADCIN1 is configured for PF4 and follows Port F DDR assignment. When ADC1 bit is set, PF4 is configured as ADCIN1 analog input, and Port F DDR has no effect on this pin. Reading PF4 when configured as an ADC input is zero.

10.1.2 ADCIN0

ADCIN0 is a dedicated analog input channel.

10.2 Program Example

The following example shows how to convert analog input channel 0 (ADCIN0). For ADCIN1 conversion, change #$00 to #$20. ADCSR is the ADC Control/Status register.

```
       LDA    #$00
       STA    ADCSR         ;ADC Control and Status Register
DTA    BRSET  7, ADCSR, ATD
       INC    ADCSR
       LDA    ADCSR
       AND    #$1F
       CMP    #$1F
       BLS    DTA
;out of range
ATD    ...    ;analog value in ADC.
              ;ANALOG IN = ([AD4:0] +1)*0.15625V at Vdd = 5V
```

10.3 ADC Control and Status Register

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$3C	RESULT		CHNL	AD4	AD3	AD2	AD1	AD0	u000 0000

This read/write register, located at address $3C, contains six control bits and one status bit.

RESULT - Comparator Status (Read Only)

1 (set) – AD4-0 value greater than analog in.

0 (clear) – AD4-0 value is less than analog in.

CHNL - Channel Select

1 (set) – ADCIN1 is selected for conversion.

0 (clear) – ADCIN0 is selected for conversion

AD4-0 - ADC Digital Result

These bits are written by the user to perform successive approximations in software. When a value causes the RESULT bit to change state from the value immediately before or after it, AD4-0 are considered to be the digital equivalent of the analog input. Note that when AD4-0 are all 1's, ADC is virtually turned off to minimize power consumption.

THIS PAGE LEFT BLANK INTENTIONALLY

11
CPU CORE AND INSTRUCTION SET

This section provides a description of the CPU core registers, the instruction set and the addressing modes of the MC68HC05L1.

11.1 Registers

The MCU contains five registers, as shown in the programming model of Figure 11-1. The interrupt stacking order is shown in Figure 11-2.

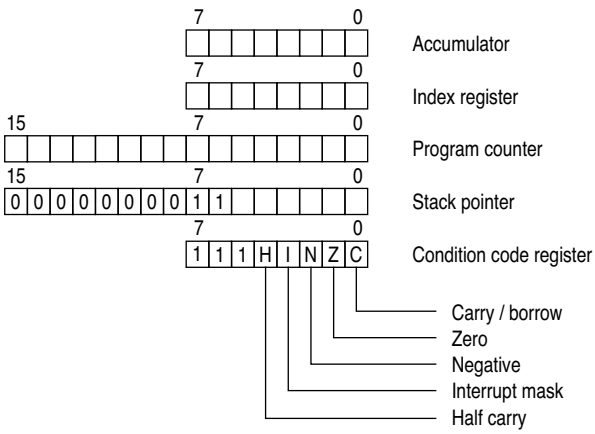


Figure 11-1 Programming model

11.1.1 Accumulator (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

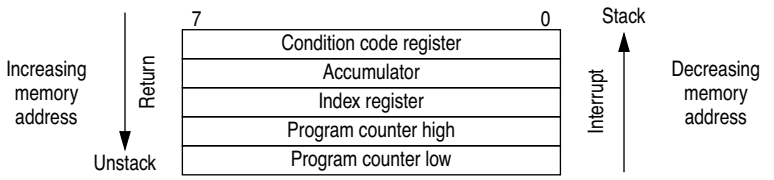


Figure 11-2 Stacking order

11.1.2 Index register (X)

The index register is an 8-bit register, which can contain the indexed addressing value used to create an effective address. The index register may also be used as a temporary storage area.

11.1.3 Program counter (PC)

The program counter is a 16-bit register, which contains the address of the next byte to be fetched.

11.1.4 Stack pointer (SP)

The stack pointer is a 16-bit register, which contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the ten most significant bits are permanently set to 0000000011. These ten bits are appended to the six least significant register bits to produce an address within the range of $00C0 to $00FF. Subroutines and interrupts may use up to 64 (decimal) locations. If 64 locations are exceeded, the stack pointer wraps around and overwrites the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.

11.1.5 Condition code register (CCR)

The CCR is a 5-bit register in which four bits are used to indicate the results of the instruction just executed, and the fifth bit indicates whether interrupts are masked. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.

Half carry (H)

This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

Interrupt (I)

When this bit is set, all maskable interrupts are masked. If an interrupt occurs while this bit is set, the interrupt is latched and remains pending until the interrupt bit is cleared.

Negative (N)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative.

Zero (Z)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

Carry/borrow (C)

When set, this bit indicates that a carry or borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions and during shifts and rotates.

11.2 Instruction set

The MCU has a set of 62 basic instructions. They can be grouped into five different types as follows:

- Register/memory
- Read/modify/write
- Branch
- Bit manipulation
- Control

The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

This MCU uses all the instructions available in the M146805 CMOS family plus one more: the unsigned multiply (MUL) instruction. This instruction allows unsigned multiplication of the contents of the accumulator (A) and the index register (X). The high-order product is then stored in the index register and the low-order product is stored in the accumulator. A detailed definition of the MUL instruction is shown in Table 11-1.

11.2.1 Register/memory Instructions

Most of these instructions use two operands. The first operand is either the accumulator or the index register. The second operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 11-2 for a complete list of register/memory instructions.

11.2.2 Branch instructions

These instructions cause the program to branch if a particular condition is met; otherwise, no operation is performed. Branch instructions are two-byte instructions. Refer to Table 11-3.

11.2.3 Bit manipulation instructions

The MCU can set or clear any writable bit that resides in the first 256 bytes of the memory space (page 0). All port data and data direction registers, timer and serial interface registers, control/status registers and a portion of the on-chip RAM reside in page 0. An additional feature allows the software to test and branch on the state of any bit within these locations. The bit set, bit clear, bit test and branch functions are all implemented with single instructions. For the test and branch instructions, the value of the bit tested is also placed in the carry bit of the condition code register. Refer to Table 11-4.

11.2.4 Read/modify/write instructions

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to this sequence of reading, modifying and writing, since it does not modify the value. Refer to Table 11-5 for a complete list of read/modify/write instructions.

11.2.5 Control instructions

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 11-6 for a complete list of control instructions.

11.2.6 Tables

Tables for all the instruction types listed above follow. In addition there is a complete alphabetical listing of all the instructions (see Table 11-7), and an opcode map for the instruction set of the M68HC05 MCU family (see Table 11-8).

Table 11-1 MUL instruction

Operation	**X:A ← X*A**			
Description	Multiplies the eight bits in the index register by the eight bits in the accumulator and places the 16-bit result in the concatenated accumulator and index register.			
Condition codes	H : Cleared I : Not affected N : Not affected Z : Not affected C : Cleared			
Source	MUL			
Form	Addressing mode Inherent	Cycles 11	Bytes 1	Opcode $42

Table 11-2 Register/memory instructions

		Addressing modes																	
		Immediate			**Direct**			**Extended**			**Indexed (no offset)**			**Indexed (8-bit offset)**			**Indexed (16-bit offset)**		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**
Load A from memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in memory	STA				B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in memory	STX				BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add memory and carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract memory from A with borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND memory with A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic compare A with memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic compare X with memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit test memory with A (logical compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump unconditional	JMP				BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to subroutine	JSR				BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

Table 11-3 Branch instructions

		Relative addressing mode		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**
Branch always	BRA	20	2	3
Branch never	BRN	21	2	3
Branch if higher	BHI	22	2	3
Branch if lower or same	BLS	23	2	3
Branch if carry clear	BCC	24	2	3
(Branch if higher or same)	(BHS)	24	2	3
Branch if carry set	BCS	25	2	3
(Branch if lower)	(BLO)	25	2	3
Branch if not equal	BNE	26	2	3
Branch if equal	BEQ	27	2	3
Branch if half carry clear	BHCC	28	2	3
Branch if half carry set	BHCS	29	2	3
Branch if plus	BPL	2A	2	3
Branch if minus	BMI	2B	2	3
Branch if interrupt mask bit is clear	BMC	2C	2	3
Branch if interrupt mask bit is set	BMS	2D	2	3
Branch if interrupt line is low	BIL	2E	2	3
Branch if interrupt line is high	BIH	2F	2	3
Branch to subroutine	BSR	AD	2	6

Table 11-4 Bit manipulation instructions

		Addressing modes					
		Bit set/clear			Bit test and branch		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**
Branch if bit n is set	BRSET n (n=0–7)				2•n	3	5
Branch if bit n is clear	BRCLR n (n=0–7)				01+2•n	3	5
Set bit n	BSET n (n=0–7)	10+2•n	2	5			
Clear bit n	BCLR n (n=0–7)	11+2•n	2	5			

Table 11-5 Read/modify/write instructions

		Addressing modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (no offset)			Indexed (8-bit offset)		
Function	Mnemonic	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles	Opcode	# Bytes	# Cycles
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (two's complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate left through carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate right through carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical shift left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical shift right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic shift right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for negative or zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5
Multiply	MUL	42	1	11												

Table 11-6 Control instructions

		Inherent addressing mode		
Function	Mnemonic	Opcode	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set carry bit	SEC	99	1	2
Clear carry bit	CLC	98	1	2
Set interrupt mask bit	SEI	9B	1	2
Clear interrupt mask bit	CLI	9A	1	2
Software interrupt	SWI	83	1	10
Return from subroutine	RTS	81	1	6
Return from interrupt	RTI	80	1	9
Reset stack pointer	RSP	9C	1	2
No-operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

Table 11-7 Instruction set

Mnemonic	Addressing modes										Condition codes				
	INH	IMM	DIR	EXT	REL	IX	IX1	IX2	BSC	BTB	H	I	N	Z	C
ADC											◊	•	◊	◊	◊
ADD											◊	•	◊	◊	◊
AND											•	•	◊	◊	•
ASL											•	•	◊	◊	◊
ASR											•	•	◊	◊	◊
BCC											•	•	•	•	•
BCLR											•	•	•	•	•
BCS											•	•	•	•	•
BEQ											•	•	•	•	•
BHCC											•	•	•	•	•
BHCS											•	•	•	•	•
BHI											•	•	•	•	•
BHS											•	•	•	•	•
BIH											•	•	•	•	•
BIL											•	•	•	•	•
BIT											•	•	◊	◊	•
BLO											•	•	•	•	•
BLS											•	•	•	•	•
BMC											•	•	•	•	•
BMI											•	•	•	•	•
BMS											•	•	•	•	•
BNE											•	•	•	•	•
BPL											•	•	•	•	•
BRA											•	•	•	•	•
BRN											•	•	•	•	•
BRCLR											•	•	•	•	◊
BRSET											•	•	•	•	◊
BSET											•	•	•	•	•
BSR											•	•	•	•	•
CLC											•	•	•	•	0
CLI											•	0	•	•	•
CLR											•	•	0	1	•
CMP											•	•	◊	◊	◊

Address mode abbreviations

BSC	Bit set/clear	IMM	Immediate
BTB	Bit test & branch	IX	Indexed (no offset)
DIR	Direct	IX1	Indexed, 1 byte offset
EXT	Extended	IX2	Indexed, 2 byte offset
INH	Inherent	REL	Relative

Not implemented

Condition code symbols

H	Half carry (from bit 3)	◊	Tested and set if true, cleared otherwise
I	Interrupt mask	•	Not affected
N	Negate (sign bit)	?	Load CCR from stack
Z	Zero	0	Cleared
C	Carry/borrow	1	Set

Table 11-7 Instruction set (Continued)

Mnemonic	Addressing modes										Condition codes				
	INH	IMM	DIR	EXT	REL	IX	IX1	IX2	BSC	BTB	H	I	N	Z	C
COM											•	•	◊	◊	1
CPX											•	•	◊	◊	◊
DEC											•	•	◊	◊	•
EOR											•	•	◊	◊	•
INC											•	•	◊	◊	•
JMP											•	•	•	•	•
JSR											•	•	•	•	•
LDA											•	•	◊	◊	•
LDX											•	•	◊	◊	•
LSL											•	•	◊	◊	◊
LSR											•	•	0	◊	◊
MUL											0	•	•	•	0
NEG											•	•	◊	◊	◊
NOP											•	•	•	•	•
ORA											•	•	◊	◊	•
ROL											•	•	◊	◊	◊
ROR											•	•	◊	◊	◊
RSP											•	•	•	•	•
RTI											?	?	?	?	?
RTS											•	•	•	•	•
SBC											•	•	◊	◊	◊
SEC											•	•	•	•	1
SEI											•	1	•	•	•
STA											•	•	◊	◊	•
STOP											•	0	•	•	•
STX											•	•	◊	◊	•
SUB											•	•	◊	◊	◊
SWI											•	1	•	•	•
TAX											•	•	•	•	•
TST											•	•	◊	◊	•
TXA											•	•	•	•	•
WAIT											•	0	•	•	•

Address mode abbreviations

BSC	Bit set/clear	IMM	Immediate
BTB	Bit test & branch	IX	Indexed (no offset)
DIR	Direct	IX1	Indexed, 1 byte offset
EXT	Extended	IX2	Indexed, 2 byte offset
INH	Inherent	REL	Relative

Not implemented

Condition code symbols

H	Half carry (from bit 3)	◊	Tested and set if true, cleared otherwise
I	Interrupt mask	•	Not affected
N	Negate (sign bit)	?	Load CCR from stack
Z	Zero	0	Cleared
C	Carry/borrow	1	Set

Table 11-8 M68HC05 opcode map

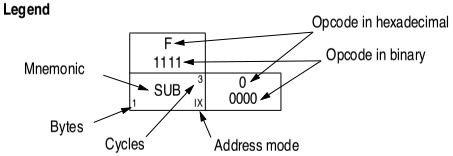
	Bit manipulation		Branch	Read/modify/write					Control		Register/memory						
	BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	High
High / Low	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Low
0 0000	BRSET0 5 3 BTB	BSET0 5 2 BSC	BRA 3 2 REL	NEG 5 2 DIR	NEGA 3 1 INH	NEGX 3 1 INH	NEG 6 2 IX1	NEG 5 1 IX	RTI 9 1 INH		SUB 2 2 IMM	SUB 3 2 DIR	SUB 4 3 EXT	SUB 5 3 IX2	SUB 4 2 IX1	SUB 3 1 IX	0 0000
1 0001	BRCLR0 5 3 BTB	BCLR0 5 2 BSC	BRN 3 2 REL						RTS 6 1 INH		CMP 2 2 IMM	CMP 3 2 DIR	CMP 4 3 EXT	CMP 5 3 IX2	CMP 4 2 IX1	CMP 3 1 IX	1 0001
2 0010	BRSET1 5 3 BTB	BSET1 5 2 BSC	BHI 3 2 REL		MUL 11 1 INH						SBC 2 2 IMM	SBC 3 2 DIR	SBC 4 3 EXT	SBC 5 3 IX2	SBC 4 2 IX1	SBC 3 1 IX	2 0010
3 0011	BRCLR1 5 3 BTB	BCLR1 5 2 BSC	BLS 3 2 REL	COM 5 2 DIR	COMA 3 1 INH	COMX 3 1 INH	COM 6 2 IX1	COM 5 1 IX	SWI 10 1 INH		CPX 2 2 IMM	CPX 3 2 DIR	CPX 4 3 EXT	CPX 5 3 IX2	CPX 4 2 IX1	CPX 3 1 IX	3 0011
4 0100	BRSET2 5 3 BTB	BSET2 5 2 BSC	BCC 3 2 REL	LSR 5 2 DIR	LSRA 3 1 INH	LSRX 3 1 INH	LSR 6 2 IX1	LSR 5 1 IX			AND 2 2 IMM	AND 3 2 DIR	AND 4 3 EXT	AND 5 3 IX2	AND 4 2 IX1	AND 3 1 IX	4 0100
5 0101	BRCLR2 5 3 BTB	BCLR2 5 2 BSC	BCS 3 2 REL								BIT 2 2 IMM	BIT 3 2 DIR	BIT 4 3 EXT	BIT 5 3 IX2	BIT 4 2 IX1	BIT 3 1 IX	5 0101
6 0110	BRSET3 5 3 BTB	BSET3 5 2 BSC	BNE 3 2 REL	ROR 5 2 DIR	RORA 3 1 INH	RORX 3 1 INH	ROR 6 2 IX1	ROR 5 1 IX			LDA 2 2 IMM	LDA 3 2 DIR	LDA 4 3 EXT	LDA 5 3 IX2	LDA 4 2 IX1	LDA 3 1 IX	6 0110
7 0111	BRCLR3 5 3 BTB	BCLR3 5 2 BSC	BEQ 3 2 REL	ASR 5 2 DIR	ASRA 3 1 INH	ASRX 3 1 INH	ASR 6 2 IX1	ASR 5 1 IX		TAX 2 1 INH		STA 4 2 DIR	STA 5 3 EXT	STA 6 3 IX2	STA 5 2 IX1	STA 4 1 IX	7 0111
8 1000	BRSET4 5 3 BTB	BSET4 5 2 BSC	BHCC 3 2 REL	LSL 5 2 DIR	LSLA 3 1 INH	LSLX 3 1 INH	LSL 6 2 IX1	LSL 5 1 IX		CLC 2 1 INH	EOR 2 2 IMM	EOR 3 2 DIR	EOR 4 3 EXT	EOR 5 3 IX2	EOR 4 2 IX1	EOR 3 1 IX	8 1000
9 1001	BRCLR4 5 3 BTB	BCLR4 5 2 BSC	BHCS 3 2 REL	ROL 5 2 DIR	ROLA 3 1 INH	ROLX 3 1 INH	ROL 6 2 IX1	ROL 5 1 IX		SEC 2 1 INH	ADC 2 2 IMM	ADC 3 2 DIR	ADC 4 3 EXT	ADC 5 3 IX2	ADC 4 2 IX1	ADC 3 1 IX	9 1001
A 1010	BRSET5 5 3 BTB	BSET5 5 2 BSC	BPL 3 2 REL	DEC 5 2 DIR	DECA 3 1 INH	DECX 3 1 INH	DEC 6 2 IX1	DEC 5 1 IX		CLI 2 1 INH	ORA 2 2 IMM	ORA 3 2 DIR	ORA 4 3 EXT	ORA 5 3 IX2	ORA 4 2 IX1	ORA 3 1 IX	A 1010
B 1011	BRCLR5 5 3 BTB	BCLR5 5 2 BSC	BMI 3 2 REL							SEI 2 1 INH	ADD 2 2 IMM	ADD 3 2 DIR	ADD 4 3 EXT	ADD 5 3 IX2	ADD 4 2 IX1	ADD 3 1 IX	B 1011
C 1100	BRSET6 5 3 BTB	BSET6 5 2 BSC	BMC 3 2 REL	INC 5 2 DIR	INCA 3 1 INH	INCX 3 1 INH	INC 6 2 IX1	INC 5 1 IX		RSP 2 1 INH		JMP 2 2 DIR	JMP 3 3 EXT	JMP 4 3 IX2	JMP 3 2 IX1	JMP 2 1 IX	C 1100
D 1101	BRCLR6 5 3 BTB	BCLR6 5 2 BSC	BMS 3 2 REL	TST 4 2 DIR	TSTA 3 1 INH	TSTX 3 1 INH	TST 5 2 IX1	TST 4 1 IX		NOP 2 1 INH	BSR 6 2 REL	JSR 5 2 DIR	JSR 6 3 EXT	JSR 7 3 IX2	JSR 6 2 IX1	JSR 5 1 IX	D 1101
E 1110	BRSET7 5 3 BTB	BSET7 5 2 BSC	BIL 3 2 REL						STOP 2 1 INH		LDX 2 2 IMM	LDX 3 2 DIR	LDX 4 3 EXT	LDX 5 3 IX2	LDX 4 2 IX1	LDX 3 1 IX	E 1110
F 1111	BRCLR7 5 3 BTB	BCLR7 5 2 BSC	BIH 3 2 REL	CLR 5 2 DIR	CLRA 3 1 INH	CLRX 3 1 INH	CLR 6 2 IX1	CLR 5 1 IX	WAIT 2 1 INH	TXA 2 1 INH		STX 4 2 DIR	STX 5 3 EXT	STX 6 3 IX2	STX 5 2 IX1	STX 4 1 IX	F 1111

Abbreviations for address modes and registers

BSC	Bit set/clear	IX	Indexed (no offset)
BTB	Bit test and branch	IX1	Indexed, 1 byte (8-bit) offset
DIR	Direct	IX2	Indexed, 2 byte (16-bit) offset
EXT	Extended	REL	Relative
INH	Inherent	A	Accumulator
IMM	Immediate	X	Index register

Not implemented

Legend



11.3 Addressing modes

Ten different addressing modes provide programmers with the flexibility to optimize their code for all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions; the longest instructions (three bytes) enable access to tables throughout memory. Short absolute (direct) and long absolute (extended) addressing are also included. One or two byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory locations.

The term ‘effective address’ (EA) is used in describing the various addressing modes. The effective address is defined as the address from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate ‘contents of’ the location or register referred to. For example, (PC) indicates the contents of the location pointed to by the PC (program counter). An arrow indicates ‘is replaced by’ and a colon indicates concatenation of two bytes. For additional details and graphical illustrations, refer to the ***M6805 HMOS/M146805 CMOS Family Microcomputer/ Microprocessor User's Manual*** or to the ***M68HC05 Applications Guide***.

11.3.1 Inherent

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, as well as the control instruction, with no other arguments are included in this mode. These instructions are one byte long.

11.3.2 Immediate

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants that do not change during program execution (e.g. a constant used to initialize a loop counter).

$$EA = PC+1;\ PC \leftarrow PC+2$$

11.3.3 Direct

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two-byte instruction.

$$EA = (PC+1);\ PC \leftarrow PC+2$$
$$\text{Address bus high} \leftarrow 0;\ \text{Address bus low} \leftarrow (PC+1)$$

11.3.4 Extended

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode byte. Instructions with extended addressing mode are capable of referencing arguments anywhere in memory with a single three-byte instruction. When using the Motorola assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the short form of the instruction.

EA = (PC+1):(PC+2); PC ← PC+3
Address bus high ← (PC+1); Address bus low ← (PC+2)

11.3.5 Indexed, no offset

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. This addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

EA = X; PC ← PC+1
Address bus high ← 0; Address bus low ← X

11.3.6 Indexed, 8-bit offset

In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. Therefore the operand can be located anywhere within the lowest 511 memory locations. This addressing mode is useful for selecting the mth element in an n element table.

EA = X+(PC+1); PC ← PC+2
Address bus high ← K; Address bus low ← X+(PC+1)
where K = the carry from the addition of X and (PC+1)

11.3.7 Indexed, 16-bit offset

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This address mode can be used in a manner similar to indexed, 8-bit offset except that this three-byte instruction allows tables to be anywhere in memory. As with direct and extended addressing, the Motorola assembler determines the shortest form of indexed addressing.

EA = X+[(PC+1):(PC+2)]; PC ← PC+3
Address bus high ← (PC+1)+K; Address bus low ← X+(PC+2)
where K = the carry from the addition of X and (PC+2)

11.3.8 Relative

The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte (the offset) following the opcode are added to the PC if, and only if, the branch conditions are true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from –126 to +129 from the opcode address. The programmer need not calculate the offset when using the Motorola assembler, since it calculates the proper offset and checks to see that it is within the span of the branch.

EA = PC+2+(PC+1); PC ← EA if branch taken;
otherwise EA = PC ← PC+2

11.3.9 Bit set/clear

In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode. The byte following the opcode specifies the address of the byte in which the specified bit is to be set or cleared. Any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single two-byte instruction.

EA = (PC+1); PC ← PC+2
Address bus high ← 0; Address bus low ← (PC+1)

11.3.10 Bit test and branch

The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit to be tested and its condition (set or clear) is included in the opcode. The address of the byte to be tested is in the single byte immediately following the opcode byte (EA1). The signed relative 8-bit offset in the third byte (EA2) is added to the PC if the specified bit is set or cleared in the specified memory location. This single three-byte instruction allows the program to branch based on the condition of any readable bit in the first 256 locations of memory. The span of branch is from –125 to +130 from the opcode address. The state of the tested bit is also transferred to the carry bit of the condition code register.

EA1 = (PC+1); PC ← PC+2
Address bus high ← 0; Address bus low ← (PC+1)
EA2 = PC+3+(PC+2); PC ← EA2 if branch taken;
otherwise PC ← PC+3

THIS PAGE LEFT BLANK INTENTIONALLY

12
LOW POWER MODES

The STOP and WAIT instructions have different effects on the Programmable Timer, M-Bus, Pulse Accumulator, PWM, OSD, and ADC. These are discussed in the following paragraphs.

12.1 Stop Mode

This is the lowest power consumption mode for the MCU. When the processor executes the STOP instruction, the internal clock is turned off. This halts all internal CPU processing, including the operation of the Programmable Timer, M-Bus, Pulse Accumulator, PWM, OSD, and ADC. The I bit in the Condition Code register is cleared to enable external interrupt $\overline{IRQ}$. All registers and memory remain unaltered, and all input/output lines remain unchanged.

The MCU is exited from Stop mode by an interrupt on $\overline{IRQ}$, or any resets (logic low on $\overline{RESET}$ pin or a power-on reset). On exit from Stop mode, the program counter is loaded with the corresponding interrupt vector (see Table 5-1). The effects of the Stop mode on each of the MCU peripheral systems are below.

12.1.1 Timer during Stop Mode

When Stop mode is entered, the timer counter stops counting (the internal processor clock is stopped) and remains at that particular count value until Stop mode is exited. If the exit was caused by reset, the counter is forced to $FFFC. If the Stop mode is exited by an interrupt $\overline{IRQ}$, the counter resumes counting from the value when it entered the Stop mode. Another feature of the programmable timer in the Stop mode is, that if at least one valid input capture edge occurs at the TCAP pin, the input capture detect circuitry is armed. This action does not set any timer flags or “wake up” the MCU, but when the MCU does “wake up” there will be an active input capture flag (and data) from that first valid edge which occurred during the Stop mode. Notice that an exit by a reset will reset the entire MCU and thus, this function on the TCAP will not happen.

12.1.2 M-Bus during Stop Mode

When Stop mode is entered, the internal clock driving the M-Bus module will be held at a static state, thus disabling the operation of the M-Bus module. The M-Bus module hence cannot wake up the CPU.

12.1.3 Pulse Accumulator during Stop Mode

When Stop mode is entered, the internal clock driving the Pulse Accumulator module will be held at a static state, thus disabling the operation of the Pulse Accumulator module. The Pulse Accumulator module hence cannot wake up the CPU.

12.1.4 PWM during Stop Mode

When Stop mode is entered, the internal clock driving the PWM module will be held at a static state, thus disabling the operation of the PWM module. The PWM module hence cannot wake up the CPU.

12.1.5 OSD during Stop Mode

When Stop mode is entered, the internal clock driving most of the OSD logic will be held at a static state, disabling the operation of the OSD module. If the PLL is not stopped by clearing PLLEN bit, the OSD pixel clock will still run, causing power consumption in Stop mode. The OSD module cannot wake up the CPU when in Stop mode.

12.1.6 ADC during Stop Mode

The ADC module operates with the presence of the internal clock, therefore, in Stop mode, ADC operation is halted.

12.1.7 COP during Stop Mode

The COP watchdog system stops counting in Stop mode. It continues counting again after 4069 bus cycles when the exit is caused by a external interrupt on $\overline{\text{IRQ}}$. If exit from Stop mode was caused by a reset, the MCU will be initialized and the COP watchdog system will be disabled.

12.2 Wait Mode

When the MCU enters Wait mode, the CPU clock is halted. All CPU activities are halted, but the peripheral modules remain active. Any interrupts from the peripherals will cause the processor to exit the Wait mode. A reset will also take the MCU out of Wait mode.

The operation of the COP system in Wait mode is as for Stop mode, but counting is resumed immediately after the exit; i.e. without the 4069 bus cycles.

The Wait mode power consumption depends on how many systems are active. If a non-reset exit from the Wait mode is performed (e.g. timer overflow interrupt exit), the state of the remaining systems will be unchanged. If a reset exit from the Wait mode is performed, all the systems revert to the default reset state.

THIS PAGE LEFT BLANK INTENTIONALLY

12

13
OPERATING MODES

The MC68HC05T16/*MC68HC705T16* MCU has two modes of operation, the User Mode and the Self-Check/*Bootstrap* Mode. Figure 13-1 shows the flowchart of entry to these two modes, and Table 13-1 shows operating mode selection.

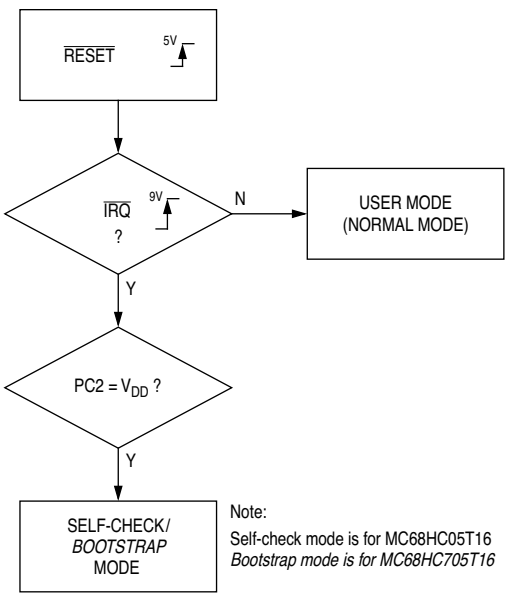


Figure 13-1 Flowchart of Mode Entering

Table 13-1 Mode Selection

RESET	IRQ	PC2	MODE
5V	V_{SS} to V_{DD}	V_{SS} to V_{DD}	USER
5V	9V +9V Rising Edge*	V_{DD}	SELF-CHECK/ *BOOTSTRAP*
* Minimum hold time should be 2 clock cycles, after that it can be used as a normal IRQ function pin.			

13.1 User Mode (Normal Operation)

The normal operating mode of the MC68HC05T16/*MC68HC705T16* is the user mode. The user mode will be entered if the RESET line is brought low, and the IRQ pin is within its normal operational range (V_{SS} to V_{DD}), the rising edge of the RESET will cause the MCU to enter the user mode.

13.2 Self-Check Mode

The MC68HC05T16 self-check mode is for the user to check device functions with an on-chip self-check program masked at location $FE00 to $FFEF under minimum hardware support. The hardware is shown in Figure 13-3. Figure 13-2 is the criteria to enter self-check mode, where PC2's condition is latched within first two clock cycles after the rising edge of the reset. PC2 can then be used for other purposes. After entering the self-check mode, CPU branches to the self-check program and carries out the self-check. Self-check is a repetitive test, i.e. if all parts are checked to be good, the CPU will repeat the self-check again. Therefore, the LEDs attached to Port A will be flashing if the device is good; else the combination of LEDs' on-off pattern can show what part of the device is suspected to be bad. Table 13-2 lists the LEDs' on-off patterns and their corresponding indications.

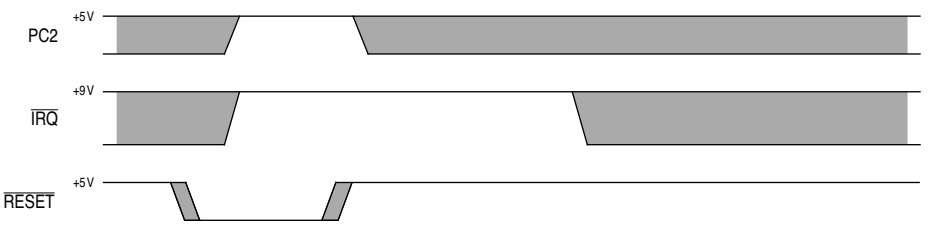


Figure 13-2 Self-Check Mode Timing

13

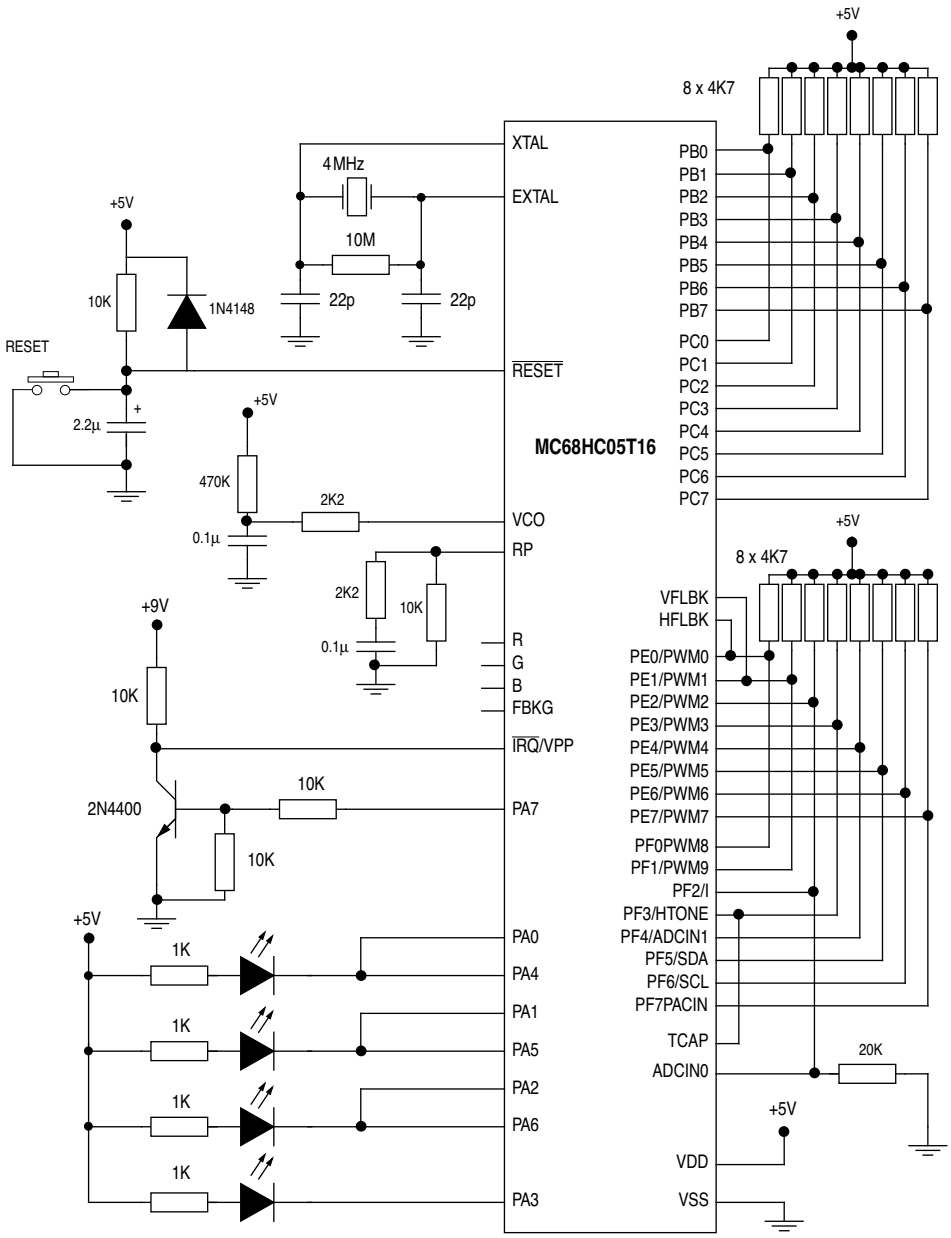


Figure 13-3 MC68HC05T16 Self-Test Circuit

Table 13-2 Self-Check Report

PA3	PA2	PA1	PA0	REMARKS
1	1	1	1	Faulty part, port A bad
1	1	1	0	Bad I/O
1	1	0	1	Bad RAM
1	1	0	0	Bad ROM
1	0	1	1	Bad TIMER
1	0	1	0	Bad PAC
1	0	0	1	Bad ADC
1	0	0	0	Bad OSD
0	1	1	1	Bad MFT
Flashing				Good Device
All Others				Bad Device, Bad Port A, etc.

1=LED off; 0=LED on.

13.3 Bootstrap Mode

The bootstrap mode is provided in the EPROM part (MC68HC705T16) as a mean of self-programming its EPROM with minimal circuitry. It is entered on the rising edge of $\overline{RESET}$ if $\overline{IRQ}$ pin is at 1.8V_{DD} and PC2 is at logic one. $\overline{RESET}$ must be held low for 4064 cycles after POR (power-on reset).

13.3.1 EPROM Programming

The 4K-bytes OSD CHAR EPROM is positioned from $8000 to $8FFF, and the 23.5K-bytes user EPROM is positioned from $A000 to $FDFF. The erased state of EPROM locations is $FF.

Programming boards are available from Motorola for programming the on-chip EPROM, please contact your Motorola representative.

The Program Control register (PCR) is provided for EPROM programming. The function of the EPROM depends on the device operating mode.

Please contact Motorola for Programming board availability.

13

13.3.2 Program Control Register (PCR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$3D							ELAT	PGM	0000 0000

ELAT - EPROM Latch Control

1 (set) – *EPROM address and data bus configured for programming (writes to EPROM cause address data to be latched). EPROM is in programming mode and cannot be read if ELAT is 1. This bit should not be set unless a programming voltage is applied to the V_{PP} pin.*

0 (clear) – *EPROM address and data bus configured for normal reads.*

PGM - EPROM Program Command

1 (set) – *Programming power connected to the EPROM array. If ELAT not = 1 then PGM = 0.*

0 (clear) – *Programming power disconnected from the EPROM array.*

13.3.3 EPROM Programming Sequence

Programming the EPROM of the MC68HC705T16 is as follows:

1) *Set the ELAT bit.*
2) *Write the data to be programmed to the address to be programmed.*
3) *Set the PGM bit.*
4) *Delay for the appropriate amount of time.*
5) *Clear the PGM and the ELAT bits.*

The last action may be carried out in a single CPU write operation. It is important to remember that an external programming voltage must be applied to the V_{PP} pin while programming, but should be equal to V_{DD} during normal operation.

Example shows address $B000 is programmed with $00.

```
CLR    PCR          ;reset PCR
LDX    #$00         ;load index register with 00
BSET   1,PCR        ;set ELAT bit
LDA    #$00         ;load data=00 in to A
STA    $B000,X      ;latch data and address (if programming OSD CHAR
                    ;EPROM, the address should be in the range of
                    ;$8000 to $8FFF)
BSET   0,PCR        ;program
JSR    DELAY        ;call delay subroutine for 1ms
CLR    PCR          ;reset PCR
```

THIS PAGE LEFT BLANK INTENTIONALLY

14
ELECTRICAL SPECIFICATIONS

This section contains the electrical specifications and associated timing information for the MC68HC05T16.

14.1 Maximum Ratings

(Voltages referenced to V_{SS})

RATINGS	SYMBOL	VALUE	UNIT
Supply Voltage	V_{DD}	–0.3 to +7.0	V
Input Voltage	V_{in}	V_{SS}–0.3 to V_{DD}+0.3	V
Input Voltage at Open Drain pins	V_{inod}	12	V
$\overline{IRQ}$ (MC68HC05T16)	V_{in}	V_{SS}–0.3 to 10	V
V_{PP} (MC68HC705T16)	*V_{PP}*	*V_{SS}–0.3 to 12+0.5*	*V*
Current Drain per pin excluding V_{DD} and V_{SS}	I_D	25	mA
Operating Temperature	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

14.2 Thermal Characteristics

CHARACTERISTICS	SYMBOL	VALUE	UNIT
Thermal resistance - Plastic 56-pin SDIP package	θ_{JA}	50	°C/W

14.3 DC Electrical Characteristics

Table 14-1 DC Electrical Characteristics for 5V Operation

(V_{DD}=5.0Vdc ±10%, V_{SS}=0Vdc, temperature range=0 to 70°C)

CHARACTERISTICS	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
Output voltage I_{LOAD}=+10µA I_{LOAD}=−10µA	 V_{OL} V_{OH}	 – V_{DD}-0.1	 – –	 0.1 –	 V V
Output high voltage (I_{LOAD}=−5mA) PA0-PA7, PC0-PC3, R, G, B, FBKG, PF2-PF7	V_{OH}	V_{DD}-0.8	–	–	V
Output low voltage (I_{LOAD}=+5mA) PA0-PA7, PC0-PC3, R, G, B, FBKG, PF2-PF7	V_{OL}	–	–	0.4	V
Input high voltage PA0-PA7, PB0-PB7, PC0-PC7, PE0-PE7, PF0-PF7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, EXTAL, HFLBK, VFLBK	V_{IH}	0.7xV_{DD}	–	–	V
Input low voltage PA0-PA7, PB0-PB7, PC0-PC7, PE0-PE7, PF0-PF7, TCAP, $\overline{IRQ}$, $\overline{RESET}$, EXTAL, HFLBK, VFLBK	V_{IL}	V_{SS}	–	0.2xV_{DD}	V
Data Retention Mode	V_{RM}	2.0	–	–	V
Supply current: Run Wait Stop (4.2MHz oscillator on) (4.2MHz oscillator off)	I_{DD}	 – – – –	 5 1 100 50	 10 2 200 100	 mA mA µA µA
I/O ports high-Z leakage current PA0-PA7, PB0-PB7, PC0-PC7, PE0-PE7, PF0-PF7	I_{OZ}	–	–	±10	µA
Input current TCAP, $\overline{IRQ}$, $\overline{RESET}$, EXTAL, ADCIN0, HFLBK, VFLBK	I_{IN}	–	–	±1	µA
Capacitance All signal pins	C_{OUT} C_{IN}			12 8	pF pF

14.4 Open Drain Electrical Specification

Table 14-2 Open Drain Parameters

(V_{DD}=5.0Vdc ±10%, V_{SS}=0Vdc, temperature range=0 to 70°C)

CHARACTERISTICS	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
Output low voltage: +V_{CC} pins (I_{LOAD} = 15mA) PB0-PB7, PC4-PC7, PE0-PE7, PF0-PF1	V_{OL}	–	–	0.4	V
Output low voltage: +V_{DD} pins (I_{LOAD} = 15mA) PF5/SDA, PF6/SCL	V_{OL}	–	–	0.4	V

14.5 On-Screen Display Timing

Table 14-3 On-Screen Display Timings

(V_{DD}=5.0Vdc ±10%, V_{SS}=0Vdc, temperature range=0 to 70°C)

CHARACTERISTICS	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
Rise Time (I_{LOAD}=2K, 12pF; 0.1 to 0.9 V_{DD}) R, G, B, FBKG, HTONE, I	t_R	–	5	–	ns
Fall Time (I_{LOAD}=2K, 12pF; 0.9 to 0.1 V_{DD}) R, G, B, FBKG, HTONE, I	t_F	–	5	–	ns
Dot clock frequency	t_{OSD}	–	16.128	–	MHz
HFLBK rise time	t_{RH}	–	100	–	ns
VFLBK rise time	t_{RV}	–	100	–	ns
V_{DD} ripple	t_{RIP}	–	100	–	mV

14.6 M-Bus Interface Timing

Table 14-4 M-Bus Interface Input Signal Timing

(V_{DD}=5.0Vdc ±10%, V_{SS}=0Vdc, temperature range=0 to 70°C)

PARAMETERS	SYMBOL	MINIMUM	MAXIMUM	UNIT
START condition hold time	$t_{HD.STA}$	2	–	t_{CYC}
START condition setup time (for repeated START condition only)	$t_{SU.STA}$	2	–	t_{CYC}
SCL clock low period	t_{LOW}	4.7	–	t_{CYC}
SCL clock high period	t_{HIGH}	4.0	–	t_{CYC}
SDA data setup time	$t_{SU.DAT}$	250	–	µs
SDA data hold time	$t_{HD.DAT}$	0	–	µs
STOP condition setup time	$t_{SU.STO}$	2	–	t_{CYC}

Table 14-5 M-Bus Interface Output Signal Timing

(V_{DD}=5.0Vdc ±10%, V_{SS}=0Vdc, temperature range=0 to 70°C)

CHARACTERISTICS	SYMBOL	MINIMUM	MAXIMUM	UNIT
START condition hold time	$t_{HD.STA}$	8	–	t_{CYC}
START condition setup time (for repeated START condition only)	$t_{SU.STA}$	10	–	t_{CYC}
SCL clock low period	t_{LOW}	11	–	t_{CYC}
SCL clock high period	t_{HIGH}	11	–	t_{CYC}
SDA/SCL rise time (see note 1)	t_R	–	1	µs
SDA/SCL fall time (see note 1)	t_F	–	300	ns
SDA data setup time	$t_{SU.DAT}$	t_{LOW}-$2t_{CYC}$	–	µs
SDA data hold time	$t_{HD.DAT}$	170	–	ns
STOP condition setup time	$t_{SU.STO}$	10	–	t_{CYC}

Note:

1. With 200pF loading on the SDA/SCL pins

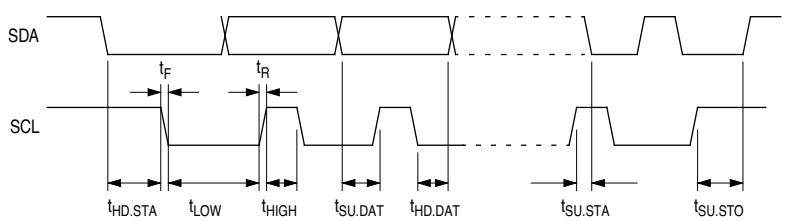


Figure 14-1 M-Bus Timing Diagram

14.7 Control Timing

Table 14-6 Control Timing for 5V Operation

(V_{DD}=5.0Vdc ±10%, V_{SS}=0Vdc, temperature range=0 to 70°C)

CHARACTERISTICS	SYMBOL	MINIMUM	MAXIMUM	UNIT
Frequency of operation Crystal option External clock option	 f_{OSC} f_{OSC}	 – dc	 4.2 4.2	 MHz MHz
Internal operating frequency Crystal (f_{OSC}/2) External clock (f_{OSC}/2)	 f_{OP} f_{OP}	 – dc	 2.1 2.1	 MHz MHz
Cycle time (1/f_{OP})	t_{CYC}	480	–	ns
Crystal oscillator start-up time	t_{OXOV}	–	100	ms
Stop recovery start-up time	t_{ILCH}	–	100	ms
$\overline{\text{RESET}}$ pulse width	t_{RL}	1.5	–	t_{CYC}
$\overline{\text{IRQ}}$ pulse width low (edge-triggered)	t_{ILIH}	125	–	ns
$\overline{\text{IRQ}}$ pulse period	t_{ILIL}	see note 1	–	t_{CYC}
ADC comparator stabilization time	t_{SETTLE}	–	10	µs
ADC comparator conversion time	t_{CONV}	2	3	t_{CYC}
Timer resolution Timer TCAP pulse width Timer TCAP period	t_{RESL} t_{TH}, t_{TL} t_{TLTL}	4 125 (see note 2) see note 3	– – –	t_{CYC} ns t_{CYC}

Notes:

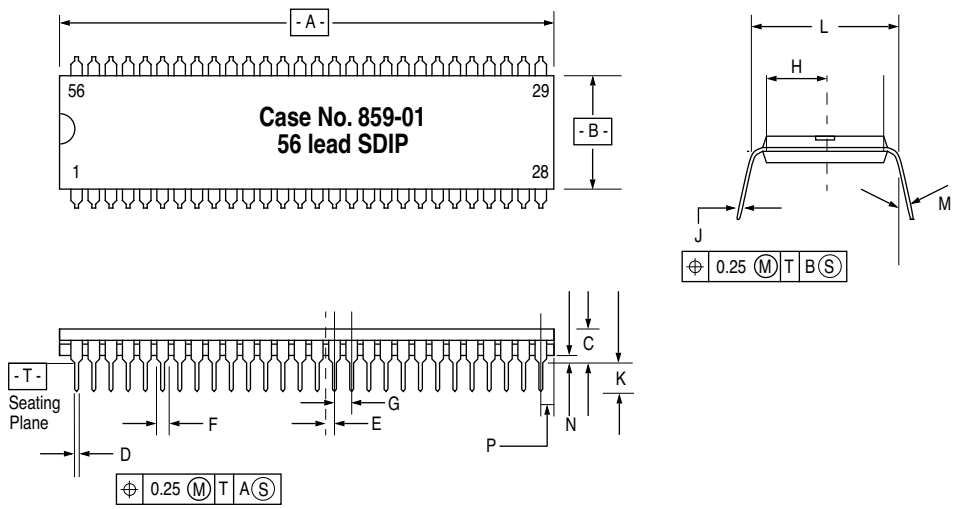
1. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the $\overline{\text{IRQ}}$ interrupt service routine plus 21 t_{CYC}.
2. Depending on the active edge of TCAP, either t_{TH}, the high TCAP pulse width, or t_{TL}, the low TCAP pulse width applies.
3. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the input capture interrupt service routine plus 24 t_{CYC}.

THIS PAGE LEFT BLANK INTENTIONALLY

15
MECHANICAL SPECIFICATIONS

This section provides the mechanical dimension for the 56-pin SDIP package for the MC68HC05T16.

15.1 56-pin SDIP Package



Dim.	Min.	Max.	Notes	Dim.	Min.	Max.
A	51.69	52.45	1. Dimensions and tolerancing per ANSI Y 14.5 1982. 2. All dimensions in mm. 3. Dimension L to centre of lead when formed parallel. 4. Dimensions A and B do not include mould flash. Allowable mould flash is 0.25 mm.	H	7.62 BSC	
B	13.72	14.22		J	0.20	0.38
C	3.94	5.08		K	2.92	3.43
D	0.36	0.56		L	15.24 BSC	
E	0.89 BSC			M	0°	15°
F	0.81	1.17		N	0.51	1.02
G	1.778 BSC			P	1.78	2.29

Figure 15-1 56-pin SDIP Mechanical Dimensions

THIS PAGE LEFT BLANK INTENTIONALLY

How to reach us:

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244-6609

INTERNET: http://Design-NET.com

USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298