MC68HC705C8

Addendum to
MC68HC705C8
HCMOS Microcontroller Unit
Technical Data

This addendum supplements *MC68HC705C8 Technical Data*, Rev. 1 (Motorola document number MC68HC705C8/D) with the following information:

- Corrections to *MC68HC705C8 Technical Data*
- Additional mechanical information for *MC68HC705C8 Technical Data*

CORRECTIONS
MC68HC705C8/D, REV. 1

Corrections to the technical data manual are as follows:

1. Page 2-11, **Figure 2-4. OTPROM/EPROM Programming**:
   a. There should only be one box labeled WAIT 1 ms.
   b. YES label on output of NTRYS = 2 decision box should be NO.

2. Page 3-2, **3.1.3.1 COP RESET REGISTER**: Address of COP reset register should be $001D.

3. Page 3-2, **3.1.3.2 COP CONTROL REGISTER**: The last sentence under the CME bit description should read as follows:

   CME is readable and writable at any time.

4. Page 3-3, **3.1.3.2 COP CONTROL REGISTER**: The second sentence under the CM1 bit description should read as follows:

   CM1 can be read anytime but may be written only once.

5. Page 3-3, **3.1.3.2 COP CONTROL REGISTER**: The second sentence under the CM0 bit description should read as follows:

   CM0 can be read anytime, but may be written only once.

6. Page 3-10, (**3.3.1 STOP Mode**): The first three sentences from the paragraph at the top of the page should read as follows:

   During the STOP mode, the I bit in the CCR is cleared to enable external interrupts.

7. Page 7-9, **Table 7-2. Opcode Map**: Bit Manipulation column heads BTB and BSC should be DIR and DIR.

8. Page 8-1, **8.2 THERMAL CHARACTERISTICS**: Thermal resistance of cerdip package should be 50 °C/W.

9. Page 8-3, **8.4 DC ELECTRICAL CHARACTERISTICS**:

   a. Pins specified under I/O Ports Hi-Z Leakage Current should be PA0–PA7, PB0–PB7, PC0–PC7, PD1–PD4, PD7, $\overline{\text{RESET}}$.

   b. Pins specified under Input Current should be $\overline{\text{IRQ}}$, TCAP, OSC1, PD0, PD5.

10. Page 8-4, **8.5 DC ELECTRICAL CHARACTERISTICS**:

    a. Pins specified under I/O Ports Hi-Z Leakage Current should be PA0–PA7, PB0–PB7, PC0–PC7, PD1–PD4, PD7, $\overline{\text{RESET}}$.

    b. Pins specified under Input Current should be $\overline{\text{IRQ}}$, TCAP, OSC1, PD0, PD5.

    c. NOTE 3 should be
    Run (Operating) I_{DD} and WAIT I_{DD} measured using external square wave clock source (f_{OSC} = 2.0 MHz). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. C_L = 20 pF on OSC2.

11. Page 8-7, **Figure 8-4. Total Current Drain vs Frequency** (V_{DD} = 3.3 V graph): Internal clock frequencies should read as follows:

    0 250 kHz 500 kHz 750 kHz 1 MHz.

12. Page 8-11, **8.8 SERIAL PERIPHERAL INTERFACE (SPI) TIMING**: Slave enable lag time (Num. 3) should be 720 ns.

13. Page 8-12, **8.8 SERIAL PERIPHERAL INTERFACE (SPI) TIMING**: Slave enable lag time (Num. 3) should be 1500 ns.

ADDITIONAL MECHANICAL DATA
MC68HC705C8 TECHNICAL DATA, REV. 1

The following section supplements SECTION 9 of *MC68HC705C8 Technical Data,* REV. 1 with specifications of the 42-pin shrink dual in-line package (SDIP), the 44-pin quad flat pack (QFP), and the 44-lead ceramic-leaded chip carrier (CLCC). The information on pages 9-1 through 9-4 of *MC68HC705C8 Technical Data,* REV. 1 is still valid and **must not be removed**.

SECTION 9
MECHANICAL DATA

9.1 ORDERING INFORMATION

The following table provides additional ordering information for the MC68HC705C8 MCU.

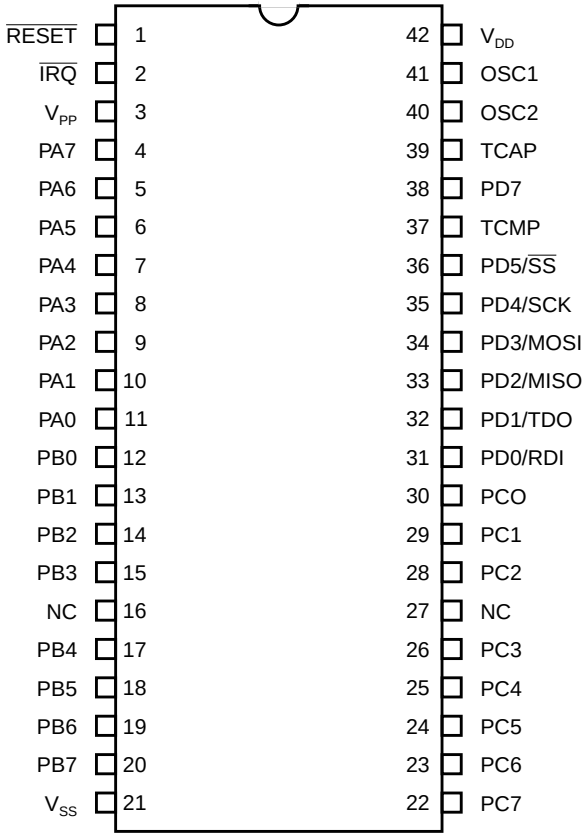
OTPROM MCUs

Package Type	Temperature Range	Order Number
Shrink Dual In-Line Package (SDIP)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C8B MC68HC705C8CB
Quad Flat Pack (QFP)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C8FB MC68HC705C8CFB
Ceramic-Leaded Chip Carrier (CLCC)	0 °C to +70 °C –40 °C to +85 °C	MC68HC705C8FS MC68HC705C8CFS

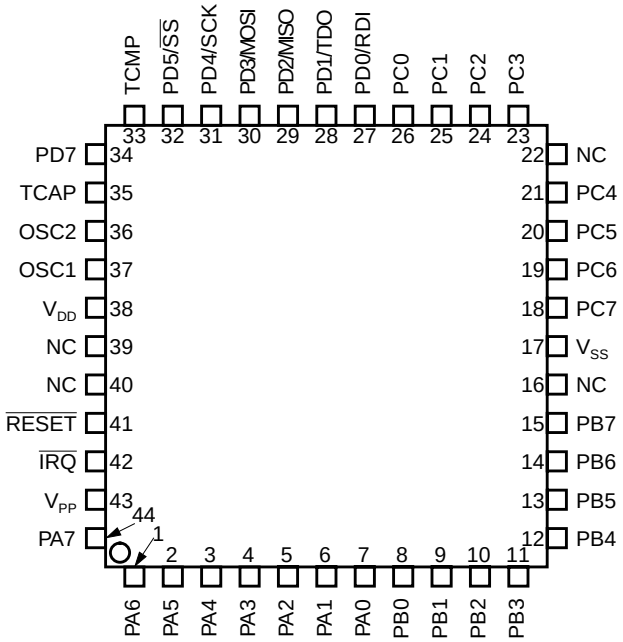
9.2 PIN ASSIGNMENTS

The following figures show the SDIP and QFP pin assignments.

9.2.3 42-Pin SDIP



9.2.4 44-Lead QFP



9.2.4 44-Lead CLCC

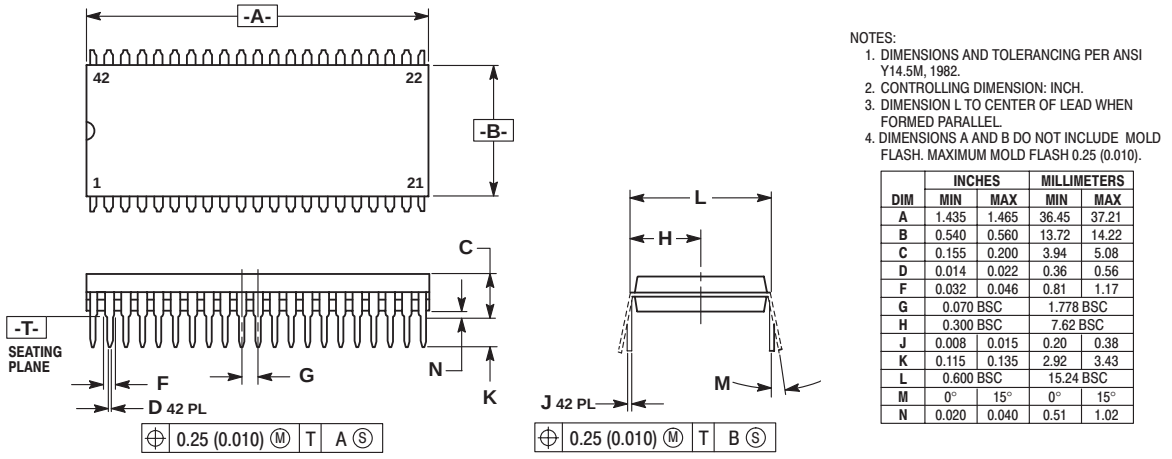
Pin assignments for this package are the same as for the 44-lead PLCC package.

9.3 PACKAGE DIMENSIONS

The MC68HC705C8 is available in a 42-pin shrink dual in-line package, a 44-lead quad flat pack (QFP) package, and a 44-lead ceramic-leaded chip carrier (CLCC) package. Package dimensions available at time of this publication are provided in this section. To make sure that you have the latest case outline specifications, contact one of the following:

- Local Motorola Sales Office
- Motorola Mfax
  - Phone 602-244-6609
  - EMAIL rmfax0@email.sps.mot.com
- Worldwide Web (wwweb) at http://design-net.com

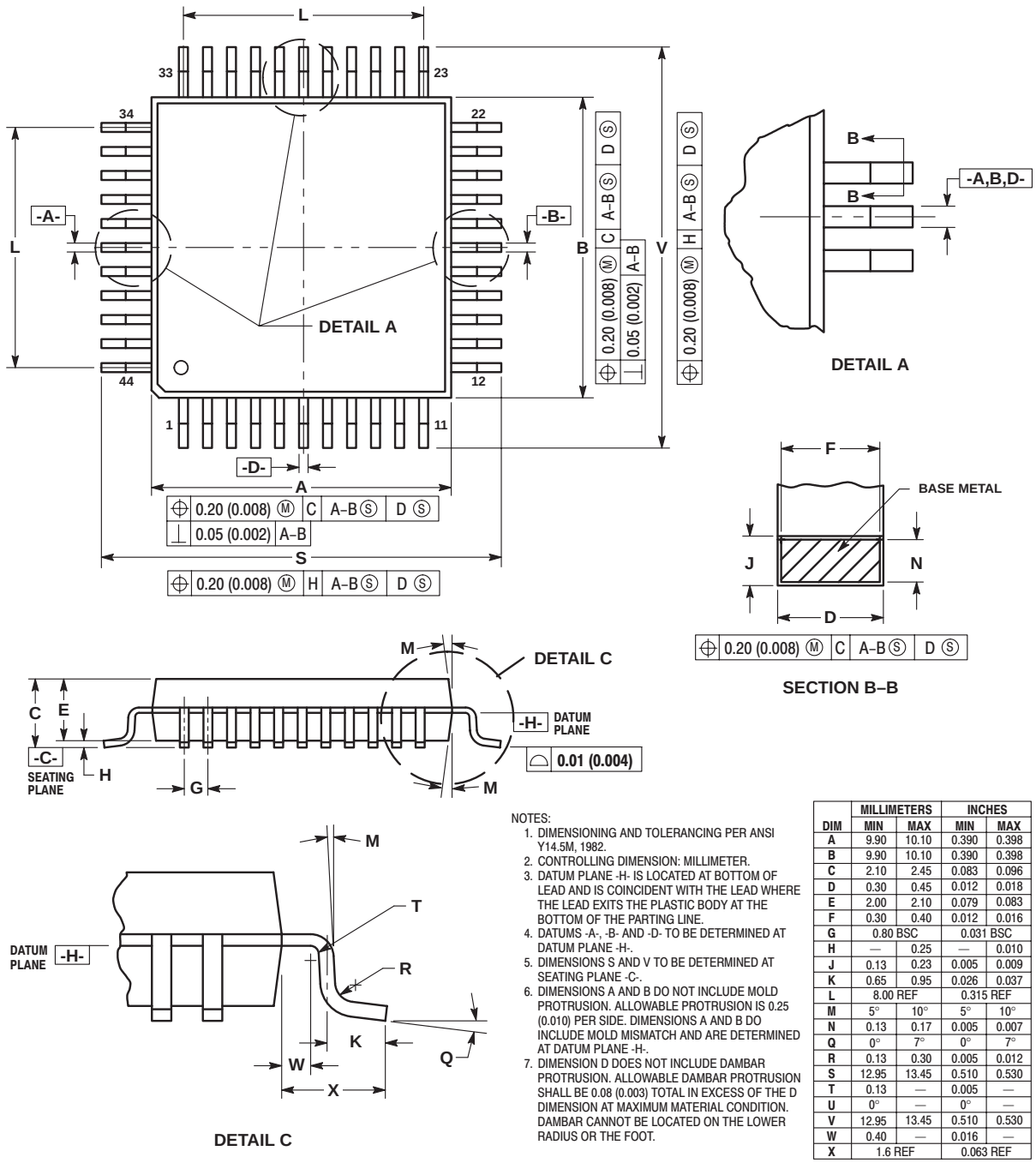
Follow Mfax or wwweb on-line instructions to retrieve the current mechanical specifications.



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

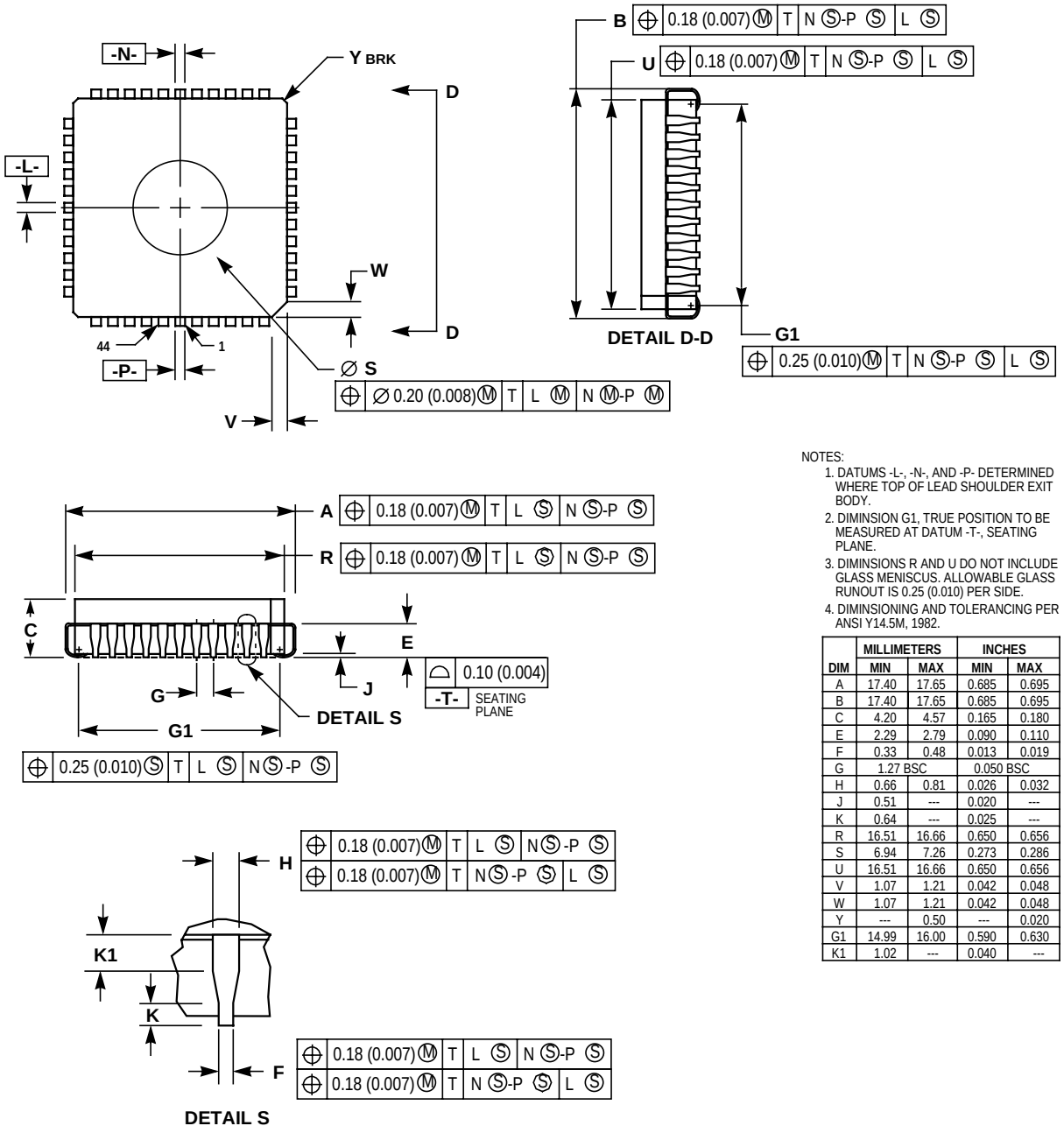
Figure 9-1. 42-Pin Shrink Dual In-Line Package (Case #858)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.40	—	0.016	—
X	1.6 REF		0.063 REF	

Figure 9-2. 44-Lead Quad Flat Pack (Case #824E)



NOTES:
1. DATUMS -L-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT BODY.
2. DIMINSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMINSIONS R AND U DO NOT INCLUDE GLASS MENISCUS. ALLOWABLE GLASS RUNOUT IS 0.25 (0.010) PER SIDE.
4. DIMINSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	---	0.020	---
K	0.64	---	0.025	---
R	16.51	16.66	0.650	0.656
S	6.94	7.26	0.273	0.286
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
Y	---	0.50	---	0.020
G1	14.99	16.00	0.590	0.630
K1	1.02	---	0.040	---

Figure 9-3. 44-Lead Ceramic-Leaded Chip Carier (CLCC) (Case #777B)

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