TECHNICAL DATA

MC68HC711L6

Technical Summary
8-Bit Microcontrollers

Introduction

The MC68HC711L6 high-performance microcontroller unit (MCU) is a simplified erasable programmable read-only memory (EPROM)-based derivative of the MC68HC11L6, and has 16 Kbytes of EPROM or OTPROM, 512 bytes of RAM, and 512 bytes of electrically erasable programmable read-only memory (EEPROM). It is a high speed, low power consumption chip with a multiplexed bus and a fully static design. The chip runs at frequencies from 3 MHz to dc.

The MC68HC711L6 offers an alternative for applications that require an HC11 CPU, and where large quantities of EPROM/OTPROM with EEPROM and RAM available are required.

For detailed information about subsystems, programming and the instruction set, refer to the *M68HC11 Reference Manual*, document number M68HC11 RM/AD.

Features

- MC68HC11 CPU
- Power-Saving STOP and WAIT Modes
- 16 Kbytes of On-Chip EPROM or One-Time Programmable Read-Only Memory (OTPROM)
- 512 Bytes of On-Chip RAM (All Saved During Standby)
- 512 Bytes of On-Chip EEPROM with Block Protect
- 16-Bit Timer System
  - — Three Input Capture (IC) Channels
  - — Four Output Compare (OC) Channels
  - — An Additional Channel, Software Selectable as Fourth IC or Fifth OC
- 8-Bit Pulse Accumulator
- Real-Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog System
- Synchronous Serial Peripheral Interface (SPI)
- Asynchronous Nonreturn to Zero (NRZ) Serial Communications Interface (SCI)
- 46 General-Purpose Input/Output (I/O) Pins
  - — 24 Bidirectional I/O Pins
  - — 11 Input-Only and 11 Output-Only Pins
- Available in Plastic and Ceramic Packages of Both 64-Pins (QFP) or 68-Pins (PLCC/CERQUAD)

Package	Temperature	MC Order Number
64-Pin Ceramic Cerquad (EPROM)	– 40° to + 85°C	MC68HC711L6CFS
68-Pin Plastic Quad PLCC (OTPROM)	– 40° to + 85°C	MC68HC711L6CFN

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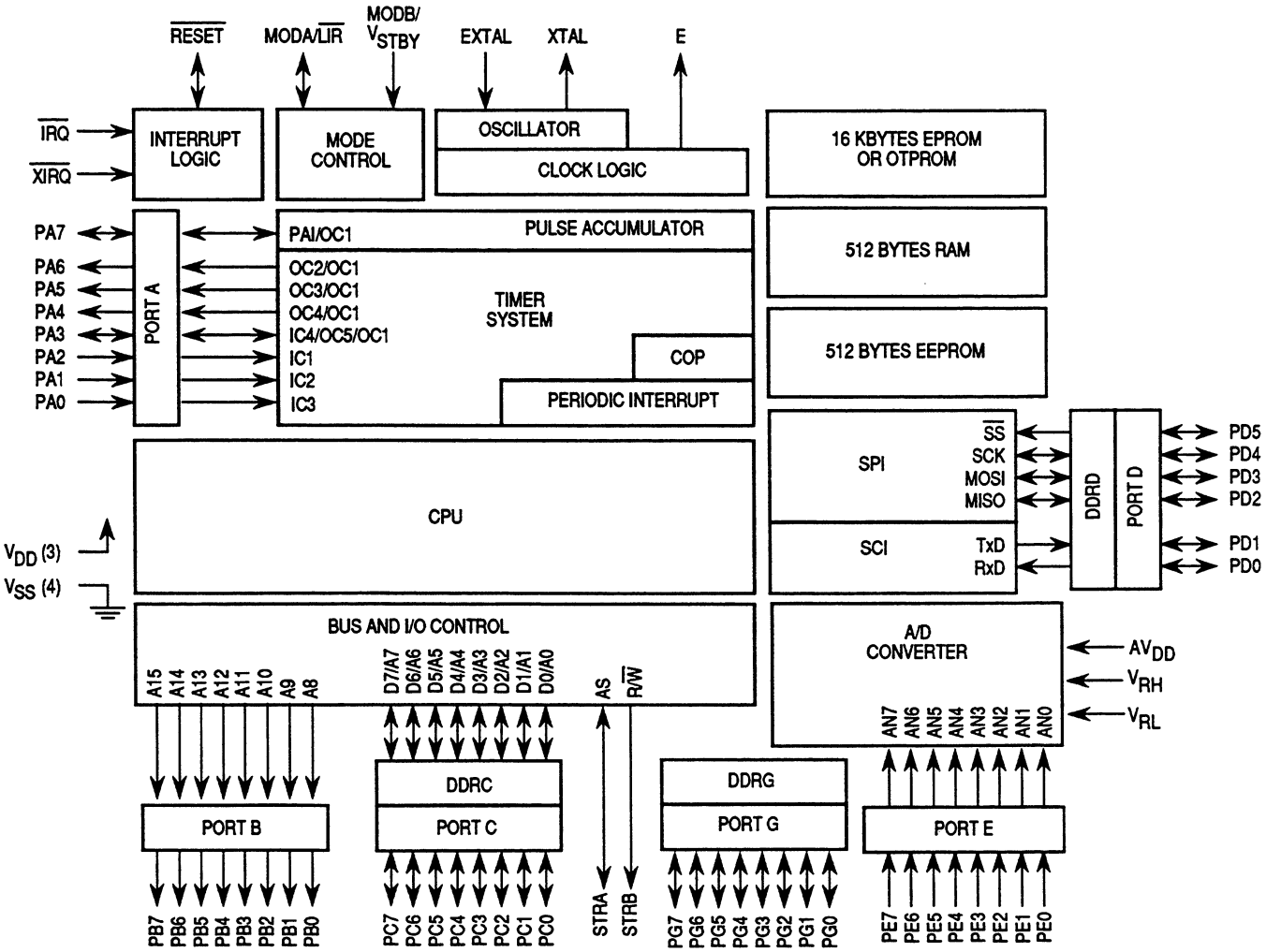
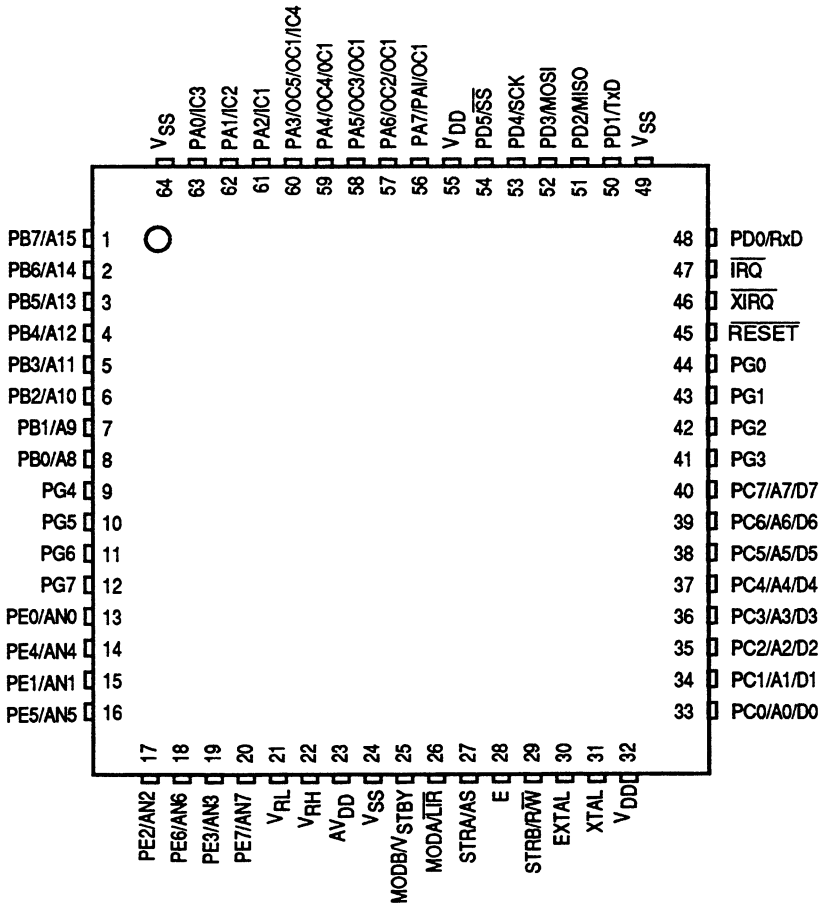
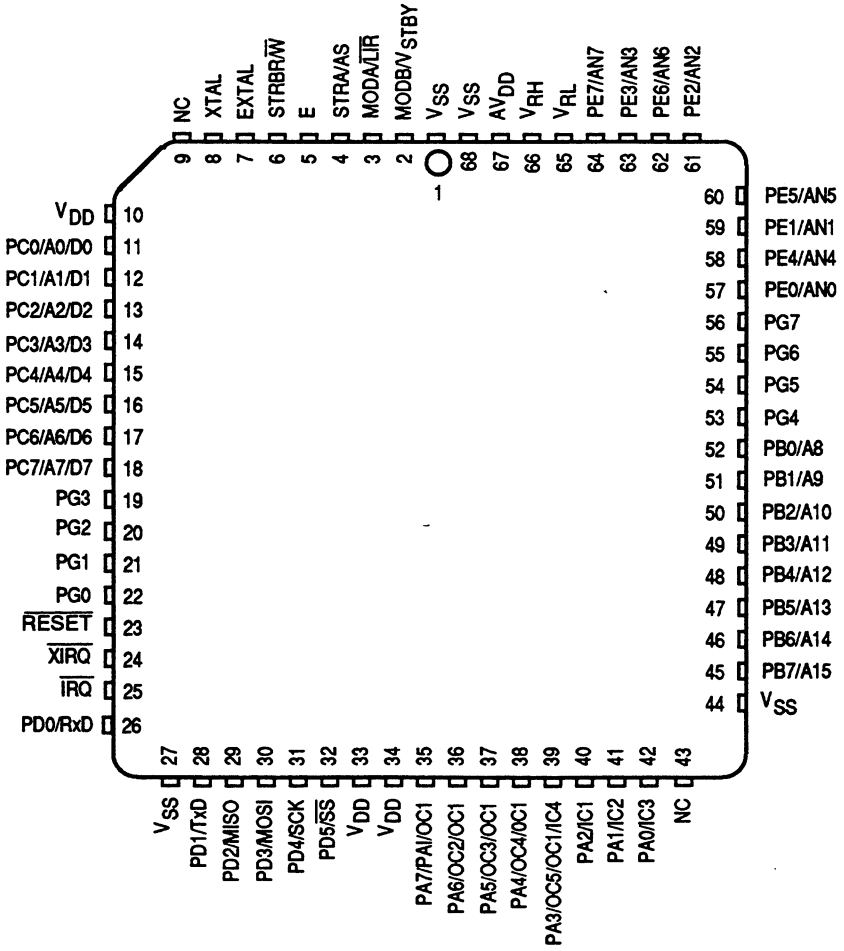


MC68HC711L6 Block Diagram



Pin Assignments for 64-Pin QFP

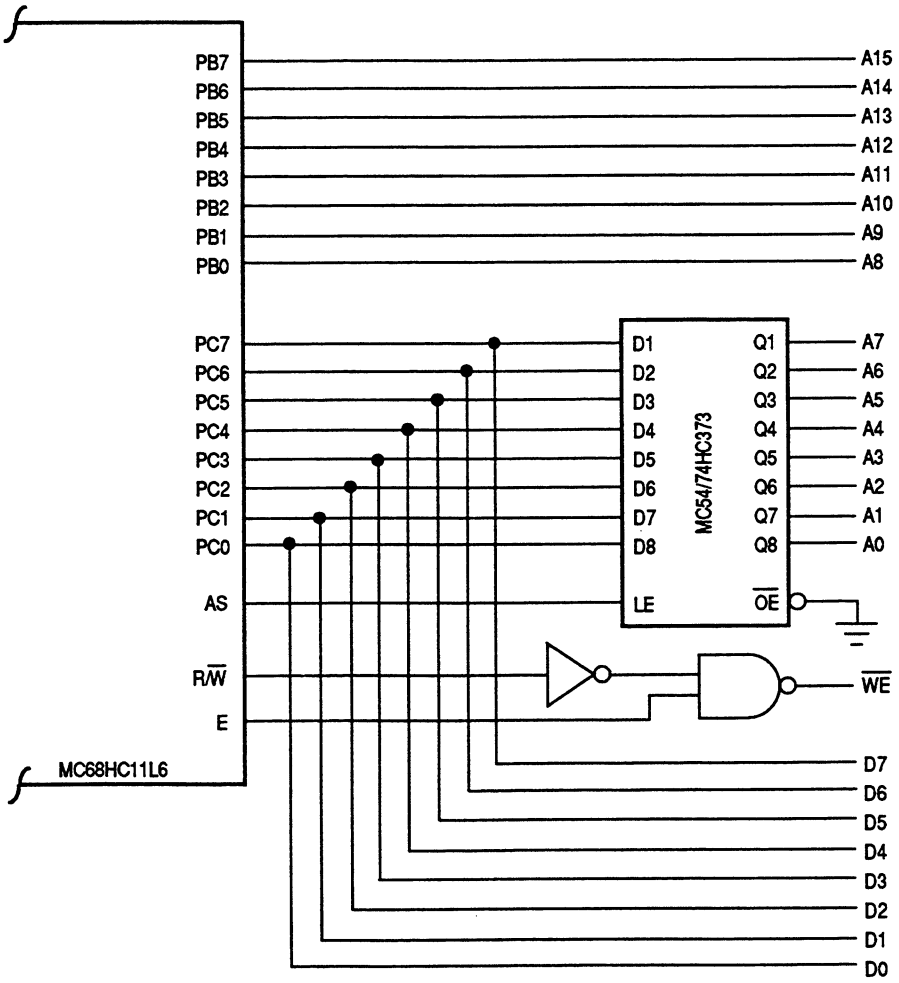


Pin Assignments for 68-Pin PLCC

Operating Modes and Memory Maps

In single-chip operating mode, the MC68HC711L6 is a monolithic microcontroller without external address or data buses.

In expanded multiplexed operating mode, the MCU can access a 64 Kbyte address space. The space includes the same on-chip memory addresses used for single chip mode plus external peripheral and memory devices. The expansion bus is made up of ports B and C and control signals AS and R/$\overline{W}$. The address, R/$\overline{W}$, and AS signals are active and valid for all bus cycles including accesses to internal memory locations. The following figure demonstrates a recommended method of demultiplexing low order addresses from data at port C.



Address/Data Demultiplexing

Special bootstrap mode allows special purpose programs to be entered into internal RAM. The bootloader program uses the SCI to read up to a 512-byte program into on-chip RAM at $0000 through $01FF. After receiving the character for address $01FF, or a four-character delay to allow a variable length download, control passes to the program loaded at $0000.

Special test mode is used primarily for factory testing.

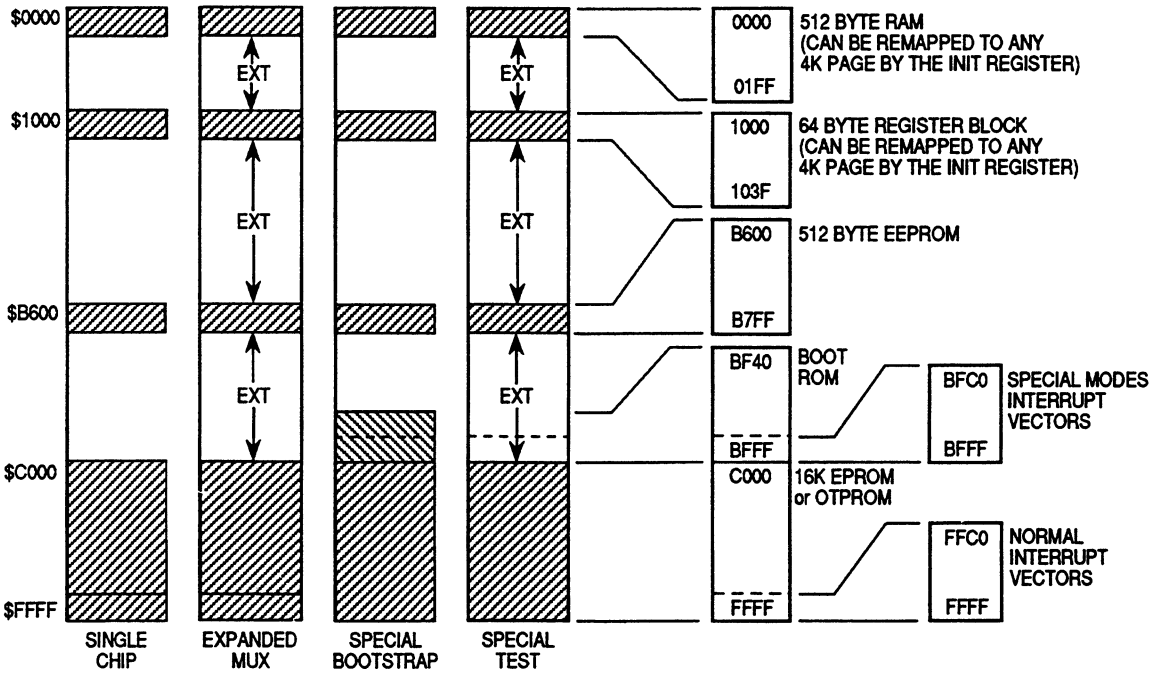
Memory Maps

Memory locations are the same for expanded multiplexed and single-chip modes. The 64-byte register block originates at $1000, but can be placed at any other 4K boundary ($x000) after reset by writing an appropriate value to the INIT register. The 512-byte EEPROM is located at $B600 through $B7FF, if it is enabled, and the 16 Kbyte EPROM/OTPROM is located at $C000 through $FFFF, if it is enabled. The on-board 512-byte RAM is located at $0000 after reset.

Hardware priority is built into the memory remapping. Registers have priority over RAM, which has priority over EPROM. Where there is a conflict, the higher priority resource covers the lower, making the underlying locations inaccessible.

In special bootstrap mode, a bootloader ROM is enabled at locations $BF40 through $BFFF.

In special test mode and special bootstrap mode, reset and interrupt vectors are at $BFC0 through $BFFF.



MC68HC711L6 Memory Map

MC68HC711L6 Register and Control Bit Assignments (1 of 2)

(The register block can be remapped to any 4K boundary)

	Bit 7	6	5	4	3	2	1	Bit 0	
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$1001									Reserved
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC
$1003	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$1004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$1005	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0	PORTCL
$1006									Reserved
$1007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$1008	0	0	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$1009	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$100A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
$100E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (High)
$100F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Low)
$1010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (High)
$1011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (Low)
$1012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (High)
$1013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Low)
$1014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (High)
$1015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Low)
$1016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1(High)
$1017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Low)
$1018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (High)
$1019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Low)
$101A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (High)
$101B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Low)
$101C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (High)
$101D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Low)
$101E	Bit 15	14	13	12	11	10	9	Bit 8	TI4O5 (High)
$101F	Bit 7	6	5	4	3	2	1	Bit 0	TI4O5 (Low)

MC68HC711L6 Register and Control Bit Assignments (2 of 2)

	Bit 7	6	5	4	3	2	1	Bit 0	
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$1022	OC1I	OC2I	OC3I	OC4I	I4O5I	IC1I	IC2I	IC3I	TMSK1
$1023	OC1F	OC2F	OC3F	OC4F	I4O5F	IC1F	IC2F	IC3F	TFLG1
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
$1025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2
$1026	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0	PACTL
$1027	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
$1029	SPIF	WCOL	0	MODF	0	0	0	0	SPSR
$102A	Bit 7	6	5	4	3	2	1	Bit 0	SPDR
$102B	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD
$102C	R8	T8	0	M	WAKE	0	0	0	SCCR1
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE	0	SCSR
$102F	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SCDR
$1030	CCF	0	SCAN	MULT	CD	CC	CB	CA	ADCTL
$1031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$1032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$1033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$1034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4
$1035	0	0	0	PTCON	BPRT3	BPRT2	BPRT1	BPRT0	BPROT
$1036	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	PORTG
$1037	DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0	DDRG
$1038									Reserved
$1039	ADPU	CSEL	IRQE	DLY	CME	0	CR1	CR0	OPTION
$103A	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$103B	ODD	EVEN	ELAT	BYTE	ROW	ERASE	EELAT	PGM	PPROG
$103C	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
$103E	TILOP	EPTEST	OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1
$103F	0	0	0	0	NOSEC	NOCOP	EPON	EEON	CONFIG

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous **$103C**

	Bit 7	6	5	4	3	2	1	Bit 0	
	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0	
RESETS:									
	0	0	0	0	0	1	0	1	Single-Chip Mode
	0	0	1	0	0	1	0	1	Exp'd Non-Mux'd
	1	1	0	0	0	1	0	1	Bootstrap
	0	1	1	1	0	1	0	1	Special Test

RBOOT, SMOD, MDA, and IRVNE initialization depends on mode selected at reset.

RBOOT — Read Bootstrap ROM

Can be written only when SMOD is set to one (special bootstrap or special test mode)

0 = Bootloader ROM disabled and not in map

1 = Bootloader ROM enabled and in map at $BF40–$BFFF

SMOD and MDA — Special Mode Select and Mode Select A

These two bits can be read at any time. They reflect the status of the MODB and MODA pins at the rising edge of reset. SMOD and MDA can only be written in special modes.

Inputs		Mode	Latched at Reset		
MODB	MODA		RBOOT	SMOD	MDA
1	0	Single-Chip	0	0	0
1	1	Expanded Multiplexed	0	0	1
0	0	Special Bootstrap	1	1	0
0	1	Special Test	0	1	1

IRVNE — Internal Read Visibility/Not E (IRVNE can be written once in any mode)

In expanded modes, IRVNE determines whether IRV is on or off. In special test mode, IRVNE is set to 1; in all other modes IRVNE is reset to 0.

0 = No internal read visibility on external bus

1 = Data from internal reads is driven out the external data bus

In single chip modes this bit determines whether the E clock drives out of the chip.

0 = E is driven out from the chip

1 = E pin is driven low

Mode	IRVNE Out of Reset	E Clock Out of Reset	IRV Out of Reset	IRVNE Affects Only
Single-Chip	0	On	Off	E
Expanded	0	On	Off	IRV
Boot	0	On	Off	E
Special Test	1	On	On	IRV

PSEL3 – PSEL0 — Priority Select Bits 3 through 0

Refer to **Resets and Interrupts**.

INIT — RAM and I/O Mapping **$103D**

	Bit 7	6	5	4	3	2	1	Bit 0
	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
RESET:	0	0	0	0	0	0	0	0

RAM3–RAM0 — 512-Byte Internal RAM Map Position

RAM3–RAM0 determine the upper four bits of the RAM address, positioning RAM at the selected 4K boundary ($x000).

REG3–REG0 — 64-Byte Register Block Map Position

REG3–REG0 determine the upper four bits of the register address, positioning registers at the selected 4K boundary ($x000).

NOTE

Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes. Refer to **Operating Modes and Memory Maps**.

TEST1 — Factory Test **$103E**

	Bit 7	6	5	4	3	2	1	Bit 0
	TILOP	EPTST	OCCR	CBYP	DISR	FCM	FCOP	TCON
RESET:	0	0	0	0	—	0	0	0

Test modes only.

TILOP — Test Illegal Opcode

EPTST — EPROM Test

OCCR — Output Condition Code Register to Timer Port

CBYP — Timer Divider Chain Bypass

DISR — Disable Resets from COP and Clock Monitor

Forced to one out of reset in special test and bootstrap modes.

FCM — Force Clock Monitor Failure

FCOP — Force COP Watchdog Failure

TCON — Test Configuration Register

CONFIG — COP, EPROM, EEPROM Enables **$103F**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	NOSEC	NOCOP	EPON	EEON
RESET:	0	0	0	0	0	—	1	0

The CONFIG register is implemented with nonvolatile EEPROM cells. Refer to **Electrically Erasable Programmable Read-Only Memory (EEPROM)** for programming and erasure procedures.

Bits 7–4 — Not implemented; always read zero

NOSEC — EEPROM and EPROM Security Disable
Refer to **Electrically Erasable Programmable Read-Only Memory (EEPROM)**.

NOCOP — COP System Disable
Refer to **Resets and Interrupts**.

EPON — EPROM Enable
In single-chip modes, EPON is forced to one out of reset.
0 = EPROM removed from the memory map
1 = EPROM present in the memory map

EEON — EEPROM Enable
0 = EEPROM removed from the memory map
1 = EEPROM present in the memory map

Resets and Interrupts

The MC68HC711L6 has three reset vectors and eighteen interrupt vectors. The reset vectors are as follows:

- $\overline{\text{RESET}}$, or power-on reset
- Clock Monitor Fail
- COP Failure

The 18 interrupt vectors service 23 interrupt sources (three non-maskable, twenty maskable). The three non-maskable interrupt vectors are as follows:

- Illegal Opcode Trap
- $\overline{\text{Software}}$ Interrupt
- XIRQ Pin (Pseudo Non-Maskable Interrupt)

On-chip peripheral systems generate maskable interrupts that are recognized only if the global interrupt mask bit (I) in the condition code register (CCR) is clear. Twenty interrupt sources in the MC68HC711L6 are subject to masking by the global interrupt mask bit. Maskable interrupts are prioritized according to a default arrangement. However, any one source can be elevated to the highest maskable priority position by HPRIO, a software-accessible control register. The HPRIO register can be written at any time, provided the I bit in the CCR is set.

In addition to the global I bit, all of these sources except the external interrupt ($\overline{IRQ}$) pin are controlled by local enable bits in control registers. Most interrupt sources in the M68HC11 have separate interrupt vectors and there is usually no need for software to poll control registers to determine the cause of an interrupt. Refer to the following table of interrupt and reset vector assignments.

Interrupt and Reset Vector Assignments

Vector Address	Interrupt Source	CC Register Mask	Local Mask
FFC0, C1 — FFD4, D5	Reserved	—	—
FFD6, D7	SCI Serial System	I Bit	—
	SCI Transmit Complete		TCIE
	SCI Transmit Data Register Empty		TIE
	SCI Idle Line Detect		ILIE
	SCI Receiver Overrun		RIE
	SCI Receive Data Register Full		RIE
FFD8, D9	SPI Serial Transfer Complete	I Bit	SPIE
FFDA, DB	Pulse Accumulator Input Edge	I Bit	PAII
FFDC, DD	Pulse Accumulator Overflow	I Bit	PAOVI
FFDE, DF	Timer Overflow	I Bit	TOI
FFE0, E1	Timer Input Capture 4/Output Compare 5	I Bit	I4O5I
FFE2, E3	Timer Output Compare 4	I Bit	OC4I
FFE4, E5	Timer Output Compare 3	I Bit	OC3I
FFE6, E7	Timer Output Compare 2	I Bit	OC2I
FFE8, E9	Timer Output Compare 1	I Bit	OC1I
FFEA, EB	Timer Input Capture 3	I Bit	IC3I
FFEC, ED	Timer Input Capture 2	I Bit	IC2I
FFEE, EF	Timer Input Capture 1	I Bit	IC1I
FFF0, F1	Real-Time Interrupt	I Bit	RTII
FFF2, F3	Parallel I/O Handshake	I Bit	STAI
	$\overline{IRQ}$ (External Pin)		None
FFF4, F5	$\overline{XIRQ}$ Pin	X Bit	None
FFF6, F7	Software Interrupt	None	None
FFF8, F9	Illegal Opcode Trap	None	None
FFFA, FB	COP Failure	None	NOCOP
FFFC, FD	Clock Monitor Fail	None	CME
FFFE, FF	$\overline{RESET}$	None	None

For some interrupt sources, such as the parallel I/O and SCI interrupts, the flags are automatically cleared during the course of responding to the interrupt requests. For example, the RDRF flag in the SCI system is cleared by the automatic clearing mechanism, which consists of a read of the SCI status register while RDRF is set, followed by a read of the SCI data register. The normal response to an RDRF interrupt request is to read the SCI status register to check for receive errors, then to read the received data from the SCI data register. These two steps satisfy the automatic clearing mechanism without requiring any special instructions.

OPTION — System Configuration Options **$1039**

	Bit 7	6	5	4	3	2	1	Bit 0
	ADPU	CSEL	IRQE*	DLY*	CME	0	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes.

ADPU — A/D Converter Power Up
Refer to **Analog-to-Digital Converter**.

CSEL — Clock Select
Refer to **Electrically Erasable Programmable Read-Only Memory (EEPROM)** and **Analog-to-Digital Converter**.

IRQE — $\overline{\text{IRQ}}$ Select Edge-Sensitive Only
0 = Low level recognition
1 = Falling edge recognition

DLY — Enable Oscillator Start-Up Delay on Exit from STOP
0 = No stabilization delay on exit from STOP
1 = Stabilization delay enabled on exit from STOP

CME — Clock Monitor Enable
0 = Clock monitor disabled; slow clocks can be used
1 = Slow or stopped clocks cause clock failure reset

Bit 2 — Not implemented; always reads zero

CR1, CR0 — COP Timer Rate Select
Refer to **Resets and Interrupts**.

COP Timer Rate Select

CR[1:0]	Divide E/2^{15} By	XTAL = 4.0 MHz Timeout – 0/+32.8 ms	XTAL = 8.0 MHz Timeout – 0/+16.4 ms	XTAL = 12.0 MHz – 0/+10.9 ms
0 0	1	32.768 ms	16.384 ms	10.923 ms
0 1	4	131.07 ms	65.536 ms	43.691 ms
1 0	16	524.29 ms	262.14 ms	174.76 ms
1 1	64	2.097 sec	1.049 sec	699.05 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

COPRST — Arm/Reset COP Timer Circuitry **$103A**

	Bit 7	6	5	4	3	2	1	Bit 0
	7	6	5	4	3	2	1	0
RESET:	0	0	0	0	0	0	0	0

Write $55 to COPRST to arm COP watchdog clearing mechanism. Write $AA to COPRST to reset COP watchdog.

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous **$103C**

	Bit 7	6	5	4	3	2	1	Bit 0
	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0
RESET:	—	—	—	—	0	1	0	1

RBOOT — Read Bootstrap ROM

Refer to **Operating Modes and Memory Maps**.

SMOD, MDA — Special Mode Select and Mode Select A

Refer to **Operating Modes and Memory Maps**.

IRVNE — Internal Read Visibility/Not E

Refer to **Operating Modes and Memory Maps**.

PSEL3–PSEL0 — Priority Select Bits 3 through 0

Writable only while the I bit in the CCR is set (interrupts disabled). These bits select one interrupt source to be elevated above all other I-bit related sources. Refer to the following table.

PSEL[3:0]	Interrupt Source Promoted
0000	Timer Overflow
0001	Pulse Accumulator Overflow
0010	Pulse Accumulator Input Edge
0011	SPI Serial Transfer Complete
0100	SCI Serial System
0101	Reserved (Default to $\overline{\text{IRQ}}$)
0110	$\overline{\text{IRQ}}$ (External Pin)
0111	Real-Time Interrupt
1000	Timer Input Capture 1
1001	Timer Input Capture 2
1010	Timer Input Capture 3
1011	Timer Output Compare 1
1100	Timer Output Compare 2
1101	Timer Output Compare 3
1110	Timer Output Compare 4
1111	Timer Output Compare 5/Input Capture 4

CONFIG — COP, EPROM, EEPROM Enables **$103F**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	NOSEC	NOCOP	EPON	EEON
RESET:	0	0	0	0	0	—	1	0

Bits 7–4 — Not implemented; always read zero

NOSEC — EEPROM and EPROM Security Disable
Refer to **Electrically Erasable Programmable Read-Only Memory (EEPROM)**.

NOCOP — COP System Disable
0 = COP enabled (forces reset on timeout)
1 = COP disabled (does not force reset on timeout)

EPON — EPROM Enable
Refer to **Operating Modes and Memory Maps**.

EEON — EEPROM Enable
Refer to **Electrically Erasable Programmable Read-Only Memory (EEPROM)**.

Electrically Erasable Programmable Read-Only Memory (EEPROM)

The 512 bytes of EEPROM in the MC68HC711L6 are located at $B600 through $B7FF. The EEON bit in CONFIG determines whether or not the EEPROM is in the memory map. When EEON = 1 (erased state), the EEPROM is enabled. When EEON = 0, the EEPROM is disabled and out of the memory map. EEON is reset to the value last programmed into CONFIG.

An on-chip charge pump develops the high voltage required for programming and erasing. When the frequency of the E clock is less than 1 MHz, select an internal clock to drive the EEPROM charge pump by writing one to the CSEL bit in the OPTION register.

Programming and erasing the EEPROM is controlled by the PPROG register and dependent upon the block protect (BPROT) register value.

To erase the EEPROM, ensure that the proper bits of the BPROT register are cleared, then complete the following steps using the PPROG register:

1. Write to PPROG with the ERASE, EELAT, and appropriate BYTE and ROW bits set.
2. Write to the appropriate EEPROM address with any data. Row erase only requires a write to any location in the row. Bulk erase is accomplished by writing to any location in the array.
3. Write to PPROG with ERASE, EELAT, EEPGM, and appropriate BYTE and ROW bits set.
4. Delay for 10 ms or more, as appropriate.
5. Clear the EEPGM bit in PPROG to turn off the high voltage.
6. Clear the PPROG register to reconfigure the EEPROM address and data buses for normal operation.

To program the EEPROM, ensure the proper bits of the BPROT register are cleared, then complete the following steps with the PPROG register:

1. Write to PPROG with the EELAT bit set.
2. Write data to the desired address.
3. Write to PPROG with the EELAT and EEPGM bits set.
4. Delay for 10 ms or more, as appropriate.
5. Clear the EEPGM bit in PPROG to turn off the high voltage.
6. Clear the PPROG register to reconfigure the EEPROM address and data buses for normal operation.

BPROT — Block Protect **$1035**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	PTCON	BPRT3	BPRT2	BPRT1	BPRT0
RESET:	0	0	0	1	1	1	1	1

Block protect register bits can be written to zero (protection disabled) within 64 cycles of a reset in normal modes, or any time in special modes. Block protect register bits can be written to one (protection enabled) at any time.

PTCON — Protect for CONFIG

0 = CONFIG register can be programmed or erased normally
1 = CONFIG register can not be programmed or erased

BPRT3–BPRT0 — Block Protect Bits for EEPROM

0 = Protection disabled for associated block
1 = Protection enabled for associated block

Bit Name	Block Protected	Block Size
BPRT0	$B600–$B61F	32 Bytes
BPRT1	$B620–$B65F	64 Bytes
BPRT2	$B660–$B6DF	128 Bytes
BPRT3	$B6E0–$B7FF	288 Bytes

OPTION — System Configuration Options **$1039**

	Bit 7	6	5	4	3	2	1	Bit 0
	ADPU	CSEL	IRQE*	DLY*	CME	0	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes.

ADPU — A/D Converter Power Up

Refer to **Analog-to-Digital Converter**.

CSEL — Clock Select

0 = A/D and EEPROM use system E clock
1 = A/D and EEPROM use internal RC clock

IRQE — $\overline{\text{IRQ}}$ Select Edge-Sensitive Only
Refer to **Resets and Interrupts**.

DLY — Enable Oscillator Start-Up Delay on Exit from STOP
Refer to **Resets and Interrupts**.

CME — Clock Monitor Enable
Refer to **Resets and Interrupts**.

Bit 2 — Not implemented; always reads zero

PPROG — EEPROM and EPROM Programming Control **$103B**

	Bit 7	6	5	4	3	2	1	Bit 0
	ODD	EVEN	ELAT	BYTE	ROW	ERASE	EELAT	PGM
RESET:	0	0	0	0	0	0	0	0

ODD — Program Odd Rows in Half of EEPROM (TEST)

EVEN — Program Even Rows in Half of EEPROM (TEST)

ELAT — EPROM (OTPROM) Latch Control
0 = EPROM address and data bus configured for normal reads and cannot be programmed
1 = EPROM address and data bus configured for programming and cannot be read

BYTE — Byte/Other EEPROM Erase Mode
ROW — Row/All EEPROM Erase Mode
Refer to the following table.

BYTE	ROW	Action
0	0	Bulk Erase (All 512 Bytes)
0	1	Row Erase (16 Bytes)
1	0	Byte Erase
1	1	Byte Erase

ERASE — Erase/Normal Control for EEPROM
0 = Normal read or program mode
1 = Erase mode

EELAT — EEPROM Latch Control
0 = EEPROM address and data bus configured for normal reads
1 = EEPROM address and data bus configured for programming or erasing

PGM — EEPROM and EPROM (OTPROM) Program Command
0 = Programming voltage switched off to EEPROM and EPROM array
1 = Programming voltage switched on to EEPROM or EPROM array

CONFIG — COP, EPROM, EEPROM Enables **$103F**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	NOSEC	NOCOP	EPON	EEON
RESET:	0	0	0	0	0	—	1	0

Bits 7–4 — Not implemented; always read zero

NOSEC — EEPROM and EPROM Security Disable
NOSEC has no meaning unless the security mask option was specified at the time of manufacture.
0 = Security enabled
1 = Security disabled

NOCOP — COP System Disable
Refer to **Resets and Interrupts**.

EPON — EPROM Enable
Refer to **Erasable Programmable Read-Only Memory (EPROM)**.

EEON — EEPROM Enable
0 = EEPROM removed from the memory map
1 = EEPROM present in the memory map

Erasable Programmable Read-Only Memory (EPROM)

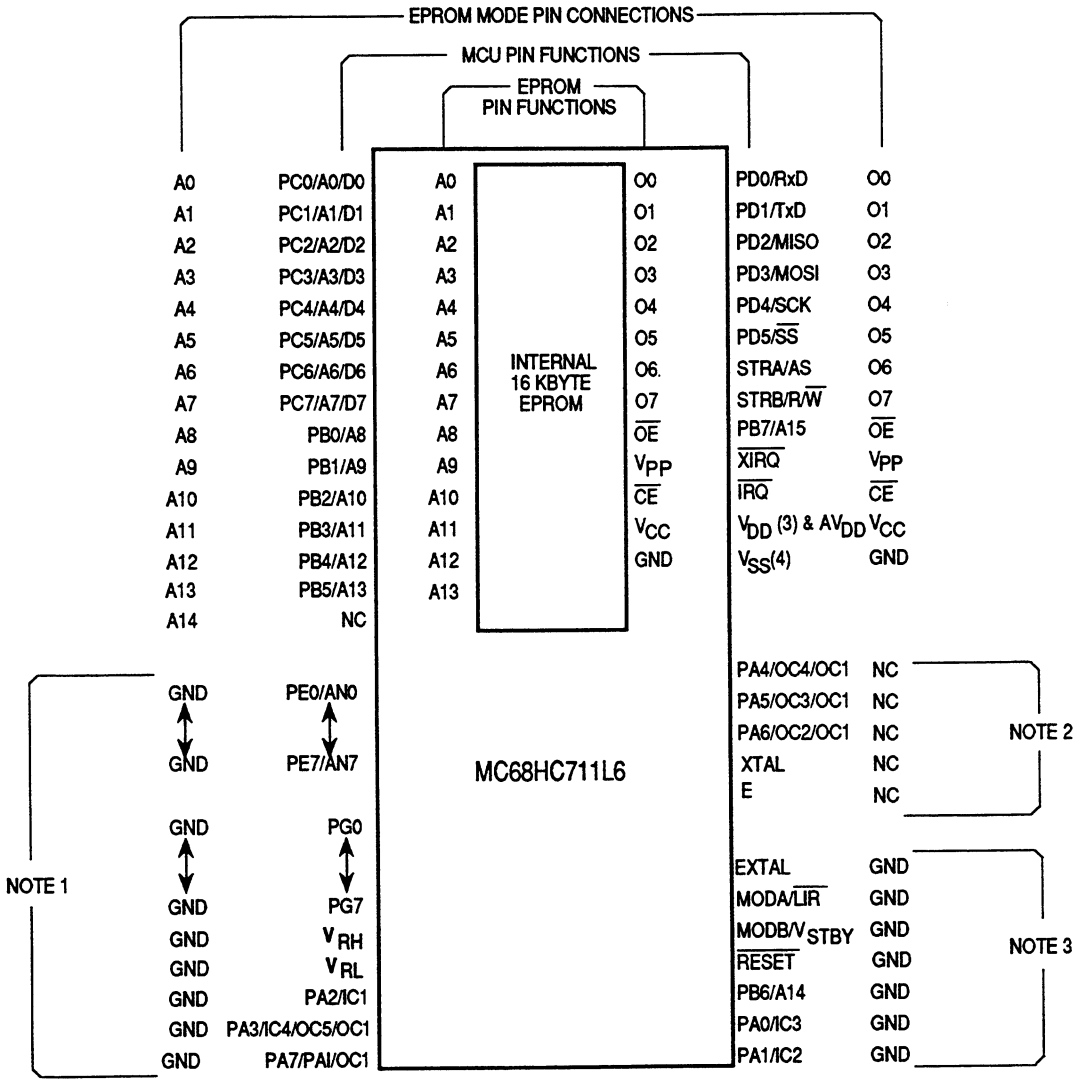
The MC68HC711L6 has 16 Kbytes of ultraviolet-erasable programmable read-only memory (EPROM). When the MCU is packaged in an opaque plastic package, the EPROM cannot be erased. This is referred to as one-time programmable read-only memory (OTPROM).

The 16 Kbyte EPROM is located at $C000 through $FFFF. The EPROM can be removed from the memory map in all modes except single chip by programming the EPON bit in the CONFIG register to zero.

Programming EPROM requires an external 12.25 volt nominal power supply (V_{PP}). The erased state of EPROM is $FF (all ones). There are two methods used to program and verify EPROM:

1. In PROG mode, the EPROM is programmed as a stand-alone EPROM by adapting the MCU footprint to that of the 27256-type EPROM and using an appropriate EPROM programmer.
2. In normal MCU mode, the EPROM can be programmed in any operating mode; however, special test and bootstrap are preferred. Normal programming is done through the PPROG register.

Refer to the following diagram, which shows the programming pin connections in PROG mode.



NOTES: 1. Unused Inputs — grounding is recommended.
2. Unused outputs — these pins should be left unterminated.
3. These pins must be grounded for PROG mode.

MC68HC711L6 Block Diagram in PROG Mode

PPROG — EEPROM and EPROM Programming Control **$103B**

	Bit 7	6	5	4	3	2	1	Bit 0
	ODD	EVEN	ELAT	BYTE	ROW	ERASE	EELAT	PGM
RESET:	0	0	0	0	0	0	0	0

ODD — Program Odd Rows in Half of EEPROM (TEST)
Refer to **Electrically Erasable Programmable Read-Only Memory (EEPROM)**.

EVEN — Program Even Rows in Half of EEPROM (TEST)
Refer to **Electrically Erasable Programmable Read-Only Memory (EEPROM).**

ELAT — EPROM (OTPROM) Latch Control
0 = EPROM address and data bus configured for normal reads and cannot be programmed
1 = EPROM address and data bus configured for programming and cannot be read

BYTE — Byte/Other EEPROM Erase Mode
Refer to **Electrically Erasable Programmable Read-Only Memory (EEPROM).**

ROW — Row/All EEPROM Erase Mode
Refer to **Electrically Erasable Programmable Read-Only Memory (EEPROM).**

ERASE — Erase/Normal Control for EEPROM
Refer to **Electrically Erasable Programmable Read-Only Memory (EEPROM).**

EELAT — EEPROM Latch Control
Refer to **Electrically Erasable Programmable Read-Only Memory (EEPROM).**

PGM — EEPROM and EPROM Program Command
0 = Programming or erase voltage to EEPROM and EPROM array switched off
1 = Programming or erase voltage to EEPROM and EPROM array switched on

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CONFIG — COP, EPROM, EEPROM Enables **$103F**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	0	NOSEC	NOCOP	EPON	EEON
RESET:	0	0	0	0	0	—	1	0

Bits 7–4 — Not implemented; always read zero

NOSEC — EEPROM and EPROM Security Disable
NOSEC is invalid unless the security mask option is specified before the MCU is manufactured.
0 = Security enabled
1 = Security disabled

NOCOP — COP System Disable
Refer to **Resets and Interrupts.**

EPON — EPROM Enable
Forced to one out of reset in single-chip and bootstrap modes.
0 = EPROM removed from the memory map
1 = EPROM present in the memory map

EEON — EEPROM Enable
Refer to **Electrically Erasable Programmable Read-Only Memory (EEPROM).**

Parallel Input/Output

The MC68HC711L6 has up to 46 input/output lines, depending on the operating mode. In single-chip and bootstrap modes, all ports are parallel I/O data ports. In expanded multiplexed and test modes, ports B and C and lines AS and R/W are a memory expansion bus. Port B is the high-order address bus, port C is the multiplexed address and data bus, AS is the demultiplexing signal, and R/W is the data bus direction control. Refer to the following table.

Port	Input Pins	Output Pins	Bidirectional pins	Shared Functions
Port A	3	3	2	Timer
Port B	—	8	—	High Order Address
Port C	—	—	8	Low Order Address and Data Bus
Port D	—	—	6	SCI, SPI
Port E	8	—	—	A/D Converter System
Port G	—	—	8	None

Parallel I/O Handshake

Simple and full handshake input and output functions are available on ports B and C in single-chip modes. In simple strobed mode, port B is a strobed output port and port C is a latching input port. The two activities are available simultaneously.

The STRB output is pulsed for two E-clock periods each time there is a write to the PORTB register. The INVB bit in the PIOC register controls the polarity of STRB pulses. Port C levels are latched into the alternate port C latch (PORTCL) register on each assertion of the STRA input. STRA edge select, flag and interrupt enable bits are located in the PIOC register. Any or all of the port C lines can still be used as general-purpose I/O while in strobed input mode.

Full handshake modes use port C pins and the STRA and STRB lines. Input and output handshake modes are supported, and output handshake mode has a three-stated variation. STRA is an edge-detecting input, and STRB is a handshake output. Control and enable bits are located in the PIOC register.

In full input handshake mode, the MCU uses STRB as a "ready" line to an external system. Port C logic levels are latched into PORTCL when the STRA line is asserted by the external system. The MCU then deasserts STRB. The MCU reasserts STRB after the PORTCL register is read. A mix of latched inputs, static inputs, and static outputs is allowed on port C, differentiated by the data direction bits and use of the PORTC and PORTCL registers.

In full output handshake mode, the MCU writes data to PORTCL, which, in turn, asserts the STRB output to indicate that data is ready. The external system reads the STRB output (port C) and asserts the STRA input to acknowledge that data has been received.

In the three-state variation of output handshake mode, lines intended as three-state handshake outputs are configured as inputs by clearing the corresponding DDRC bits. The MCU writes data to PORTCL and asserts STRB. The external system responds by activating the STRA input, which forces the MCU to drive the data in PORTCL out on all of the port C lines. The mode variation does not allow part of port C to be used for static inputs while other port C pins are being used for handshake outputs. Refer to the PIOC register description.

PORTA — Port A Data **$1000**

	Bit 7	6	5	4	3	2	1	Bit 0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	HiZ	0	0	0	HiZ	HiZ	HiZ	HiZ
Alt. Pin Func.:	PAI	OC2	OC3	OC4	OC5/IC4	IC1	IC2	IC3
And/or:	OC1	OC1	OC1	OC1	OC1	—	—	—

PIOC — Parallel I/O Control **$1002**

	Bit 7	6	5	4	3	2	1	Bit 0
	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB
RESET:	0	0	0	0	0	U	1	1

STAF — Strobe A Interrupt Status Flag

Set when selected edge occurs on Strobe A. Cleared by PIOC read with STAF set followed by PORTCL read (simple strobed or full input handshake mode) or PORTCL write (output handshake mode).

STAI — Strobe A Interrupt Enable Mask

0 = STAF interrupts disabled
1 = STAF interrupts enabled

CWOM — Port C Wire-OR Mode (affects all eight port C pins)

0 = Port C outputs are normal CMOS outputs
1 = Port C outputs are open-drain outputs

HNDS — Handshake Mode

0 = Simple strobe mode
1 = Full input or output handshake mode

OIN — Output or Input Handshake Select

HNDS must be set to one for this bit to have meaning.

0 = Input handshake
1 = Output handshake

PLS — Pulsed/Interlocked Handshake Operation

HNDS must be set to one for this bit to have meaning.

0 = Interlocked handshake
1 = Pulsed handshake (Strobe B pulses high for two E-clock cycles.)

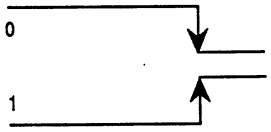
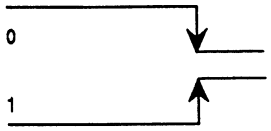
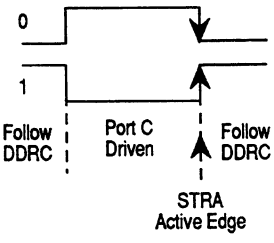
EGA — Active Edge for Strobe A

0 = STRA falling edge selected
1 = STRA rising edge selected

INVB — Invert Strobe B

0 = Active level is logic zero
1 = Active level is logic one

Parallel I/O Control

	STAF Clearing Sequence	HNDS	OIN	PLS	EGA	Port C	Port B
Simple strobed mode	Read PIOC with STAF =1 then read PORTCL	0	X	X		Inputs latched into PORTCL on any active edge on STRA	STRB pulses on writes to port B
Full input handshake	Read PIOC with STAF =1 then read PORTCL	1	0	0 = STRB active level 1 = STRB active pulse		Inputs latched into PORTCL on any active edge on STRA	Normal output port, unaffected in hand-shake modes
Full output handshake	Read PIOC with STAF =1 then write to PORTCL	1	1	0 = STRB active level 1 = STRB active pulse		Driven as outputs if STRA at active level, follows DDRC if STRA not at active level	Normal output port, unaffected in hand-shake modes

PORTC — Port C Data **$1003**

	Bit 7	6	5	4	3	2	1	Bit 0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
S. Chip or Boot:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	0	0	0	0	0	0	0	0
Expan. or Test:	A7/D7	A6/D6	A5/D5	A4/D4	A3/D3	A2/D2	A1/D1	A0/D0

NOTE

In single chip and boot modes, port C pins reset to high impedance inputs (DDRC registers are set to zero). In expanded and special test modes, port C pins become multiplexed address/data bus pins and the port C register address is treated as an external memory location.

PORTB — Port B Data **$1004**

	Bit 7	6	5	4	3	2	1	Bit 0
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
S. Chip or Boot:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
RESET:	Reset forces port B pins low							
Expan. or Test:	A15	A14	A13	A12	A11	A10	A9	A8
RESET:	Reset configures pins as high order address outputs							

PORTCL — Port C Latched **$1005**

	Bit 7	6	5	4	3	2	1	Bit 0
	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
RESET:	U	U	U	U	U	U	U	U

Writes affect port C pins. PORTCL is used in the handshake clearing mechanism. When an active edge occurs on the STRA pin, port C data is latched into the PORTCL register.

DDRC — Data Direction Register for Port C **$1007**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
RESET:	0	0	0	0	0	0	0	0

DDC7–DDC0 — Data Direction for Port C
0 = Configure corresponding I/O pin for input
1 = Configure corresponding I/O pin for output

PORTD — Port D Data **$1008**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	—	—	$\overline{SS}$	SCK	MOSI	MISO	TxD	RxD

DDRD — Data Direction Register for Port D **$1009**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	—	—	$\overline{SS}$	SCK	MOSI	MISO	TxD	RxD

DDD5–DDD0 — Data Direction for Port D

When DDRD bit 5 is one and MSTR = 1 in SPCR, PD5/$\overline{SS}$ is a general-purpose output, and mode fault logic is disabled.

0 = Input
1 = Output

PORTE — Port E Data **$100A**

	Bit 7	6	5	4	3	2	1	Bit 0
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
RESET:	U	U	U	U	U	U	U	U
Alt. Pin Func.:	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

PACTL — Pulse Accumulator Control **$1026**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

DDRA7 — Data Direction for Port A Bit 7

0 = Input
1 = Output

PAEN — Pulse Accumulator Enable

Refer to **Pulse Accumulator**.

PAMOD — Pulse Accumulator Mode Select

Refer to **Pulse Accumulator**.

PEDGE — Pulse Accumulator Edge Select

Refer to **Pulse Accumulator**.

DDRA3 — Data Direction for Port A Bit 3

Overridden if an output compare function is configured to control the PA3 pin.

0 = Input
1 = Output

I4/O5 — Input Capture 4/Output Compare 5
0 = OC5 enabled
1 = IC4 enabled

RTR1, RTR0 — Real-Time Rate Selects
Refer to **Main Timer**.

PORTG — Port G Data **$1036**

	Bit 7	6	5	4	3	2	1	Bit 0
	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
RESET:	0	0	0	0	0	0	0	0

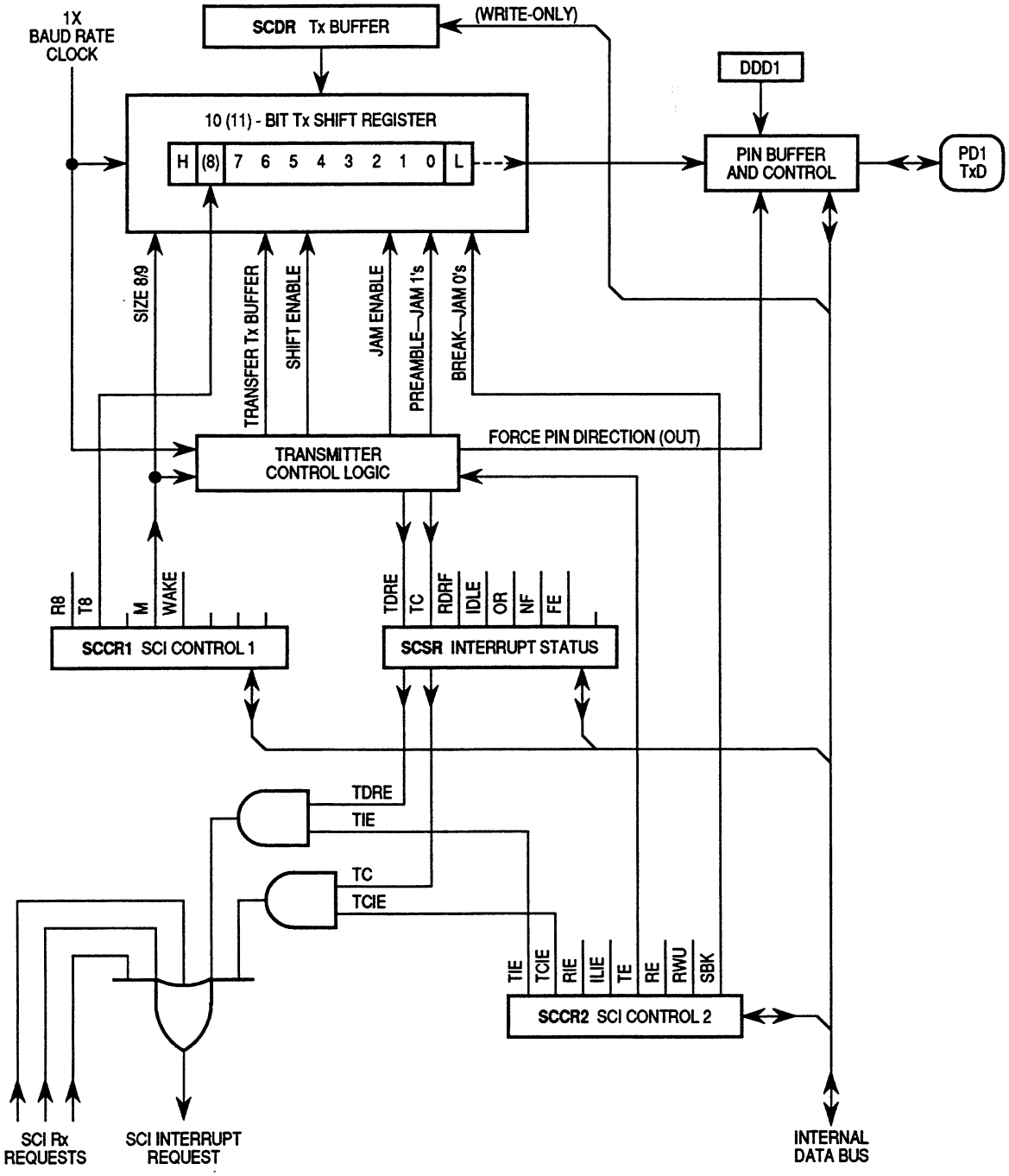
DDRG — Data Direction Register for Port G **$1037**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDG7	DDG6	DDG5	DDG4	DDG3	DDG2	DDG1	DDG0
RESET:	0	0	0	0	0	0	0	0

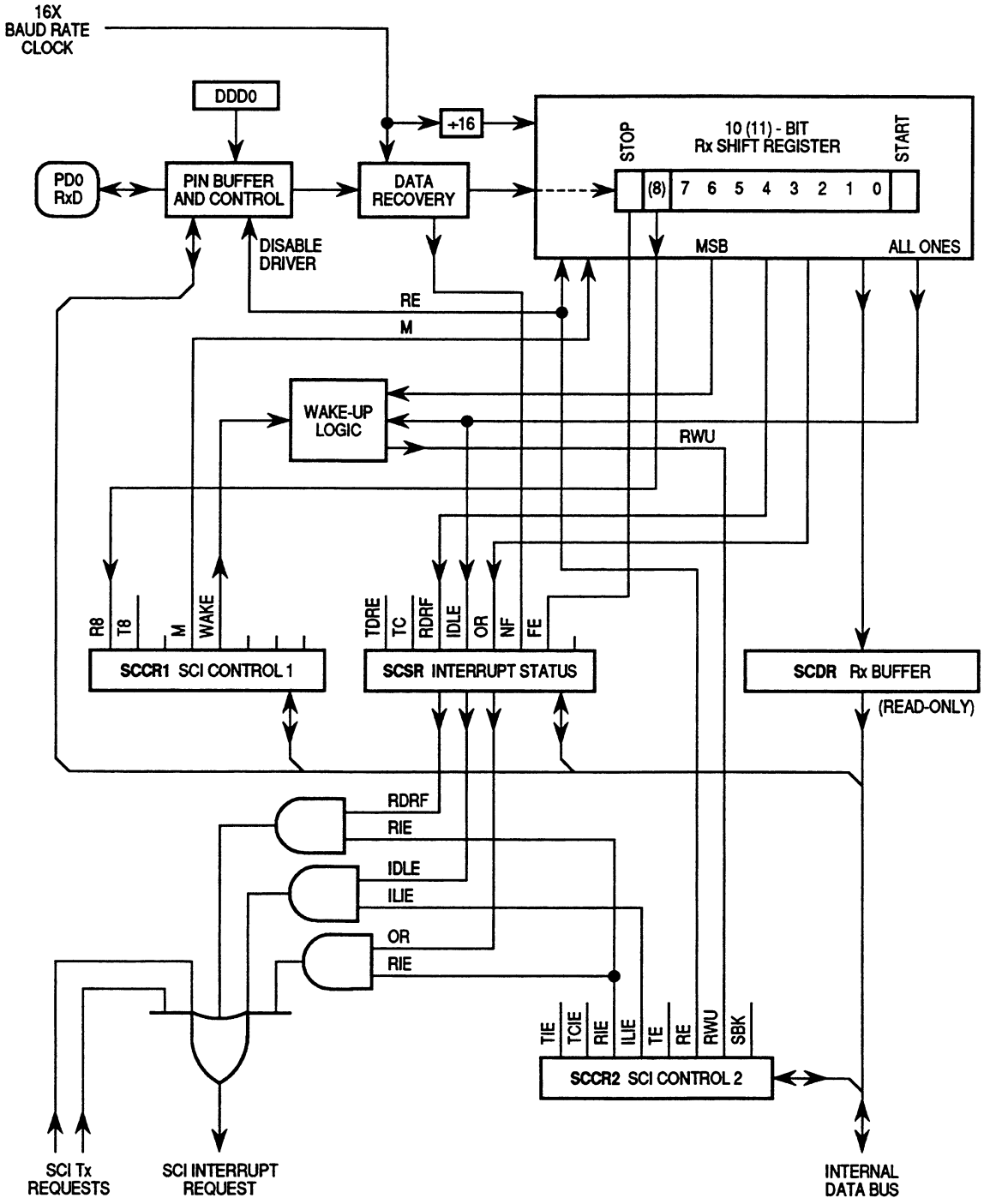
DDG7–DDG0 — Data Direction for Port G
0 = Input
1 = Output

Serial Communications Interface (SCI)

The SCI, a universal asynchronous receiver transmitter (UART) serial communications interface, is one of two independent serial I/O subsystems in the MC68HC711L6. It has a standard nonreturn to zero (NRZ) format (one start, eight or nine data and one stop bit) and several baud rates available. The SCI transmitter and receiver are independent but use the same data format and bit rate.



SCI Transmitter Block Diagram



SCI Receiver Block Diagram

SPCR — Serial Peripheral Control Register **$1028**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

SPIE — Serial Peripheral Interrupt Enable
Refer to **Serial Peripheral Interface (SPI)**.

SPE — Serial Peripheral System Enable
Refer to **Serial Peripheral Interface (SPI)**.

DWOM — Port D Wired-OR Mode Option for Pins PD5–PD0
0 = Normal CMOS outputs
1 = Open-drain outputs

MSTR — Master Mode Select
Refer to **Serial Peripheral Interface (SPI)**.

CPOL, CPHA — Clock Phase, Clock Polarity
Refer to **Serial Peripheral Interface (SPI)**.

SPR1, SPR0 — SPI Clock Rate Selects
Refer to **Serial Peripheral Interface (SPI)**.

BAUD — Baud Rate **$102B**

	Bit 7	6	5	4	3	2	1	Bit 0
	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
RESET:	0	0	0	0	0	U	U	U

TCLR — Clear Baud Rate Counters (TEST)

Bit 6 — Not implemented; this bit always reads zero

SCP1, SCP0 — SCI Baud Rate Prescaler Selects
Refer to the following baud rate tables and to the figure that illustrates the baud rate clock divider chain.

RCKB — SCI Baud Rate Clock Check (TEST)

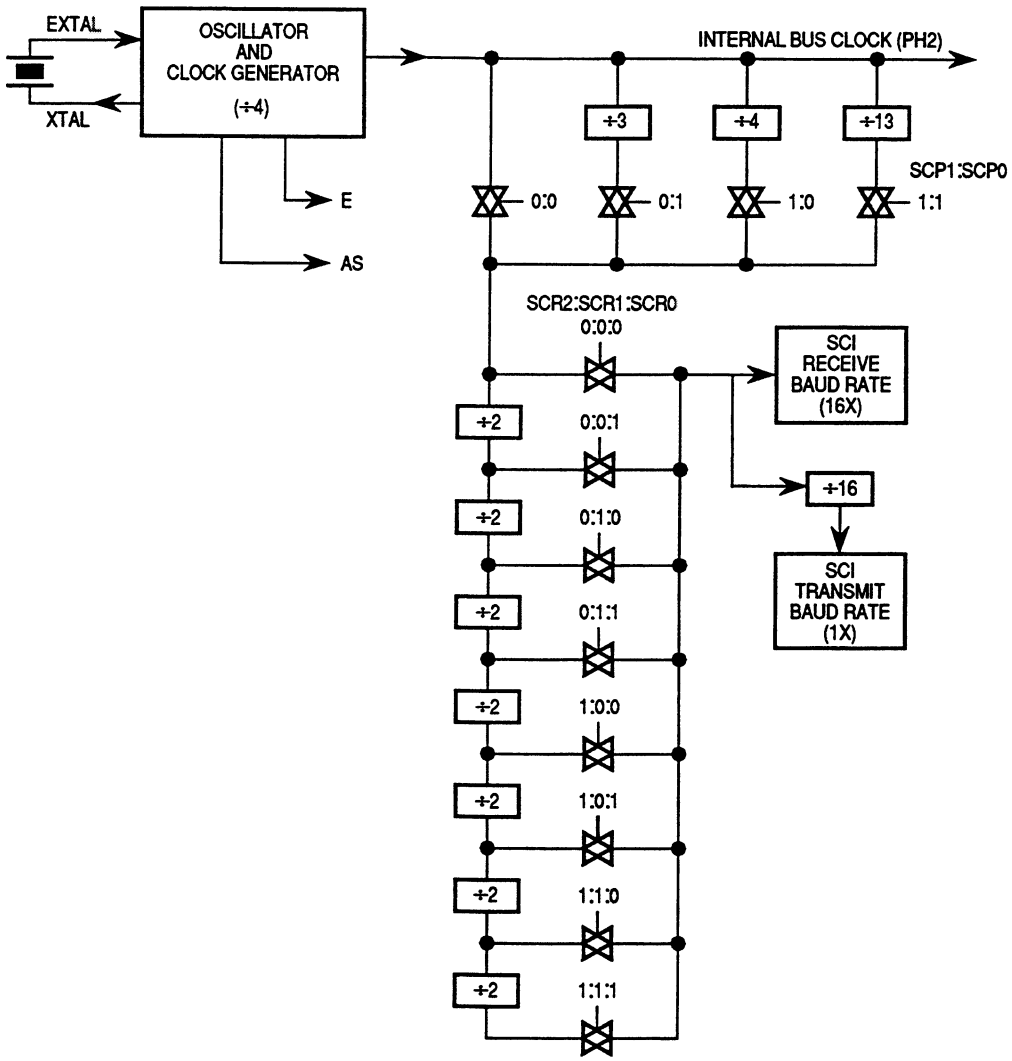
SCR2, SCR1, and SCR0 — SCI Baud Rate Selects
Selects receiver and transmitter baud rate based on output from baud rate prescaler stage. Refer to the baud rate clock divider chain.

Baud Rate Prescaler Sets Highest Rate

SCP[1:0]	Divide Internal Clock By	Crystal Frequency in MHz			
		4.0 MHz (Baud)	8.0 MHz (Baud)	10.0 MHz (Baud)	12.0 MHz (Baud)
00	1	62.50K	125.0K	156.25K	187.5K
01	3	20.83K	41.67K	52.08K	62.5K
10	4	15.625K	31.25K	38.4K	46.88K
11	13	4800	9600	12.02K	14.42K

Baud Rate Selection Table

SCR[2:0]	Divide Prescaler By	Highest Baud Rate (Prescaler Output from Previous Table)		
		4800	9600	38.4K
000	1	4800	9600	38.4K
001	2	2400	4800	19.2K
010	4	1200	2400	9600
011	8	600	1200	4800
100	16	300	600	2400
101	32	150	300	1200
110	64	—	150	600
111	128	—	—	300



Baud Rate Clock Divider Chain

SCCR1 — SCI Control Register 1 **$102C**

	Bit 7	6	5	4	3	2	1	Bit 0
	R8	T8	0	M	WAKE	0	0	0
RESET:	U	U	0	0	0	0	0	0

R8 — Receive Data Bit 8

If M bit is set, R8 stores ninth bit in receive data character.

T8 — Transmit Data Bit 8

If M bit is set, T8 stores ninth bit in transmit data character.

Bits 5 and 2–0 — These bits are not implemented; always read zero

M — Mode (Select Character Format)
- 0 = Start bit, 8 data bits, 1 stop bit
- 1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wake up by Address Mark/Idle
- 0 = Wake up by IDLE line recognition
- 1 = Wake up by address mark (most significant data bit set)

SCCR2 — SCI Control Register 2 **$102D**

	Bit 7	6	5	4	3	2	1	Bit 0
	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET:	0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
- 0 = TDRE interrupts disabled
- 1 = SCI interrupt requested when TDRE status flag is set

TCIE — Transmit Complete Interrupt Enable
- 0 = TC interrupts disabled
- 1 = SCI interrupt requested when TC status flag is set

RIE — Receiver Interrupt Enable
- 0 = RDRF and OR interrupts disabled
- 1 = SCI interrupt requested when RDRF flag or the OR status flag is set

ILIE — Idle Line Interrupt Enable
- 0 = IDLE interrupts disabled
- 1 = SCI interrupt requested when IDLE status flag is set

TE — Transmitter Enable
- 0 = Transmitter disabled
- 1 = Transmitter enabled

RE — Receiver Enable
- 0 = Receiver disabled
- 1 = Receiver enabled

RWU — Receiver Wake-up Control
- 0 = Normal SCI receiver
- 1 = Wake-up enabled and receiver interrupts inhibited

SBK — Send Break
- 0 = Break generator off
- 1 = Break codes generated as long as SBK = 1

SCSR — SCI Status Register **$102E**

	Bit 7	6	5	4	3	2	1	Bit 0
	TDRE	TC	RDRF	IDLE	OR	NF	FE	0
RESET:	1	1	0	0	0	0	0	0

TDRE — Transmit Data Register Empty Flag

Set if transmit data can be written to SCDR; if TDRE = 0, transmit data register is busy. Cleared by SCSR read with TDRE set, followed by SCDR write.

TC — Transmit Complete Flag

Set if transmitter is idle (no data, preamble, or break transmission in progress). Cleared by SCSR read with TC set, followed by SCDR write.

RDRF — Receive Data Register Full Flag

Set if a received character is ready to be read from SCDR. Cleared by SCSR read with RDRF set, followed by SCDR read.

IDLE — Idle Line Detected Flag

Set if the RxD line is idle. Cleared by SCSR read with IDLE set, followed by SCDR read. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again.

OR — Overrun Error Flag

Set if a new character is received before a previously received character is read from SCDR. Cleared by SCSR read with OR set, followed by SCDR read.

NF — Noise Error Flag

Set if majority sample logic detects anything other than a unanimous decision. Cleared by SCSR read with NF set, followed by SCDR read.

FE — Framing Error

Set if a 0 is detected where a stop bit was expected. Cleared by SCSR read with FE set, followed by SCDR read.

Bit 0 — Not implemented; this bit always reads zero

SCDR — SCI Data Register **$102F**

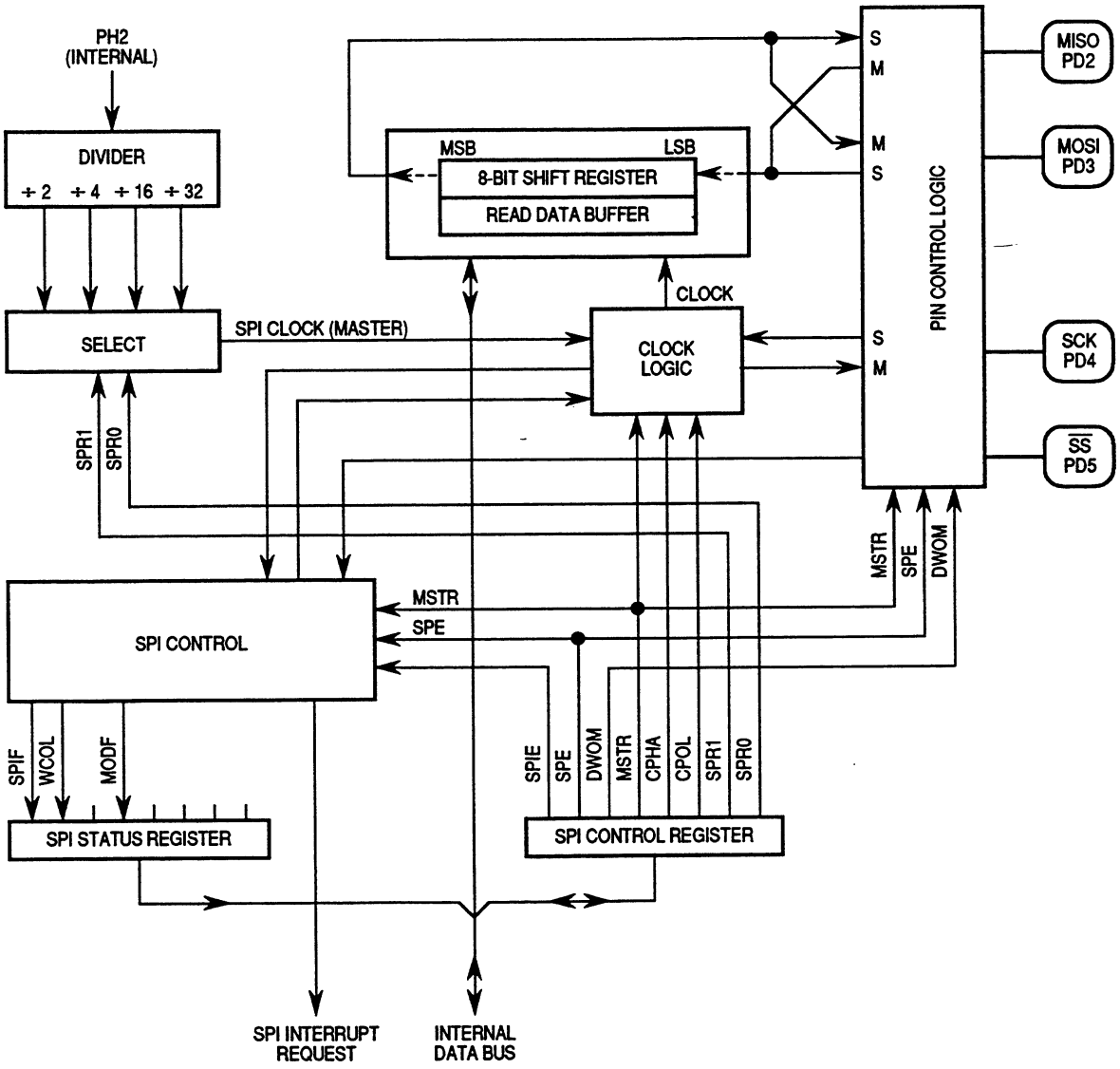
	Bit 7	6	5	4	3	2	1	Bit 0
	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
RESET:	U	U	U	U	U	U	U	U

NOTE

Receive and transmit are double buffered. Reads access the receive data buffer, and writes access the transmit data buffer.

Serial Peripheral Interface (SPI)

The SPI is one of two independent serial communications subsystems that allow the MCU to communicate synchronously with peripheral devices and other microprocessors. The SPI protocol facilitates rapid exchange of serial data between devices in a control system. Each SPI compatible component in a system can be set up for master or slave operation. Data rates can be as high as one half of the E-clock rate when configured as master, and as fast as the E clock when configured as slave.



SPI Block Diagram

DDRD — Data Direction Register for Port D **$1009**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	—	—	$\overline{SS}$	SCK	MOSI	MISO	TxD	RxD

DDD5–DDD0 — Data Direction for Port D

When DDRD bit 5 is one and MSTR = 1 in SPCR, PD5/$\overline{SS}$ is a general-purpose output and mode fault logic is disabled.

0 = Input
1 = Output

SPCR — Serial Peripheral Control Register **$1028**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

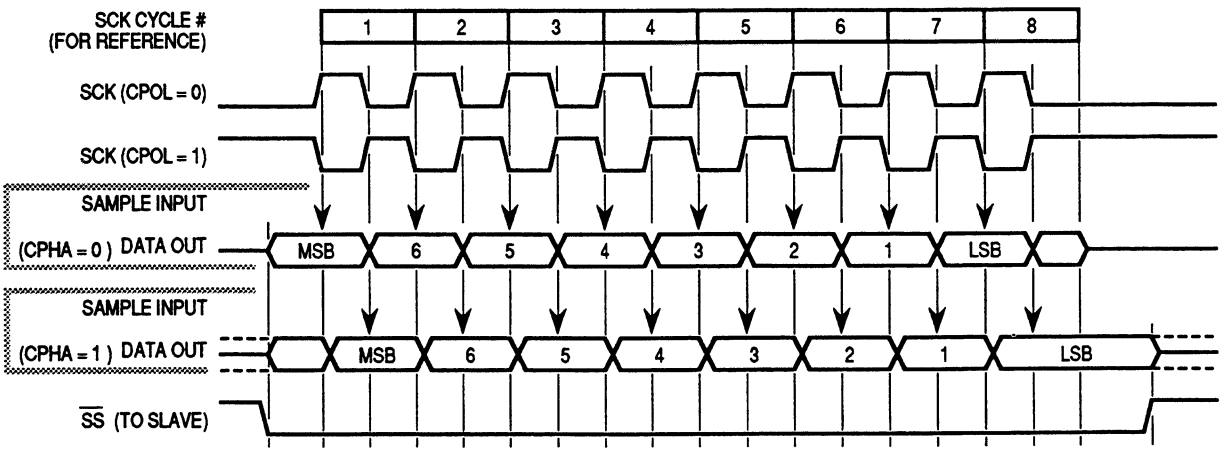
SPIE — Serial Peripheral Interrupt Enable
0 = SPI interrupt disabled
1 = SPI interrupt enabled

SPE — Serial Peripheral System Enable
0 = SPI off
1 = SPI on

DWOM — Port D Wired-OR Mode Option for Pins PD5–PD0
Affects all six port D pins
0 = Normal CMOS outputs
1 = Open-drain outputs

MSTR — Master Mode Select
0 = Slave mode
1 = Master mode

CPOL, CPHA — Clock Phase, Clock Polarity
Refer to figure (SPI Transfer Format).



SPI Transfer Format

SPR1 and SPR0 — SPI Clock Rate Selects

SPR[1:0]	E Clock Divide By	Frequency at E = 2 MHz (Baud)
0 0	2	1.0 MHz
0 1	4	500 kHz
1 0	16	125 kHz
1 1	32	62.5 kHz

SPSR — Serial Peripheral Status Register **$1029**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIF	WCOL	0	MODF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

SPIF — SPI Transfer Complete Flag

Set when an SPI transfer is complete. Cleared by reading SPSR with SPIF set, followed by SPDR access.

WCOL — Write Collision

Set when SPDR is written while transfer is in progress. Cleared by SPSR with WCOL set, followed by SPDR access.

Bits 5 and 3–0 — Not Implemented; always read zero

MODF — Mode Fault (A Mode Fault Terminates SPI Operation)

Set when $\overline{SS}$ is pulled low while MSTR = 1. Cleared by SPSR read with MODF set, followed by SPCR write.

SPDR — SPI Data Register **$102A**

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

NOTE

SPI is double buffered in, single buffered out.

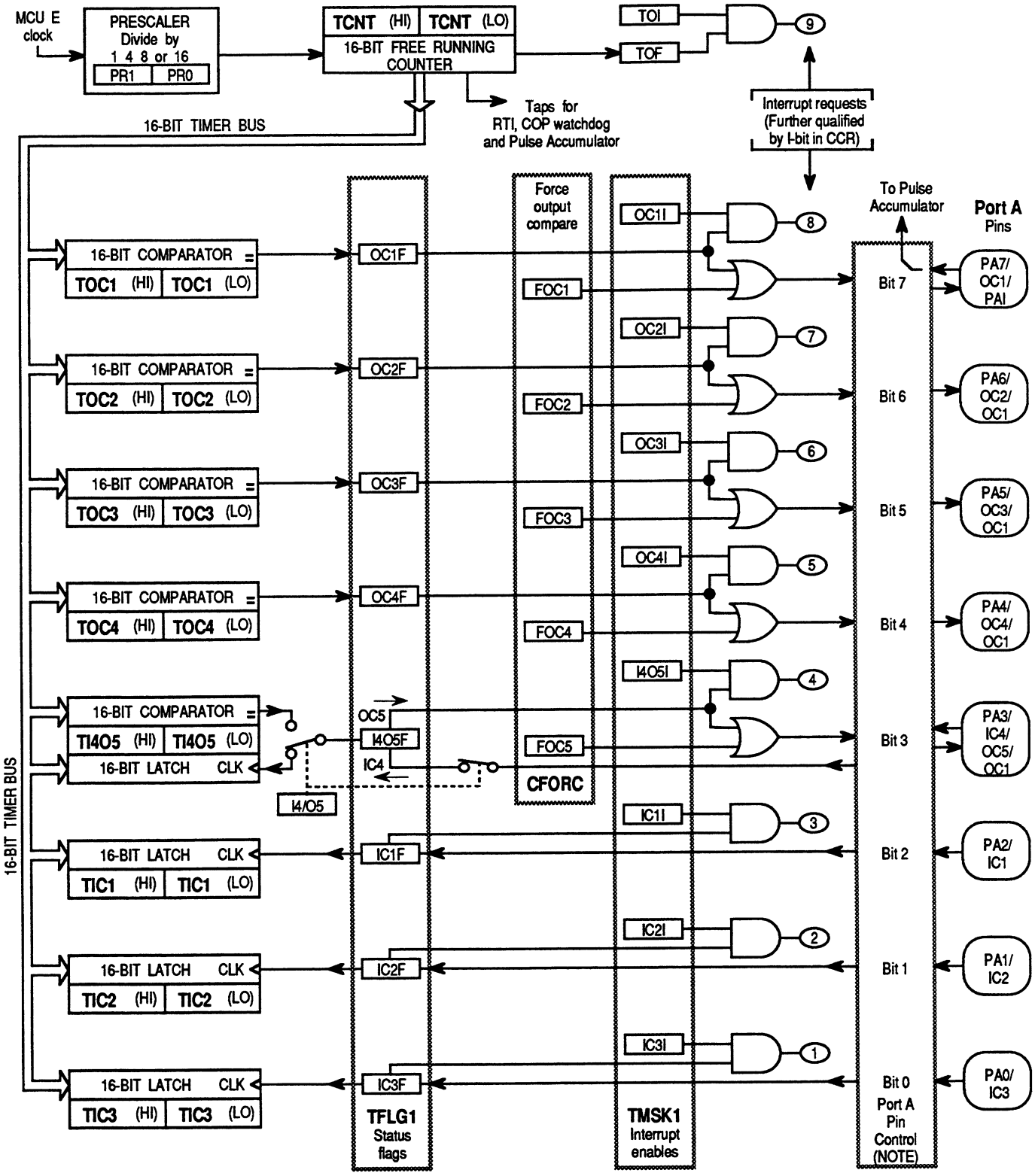
Main Timer

The main timer is based on a free-running 16-bit counter with a four-stage programmable prescaler. The timer shares Port A pins, which can be configured for 3 timer input capture (IC) and 4 timer output compare (OC), and either a fourth IC or a fifth OC. A timer overflow function allows software to extend the system's timing capability beyond the counter's 16-bit range.

Refer to the following table for a summary of crystal-related frequencies and periods.

Timer Summary

Control Bits	XTAL Frequencies			
	4.0 MHz	8.0 MHz	12.0 MHz	Other Rates
	1.0 MHz	2.0 MHz	3.0 MHz	(E)
	1000 ns	500 ns	333 ns	(1/E)
PR[1:0]	Main Timer Count Rates			
0 0 1 count — overflow —	1.0 µs 65.536 ms	500 ns 32.768 ms	333 ns 21.845 ms	(E/1) ($E/2^{16}$)
0 1 1 count — overflow —	4.0 µs 262.14 ms	2.0 µs 131.07 ms	1.333 µs 87.381 ms	(E/4) ($E/2^{18}$)
1 0 1 count — overflow —	8.0 µs 524.29 ms	4.0 µs 262.14 ms	2.667 µs 174.76 ms	(E/8) ($E/2^{19}$)
1 1 1 count — overflow —	16.0 µs 1.049 s	8.0 µs 524.29 ms	5.333 µs 349.52 ms	(E/16) ($E/2^{20}$)
RTR[1:0]	Periodic (RTI) Interrupt Rates			
0 0 0 1 1 0 1 1	8.192 ms 16.384 ms 32.768 ms 65.536 ms	4.096 ms 8.192 ms 16.384 ms 32.768 ms	2.731 ms 5.461 ms 10.923 ms 21.845 ms	($E/2^{13}$) ($E/2^{14}$) ($E/2^{15}$) ($E/2^{16}$)



Main Timer

NOTE: Port A pin actions are controlled by Port A, OC1M, OC1D, PACTL, TCTL1, and TCTL2 registers.

CFORC — Timer Compare Force **$100B**

	Bit 7	6	5	4	3	2	1	Bit 0
	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0
RESET:	0	0	0	0	0	0	0	0

FOC5–FOC1 — Write Ones to Force Compare(s)
0 = Not affected
1 = Output compare x action occurs

Bits 2–0 — Not implemented; always read zero

OC1M — Output Compare 1 Mask **$100C**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0
RESET:	0	0	0	0	0	0	0	0

Set bit(s) to enable OC1D to control corresponding pin(s) of port A.

Bits 2–0 — Not implemented; always read zero

OC1D — Output Compare 1 Data **$100D**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0
RESET:	0	0	0	0	0	0	0	0

If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1D compares.

Bits 2–0 — Not implemented; always read zero

TCNT — Timer Counter **$100E, $100F**

$100E	Bit 15	14	13	12	11	10	9	Bit 8	High	**TCNT**
$100F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TCNT resets to $0000. In normal modes, TCNT is read-only.

TIC1–TIC3 — Timer Input Capture **$1010–$1015**

$1010	Bit 15	14	13	12	11	10	9	Bit 8	High	TIC1
$1011	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1012	Bit 15	14	13	12	11	10	9	Bit 8	High	TIC2
$1013	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1014	Bit 15	14	13	12	11	10	9	Bit 8	High	TIC3
$1015	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TICx not affected by reset.

TOC1–TOC4 — Timer Output Compare **$1016–$101D**

$1016	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC1
$1017	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1018	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC2
$1019	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$101A	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC3
$101B	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$101C	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC4
$101D	Bit 7	6	5	4	3	2	1	Bit 0	Low	

All TOCx register pairs reset to ones ($FFFF).

TI4O5 — Timer Input Capture 4/Output Compare 5 **$101E, $101F**

$101E	Bit 15	14	13	12	11	10	9	Bit 8	High	TI4O5
$101F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TI4O5 register pair resets to ones ($FFFF).

TCTL1 — Timer Control 1 **$1020**

	Bit 7	6	5	4	3	2	1	Bit 0
	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET:	0	0	0	0	0	0	0	0

OM2–OM5 — Output Mode
OL2–OL5 — Output Level

OMx	OLx	Action Taken on Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to 0
1	1	Set OCx output line to 1

TCTL2 — Timer Control 2 **$1021**

	Bit 7	6	5	4	3	2	1	Bit 0
	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
RESET:	0	0	0	0	0	0	0	0

Timer Control Configuration

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge

TMSK1 — Timer Interrupt Mask 1 **$1022**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1I	OC2I	OC3I	OC4I	I4O5I	IC1I	IC2I	IC3I
RESET:	0	0	0	0	0	0	0	0

OC1I–OC4I — Output Compare x Interrupt Enable

I4O5I — Input Capture 4 or Output Compare 5 Interrupt Enable

IC1I–IC3I — Input Capture x Interrupt Enable

NOTE

Bits in TMSK1 correspond bit for bit with flag bits in TFLG1. Ones in TMSK1 enable the corresponding interrupt sources.

TFLG1 — Timer Interrupt Flag 1 **$1023**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1F	OC2F	OC3F	OC4F	I4O5F	IC1F	IC2F	IC3F
RESET:	0	0	0	0	0	0	0	0

Cleared by writing a one to the corresponding bit position(s).

OC1F–OC4F — Output Compare x Flag
Set each time the counter matches output compare x value.

I4O5F — Input Capture 4/Output Compare 5 Flag
Set by IC4 or OC5, depending on which function was enabled by I4/O5 of PACTL.

IC1F–IC3F — Input Capture x Flag
Set each time a selected active edge is detected on the ICx input line.

TMSK2 — Timer Interrupt Mask 2 **$1024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

TOI — Timer Overflow Interrupt Enable

RTII — Real-Time Interrupt Enable

PAOVI — Pulse Accumulator Overflow Interrupt Enable

PAII — Pulse Accumulator Input Interrupt Enable

Bits 3–2 — Not implemented; always read zero

PR1 and PR0 — Timer Prescaler Select
In normal modes, PR1 and PR0 can only be written once. The write must be within 64 cycles after reset. Refer to Timer Summary for specific timing values.

PR[1:0]	Prescaler (Divide E Clock by)
0 0	1
0 1	4
1 0	8
1 1	16

TFLG2 — Timer Interrupt Flag 2 **$1025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Cleared by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Flag
Set when TCNT changes from $FFFF to $0000

RTIF — Real-Time (Periodic) Interrupt Flag
Set periodically (see RTR[1:0] bits in PACTL register).

PAOVF — Pulse Accumulator Overflow Flag
Set when PACNT changes from $FF to $00.

PAIF — Pulse Accumulator Input Edge Flag
Set each time a selected active edge is detected on the PAI input line.

Bits 3–0 — Not implemented; always read zero

PACTL — Pulse Accumulator Control **$1026**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

DDRA7 — Data Direction for Port A Bit 7
Refer to **Parallel I/O**.

PAEN — Pulse Accumulator System Enable
Refer to **Pulse Accumulator**.

PAMOD — Pulse Accumulator Mode
Refer to **Pulse Accumulator**.

PEDGE — Pulse Accumulator Edge Control
Refer to **Pulse Accumulator**.

DDRA3 — Data Direction for Port A Bit 3
Refer to **Parallel I/O**.

I4/O5 — Input Capture 4/Output Compare 5
0 = Output compare 5 selected
1 = Input capture 4 selected

RTR1–RTR0 — RTI Interrupt Rate Selects

These two bits select one of four rates for the real-time periodic interrupt circuit. Refer to the following table for additional detail.

Real-Time Interrupt Rates

RTR[1:0]	Divide E By	XTAL = 4.0 MHz	XTAL = 8.0 MHz	XTAL = 12.0 MHz
0 0	2^{13}	8.19 ms	4.096 ms	2.731 ms
0 1	2^{14}	16.38 ms	8.192 ms	5.461 ms
1 0	2^{15}	32.77 ms	16.384 ms	10.923 ms
1 1	2^{16}	65.54 ms	32.768 ms	21.845 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

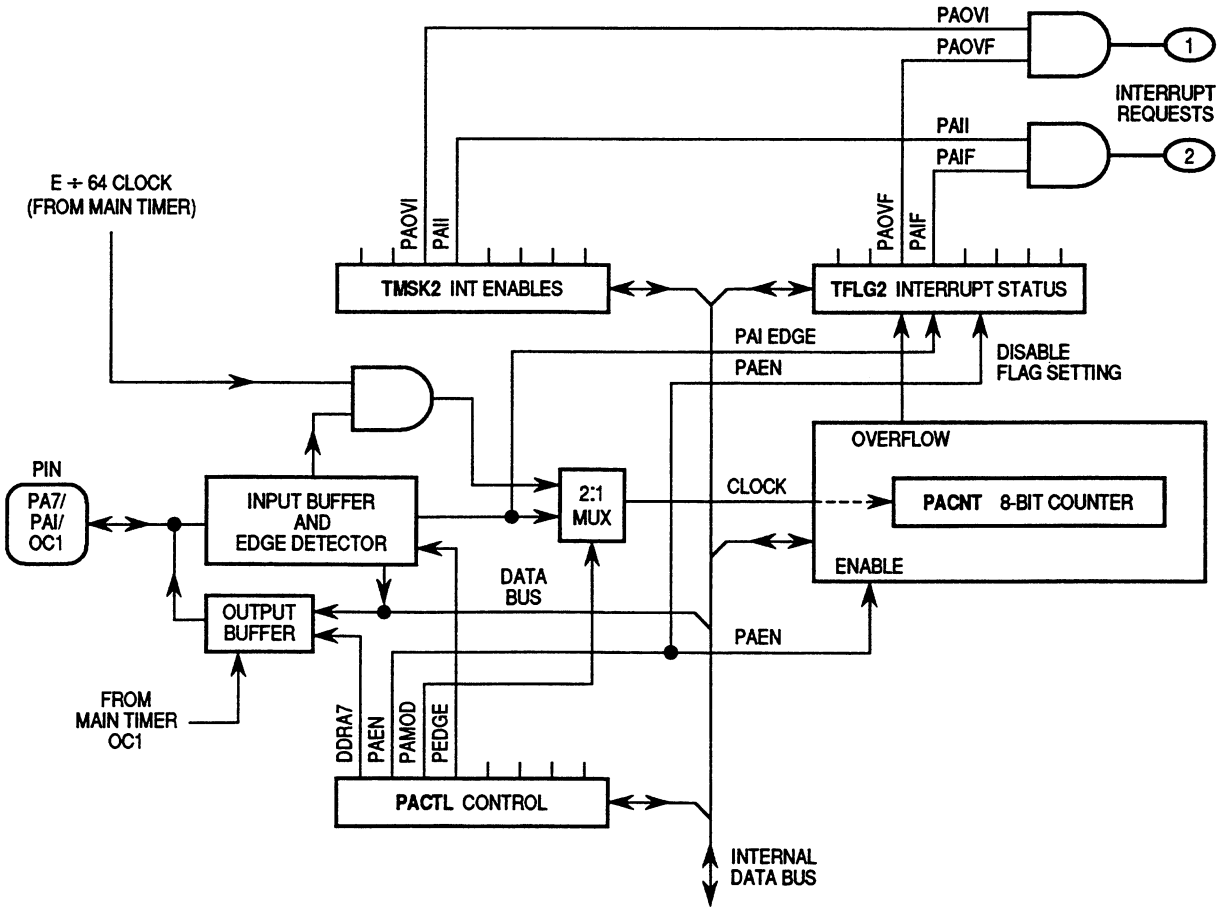
Pulse Accumulator

The pulse accumulator system, based on an 8-bit counter, can be configured to operate as a simple event counter or as a gated time accumulator. Unlike the main timer, the 8-bit pulse accumulator counter can be read or written at any time.

The port A bit 7 I/O pin (PA7/PAI/OC1) associated with the pulse accumulator can be configured to act as a clock (event counting mode) or as a gate signal, to enable a free-running E divided by 64 clock to the 8-bit counter (gated time accumulation mode).

Pulse Accumulator Timing

	Selected Crystal	Common XTAL Frequencies		
		4.0 MHz	8.0 MHz	12.0 MHz
CPU Clock	(E)	1.0 MHz	2.0 MHz	3.0 MHz
Cycle Time	(1/E)	1000 ns	500 ns	333 ns
Pulse Accumulator (in Gated Mode)				
$(E/2^6)$ $(E/2^{14})$	1 count — overflow —	64.0 µs 16.384 ms	32.0 µs 8.192 ms	21.33 µs 5.461 ms



Pulse Accumulator System Block Diagram

TMSK2 — Timer Interrupt Mask 2 **$1024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

TOI — Timer Overflow Interrupt Enable
Refer to **Main Timer**.

RTII — Real-Time Interrupt Enable
Refer to **Main Timer**.

PAOVI — Pulse Accumulator Overflow Interrupt Enable
0 = Pulse accumulator overflow interrupt disabled
1 = Interrupt requested when bit PAOVF of TFLG2 is set

PAII — Pulse Accumulator Interrupt Enable
0 = Pulse accumulator interrupt disabled
1 = Interrupt requested when bit PAIF of TFLG2 is set

Bits 3–2 — Not implemented; always read zero

PR1, PR0 — Timer Prescaler Select
Refer to **Main Timer**.

TFLG2 — Timer Interrupt Flag 2 **$1025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Cleared by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Flag
Refer to **Main Timer**.

RTIF — Real-Time Interrupt Flag
Refer to **Main Timer**.

PAOVF — Pulse Accumulator Overflow Flag
Set when PACNT changes from $FF to $00.

PAIF — Pulse Accumulator Input Edge Flag
Set each time a selected active edge is detected on the PAI input line.

Bits 3–0 — Not implemented; always read zero

PACTL — Pulse Accumulator Control **$1026**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

DDRA7 — Data Direction for Port A Bit 7
Refer to **Parallel I/O**.

I4/O5 — Input Capture 4/ Output Compare 5
Refer to **Parallel I/O**.

PAEN — Pulse Accumulator System Enable
0 = Pulse Accumulator disabled
1 = Pulse Accumulator enabled

PAMOD — Pulse Accumulator Mode
0 = Event counter
1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control
0 = Falling edges increment counter: high level enables accumulation
1 = Rising edges increment counter: low level enables accumulation

PAMOD	PEDGE	Action on Clock
0	0	PAI Falling Edge Increments the Counter
0	1	PAI Rising Edge Increments the Counter
1	0	A Zero on PAI Inhibits Counting
1	1	A One on PAI Inhibits Counting

RTR1, RTR0 — Real-Time Rate Selects
Refer to **Main Timer**.

PACNT — Pulse Accumulator Counter **$1027**

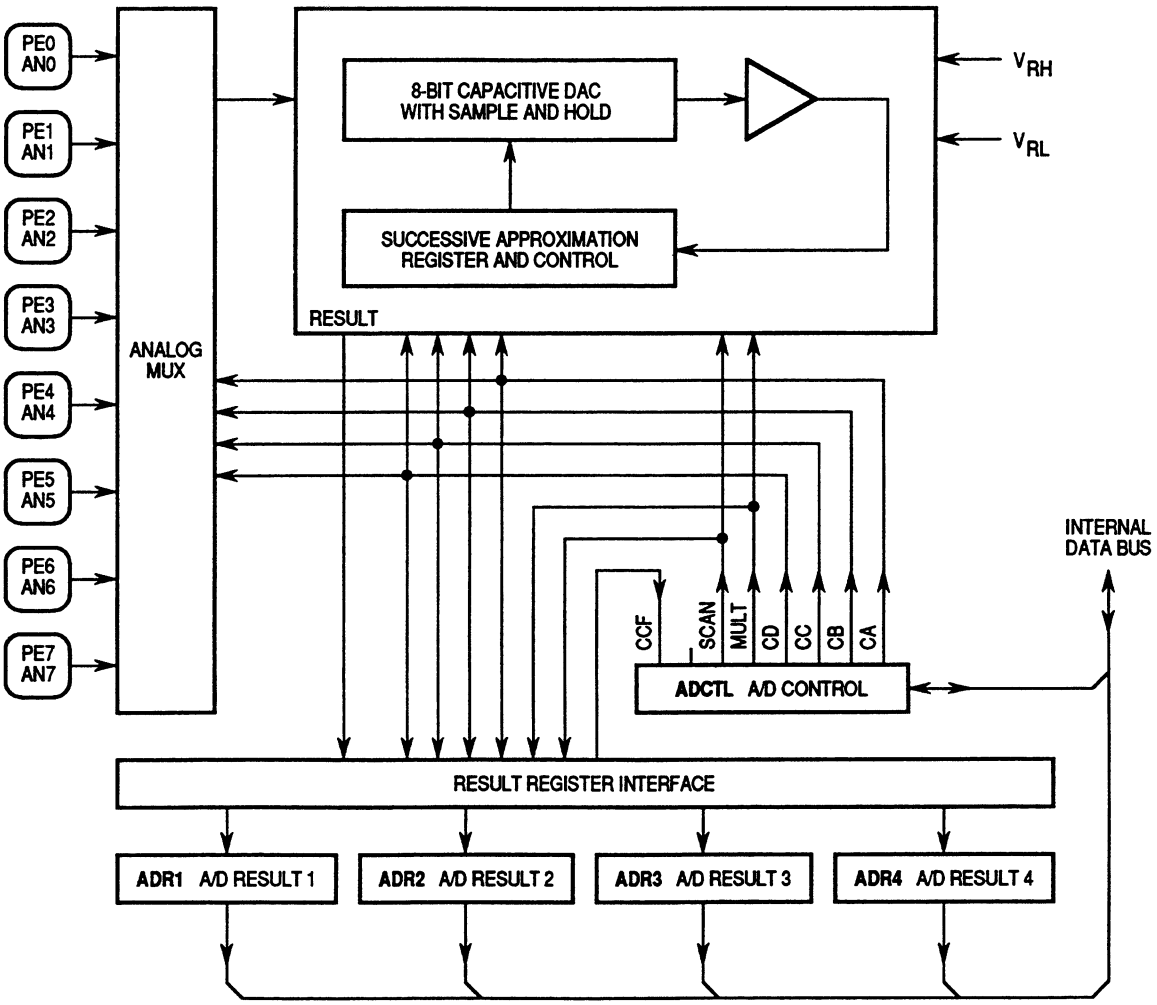
Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

Readable and writable.

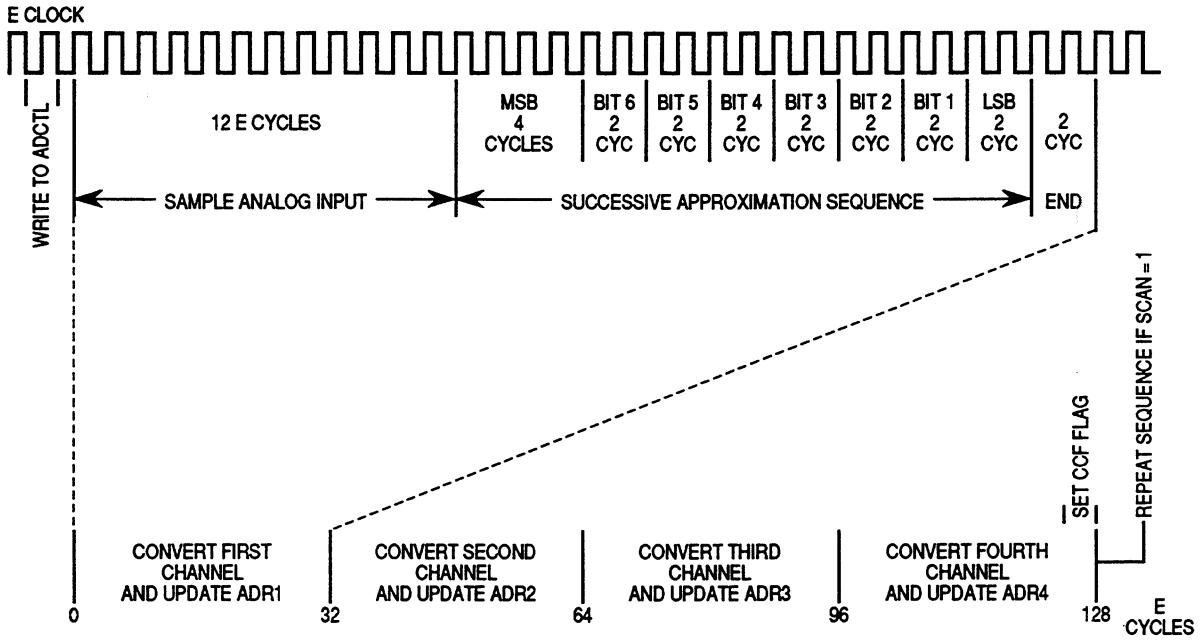
Analog-to-Digital Converter

The A/D converter uses an all-capacitive charge-redistribution technique to convert analog signals to digital values. The MC68HC11L6 A/D system is an 8-channel, 8-bit, multiplexed input, successive approximation converter, accurate to ±1 least significant bit (LSB). It does not require external sample and hold circuits because of the type of charge redistribution technique used.

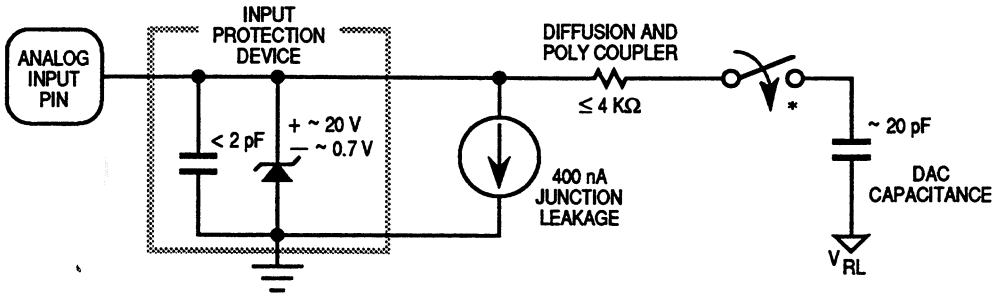
Dedicated lines V_{RH} and V_{RL} provide the reference supply voltage inputs. A multiplexer allows the single A/D converter to select one of 16 analog signals.



A/D Converter Block Diagram



A/D Conversion Sequence



*This analog switch is closed only during the 12-cycle sample time.

Electrical Model of an Analog Input Pin (Sample Mode)

ADCTL — A/D Control/Status **$1030**

	Bit 7	6	5	4	3	2	1	Bit 0
$1030	CCF	0	SCAN	MULT	CD	CC	CB	CA
RESET:	0	0	U	U	U	U	U	U

CCF — Conversions Complete Flag

Set after the fourth conversion in an A/D conversion cycle, cleared when ADCTL is written.

Bit 6 — Not implemented; always reads zero

SCAN — Continuous Scan Control
0 = Do four conversions and stop
1 = Convert four channels in selected group continuously

MULT — Multiple Channel/Single Channel Control
0 = Convert single channel selected
1 = Convert four channels in selected group

CD–CA — Channel Select D through A

A/D Converter Channel Assignments

Channel Select Control Bits				Channel	Result in ADRx if
CD	CC	CB	CA	Signal	MULT = 1
0	0	0	0	AN0	ADR1
0	0	0	1	AN1	ADR2
0	0	1	0	AN2	ADR3
0	0	1	1	AN3	ADR4
0	1	0	0	AN4	ADR1
0	1	0	1	AN5	ADR2
0	1	1	0	AN6	ADR3
0	1	1	1	AN7	ADR4
1	0	X	X	Reserved	—
1	1	0	0	V_{RH}*	ADR1
1	1	0	1	V_{RL}*	ADR2
1	1	1	0	$(V_{RH})/2$*	ADR3
1	1	1	1	Reserved*	ADR4

*Used for factory testing

ADR1–ADR4 — A/D Results **$1031–$1034**

$1031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$1032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$1033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$1034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4

Analog Input to 8-Bit Result Translation Table

	Bit 7	6	5	4	3	2	1	Bit 0
% (1)	50%	25%	12.5%	6.25%	3.12%	1.56%	0.78%	0.39%
Volts (2)	2.500	1.250	0.625	0.3125	0.1562	0.0781	0.0391	0.0195

(1) % of V_{RH}–V_{RL} (2) Volts for V_{RL} = 0; V_{RH} = 5.0 V

OPTION — System Configuration Options **$1039**

	Bit 7	6	5	4	3	2	1	Bit 0
	ADPU	CSEL	IRQE*	DLY*	CME	0	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes.

ADPU — A/D Power Up
0 = A/D converter powered down
1 = A/D converter powered up

CSEL — Clock Select
0 = A/D and EEPROM use system E clock
1 = A/D and EEPROM use internal RC clock

IRQE — $\overline{\text{IRQ}}$ Select Edge-Sensitive Only
Refer to **Resets and Interrupts**.

DLY — Enable Oscillator Startup Delay on Exit from Stop
Refer to **Resets and Interrupts**.

CME — Clock Monitor Enable
Refer to **Resets and Interrupts**.

Bit 2 — Not implemented; always reads zero

CR1, CR0 — COP Timer Rate Select
Refer to **Resets and Interrupts**.

NOTES

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