



Addendum

*HC908GP20AD/D
Rev. 1, 11/2001*

*Addendum to
MC68HC908GP20
Advance Information*

This addendum provides corrections to:

MC68HC908GP20 Advance Information (Freescale document number MC68HC908GP20/D Rev. 2.0)

Page 338 Correct the SPRIE description under **20.14.1 SPI Control Register**

From: SPRIE — SPI Receiver Interrupt Enable Bit

This read/write bit enables CPU interrupt requests generated by the SPRF bit. The SPRF bit is set when a byte transfers from the shift register to the receive data register. Reset clears the SPRIE bit.

1 = SPRF CPU interrupt requests

0 = SPRF CPU interrupt requests

To: SPRIE — SPI Receiver Interrupt Enable Bit

This read/write bit enables CPU interrupt requests generated by the SPRF bit. The SPRF bit is set when a byte transfers from the shift register to the receive data register. Reset clears the SPRIE bit.

1 = SPRF CPU interrupt requests enabled

0 = SPRF CPU interrupt requests disabled



Page 363 Correct the TIM TOF description under **22.6 Interrupts**

- From:*
- TIM overflow flag (TOF) — The TOF bit is set when the TIM counter value rolls over to \$0000 after matching the value in the TIM counter modulo registers. The TIM overflow interrupt enable bit, TOIE, enables TIM overflow CPU interrupt requests. TOF and TOIE are in the TIM status and control register.
- To:*
- TIM timer overflow flag (TOF) — The timer counter value changes on the falling edge of the internal bus clock. The timer overflow flag (TOF) bit is set on the falling edge of the internal bus clock following the timer rollover to \$0000. The TIM overflow interrupt enable bit, TOIE, enables TIM overflow interrupt requests. TOF and TOIE are in the TIM status and control registers.

Page 372 Correct the CHxMAX description under **22.10.5 TIM Channel Status and Control Registers**

From: CHxMAX — Channel x Maximum Duty Cycle Bit

When the TOVx bit is at logic 0, setting the CHxMAX bit forces the duty cycle of buffered and unbuffered PWM signals to 100%. As **Figure 22-13** shows, the CHxMAX bit takes effect in the cycle after it is set or cleared. The output stays at the 100% duty cycle level until the cycle after CHxMAX is cleared.

To: CHxMAX — Channel x Maximum Duty Cycle Bit

When TOVx bit is at logic 1 and clear output on compare is selected, setting the CHxMAX bit forces the duty cycle of buffered and unbuffered PWM signals to 100 percent. As **Figure 22-13** shows, the CHxMAX bit takes effect in the cycle after it is set or cleared. The output stays at 100 percent duty cycle level until the cycle after CHxMAX is cleared.

NOTE: *The PWM 0 percent duty cycle is defined as output low all of the time. To generate the 0 percent duty cycle, select clear output on compare and then clear the TOVx bit (CHxMAX = 0). The PWM 100 percent duty cycle is defined as output high all of the time. To generate the 100 percent duty cycle, use the CHxMAX bit in the TSCx register.*



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