MC68SC302

Product Brief

Passive ISDN Protocol Engine

The MC68SC302 Passive ISDN Protocol Engine (PIPE) is a communication controller optimized for ISDN passive cards, with an ISA PNP interface and a PCMCIA slave interface. The MC68SC302 is a descendant of the popular MC68302 Integrated Multiprotocol Processor. The microcoded RISC communications processor from the 68302 was modified to form the core of the 68SC302. The 68000 core and many related system integration features were removed to further optimize the device for passive ISDN card applications. The serial communication channels (SCC) have been optimized for supporting a full ISDN basic rate interface. The three SCCs support two 64kbit per second B-channels and one 16kbit per second D-channel. The 68SC302 connects gluelessly to Motorola's MC145572 U transceiver or MC145574 S/T transceiver and, as an added bonus, eliminates the need for a second oscillator for the transceiver chip.

MC68SC302 KEY FEATURES

- ISA Bus Interface
  - ISA Plug and Play Interface
  - Glueless Connections to ISA
  - 24mA Buffers for ISA Bus Pins
  - Full Support of Plug and Play Standard
  - All Chip Registers Accessed from ISA Bus.
  - Support for 8- or 16-bit I/O or Memory ISA Cycles
  - 11 Selectable Interrupt Output Pins to ISA Bus.
  - Additional Chip Select Allows Another Device to Be Accessed from the ISA Bus.
  - Plug and Play Register Settings Stored in External Low Cost E^2PROM.
- PCMCIA Interface
  - PC Card 95 Compatible
  - Two CIS Storage Options:
    - CIS stored in Serial E^2PROM and Downloaded At Runtime to Internal Dual Port RAM
    - CIS Optionally Stored in Parallel E^2PROM on the PC Card Bus with Dedicated Chip Select, Saving Dual Port RAM Buffer Space and Always Available for PC Accesses.

- Memory Mode Accesses Supported (I/O Not Supported)
- Supports 8- or 16-bit Memory Cycles
- Supports Ring Detect through Status Change Pin
- Additional Chip Select Allows Another Device to be Address Mapped on the PC Card Bus.

- ISDN Communications Processor
  - Requires No External (Local) RAM
  - Flexible Channel Handling
  - RISC Processor Decreases CPU Load with Flexible Buffer Descriptor Structure and HDLC Capability (UART Mode Not Supported).
  - Totally Independent Programming for Rx/Tx for each of the B and D Channels
  - Supports Any Sub-Channeling for Each of the B Channels
  - Enables a Concatenation of 2 B Channels (or Any Selected Bits) to a Super-Channel
  - HDLC with Retry Capability for the D Channel
  - Allows Dynamic Connection/Disconnection for each of the B Channels
  - Total 1536KB Dual Port RAM Divided into Parameter and Data Buffer RAM
  - 256 Byte Parameter RAM (As in PM302)
  - 1280 Byte Data RAM with Efficient FIFO Organization and Flexible Buffer Size
  - Independent Programmable Channel FIFO Length, if Split Equally:
    - 4 x 256 Bytes FIFO for B1 and B2 Channel (Rx/Tx)
    - 2 x 64 Bytes FIFO for D Channel (Rx/Tx)
  - Glueless Interface to Freescale and Other Popular ISDN S/T and U Interface Chips
  - Supports Freescale Interchip Digital Link (IDL)
  - Supports General Circuit Interface (GCI), Also Known as IOM-2[1]
  - Includes Serial Communication Port (SCP) for Synchronous Communication
  - Includes one SMC That Can Support Both the C/I and Monitor Channel of GCI
  - Two Strobes Support Time-Slot Assignment of Non-Intelligent Peripherals
  - Only One Crystal Required for TA Application.
  - Clock Output (CLKO) Generation from a Crystal. CLKO Can Be Connected to S/T XTAL Input.
  - Clock Input for U-Chip (MC145572) can be Used to Drive SC302

1. IOM-2 is a trademark of Siemens AG

- Other System Integration Features
  - Gluelessly Connects to Serial E^2PROM via SCP Port for PNP ISA ID and CIS Storage.
  - 25XXX Series or 93XX Series E^2PROMs Supported.
  - Flexible Pin Configuration Allows Trade-Offs between 16-Bit Wide ISA/PC Card Interface and Extra I/O Pins.
    - Up to 16 Parallel I/O Pins for Controlling Other Functions.
  - On-Chip Interrupt Controller
    - 8 Internal Interrupt Sources
    - 7 External Pin Sources for External Devices.
  - 2 Low-Power Modes
    - Wait - Oscillator Keeps Running ~5 mA
    - Stop - Oscillator Stops - <100uA
  - Operating Speed: 0-20.48 Mhz
  - Operating Voltage: 5V
  - 100 pin TQFP (14mm x 14mm)

MC68SC302 OVERVIEW

The block diagram for the MC68SC302 is shown in Figure 1. The MC68SC302 architecture is based on a microcoded RISC communications processor that services the three main high speed serial channels (SCC), two serial management channels (SMC) and a serial communications port (SCP). The three SCC channels support simultaneous operation of the three channels specified by the ISDN basic rate interface (2B+D). Each SCC can support onboard HDLC processing as well as totally transparent operation. The dual-port RAM provides 1536 bytes of memory. A maximum of 1280 bytes can be allocated for serial channel buffer space, which, when allocated evenly for a basic rate interface, allows 256 bytes per B channel per direction and 64 bytes per direction for the D channel. This provides 32msec worth of basic rate data to be stored in the buffers, allowing ample interrupt latency time for host platform operating systems. The IDL or GCI interface provides direct connection to the Freescale MC145572 U interface transceiver, the MC145574 S/T interface transceiver, and other popular ISDN transceivers. A non-multiplexed serial interface (NMSI) is also provided for SCC2.

The MC68SC302 has an ISA Plug and Play interface which supports the ISA Plug and Play specification version 1.0a. The ISA bus interface can be configured for either I/O mode accesses or memory mode accesses. The ISA interface can be either an 8- or 16-bit wide data bus allowing pin usage trade-offs to be made. I/O mode accesses are based on a self-incrementing pointer, allowing the PC to write or read data from a fixed ISA I/O address. Memory mode access allows the PC to write or read data into a predefined ISA window. In addition to supporting access to the internal MC68SC302 register and memory map, an additional chip-select is provided for an external device, and can be programmed for either memory or I/O and either 8 or 16 bit bus independent of internal space.

The MC68SC302 can also be configured to provide a PC Card interface based on the PC Card 95 specification. Either 8- or 16-bit wide memory cards can be implemented. There are two options available for supporting the Card Information Structure (CIS): 1)The CIS can be stored in external serial EEPROM which is downloaded on reset into the Dual Port RAM (DPRAM) space. 2) To save DPRAM space, the CIS can be

stored in a parallel EEPROM on the external PCMCIA bus. An additional chip select is provided to support access to an external device from the PC Card interface.

The MC68SC302 also has up to 12 general purpose I/O pins to connect to external circuits. Five external chip interrupts can be brought in and routed through a built-in interrupt controller to any one of 11 ISA interrupts (or to the PC Card interface interrupt). The MC68SC302 can be clocked at the same rate as the physical layer transceiver clock which eliminates the need for a dedicated oscillator or crystal.

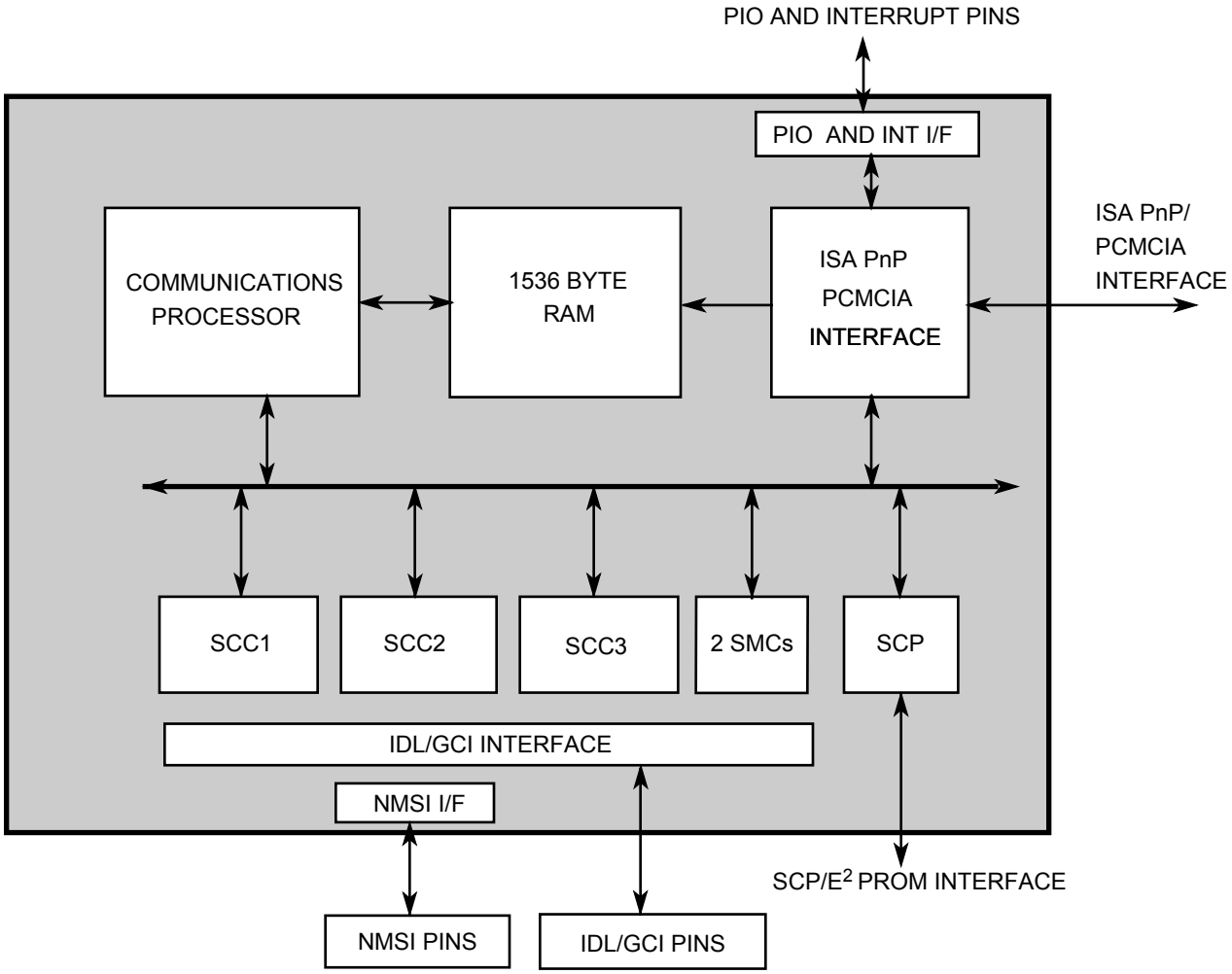

Figure 1. MC68SC302 Block Diagram

REFERENCE DESIGNS

Figure 2 shows the 68SC302 in an NT1 terminal adaptor (TA) application using the MC68SC302. The TA supports a basic rate interface (BRI). The 68SC302 is connected gluelessly to the ISA bus connector and performs the Plug and Play interface using the serial EEPROM for storage of non-volatile Plug and Play data. Data and control accesses from the PC to the MC68SC302 can be selectively memory or I/O mapped. Only one clock source (crystal or oscillator) is needed for a simple terminal adaptor.

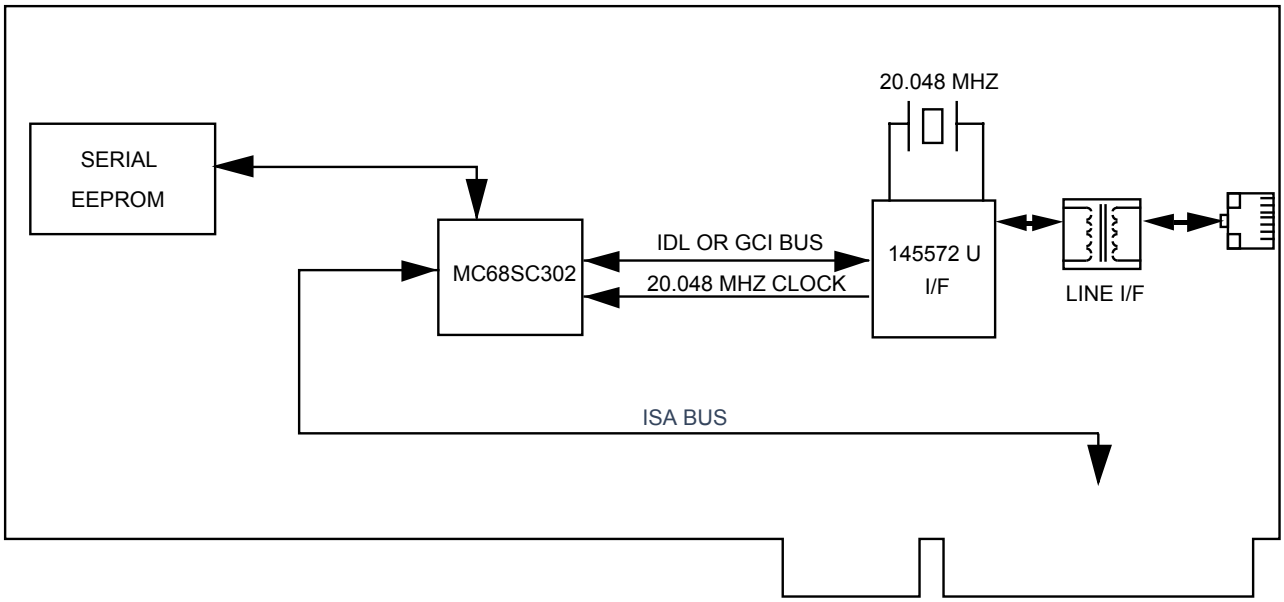

Figure 2. Passive NT Terminal Adaptor Block Diagram

Figure 3 shows a basic rate terminal adaptor with the 4-wire S/T interface. This architecture is almost identical to the U interface TA with the exception that the TA clock source is provided to the S/T transceiver from the MC68SC302.

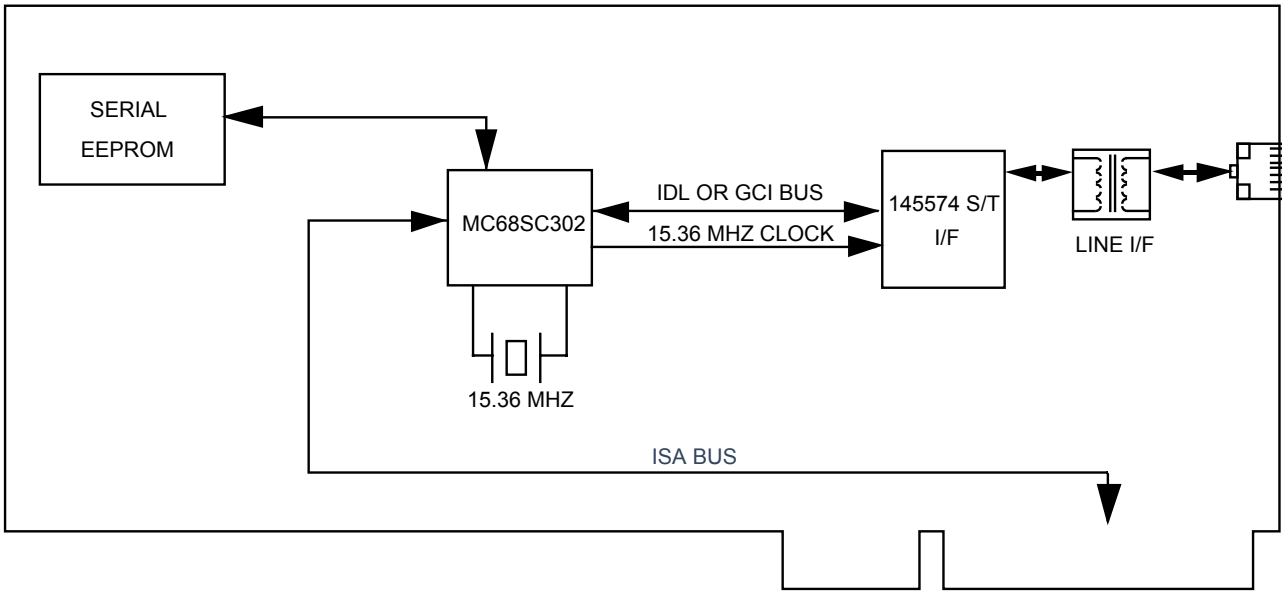

Figure 3. Passive TE Terminal Adaptor Block Diagram with S/T Interface

Figure 4 shows a more full featured terminal adaptor. The two added features are the “Plain Old Telephone” (POTs) interface and a optional modem datapump. Up to two POTs interfaces can be added on the board to support simultaneous B channel voice call. The ISA interface provides a separate chip select for an external data pump which uses an MC145480 to produce an 8khz PCM output that can be directly connected to the IDL or GCI bus.

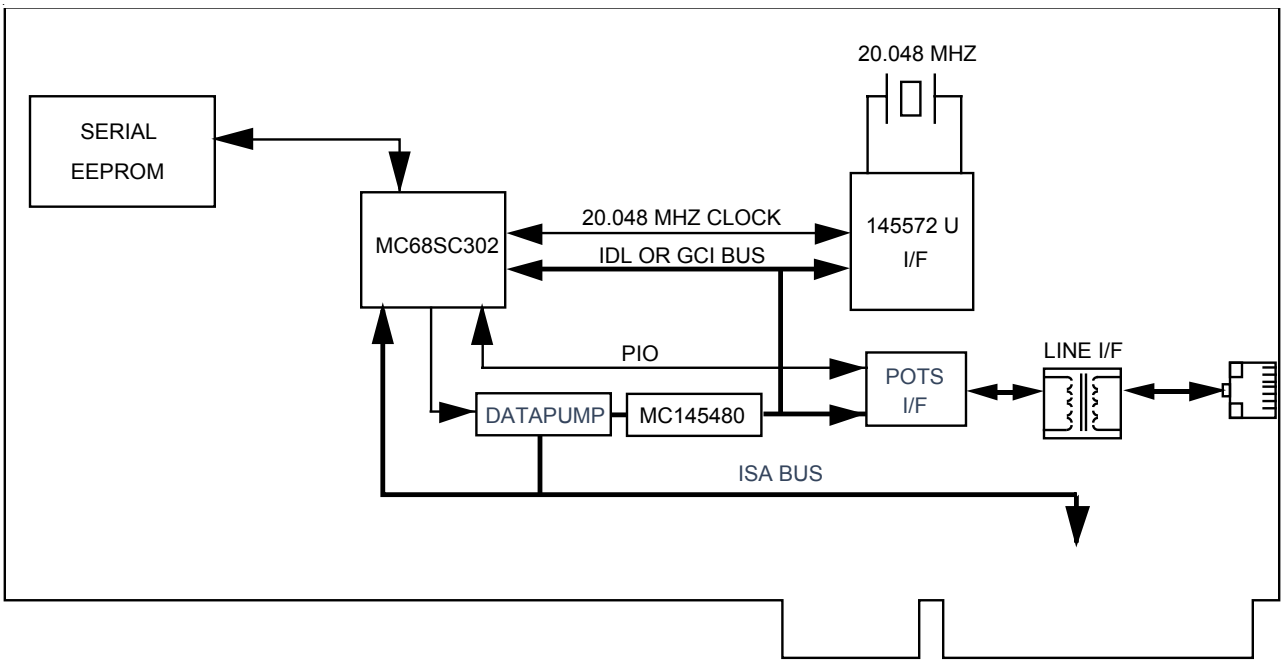

Figure 4. NT Terminal Adaptor Block Diagram with POTS Interface and Datapump

Figure 5 shows a PC Card terminal adaptor based on the SC302.

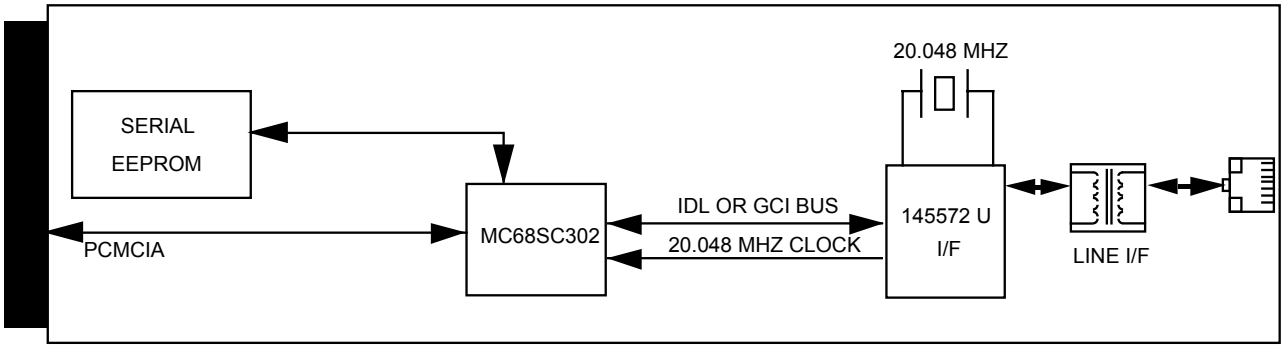

Figure 5. PC Card Terminal Adaptor

ORDERING INFORMATION

PACKAGE TYPE	FREQUENCY (MHZ)	TEMPERATURE	ORDER NUMBER
Surface Mount TQFP 100-Pin (PU Suffix)	20.048	0°C to 70°C	MC68SC302PU20

RELATED DOCUMENTATION

DOCUMENT TITLE	ORDER NUMBER	CONTENT
MC68SC302 User's Manual	MC68SC302UM/AD	Detailed technical information about the MC68SC302

MC68SC302 APPLICATION DEVELOPMENT SYSTEM

The MC68SC302 Application Development System (ADS) is a platform for developing a passive terminal adaptor using the MC68SC302. In addition to being an ISA half-card form factor plug-in card, the MC68SC302 can also be plugged into a PC card slot for development of PC card applications. The board includes both an MC145572 U interface transceiver and an MC145574 S/T interface transceiver along with the associated line interface circuitry. A 128-pin expansion connector is onboard for customer specific circuits such as a POTs interface or a modem datapump. Logic analyzer connectors provide convenient access to ISA and PCMCIA bus signals. Figure 6 shows the ADS block diagram.

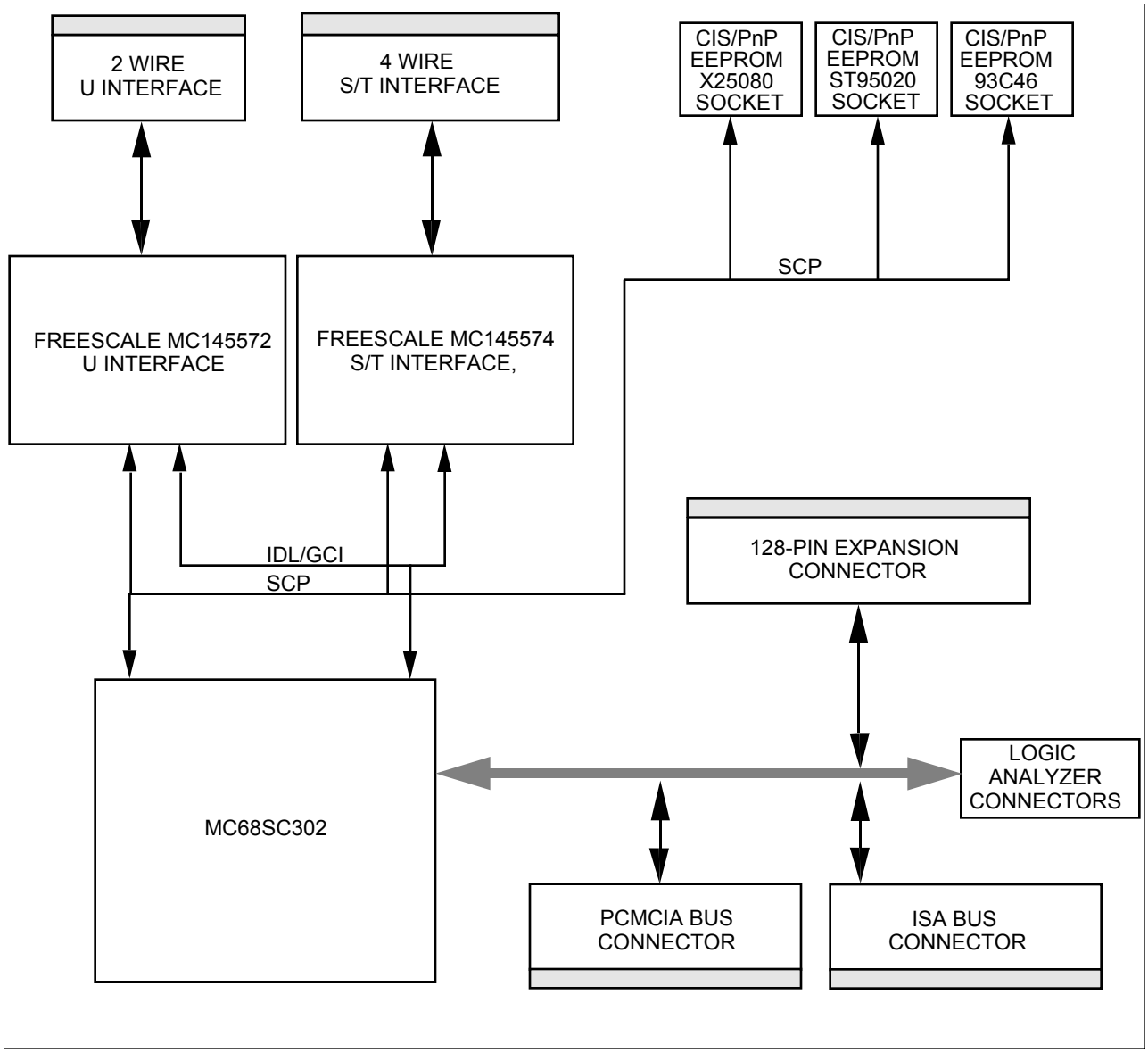

Figure 6. ADS Block Diagram

ADS FEATURES

- MC68SC302 operating at 20.48Mhz.
- ISA half-card form factor modified with PCMCIA extender card.
- Host PC connection via either ISA Bus or PCMCIA bus.
- ISA Plug and Play Interface.
- Powered by the ISA or PCMCIA connectors with option to power from bench supply.
- The U interface transceiver MC145572 configurable to either NT or LT mode.
- The S/T interface transceiver MC145574 configurable to either TE or NT mode.
- Options to communicate with U and S/T transceivers via either the IDL/SCP bus or the GCI bus.
- Logic analyzer connectors to probe MC68SC302 and ISA/PCMCIA bus activity.
- 128-pin expansion connector providing access to the SC302 pins for customer daughter cards. This includes access to the ISA/PCMCIA bus pins.
- Options for three types of serial EEPROM for the PCMCIA or ISA Configuration.

ADS ORDERING INFORMATION

DEVELOPMENT PLATFORM	ORDER NUMBER
ADS Board for M68SC302	M68SC302ADS

RoHS-compliant and/or Pb- free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb- free counterparts. For further information, see http://www.freescale.com or contact your Freescale sales representative.

For information on Freescale.s Environmental Products program, go to http://www.freescale.com/epp.

freescale™ semiconductor

SEMICONDUCTOR PRODUCT INFORMATION

For More Information On This Product,
Go to: www.freescale.com