Data Sheet

MGT5100TS/D
Rev. 0, 04/2002

MGT5100 Microprocessor Technical Summary

The MGT5100 embeds an enhanced version of the 32-bit MPC603e core that includes a rich set of integrated I/O, including Ethernet, CAN, USB, and PCI. Operating systems are enhanced by a SmartComm™ intelligent DMA unit that significantly off loads the processor core from routine I/O tasks. The raw processing power (440 MIPs) is further augmented by a double precision FPU. The MGT5100 is the baseline of the pin-compatible MGT5x00 family and builds upon the legacy of code-compatible devices from the MPC5xx, MPC82xx, and MPC8xxx product lines.This combination of features makes the MGT5100 well suited for telematics, network and internet-access devices, wireless access control, industrial automation control, and electronic and medical instrumentation.

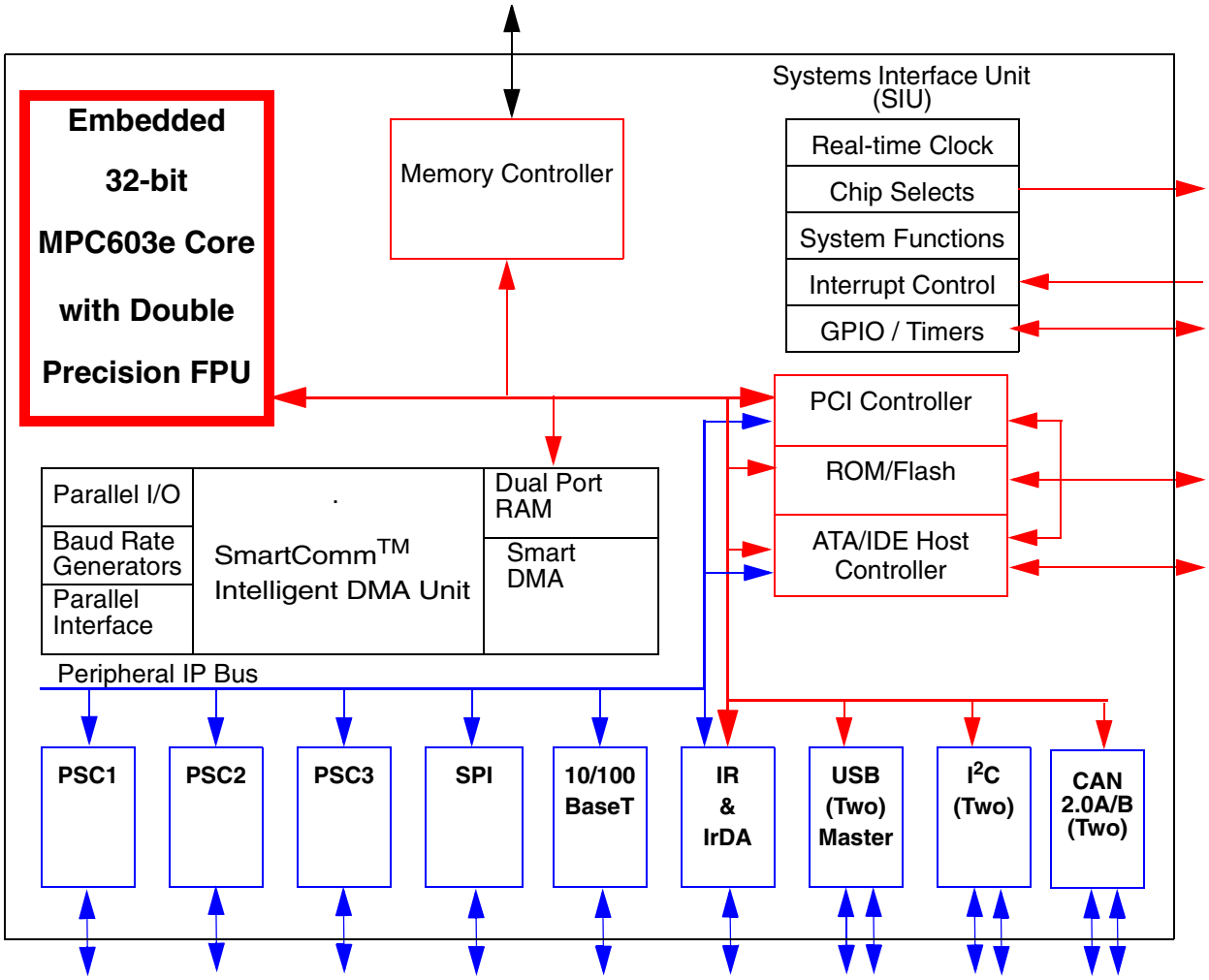


Figure 1 MGT5100 Block Diagram

The MGT5100 supports an external dual-bus architecture with a separate high speed SDRAM/DDR controller used primarily by the G2 core. A Peripheral Component Interconnect (PCI) compatible interface may be used as a generalized interface to system level peripherals in addition to the ATA/IDE interface which provides access to bus peripherals.

Key Features

603e series processor core that implements the PowerPC architecture

- Superscalar architecture
- 0 – 231MHz static operation (extended temperature range)
- 16K Instruction/16K Data Caches
- Double precision FPU
- Instruction and Data MMU
- Dynamic power management including Doze and Sleep modes
- True little endian and big endian support
- Standard & critical interrupt capability

High speed SDRAM memory interface

- 66MHz operation
- SDRAM & DDR SRAM support
- 128Mbyte addressing range
- 32-bit data bus
- Built-in initialization and refresh

Flexible multi-function external bus

- Supports PCI, ATA/IDE, and ROM/RAM/Flash interfaces
- Version 2.2 PCI master compatibility
  - 32-bit muxed address/data
  - 33MHz operation with SmartComm‘ enabled
- Version 4 ATA compatible external interface
  - IDE Disk Drive connectivity
- ROM/RAM/Flash interface
  - Boot ROM, external peripheral connectivity

SmartComm I/O subsystem

- SmartComm virtual DMA controller
- Dedicated DMA channels for reception and transmission for all peripheral interfaces
- Programmable Serial Controllers (PSCx)
  - UART or RS232 interface
  - CODEC interface for modem or AC97 audio
  - Bluetooth, cellular, GPS, digital radio interface

- 10/100 BaseT Ethernet
- USB Master 1.1 with OHCI support
  - Support for two independent USB ports
- Infrared (IR) data port
  - Two IR receive ports (Standard IR & IrDA)
  - IRBlaster
  - IrDA 1.0 SIR mode to 115.2kbps
  - IrDA 1.1 MIR and FIR modes to 4.0Mbps
- I2C Controller(s) to 520Kbps
  - Support for two independent I2C ports
- Serial Peripheral Interface (SPI) controller

Dual MSCAN 2.0 A/B Controller modules

- Motorola Scalable Controller Area Network (MSCAN) architecture
- V2.0 A/B CAN protocol
- Standard and extended data frames
- Programmable bit rate up to 1Mbps (High Speed or Low Speed)

System level features

- Six programmable chip selects
- Interrupt controller
  - Four external interrupt request lines supporting standard and/or critical interrupts
  - Support for all other internal interrupt sources
- GPIO / Timer functions
  - Two dedicated GPIO pins supporting WakeUp capability
  - Eight dedicated GPIO pins with timer capability supporting input capture, output compare, and Pulse Width Modulation (PWM) functions
  - Up to 56 total GPIO pins (depending on functional muxing selections)
- Systems Protection (watch dog timer, bus monitor)
- Real-time clock
- Power management features

Test / Debug features

- JTAG (IEEE 1149.1 test access port)
- Common On-Chip Processor (COP) debug port

On-board PLL and clock generation

Software Development Support

- Complete software development tool chain
- Optional accessory development kits
- Robust silicon evaluation kits
- Technical support
- Professional services

Physical Characteristics

- 1.8V internal, 3.3V external operation (2.5V for DDR interface)
- TTL compatible I/O pins
- Extended Temperature Range (-40×C to +85×C)
- 272-pin plastic ball grid array (PBGA), 1.27mm ball pitch

Architecture Overview

The MGT5100 is optimized for price sensitive embedded applications in a single chip package and with extended temperature qualification. Building on Motorola's highly successful family of microcontrollers, the MGT5100 optimizes the processing power and peripheral mix for both mobile and fixed applications in markets for wireless access control, internet access, control systems, entertainment, digital radio, navigation/GPS, safety, and telematics.

The MGT5100 integrates an enhanced high-performance 603e series G2 core with dual precision floating point unit (FPU) with an I/O subsystem containing an intelligent DMA unit called SmartComm. SmartComm is capable of responding to peripheral interrupts independent of the G2 core and provides low-level peripheral management, protocol processing and peripheral data movement functions.

The MGT5100 has a high speed SDRAM controller that supports an external memory interface dedicated to the processor, allowing optimized instruction and data bursting. The dedicated memory interface coupled with on-chip 16Kbyte instruction and 16Kbyte data caches enables cache-sensitive software environments, such as Java, to run in real time while leaving plenty of processing power for peripheral management and system control tasks.

The MGT5100 also contains a full-function PCI compliant external bus. This bus allows connection to a wide variety of external peripheral devices including graphics controllers and slower memory. There is also an ATA/IDE interface for support of external drives. Additionally, there is a ROM/Flash interface for support of boot file and program storage.

The MGT5100 has an optimized peripheral mix to support today's more full-featured products. There are three programmable serial channels, one SPI, one 10/100 BaseT ethernet, one IrDA, and a programmable number of general-purpose I/O channels (GPIOs) supported directly by the SmartComm I/O subsystem. The low-level data movement and protocol processing tasks for these peripheral functions are handled independently of the G2 core by the SmartComm module. SmartComm has a dedicated DMA channel for each of these peripheral interfaces allowing incoming and outgoing data to be organized efficiently in external memory for use by the G2 core.

In addition, there are two USB, two I2C, one IR, and two MSCAN 2.0B channels available on the internal processor bus. Together, this array of diverse integrated I/O allow for very cost effective system solutions for highly networked products and applications.

A sophisticated external multiplexing scheme allows the highly integrated design to fit in a low-cost 272-pin Plastic Ball Grid Array (PBGA) package, dramatically lowering overall device footprint and system costs.

Embedded G2 Core

The MGT5100 core is derived from Motorola's 603e family of Reduced Instruction Set Computer (RISC) microprocessors. The core is a high performance, low-power implementation of this superscalar architecture. It contains 16Kbytes of instruction cache and 16Kbytes of data cache. Caches are four-way associative and use the Least Recently Used (LRU) replacement algorithm.

The core contains four independent execution units: Branch Processing Unit (BPU), Integer Unit (IU), Load and Store Unit (LSU) and System Register Unit (SRU). Up to three instructions can be issued and tiered per clock. Most instuctions execute in a single cycle. It contains an integrated, dual-precision Floating Point Unit (FPU) which is well suited to processing MP3 files or similar requirements. It has two Memory Management Units (MMU), one for each cache. The core implements the 32-bit portion of the superscalar architecture which provides 32-bit effective addresses and integer data types of 8, 16, and 32 bits.

Several enhancements to the standard 603e core include:

- True little endian support
- Improved interrupt latency (critical interrupts)
- New MMU with 8 BAT (16 total) registers and 1Kbyte page management
- Improved Background Debug Mode (BDM) interface

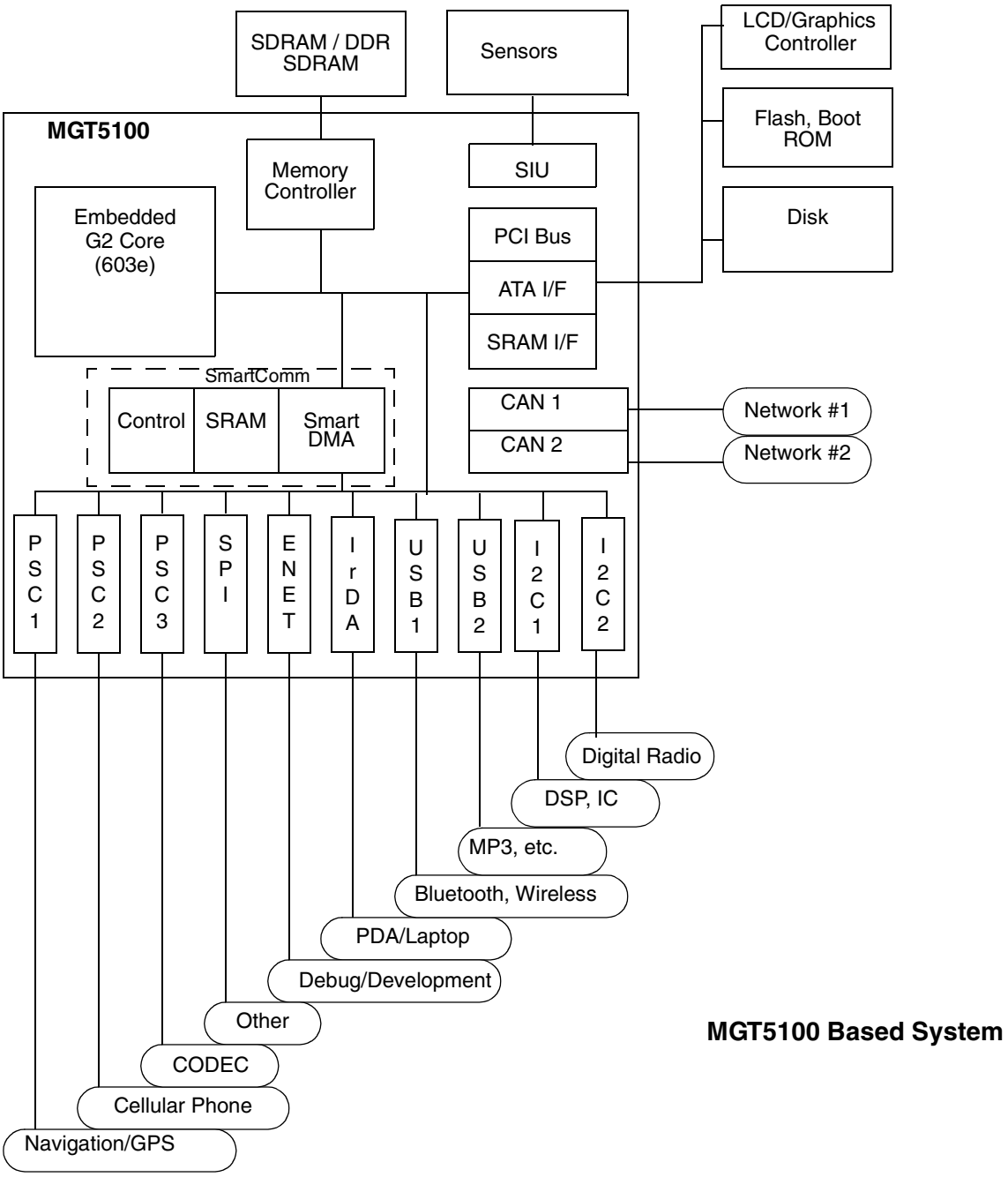
SmartComm DMA I/O Subsystem

SmartComm contains an intelligent DMA unit which provides a front-line interrupt control and data movement interface via a separate peripheral bus to the on-chip peripheral functions. This leaves the G2 core free to handle higher level activities. The concurrent operation provides a significant boost in overall system performance.

SmartComm can support up to 16 simultaneously enabled DMA tasks from up to 32 DMA requestors. SmartComm uses internal buffers to prefetch "reads" and post "writes" such that bursting is used whenever possible. This optimizes both internal and external bus activities. SmartComm also contains four independent baud rate generators and four 16-bit or two 32-bit timers.

Programmable Serial Controllers (PSC)

Three full duplex channels support both asynchronous and synchronous protocols with both 8-bit and 16-bit data widths. They may be used to connect to the following types of interfaces: RS232 peripherals, CODECs, Bluetooth modules, Digital Controlled Radio, cellular phones, navigation/GPS, 2-way pagers, or a standard UART interface to a terminal/computer for debug support.



MGT5100 Based System

Figure 2 MGT5100 Based System Block Diagram

10/100 BaseT Ethernet

Supports standard MAC-PHY interfaces: 10Mbps and 100Mbps IEEE 802.3 MII and 10Mbps 7-wire interface for debug and communication.

I2C (Inter Integrated Circuit)

Contains two separate multi-master, microwire compatible I2C interfaces and supports 520Kbps transfer rates. Both master and slave interfaces may be controlled directly by the G2 core or can utilize the SmartComm subsystem to buffer tx/rx data when the I2C interrupt frequency is high.

SPI (Serial Peripheral Bus)

Full duplex, synchronous serial communication interface. It supports master and slave modes, double-buffered operations, and can operate in polling and interrupt driven environments.

USB (Universal Serial Bus)

Implements the USB Host Controller/Root Hub in compliance with the USB 1.1 specification. Supports one or two USB ports off of the root hub which then connects to an off-chip USB transceiver. The host controller supports the Open Host Controller Interface (OHCI) standard.

IR and IrDA

Supports two independent infrared inputs and one infrared output. One input can be programmed to recognize consumer IR inputs such as keyboards/remote controllers. The second port recognizes the IrDA formats (SIR, MIR, FIR) to 4.0Mbps for communication with PDAs, laptops, etc. The required 48MHz clock can be generated internally or supplied externally. An IRBlaster tx port is also included.

System Level Interfaces

The MGT5100 integrates the most common system interfaces and signals. There are six fully programmable external chip selects, independent of the SDRAM interface. CS0 has special features to support a Boot ROM. Two of these chip selects will be used by the IDE disk drive interface, when enabled.

The interrupt controller is provided with four external interrupt signals. The controller manages external and internal interrupts. Levels and priorities of all interrupts are programmable. The interrupt controller is designed to take advantage of the new G2 core critical interrupt feature. This allows interrupting of the G2 core outside the operating system boundaries for critical real-time functions.

Integrated are several timer functions required by most embedded systems: Two internal Slice Timers are provided to create short cycle periodic interrupts. A Watch-Dog Timer is included which will interrupt the processor if not regularly serviced, catching software hang-ups. A bus monitor is included to monitor bus cycles and provide an interrupt if transactions take longer than a prescribed time.

There are ten dedicated GPIO signals, two of which support “wake up” capability to the MGT5100 bringing it out of low power modes, eight of which can be attached to eight internal full function timers. Additional GPIO ports are available depending on the functional requirements of a given system.

Many of the serial/parallel port pins serve multiple functions, allowing flexibility in optimizing the system to meet a specific set of integration requirements. For example, PSC3 could be dedicated to a 9-pin modem interface or could be split into a simple UART with five available GPIO pins.

Dual MSCAN (Motorola Scalable Controller Area Network)

The CAN is an asynchronous communications protocol used mostly in automotive and industrial control systems. It is a high speed (1Mbps), short distance, priority based protocol that can run over a variety of media. The MSCAN supports both the standard and extended identifier (ID) message formats. Each MSCAN module contains 4 receive buffers with FIFO storage scheme and 3 transmit buffers. It also contains flexible maskable identifier filters.

SDRAM Controller and Interface

A high speed SDRAM controller supports both standard SDRAM and Double Data Rate (DDR) SDRAM devices. It supports 64Mbit, 128Mbit, 256Mbit, and 512Mbit memories. Bursting is supported, allowing data transfer rates of 264Mbytes/sec with SDR @ 66MHz and 528Mbytes/sec with DDR memories at 66MHz.

Multi-function External Bus

The MGT5100 supports a multi-function external local bus to allow connections to PCI and ATA/IDE compliant devices as well as external ROM/SRAM. It integrates a 3.3V, PCI V2.2 compatible external bus controller and interface. This bus is a 32-bit multiplexed address/data bus which supports PCI bus frequencies up to 66MHz.

The external bus also provides support for an ATA/IDE disk drive interface. ATA control signals (chip selects, write, read, etc.) are provided independent of the PCI control signals to prevent bus contention, but the 32-bit data bus is shared. When it recognizes

an external access meant for the ATA controller, the function of the PCI address/data bus is transformed into 16 bits of ATA data and 3 bits of ATA address.

The external bus also allows connection to external memory or peripheral devices that adhere to a ROM or SRAM-like interface. These devices occupy a separate location in the memory map and have independent control signals. Again, when an internal access is decoded to fall in the SRAM/ROM memory space, the 32-bit PCI address/data bus is transformed into 24 bits of address and 8 bits of data, or 16 bits of address and 16 bits of data for these accesses.

The MGT5100 supports a reset configuration mode common on the family of microprocessors that implement the PowerPC architecture where 8 bits of configuration information is driven and sampled during reset to establish the initial processor configuration.

Power Management

The MGT5100 is manufactured in a low-power static CMOS technology. In addition, it supports the dynamic power management modes available on the 603e series processors including doze and sleep modes.

Several of the GPIOs, interrupt lines and the IR interface support a “wake up” capability such that the MGT5100 can be placed in a low power stand-by mode, then re-enabled by one of the “wake up” inputs.

Systems Debug and Test

The MGT5100 supports the COP debug capability common on other Motorola processors. The COP interface supports such features as memory download, single step instruction execution, break/watch point capability, access to internal registers, pipeline tracking, etc.

Supports a JTAG IEEE 1149.1 controller and Test Access Port (TAP).

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HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217
1-303-675-2140 or 1-800-441-2447

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