Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MMA6910KQ
Rev. 2, 10/2015

MMA6910KQ, High-Accuracy, Low-g, Inertial Sensor

MEMS Sensing, State Machine ASIC

The MMA6910KQ, a SafeAssure solution, is a dual axis, low-g, XY, sensor based on Freescale's HARMEMS technology, with an embedded Digital Signal Processor (DSP) ASIC, allowing for additional processing of the digital signals.

Features

- Sensitivity in X and Y axes
- ±3.5 g full-scale range per axis
- AEC-Q100 qualified, Rev. F, grade 2 ($-40 \le T_A \le 105$ °C)
- 50 Hz second order low-pass filter
- Unsigned 11-bits digital data output
- SPI-compatible serial interface
- Capture/hold input for system-wide synchronization support
- 3.3 or 5.0 V single supply operation
- On-chip temperature sensor and voltage regulator
- Bidirectional internal self-test
- Minimal external component requirements
- Pb-free 16-pin QFN package
- Pulse-code modulated output available for device evaluation

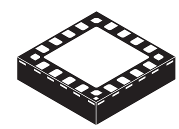
Typical applications

- With a ±3.5 g full-scale range, the newly designed, high-accuracy sensor, enables Electronic Stability Control (ESC) designers to accommodate higher original signal noise level without sacrificing resolution.
- Tilt measurement
- Electronic parking brake

Ordering information		
Device name	**Range**	**Shipping**
MMA6910KQ	±3.5 g	Tray
MMA6910KQR2	±3.5 g	Tape and Reel

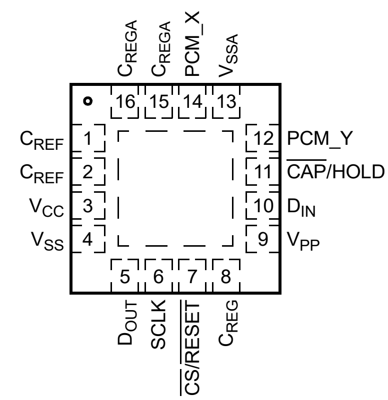
MMA6910KQ

Bottom view



16-PIN QFN
CASE 98ASA10571D

Top view



Pin connections

Contents

Related Documentation

The MMA6910KQ device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to the Freescale homepage at:

   http://www.freescale.com/

2. In the Keyword search box at the top of the page, enter the device number MMA6910KQ.
3. In the Refine Your Result pane on the left, click on the Documentation link.

1 Introduction

1.1 Introduction

MMA6910KQ is a two-axis member of Freescale's family of SPI-compatible accelerometers. These devices incorporate digital signal processing for filtering, trim, and data formatting.

1.2 Serial communication configuration

The serial communication configuration provides a 4-wire SPI interface. Device serial number, acceleration range, filter characteristics, and status information are available along with acceleration data via the SPI.

1.3 Block diagram

A block diagram illustrating the major components of the design is shown in Figure 1.

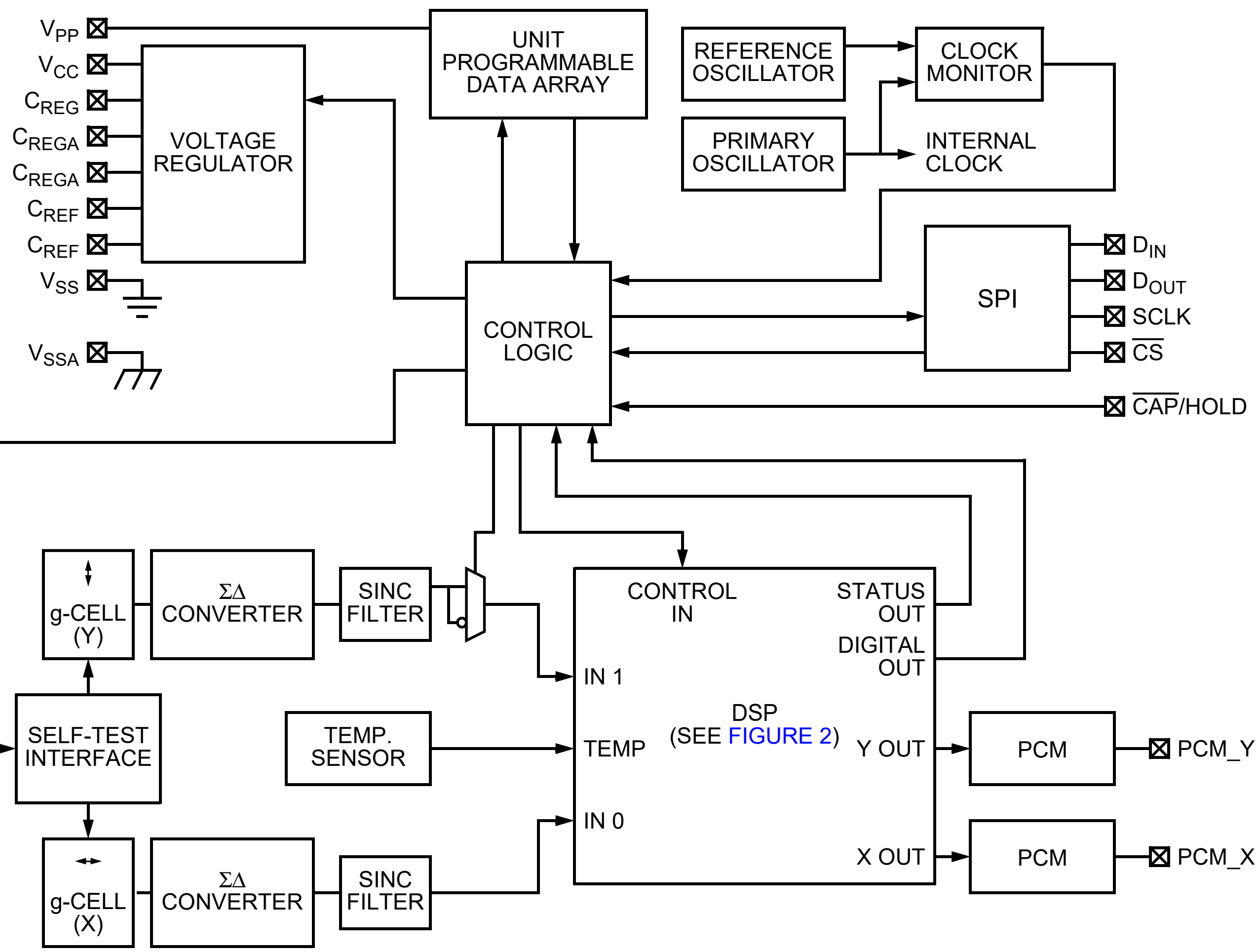


Figure 1. Block diagram

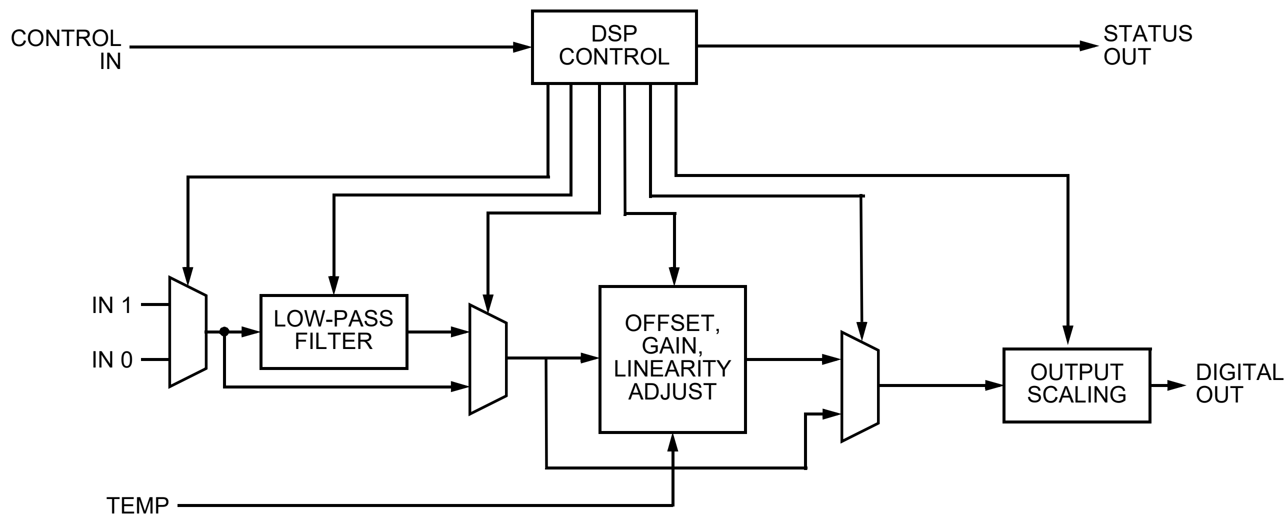


Figure 2. DSP block diagram

1.4 Pin functions

The pinout is illustrated in Figure 3. Pin functions are described in the following paragraphs. When self-test is active, the output becomes more positive in both axes, if ST1 is cleared or more negative in both axes if ST1 is set, as described in Section 2.1.3.

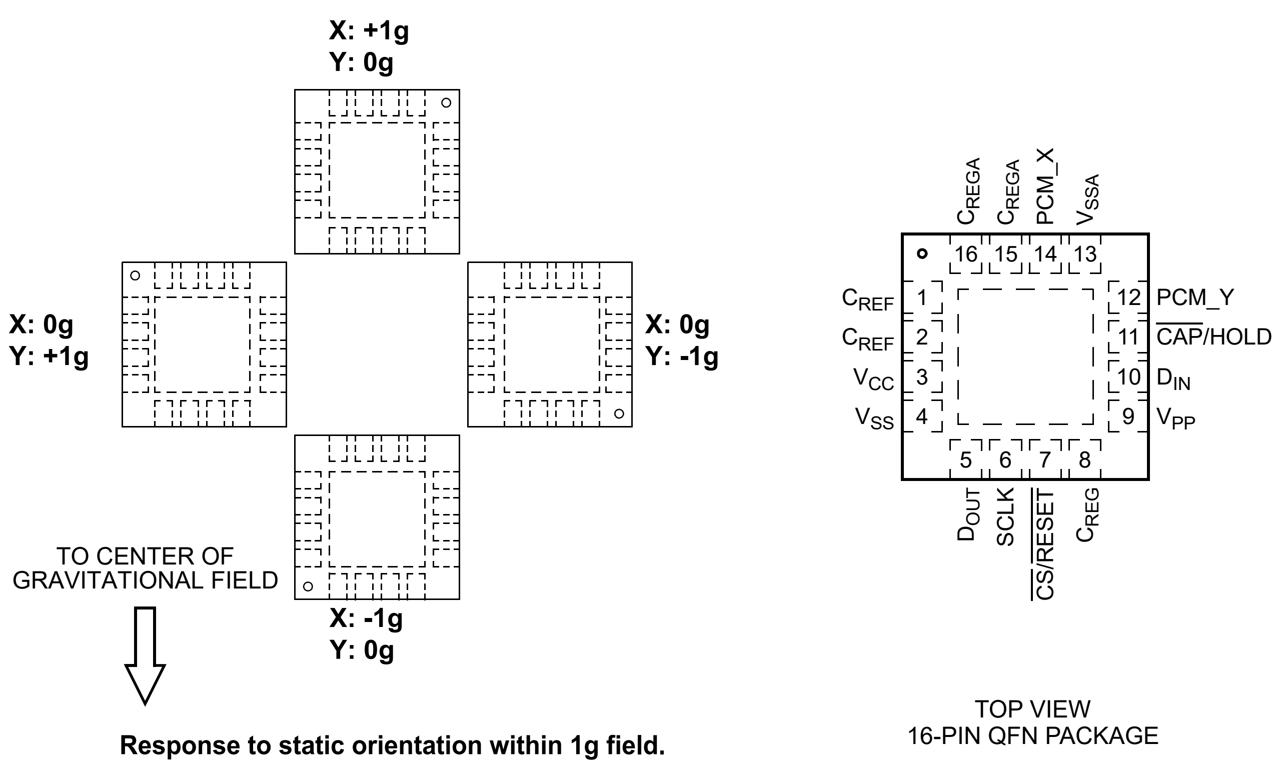


Figure 3. Pinout for MMA6910KQ

1.4.1 V_{CC}

This pin supplies power to the device. Careful printed wiring board layout and capacitor placement is critical to ensure best performance. An external bypass capacitor between this pin and V_{SS} is required, as described in Section 1.5.

1.4.2 V_{SS}

This pin is the power supply return node for the digital circuitry on the MMA6910KQ device.

1.4.3 V_{SSA}

This pin is the power supply return node for analog circuitry on the MMA6910KQ device. An external bypass capacitor between this pin and V_{CC} is required, as described in Section 1.5.

1.4.4 C_{REG}

This pin is connected to the internal digital circuitry power supply rail. An external filter capacitor must be connected between this pin and V_{SS}, as described in Section 1.5.

1.4.5 C_{REGA}

These pins are connected in parallel to the internal analog circuitry power supply rail. One or two external filter capacitors must be connected between these pins and V_{SSA}, as described in Section 1.5. Two pins are provided to support redundant connection to the printed wiring board assembly. Redundant external capacitors may be connected to these pins for maximum reliability, as described in Section 1.5.

1.4.6 C_{REF}

These pins are connected in parallel to an internal reference voltage node utilized by the analog circuitry. One or two external filter capacitors must be connected between these pins and V_{SSA}, as described shown in Section 1.5. Two pins are provided to support redundant connection to the printed wiring board assembly. Redundant external capacitors may be connected to these pins for maximum reliability, as described in Section 1.5.

1.4.7 V_{PP}

This pin should be tied directly to V_{SS}. An internal pulldown device is connected to this pin to reduce the risk of unpredictable device operation in the event that the connection to V_{SS} opens.

1.4.8 SCLK

This input pin provides the serial clock to the SPI port. The state of this pin is also used as a qualifier for externally-controlled reset. This input may be used to initiate device reset as described in Section 1.4.9 and Section 2.6. An internal pulldown device is connected to this pin.

1.4.9 $\overline{CS}/\overline{RESET}$

This pin functions as the chip select input for the SPI port. The state of the D_{IN} pin, during low-to-high transitions of SCLK, is latched internally and D_{OUT} is enabled when $\overline{CS}$ is at a logic-low level.

This pin may also be used to initiate a hardware reset. If $\overline{CS}$ is held low and SCLK is held high for 512 µs, the internal reset signal is asserted. This behavior is described in Section 2.6.

An internal pullup device is connected to this pin.

1.4.10 D_{OUT}

This pin functions as the serial data output for the SPI port. SPI data transmitted on D_{OUT} will have an odd number of logic ‘1’ bits set during normal 16-bit transfer, unless an internal oscillator fault condition has been detected. If an internal oscillator fault condition is present, D_{OUT} is driven to a logic-high level continuously, when $\overline{CS}/\overline{RESET}$ is asserted.

1.4.11 D_{IN}

This pin functions as the serial data input to the SPI port. An internal pulldown device is connected to this pin. SPI data received at D_{IN} must observe odd parity or a transient exception condition will be reported during the subsequent transfer.

1.4.12 $\overline{CAP}$/HOLD

When this input pin is low, the SPI acceleration result registers are updated by the DSP whenever a data sample becomes available. Upon a low-to-high transition of $\overline{CAP}$/HOLD, the contents of the acceleration result registers are frozen. The result registers will not be updated so long as this pin remains at a logic ‘1’ level. This pin may be tied directly to V_{SS} if the hold function is not desired. An internal pulldown device is connected to this pin, however it is recommended that $\overline{CAP}$/HOLD either be driven by a logic output or tied to V_{SS} in application circuits. If $\overline{CAP}$/HOLD is at logic ‘1’ level during initial startup and through the release of internal reset, the result register will be 0 counts, which is a reserved result, and should be discarded by the application. This state is exited by the next high-to-low transition of $\overline{CAP}$/HOLD.

1.4.13 PCM_X, PCM_Y

MMA6910KQ provides the option for a Pulse Code Modulated (PCM) output function. The PCM output is activated when PCM_EN is set in the DEVCTL register. When the PCM function is enabled, the upper nine bits of the 11-bit scaled acceleration values are used to generate PCM signals proportional to incident-respective acceleration, at 250 ns resolution. A simplified block diagram of the PCM output is shown in Figure 4.

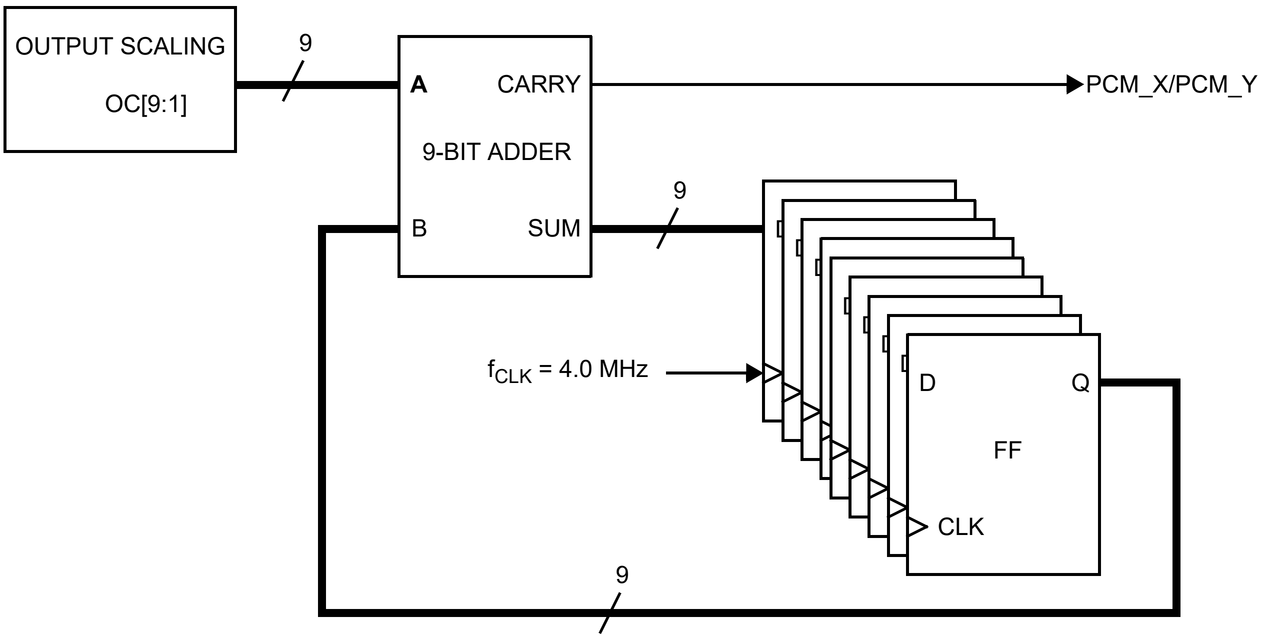
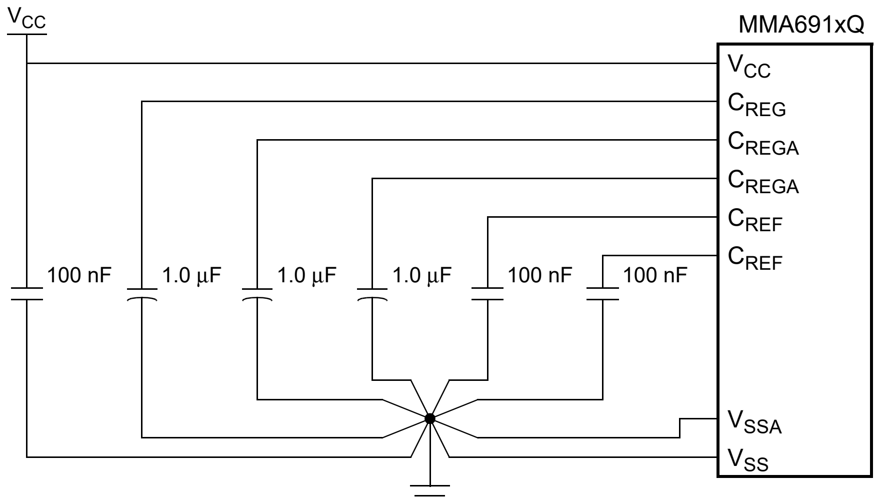


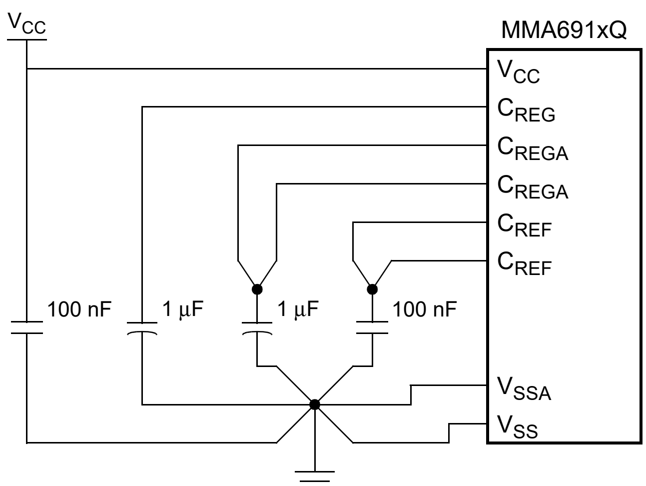
Figure 4. PCM output function block diagram

1.5 External components

The connections illustrated in Figure 5 are recommended. Careful printed wiring board layout and component placement is essential for best performance. Low-ESR capacitors must be connected to C_{REG} and C_{REGA} pins for best performance. A grounded land area with solder mask should be placed under the package for improved shielding of the device from external effects. If a land area is not provided, no signals should be routed beneath the package.



RECOMMENDED EXTERNAL COMPONENT CONFIGURATION



ALTERNATE EXTERNAL COMPONENT CONFIGURATION

Figure 5. External components

2 Internal Modules

2.1 Data array

A 400-bit data array allows each device to be customized. The array interface incorporates parity circuitry for fault detection along with a locking mechanism, to prevent unintended changes. Portions of the array are reserved for factory-programmed trim values. Customer accessible data stored in the array are shown in the Table 1.

Addresses $00 - $0D are associated with the data array. A writable register at address $0E is provided for device control operations. Two read-only registers at addresses $0F and $10 provide status information.

Unused bits within the data array are always read as ‘0’ values. Unprogrammed OTP bits are also read as ‘0’ values.

Table 1. DSP configuration register

Location		Bit function								Type
Addr	Register	7	6	5	4	3	2	1	0	
$00	SN0	SN[7]	SN[6]	SN[5]	SN[4]	SN[3]	SN[2]	SN[1]	SN[0]	F/R
$01	SN1	SN[15]	SN[14]	SN[13]	SN[12]	SN[11]	SN[10]	SN[9]	SN[8]	
$02	SN2	SN[23]	SN[22]	SN[21]	SN[20]	SN[19]	SN[18]	SN[17]	SN[16]	
$03	SN3	SN[31]	SN[30]	SN[29]	SN[28]	SN[27]	SN[26]	SN[25]	SN[24]	
$04	DEVCFG0	0	0	0	0	RNG[3]	RNG[2]	RNG[1]	RNG[0]	F/R
$05	DEVCFG1	0	0	0	0	RNG[3]	RNG[2]	RNG[1]	RNG[0]	
$06	DEVCFG2	0	0	0	0	0	0	0	0	
$07	DEVCFG3	0	0	0	0	0	0	0	0	
$08	DEVCFG4	0	0	0	0	0	0	0	0	
$09	DEVCFG5	1	0	1	0	0	0	0	0	
$0A	AXCFG_X	1	0	0	1	0	1	0	1	F/R
$0B	AXCFG_Y	1	0	0	1	0	1	0	1	
$0C	Unused									N/A
$0D	DSPCFG	0	0	1	0	0	1	0	0	F/R
$0E	DEVCTL	RES_1	RES_0	CE	PCM_EN	Unused	YINV	ST1	ST0	R/W
$0F	TEMP	TEMP[7]	TEMP[6]	TEMP[5]	TEMP[4]	TEMP[3]	TEMP[2]	TEMP[1]	TEMP[0]	R
$10	DEVSTAT	IDE	OSCF	DEVINIT	TF	0	0	0	DEVRES	
$11	COUNT	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]	
$24	ACC_X11L	ACC_X[7]	ACC_X[6]	ACC_X[5]	ACC_X[4]	ACC_X[3]	ACC_X[2]	ACC_X[1]	ACC_X[0]	
$25	ACC_X11H	0	0	0	0	0	ACC_X[10]	ACC_X[9]	ACC_X[8]	
$26	ACC_Y11L	ACC_Y[7]	ACC_Y[6]	ACC_Y[5]	ACC_Y[4]	ACC_Y[3]	ACC_Y[2]	ACC_Y[1]	ACC_Y[0]	
$27	ACC_Y11H	0	0	0	0	0	ACC_Y[10]	ACC_Y[9]	ACC_Y[8]	

F: Factory programmed OTP location R: Read-only register R/W: Read/write register N/A: Not applicable

2.1.1 Device serial number

A unique serial number is programmed into each device during manufacturing. The serial number is composed of the following information.

Table 2. Serial number assignment

Bit function	
Bit range	Content
SN12 - SN0	Serial number
SN31 - SN13	Lot number

Lot numbers begin at 1 for all devices produced and are sequentially assigned. Serial numbers begin at 1 for each lot, and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 13-bit serial number. Not all allowable lot numbers and serial numbers will be assigned.

2.1.2 Full-scale range

Full-scale range is indicated by the value programmed into DEVCFG0 and DEVCFG1. Ranges for defined part numbers are shown in Table 3 below.

Table 3. Full-scale range

Part number	Register	Range bits				Full-scale range (g)
		RNG[3]	RNG[2]	RNG[1]	RNG[0]	
MMA6910Q	DEVCFG0	0	0	0	0	3.5
	DEVCFG1	0	0	0	0	3.5

2.1.3 Device Control register (DEVCTL)

A read/write register at address $0E supports a number of device control operations as described in the following. Reserved bits within DEVCTL are always read as logic ‘0’ values.

Write operations involving DEVCTL are effective approximately 1.0 µs following negation of $\overline{CS}/\overline{RESET}$. This delay must be considered if successive SPI operations — involving write to DEVCTL, followed by acceleration data read — are conducted in the minimum-allowed transfer timing. If there is no delay, the acceleration result may indicate lingering self-test or error-status conditions. It is therefore recommended that acceleration data-read operations be delayed by at least 1.2 µs following writes to DEVCTL.

Table 4. Device Control register

Address	Register	Bit							
		7	6	5	4	3	2	1	0
$0E	DEVCTL	RES1	RES0	CE	PCM_EN	Unused	YINV	ST1	ST0

2.1.3.1 Reset Control (RES_1, RES_0)

A specific series of three write operations involving these two bits will cause the internal digital circuitry to be reset. The state of the remaining bits in the DEVCTL register do not affect the reset sequence, however any write operation involving this register in which both RES_1 and RES_0 are cleared will terminate the sequence.

To reset the internal digital circuitry, the following register write operations must be performed in the order shown:

1. Set RES1. RES0 must remain cleared.
2. Set RES1 and RES0.
3. Clear RES1 and set RES0.

RES1 and RES0 are always read as logic ‘0’ values.

2.1.3.2 Clear Error (CE)

Setting this bit to a logic ‘1’ state will clear transient error status conditions. It is necessary to either set this bit or perform a device reset if an error condition has been reported by the device before acceleration data transfer can be resumed. The device reset condition may be cleared only after device initialization has completed.

Error conditions and classification are described in Section 3.1.

The state of this bit is always read as logic ‘0’.

2.1.3.3 PCM Enable (PCM_EN)

This bit controls the PCM_X and PCM_Y outputs along with internal circuitry which generates a pulse-code modulated signal from the acceleration result. When this bit is set, the PCM outputs are enabled. When cleared, PCM_X and PCM_Y are driven to a logic-low level.

2.1.3.4 Unused

A write to this bit will have no effect. The state of this bit is always read as logic '0'.

2.1.3.5 Y-Axis Signal Inversion Control (YINV)

This control function verifies the operation of the two-channel multiplexor which alternately provides X-axis and Y-axis data to the DSP. An inverter block and multiplexor at the Y-axis input to the DSP are controlled by the YINV bit. Setting this bit when ST0 is set has the effect of changing the sign of acceleration in the Y axis. Operation of the YINV bit is illustrated in Figure 6. Y-axis inversion may be selected only during self-test; the state of this bit has no effect when ST0 is cleared.

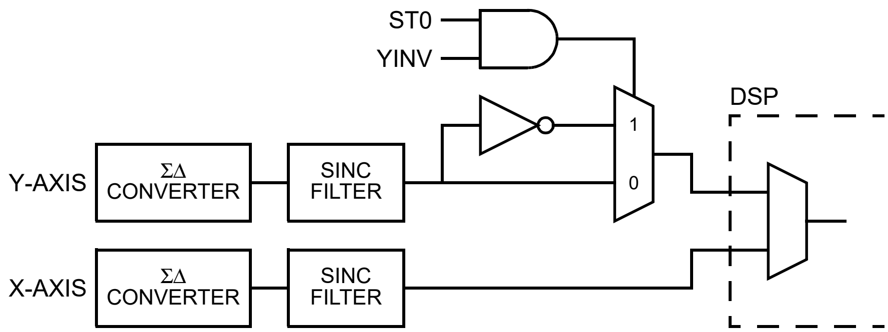


Figure 6. Y-Axis inversion function

Self-test operations controlled by YINV along with ST1 and ST0 are summarized in the Table 5.

2.1.3.6 Self-Test Control (ST1, ST0)

Bidirectional self-test control is provided through manipulation of these bits. ST1 controls direction while ST0 enables and disables the self-test circuitry. ST1 and ST0 are always cleared following internal reset. Both axes are affected simultaneously by the state of these bits. If the offset monitor is enabled, self-test activation in a single direction should be limited to less than 30 ms.

Communications protocol bits S2 - S1 are inverted when self-test is activated, as described in Section 3.2.

Table 5. Self-Test Control operations

YINV	ST1	ST0	Self-Test Operation	
			X-Axis	Y-Axis
X	X	0	Self-test Disabled, Y-Axis Signal Inversion Disabled	
0	0	1	Positive Deflection	
0	1	1	Negative Deflection	
1	0	1	Positive Deflection	Negative Deflection
1	1	1	Negative Deflection	Positive Deflection

Offset correction is applied within the DSP, and is not affected by the state of the YINV bit. Consequently, inversion of the Y-axis signal may result in saturation of the Y-axis output value.

Correct operation of the DSP input multiplexor may be confirmed by performing the operations shown in Figure 7.

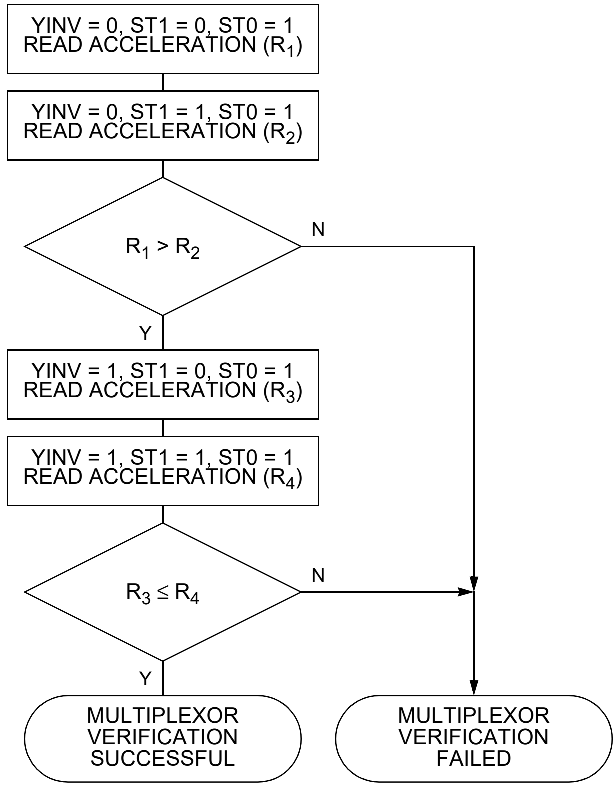


Figure 7. DSP input multiplexor verification flow chart (Y axis)

2.1.4 Temperature Sensor Value (TEMP)

This read-only register contains a signed value which provides a relative temperature indication. The temperature sensor is uncalibrated and its output for a given temperature will vary from one device to the next. The value in this register increases with temperature.

Table 6. Temperature Sensor Value register

Location		Bit function							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$0F	TEMP	TEMP[7]	TEMP[6]	TEMP[5]	TEMP[4]	TEMP[3]	TEMP[2]	TEMP[1]	TEMP[0]

2.1.5 Device Status register (DEVSTAT)

This read-only register is accessible in all modes.

Table 7. Device Status register

Location		Bit function							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$10	DEVSTAT	IDE	0	DEVINIT	TF	0	0	0	DEVRES

2.1.5.1 Internal Data Error flag (IDE)

This flag will be set if a register data-parity fault or a marginally programmed fuse is detected. Device reset is required to clear this fault condition. If a parity error is associated with the data stored in the fuse array, this fault condition cannot be cleared. This flag is disabled when the device is in test mode.

2.1.5.2 Device Initialization flag (DEVINIT)

This flag is set during the interval between negation of internal reset and completion of device initialization. DEVINIT is cleared automatically.

2.1.5.3 Temperature Fault flag (TF)

This flag is set if the value reported by the on-chip temperature sensor exceeds specified limits. TF may be cleared by writing a logic ‘1’ value to the CE bit in DEVCTL, provided that the fault condition is no longer detected.

2.1.5.4 Device Reset flag (DEVRES)

This flag is set during device initialization. A logic ‘1’ must be written to the CE bit in the Device Control register (DEVCTL) to clear this bit. This bit must be explicitly cleared following reset before acceleration results can be read from MMA6910KQ.

2.1.6 Counter register (COUNT)

This read-only register provides the value of a free-running 8-bit counter derived from the primary oscillator. A 5-bit prescaler divides the 4.0 MHz primary oscillator frequency by 32. Thus, the value in the register increases by one count every 8.0 µs, and the counter rolls over every 2.048 ms.

Table 8. Counter register

Location		Bit Function							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$11	COUNT	COUNT[7]	COUNT[6]	COUNT[5]	COUNT[4]	COUNT[3]	COUNT[2]	COUNT[1]	COUNT[0]

2.1.7 Acceleration Result registers

These read-only registers contain acceleration results produced by the DSP. The values in these registers are frozen by either of two events:

- $\overline{\text{CAP}}$/HOLD input at logic-high level
- $\overline{\text{CS}}$ input at logic-low level

Acceleration result registers are provided for each axis. ACC_X11L/ACC_X11H and ACC_Y11L/ACC_Y11H provide 11-bit results. Updates to ACC_X11L/ACC_X11H and ACC_Y11L/ACC_Y11H are halted upon reading the lower-byte register of either pair until the upper-byte register is read. There is no requirement to manipulate $\overline{\text{CAP}}$/HOLD when reading ACC_X11L/ACC_X11H or ACC_Y11L/ACC_Y11H, however ACC_X11H or ACC_Y11H must be read after reading ACC_X11L or ACC_Y11L, respectively, or further updates to the register pair will not occur.

Table 9. X-Axis Acceleration Result registers

Location		Bit Function							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$24	ACC_X11L	ACC_X[7]	ACC_X[6]	ACC_X[5]	ACC_X[4]	ACC_X[3]	ACC_X[2]	ACC_X[1]	ACC_X[0]
$25	ACC_X11H	0	0	0	0	0	ACC_X[10]	ACC_X[9]	ACC_X[8]

Table 10. Y-Axis Acceleration Result registers

Location		Bit Function							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$26	ACC_Y11L	ACC_Y[7]	ACC_Y[6]	ACC_Y[5]	ACC_Y[4]	ACC_Y[3]	ACC_Y[2]	ACC_Y[1]	ACC_Y[0]
$27	ACC_Y11H	0	0	0	0	0	ACC_Y[10]	ACC_Y[9]	ACC_Y[8]

Sign extension is applied to the upper five bits of ACC_X11H and ACC_Y11H. **If an error condition exists, the reserved value 0 will be read in place of 11-bit acceleration data.**

2.2 Voltage regulators

Separate, internal-voltage regulators supply fixed voltages to the analog and digital circuitry. External filter capacitors are required, as shown in Figure 5.

The voltage regulator module includes a voltage monitoring circuitry which holds the device in reset following startup until internal voltages have stabilized sufficiently for proper operation. The voltage monitor asserts internal reset when the external supply or internally regulated voltages fall below predetermined levels.

A reference generator provides a stable voltage which is used by the ΣΔ converter. This circuit also requires an external filter capacitor.

The voltage regulator module is illustrated in Figure 8 and Figure 9.

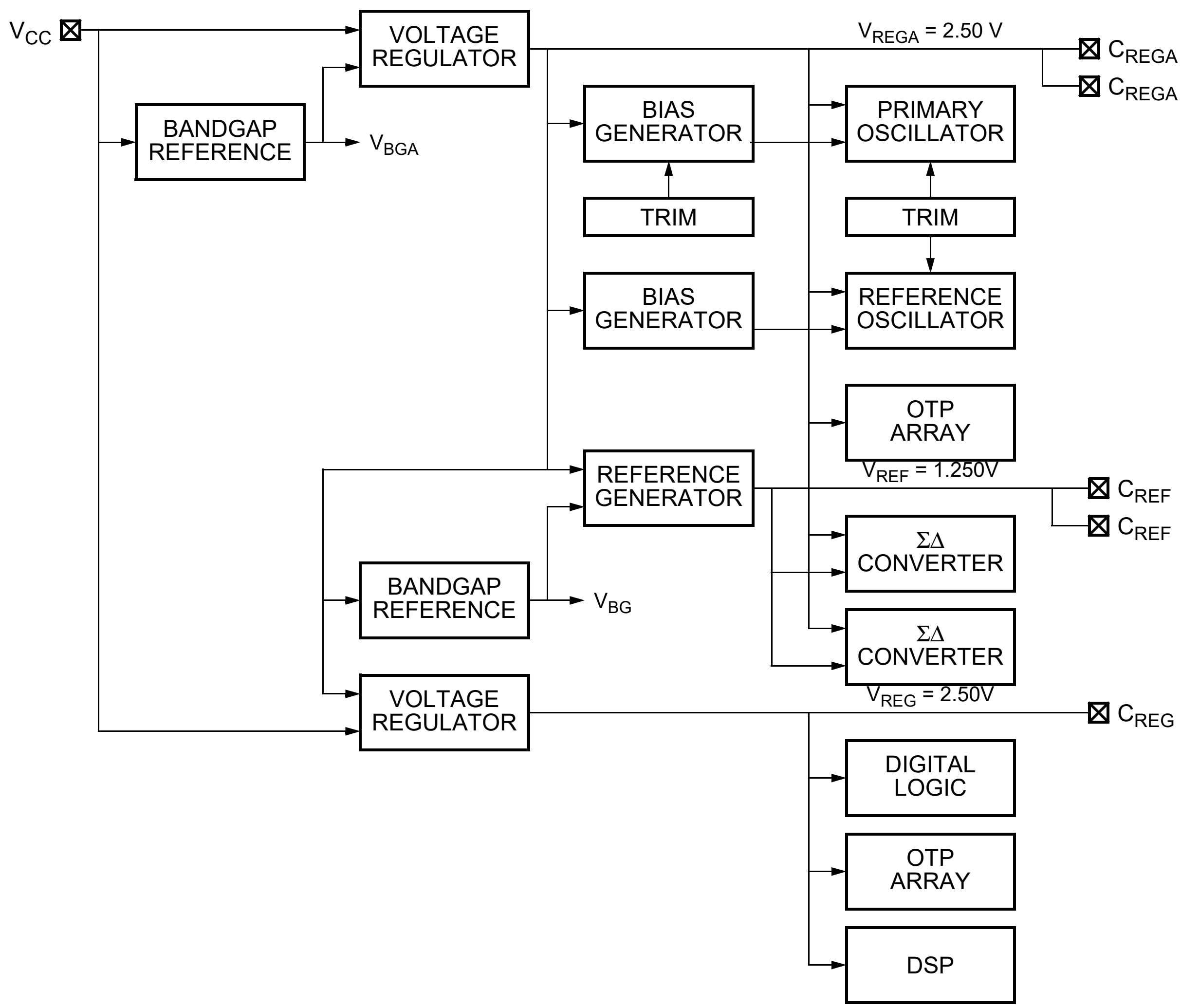
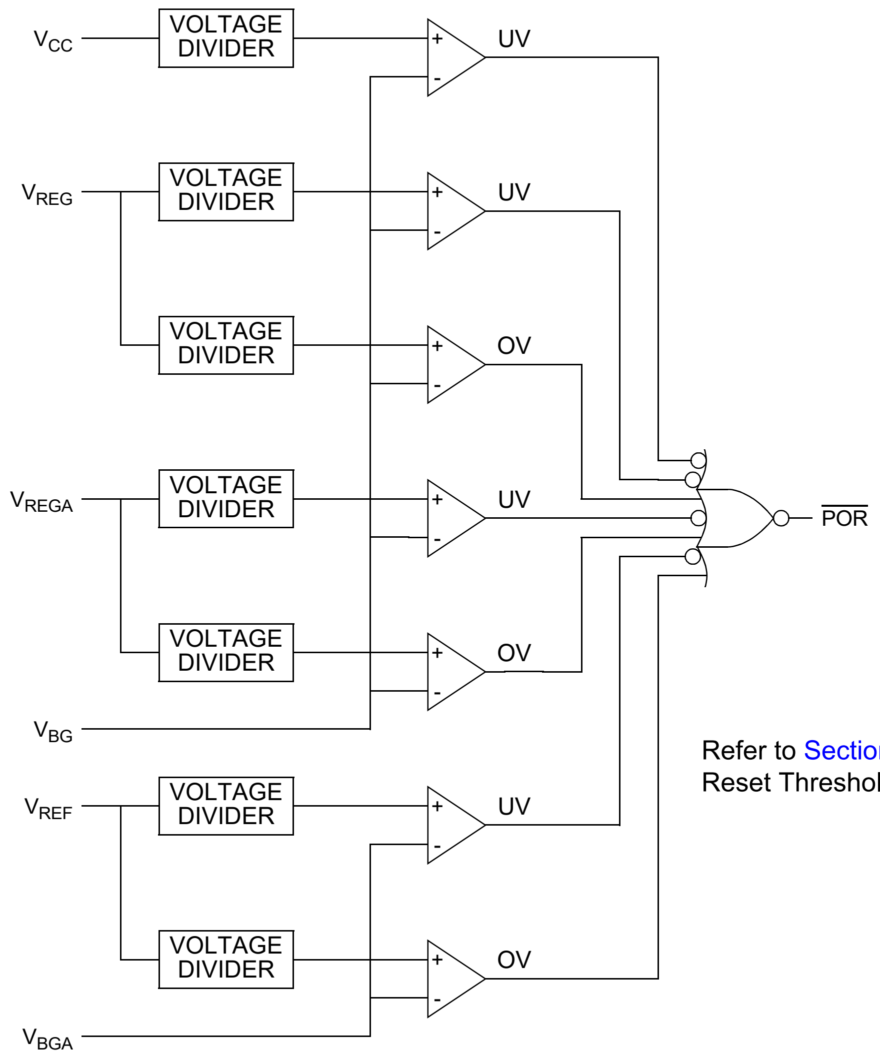


Figure 8. Power distribution



Refer to Section 5.3 for Startup Reset Threshold limits.

Figure 9. Voltage monitoring

2.3 Oscillator

An internal oscillator operating at a nominal frequency of 4.0 MHz provides a stable clock source. The oscillator is factory trimmed for best performance. A clock generator block divides the 4.0 MHz clock as needed by other blocks.

2.4 C_{REG} monitor

A monitor circuit is incorporated to ensure predictable operation of the device in the event that the connection to the external capacitor at the C_{REG} pin (pin 8) fails, or the capacitor opens. The monitor disables the 2.5V regulator which powers the digital circuitry for 2.0 µs every 249.5 µs. If the external capacitor is not present, voltage at the internal supply rail will drop below the internal reset threshold, continuously forcing the device into reset. Loss of communication from the device is a readily detectable condition. The X_{OUT} and Y_{OUT} pins are driven to the low rail when the device is in the reset state.

2.5 Clock monitor

Two independent oscillators are provided within MMA6910KQ. One is factory-trimmed and provides the timing reference used throughout the device. The second oscillator acts as a reference for the first. If the frequency of these two oscillators varies by more than 10%, an oscillator fault condition is determined. In normal operating mode, an oscillator fault will cause the D_{OUT} pin to be forced to a continuous logic-high state when $\overline{CS}$ is asserted, as described in Section 3.1.1.2.

2.6 Internal reset controller

Four conditions can result in an internal reset. The initial startup condition always results in a reset condition An internal voltage monitor will assert reset when the supply voltage or a regulated output voltage falls below specified limits. This is referred to as a low-voltage reset. Externally, a hardware reset can be initiated by holding SCLK high and driving the $\overline{CS}$ pin low for 512 μs. Finally, the device can be reset through a series of register write operations, as described in Section 2.1.3.1.

2.7 Control logic

A control logic block coordinates a number of activities within the device. These include:

- Post-reset device initialization
- Self-test
- Operating mode selection
- Data array programming
- Device support data transfers

2.8 Temperature sensor

A temperature sensor provides input to the digital signal processing block. Device temperature is incorporated into a correction value, which is applied to each acceleration result. The upper eight bits of the temperature sensor value are accessible through the TEMP register, described in Section 2.1.4. The temperature sensor output is continuously compared to under- or over-temperature limits of approximately -40 and +110 °C, respectively. A temperature fault condition is indicated if the temperature sensor value exceeds the under- or over-temperature limit.

2.8.1 Temperature sensor monitor

A monitor circuit associated with the temperature sensor is provided. The monitor will detect over- or under-temperature conditions as well as rapid fluctuations in temperature sensor output such as would be related to failure of the sensor. If a temperature related fault is detected, an error condition is indicated in lieu of acceleration data.

Rapid fluctuation of the temperature sensor output is detected by comparing the value of each sample to the previous value. This operation, as well as temperature limit detection is illustrated in Figure 10. A fault condition is indicated if predetermined limits are exceeded.

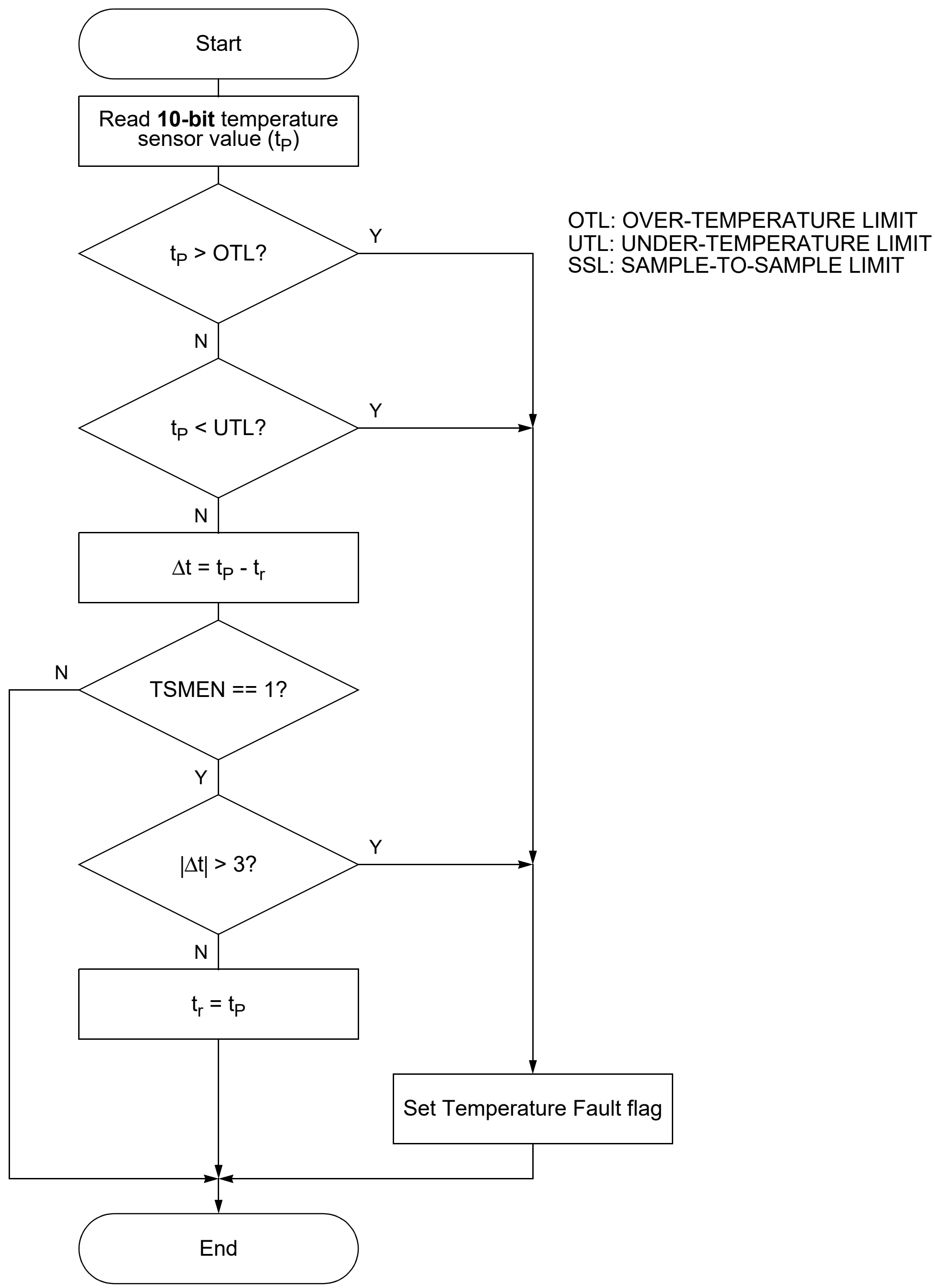


Figure 10. Temperature sensor monitor flow chart

2.9 SPI

The SPI is a full bidirectional port which is used for all configuration and control functions.

2.10 Self-test interface

The self-test interface provides a mechanism for applying a calibrated voltage to the g-cell. This results in deflection of the proof mass, causing reported acceleration results to be offset by a specified amount. Control of the self-test interface via the SPI is accommodated through write operations involving the DEVCTL register at address \$0E, described in Section 2.1.3.

2.11 ΣΔ converters

Two sigma delta converters provide the interface between the g-cell and digital signal processing block. The output of each ΣΔ converter is a data stream at a nominal frequency of 1.0 MHz.

2.12 Digital signal processing block

A digital signal processing block is used to perform all filtering and compensation operations. The signal-processing flow within the DSP block is illustrated in Figure 1. The DSP operates at 2.0 MHz, twice the frequency of the ΣΔ converters. The two interleaved bit streams from the ΣΔ converters are processed simultaneously within the DSP.

Each MMA6910KQ device is factory programmed to select the acceleration range. Filter characteristics for the X and Y axes are customer programmed.

2.12.1 Low-pass filter

Low-pass filtering occurs in two stages. The serial data stream produced by the ΣΔ converters is decimated and converted to parallel values by a sinc filter. Parallel data is then processed by an Infinite Impulse Response (IIR) low-pass filter.

Response parameters for the low-pass filter are summarized in A.2.

3 Serial Communications

Digital data communication is completed through synchronous serial transfers via the SPI port. Conventional SPI protocol is employed, acting as a slave device observing CPOL = 0, CPHA = 0, MSB first. All SPI transfers are 16-bits in length, and employ parity detection to ensure data integrity. During each SPI transfer, an odd number of bits received at D_{IN} must be set to a logic ‘1’ state, or a transient exception condition will be reported during the subsequent transfer. In all normal SPI responses, an odd number of bits transmitted on D_{OUT} will be set to a logic ‘1’ state. Besides parity detection and generation, several other data integrity features are incorporated into the transfer protocol.

3.1 Exception conditions

Under certain conditions, the MMA6910KQ will respond to serial commands with a word, which indicates that an exception condition has been detected. Response varies according to the communication protocol selected. Exceptions fall into five classes and are prioritized. If multiple exception conditions are detected, only the exception of highest priority is reported.

A reset exception condition exists following any device reset. Immediately following reset, a device initialization condition will be indicated until internal initialization of the circuitry has completed. Following internal initialization, a device reset exception condition exists until explicitly cleared by writing a logic ‘1’ to the CE bit in DEVCTL.

Transient exception conditions result from data transmission errors such as data parity faults, an invalid number of clock cycles, etc. These exceptions are indicated during the following SPI transfer operation. These exceptions do not require an explicit operation to be cleared.

Behavioral exception conditions are defined as those which affect acceleration data results but do not indicate an error condition. In the MMA6910KQ, the two behavioral exceptions are activation of self-test and a hold condition resulting from the external $\overline{CAP}$/HOLD pin being driven to a logic-high state. Register operations are unaffected by behavioral exceptions. Acceleration data transfers will complete, with the S/T1 and S/T0 bits indicating that one or both behavioral exception conditions exist.

See Section 3.2 for behavioral exceptions reported by the communications protocol.

Critical error exceptions exist when an internal fault, which affects the reliability of device operation or acceleration results, is detected. If a critical error condition exists, an invalid data value is produced by the device in lieu of acceleration results. Register operations are unaffected except for the state of S[2:0]. Some critical errors, such as temperature fault, may be cleared by writing a logic ‘1’ to the CE bit in DEVCTL, provided the underlying fault condition no longer persists. Other critical error conditions require reset of the device to clear.

3.1.1 Defined exceptions

3.1.1.1 Internal data error

Class: Critical error

During reset, a number of internal registers are loaded from a fuse array which stores factory-programmed values. The resistance of each fuse is measured and compared to thresholds to ensure integrity of programmed data. Additionally, the register array is continuously monitored for correct parity at all times while the device is powered. If either the margin test or parity verification fail, an internal data error exception is reported.

Device reset is required to clear this exception condition.

3.1.1.2 Internal oscillator fault

Class: Critical error

If an oscillator fault condition is detected, D_{OUT} is driven high continuously when $\overline{CS}$ is asserted, as illustrated in Figure 11.

Device reset is required to clear this exception condition.

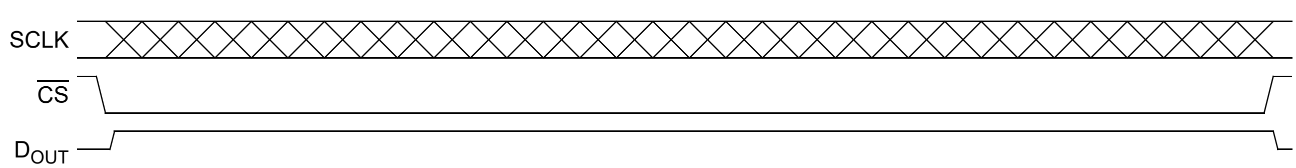


Figure 11. Oscillator failure response

3.1.1.3 Device initialization

Class: Reset

Following a reset condition, the device requires time to complete initialization of the DSP and internal registers. If multiple SPI transfers are attempted during this initialization period, the second and all subsequent transfers will result in this status. The first transfer following reset — regardless of the state of initialization — returns the device reset status.

This exception condition is cleared automatically upon completion of device initialization.

3.1.1.4 Temperature fault

Class: Critical

The internal temperature sensor value has exceeded the allowable limits for the device. This exception condition may be cleared by writing a logic ‘1’ to the CE bit in DEVCTL, provided that the temperature has returned to within the operating limits of the device.

3.1.1.5 Unexpected axis selection

Class: Transient

An acceleration data request has been received with an axis specification which is not supported.

This exception condition is reported during the subsequent transfer.

3.1.1.6 Device reset

Class: Reset

This exception condition is latched any time the device undergoes reset.

Device response will indicate the exception condition in lieu of acceleration data.The device reset exception condition must be explicitly cleared by writing a logic ‘1’ to the CE bit in DEVCTL.

3.1.1.7 SPI clock fault

Class: Transient

A SPI clock fault may result from the following conditions:

- The number of rising clock edges detected while $\overline{CS}$ is asserted is not equal to 16
- SCLK is high when $\overline{CS}$ is asserted

This exception condition is reported during the subsequent transfer.

3.1.1.8 D_{IN} parity fault

Class: Transient

A parity error was detected on D_{IN} during a data transmission.

This exception condition is reported during the subsequent transfer.

3.1.1.9 Self-test activation

Class: Behavioral

The device provides two status bits in its response to indicate that a behavioral exception is enabled. Behavioral conditions include the HOLD condition and self-test activation. As these are not error conditions, device response is otherwise unaffected. Refer to Section 3.2.1 for details regarding device response to behavioral exception conditions.

A HOLD condition exists when the $\overline{CAP}$/HOLD pin is driven to a logic-high level. Self-test activation is controlled through configuration of ST1 and ST0 in DEVCTL.

3.1.2 Exception priority

Table 11 provides a summary of exception conditions and order of priority.

Table 11. Exception conditions

Condition	Status bit	Class
SPI clock fault, previous transfer	—	Transient
D_{IN} parity fault, previous transfer	—	Transient
Internal data error	IDE	Critical error
Internal oscillator fault	—	Critical error
Device initialization	DEVINIT	Reset
Device reset	DEVRES	Reset
Temperature fault	TF	Critical error
Invalid axis selection	—	Transient
Hold condition	—	Behavioral
Self-test	—	Behavioral

If an offset fault condition is detected simultaneously in both the X and Y axes, only the X-axis exception is reported by the device. Hold-condition and self-test exceptions have equal priority; if both exceptions exist simultaneously, both are reported by the device.

3.2 Communications protocol

The communications protocol provides 11-bit acceleration data along with enhanced status notification in the event that an exception condition is detected. All transfers are 16-bits in length, with the intended operation indicated by a two-bit transfer type code transmitted by the SPI master.

Table 12. Transfer type codes

T1	T0	Transfer type
0	0	Register operation
0	1	X-axis acceleration data
1	0	Y-axis acceleration data
1	1	Unused

Device response depends upon the transfer type code and the internal state of the device. If no exception condition has been detected, the device returns register or acceleration data as requested. If an exception condition exists, response depends upon the requested operation and the exception. Exceptions are divided into four classes: behavioral, reset, transient, and critical.

Certain operations, such as register data write and register pointer write, will not be completed if an exception condition is detected during the associated SPI transfer. All exception conditions detected by MMA6910KQ are listed in Table 11. Responses to exceptions are described below, and summarized in Table 13.

If both T1 and T0 are set to a logic ‘1’ state, an invalid axis selection exception will be reported by the device.

3.2.1 Device response

Device response depends upon exception conditions which may be present at the time the transfer takes place. In case of multiple exceptions, the exception class of highest priority will determine response.

Table 13. Device response, exception conditions

Exception			Command		Response					Priority
Class	**ST**	**HOLD**	**T1**	**T0**	**S2**	**S1**	**S0**	**Register**	**Acceleration data**	
Transient	X	X	X	X	1	1	1	Status code	Status code	Highest
Reset	X	X	T1	T0	1	1	1	As requested	$7FF	—
Critical	X	X			1	1	1			—
Behavioral	1	1			0	T1	T0		As requested	—
	1	0			1	T1	T0			—
	0	1			1	T1	T0			—
None	0	0			0	T1	T0			Lowest

S: Self-test active

Commands and response under normal and exception conditions are summarized in the following tables. Note that only DEVCTL at address $0E is writable when the device is in its normal operating mode.

Table 14. Normal response summary

Operation		Bit															
		15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Acceleration data read	Command	T1	T0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Response	0	T1	T0	P	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0
Register pointer read	Command	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Response	0	0	0	0	0	P	0	0	A7	A6	A5	A4	A3	A2	A1	A0
Register pointer write	Command	0	0	0	1	0	P	0	0	A7	A6	A5	A4	A3	A2	A1	A0
	Response	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Register data read	Command	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Response	0	0	0	1	0	P	0	0	D7	D6	D5	D4	D3	D2	D1	D0
Register data write	Command	0	0	1	1	0	P	0	0	D7	D6	D5	D4	D3	D2	D1	D0
	Response	0	0	0	1	1	P	0	0	A7	A6	A5	A4	A3	A2	A1	A0

P: Parity
T[1:0]: Transfer type code

Note that only DEVCTL is writable when the device operates in normal operating mode. Attempts to write other registers do not constitute a fault condition, but have no effect.

Table 15. Behavioral response summary, one exception condition

Operation		Bit															
		15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Acceleration data read	Command	T1	T0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Response	1	$\overline{T1}$	$\overline{T0}$	P	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0
Register pointer read	Command	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Response	1	1	1	0	0	P	0	1	A7	A6	A5	A4	A3	A2	A1	A0
Register pointer write	Command	0	0	0	1	0	P	0	0	A7	A6	A5	A4	A3	A2	A1	A0
	Response	1	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0
Register data read	Command	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Response	1	1	1	1	0	P	0	1	D7	D6	D5	D4	D3	D2	D1	D0
Register data write	Command	0	0	1	1	0	P	0	0	D7	D6	D5	D4	D3	D2	D1	D0
	Response	1	1	1	1	1	P	0	1	A7	A6	A5	A4	A3	A2	A1	A0

P: Parity
T[1:0]: Transfer type code

Behavioral exception conditions exist if self-test is active or the $\overline{CAP}$/HOLD input is in a logic-high state. MMA6910KQ will respond as shown in Table 15 if either exception condition exists. If both exception conditions are true, response is as shown in Table 14.

Table 16. Critical/reset exception response detail

Operation		Bit															
		15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Acceleration data read	Command	T1	T0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Response	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
Register pointer read	Command	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Response	1	1	1	0	0	P	1	0	Register address							
Register pointer write	Command	0	0	0	1	0	P	0	0	Register address							
	Response	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0
Register data read	Command	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Response	1	1	1	1	0	P	1	0	Register data							
Register data write	Command	0	0	1	1	0	P	0	0	Register data							
	Response	1	1	1	1	1	P	1	0	Register address							

P: Parity
T[1:0]: Transfer type code

A special case exists if an internal oscillator fault is detected. This critical error condition results in D_{OUT} being driven high continuously while $\overline{CS}$ is asserted, as detailed in Section 3.1.1.2.

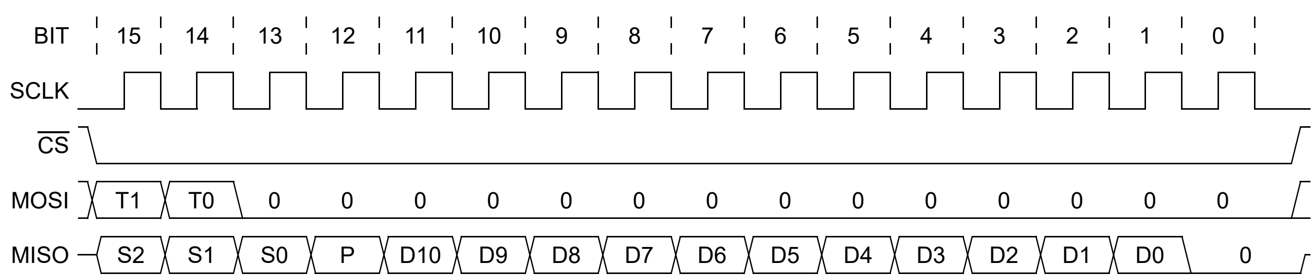
Table 17. Transient exception response detail

Operation		Bit															
		15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Acceleration data read	Command	T1	T0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Response	1	1	1	P	Reserved value (refer to Table 18)											0
Register pointer read	Command	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Response	1	1	1	0	0	P	1	1	Status code							
Register pointer write	Command	0	0	0	1	0	P	0	0	Register address							
	Response	1	1	1	0	1	P	1	1	Status code							
Register data read	Command	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Response	1	1	1	1	0	P	1	1	Status code							
Register data write	Command	0	0	1	1	0	P	0	0	Register data							
	Response	1	1	1	1	1	P	1	1	Status code							

P: Parity
T[1:0]: Transfer type code

3.2.2 Acceleration data transfer

The format of an acceleration data transfer is illustrated in Figure 12. Response to acceleration data transfers is summarized in Table 18. Note that a number of reserved values are defined to indicate error exceptions. The MMA6910KQ will produce signed or unsigned data depending upon the state of the SD bit in the DSPCFG register, as described in Section 2.1.4.



T[1:0] Transfer type code
S[2:0]: Status code

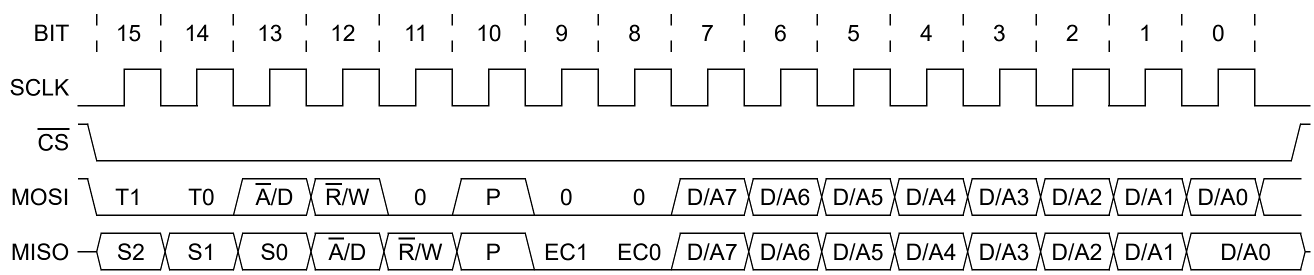
Figure 12. Communications protocol, acceleration data transfer

Table 18. Range of output, communications protocol

11-bit data value		Definition
Unsigned		
Decimal	Hexidecimal	
2047	7FF	Critical/Reset exception value
2046	7FE	Invalid axis selection
2045	7FD	Internal signal path overflow
2044	7FC	Over-range value
2043	7FB	Maximum positive signal level
• • •		• • •
1024	400	Zero signal level
• • •		• • •
5	005	Minimum negative signal level
4	004	Under-range value
3	003	Internal signal path underflow
2	002	SPI clock fault
1	001	D_{IN} parity fault
0	000	Reserved value

3.2.3 Register operations

Register operations involve four transfer types: register pointer write or read, and register data write or read. The basic format for register operations is illustrated in Figure 13. Response from MMA6910KQ under normal conditions is illustrated. Specific details for each transfer type are provided in the command/response summaries provided in Section 3.2.1.



T[1:0] Transfer type code
S[2:0]: Status code
$\overline{A}$/D: $\overline{ADDRESS}$/DATA
$\overline{R}$/W: $\overline{READ}$/WRITE
EC[1:0]: Exception class (refer to Table 3-9 below)
D/A[7:0]: Data or address, depending upon transfer type and status

Figure 13. Communications protocol, register operations

Table 19. Exception class encoding

EC1	EC0	Exception class
0	0	No exception
0	1	Behavioral (one exception)
1	0	Critical/Reset
1	1	Transient

3.3 Representation

Table 20. Nominal 11-bit, acceleration, data values

11-bit, unsigned, digital value	Nominal acceleration (3.5g range)
2047	Critical/Reset exception value
2046	Invalid axis selection
2045	Overflow
2044	Overrange
2043	+3.50g
2042	+3.50g
2041	+3.49g
• • •	• • •
1027	+10.3 mg
1026	+6.87 mg
1025	+3.43 mg
1024	0g
1023	-3.43 mg
1022	-6.87 mg
1021	-10.3 mg
• • •	• • •
7	-3.49g
6	-3.50g
5	-3.50g
4	Under range
3	Underflow
2	SPI clock fault
1	D_{IN} parity fault
0	Reserved

3.3.1 Over-range response

Positive acceleration levels which exceed the full-scale range of the device fall into two categories: over-range and overflow. Over-range conditions exist when the signal level is beyond the full-scale range of the device, but within the computational limits of the DSP. An overflow condition occurs if the output of the low-pass filter equals or exceeds the maximum digital value which can be output from the sinc filter. Sinc-filter saturation will occur before the internal data path width is exceeded. At 25 °C and OVLD = 0, the sinc filter will not saturate at sustained acceleration levels with the range of ±200g. The DSP operates predictably under all cases of over-range responses, although the signal may include residual, high-frequency components for some time after returning to the normal range of operation, due to non-linear effects of the sensor. If an overflow condition occurs, the signal is internally clipped. The DSP will recover from an overflow condition within a few sample times after the input signal returns to the input range of the DSP. Due to internal clipping within the DSP, some high-frequency artifacts may be present in the output, following an overflow condition.

For negative acceleration levels, corresponding under-range and underflow conditions are defined.

3.4 $\overline{\text{CAP}}$/HOLD input

The $\overline{\text{CAP}}$/HOLD input provides a system-level synchronization mechanism. When driven high, transfer of acceleration results from the DSP to the SPI buffers does not occur. The DSP continues its normal operation regardless of the state of $\overline{\text{CAP}}$/HOLD. Data read from the device — when $\overline{\text{CAP}}$/HOLD is high — will reflect the last values available from the DSP at the time of the signal transition.

4 Operating Modes

4.1 Startup reset

Upon application of voltage at the V_{CC} pin, the internal regulators will begin driving the internal power supply rails. The C_{REG} and C_{REGA} pins are tied to the internal rails. As voltages at V_{CC}, C_{REG} and C_{REGA} rise, the device becomes operational. An internal reset signal is asserted at this time. Separate comparators monitor all three voltages, and when all are above specified thresholds, the reset signal is negated and the device begins its initialization process.

4.2 Device initialization

Following any reset, the device completes a sequence of operations which initialize internal circuitry. Device initialization is completed in two phases. During the first phase, the fuse array is read and its contents are transferred to mirror registers. Power to the fuse array is then removed to reduce supply-current load. A voltage reference used within the sensor interface stabilizes during the second phase. If the HPFSEL bit is set in the DSP configuration register (DSPCFG), the high-pass filter is also initialized during phase two.

The device will not respond to SPI accesses during initialization phase one. Acceleration results are not available during initialization phase two, however the SPI is functional and register operations may be performed. If an acceleration data access is attempted, the device will respond with non-acceleration data. The specific response depends upon the communications protocol selected.

The first initialization phase requires approximately 800 µs to complete. The second phase completes in approximately 3.0 ms if no high-pass filter is selected and 200 ms if the HPFSEL bit is programmed to a logic ‘1’ state. The DEVINIT bit in the device status register (DEVSTAT) remains set following reset, until the second phase of device initialization completes.

Following completion of the device initialization, the DEVRES bit in DEVSTAT may be cleared by writing a logic ‘1’ value to CE in DEVCTL. This operation will clear the device reset exception. Once cleared, register operations may be completed or acceleration data values may be read from the device in any desired sequence.

5 Performance Specification

5.1 Maximum ratings

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it. The device contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table below. Keep input and output voltages within the range $V_{SS} \leq V \leq V_{CC}$.

Rating	Symbol	Value	Unit	
Supply voltage	V_{CC}	-0.3 to +7	V	(1)
C_{REG}, C_{REGA}, C_{REF}	V_{REG}	-0.3 to +3	V	(1)
V_{PP}	V_{REG}	-0.3 to +11	V	(1)
SCLK, $\overline{CS}$, D_{IN}, $\overline{CAP}$/HOLD, PCM_X, PCM_Y	V_{IN}	-0.3 to V_{CC} + 0.3	V	(1)
D_{OUT} (high-impedance state)	V_{IN}	-0.3 to V_{CC} + 0.3	V	(1)
Current drain per pin excluding V_{CC} and V_{SS}	I	10	mA	(1)
Powered shock (six sides, 0.5 ms duration)	g_{pms}	±1500	g	(1)
Unpowered shock (six sides, 0.5 ms duration)	g_{shock}	±2000	g	(1)
Drop shock (to concrete surface)	h_{DROP}	1.2	m	(1)
Electrostatic discharge Human Body Model (HBM) Charge Device Model (CDM) Machine Model (MM)	 V_{ESD} V_{ESD} V_{ESD}	 ±2000 ±500 ±200	 V V V	 (1) (1) (1)
Storage temperature range	T_{stg}	-40 to +125	°C	(1)

1. Verified by characterization, not tested in production.

5.2 Operating range

The operating ratings are the limits normally expected in the application and define the range of operation.

Characteristic	Symbol	Min	Typ	Max	Units	
Supply voltage Standard operating voltage, 3.3V operating range Standard operating voltage, 5.0V operating range	 V_{CC} V_{CC}	V_L +3.15 +4.75	 +3.3 +5.0	V_H +3.45 +5.25	 V V	 (1) (1)
Operating temperature range	T_A	T_L -40	—	T_H +105	°C	(2)

1. Characterized at all values of V_L and V_H. Production test is conducted at typical voltage unless otherwise noted.
2. Parameters tested 100% at final test.

5.3 Electrical characteristics

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $|\Delta T_A| < 4.0$ k/min. unless otherwise specified.

Characteristic	Symbol	Min	Typ	Max	Units	Note
Supply current drain						
V_{CC} = 5.25 V, t_S = 64 µs *	I_{DD}	—	—	8.0	mA	(1)
Startup reset threshold						
V_{CC} (see Figure 14)	V_{POR_N}	2.77	—	3.15	V	(2)
C_{REG}	V_{POR_N}	1.80	—	2.32	V	(2)
C_{REGA}	V_{POR_N}	2.18	—	2.50	V	(2)
C_{REF}	V_{POR_N}	1.11	—	1.29	V	(2)
Startup reset threshold						
V_{CC} (see Figure 14)	V_{POR_A}	2.77	—	2.95	V	(2)
C_{REG}	V_{POR_A}	1.80	—	2.10	V	(2)
C_{REGA}	V_{POR_A}	2.18	—	2.31	V	(2)
C_{REF}	V_{POR_A}	1.11	—	1.19	V	(2)
Internally regulated voltages						(1)
C_{REG} *	V_{DD}	2.42	2.50	2.58	V	(1)
C_{REGA}(3) *	$V_{2.5}$	2.42	2.50	2.58	V	(1)
C_{REF} *	V_{REF}	1.20	1.25	1.29	V	(1)
External filter capacitor (C_{REG}, C_{REGA})						
Value	C_{REG}	800	1000		nF	(2)
ESR (including interconnect resistance)	ESR	—	—	200	mΩ	(2)
Power supply coupling		—	—	0.004	digit/mv	(2)
Nonlinearity	NL_{OUT}	-1.0	—	1.0	% FSR	(2)
Noise (1.0 Hz-1.0 kHz)	n_{SD}	—	—	140	$\mu g/\sqrt{Hz}$	(2)
Sensitivity						
3.5g range *	SENS	—	3.43	—	mg/digit	(1)
Sensitivity error						
3.5g range *	ΔSENS	-3.0	—	+3.0	%	(1)
Offset at 0g						
11-bit unsigned data *	D_{OUT}	—	1024	—	digit	(1)
Absolute Offset error						
T_A = 25°C *	ΔD_{OUT}	-10.2	—	+10.2	digit	(1)
-40°C ≤ T_A ≤ +105°C *	ΔD_{OUT}	-20.4	—	+20.4	digit	(1)
Variation from measured Absolute Offset error						
-40°C ≤ T_A ≤ +85°C *	$\Delta\Delta D_{OUT}$	-10.2	—	+10.2	digit	(1)
-40°C ≤ T_A ≤ +105°C	$\Delta\Delta D_{OUT}$	-14.6	—	+14.6	digit	(1)

1. Parameters tested 100% at final test.
2. Verified by characterization, not tested in production.
3. Tested at $V_{CC} = V_L$ and $V_{CC} = V_H$.

* Indicates a Freescale critical characteristic.

Electrical characteristics (continued)

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $|\Delta T_A| < 4$ K/min unless otherwise specified.

Characteristic	Symbol	Min	Typ	Max	Units	Note
Range of output						
11-bit data, unsigned						
Normal	RANGE	5	—	2043	digit	(1)
Critical fault value	CFU	—	2047	—	digit	(1)
Invalid axis selection	IAU	—	2046	—	digit	(1)
Positive acceleration over-flow code	OF_U	—	2045	—	digit	(1)
Positive acceleration over-range code	OR_U	—	2044	—	digit	(1)
Negative acceleration under-range code	UR_U	—	4	—	digit	(1)
Negative acceleration under-flow code	UF_U	—	3	—	digit	(1)
SPI clock fault	SCFU	—	2	—	digit	(1)
DIN parity fault	PFU	—	1	—	digit	(1)
Unused code	UNUSED	—	0	—	digit	(1)
Output value on overrange						
11-bit data: 2043						
3.5g range	g_{OVER}	+3.22	+3.50	+3.79	g	(2)
11-bit data: 5						
3.5g range	g_{UNDER}	-3.79	-3.50	-3.22	g	(2)
Maximum acceleration without saturation of internal circuitry (OVLD = 0)	g_{SAT}	< -12	—	> +12	g	(2)
Self-test output change[3]						
$T_A = 25°C$ *	ΔST	472	525	578	mg	(4)
$-40° \leq T_A \leq 105°C$ *	ΔST	437	525	630	mg	(4)
Cross-axis sensitivity						
V_{ZX}	V_{ZX}	-3	—	+3	%	(2)
V_{YX}	V_{YX}	-3	—	+3	%	(2)
V_{ZY}	V_{ZY}	-3	—	+3	%	(2)
Output high voltage						
D_{OUT} (I_{Load} = -100 μA)	V_{OH}	0.85	—	—	V_{CC}	(5)
Output low voltage						
$D_{OUT,}$ (I_{Load} = 100 μA)	V_{OL}	—	—	0.1	V_{CC}	(5)
Output loading (D_{OUT})						
Load resistance	Z_{OUT}	47	—	—	kΩ	(2)
Load capacitance	C_{OUT}	—	—	35	pF	(2)
Input high voltage						
$\overline{\text{CS}}$/RESET, SCLK, D_{IN}, $\overline{\text{CAP}}$/HOLD	V_{IH}	0.65	—	—	V_{CC}	(5)
High impedance leakage current						
D_{OUT}, Input voltage = V_{CC} or V_{SS}	I_{IL}	-3	—	+3	μA	(4)
Input low voltage						
$\overline{\text{CS}}$/RESET, SCLK, D_{IN}, $\overline{\text{CAP}}$/HOLD	V_{IL}	—	—	0.2	V_{CC}	(5)
Input current						
High (at V_{IH})						
SCLK, D_{IN}, $\overline{\text{CAP}}$/HOLD	I_{IH}	-30	-50	-260	μA	(5)
V_{PP} (internal pulldown resistor)	R_{IN}	190	270	350	kΩ	(5)
Low (at V_{IL})						
$\overline{\text{CS/RESET}}$	I_{IL}	30	50	260	μA	(5)

1. Functionality verified 100% via scan. timing characteristic is directly determined by internal oscillator frequency.
2. Verified by characterization, not tested in production.
3. Self-test deflection is trimmed in positive direction. Deflection in negative direction is approximately equal in magnitude.
4. Parameters tested 100% at final test.
5. Parameters tested 100% at unit probe.

* Indicates a Freescale critical characteristic.

5.4 Control timing

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $|\Delta T_A| < 4$ K/min unless otherwise specified.

Characteristic	Symbol	Min	Typ	Max	Units	
DSP low-pass filter cutoff frequency	$f_{C(LPF)}$	47.5	50.0	52.5	Hz	(1)
Filter order	O_{LPF}		2		1	(1)
Startup recovery time						
POR negated to $\overline{CS}$ low	t_{OP}	—	—	840	µs	(1)
Power applied to X_{OUT}, Y_{OUT} valid	t_{XY}	—	—	15	ms	(2)
Internal oscillator frequency	f_{OSC}	3.8	4.0	4.2	MHz	(2)
Clock monitor threshold	f_{MON}	3.6	—	4.4	MHz	(1)
Chip select to internal reset (see Figure 15)	t_{CSRES}	486	512	538	µs	(1)
Serial interface timing (See Figure 16)						
Clock period	t_{SCLK}	120	—	—	ns	(3)
CS asserted to SCLK high	t_{CSCLK}	60	—	—	ns	(3)
Data setup time	t_{DC}	20	—	—	ns	(3)
Data hold time	t_{CDIN}	10	—	—	ns	(3)
SCLK low to data out	t_{CDOUT}	—	—	50	ns	(3)
SCLK high to CS negated	t_{CHCSH}	60	—	—	ns	(3)
CS negated to CS asserted	t_{CSN}	600	—	—	ns	(3)
Sensing element natural frequency	f_n	—	3	—	kHz	(3)
Sense element bandwidth (-3.0 dB)	BW_{GCELL}	—	1.2	—	kHz	(3)

1. Functionality verified 100% via scan. timing characteristic is directly determined by internal oscillator frequency.
2. Parameters tested 100% at final test.
3. Verified by characterization, not tested in production.

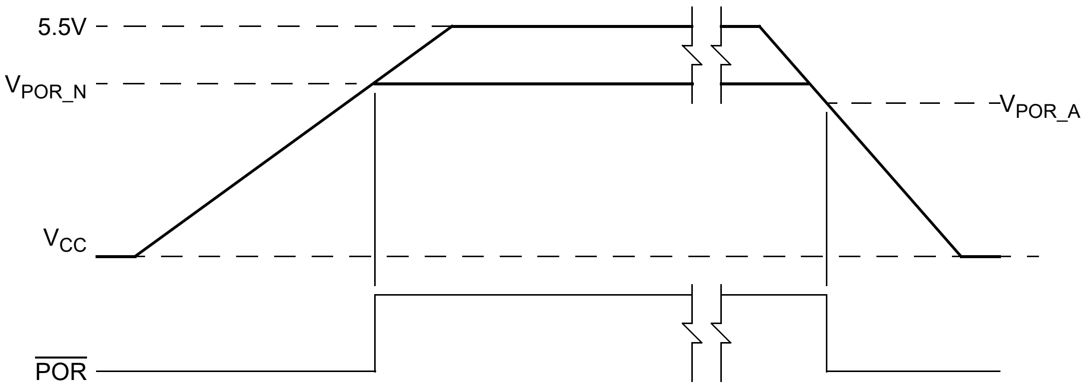


Figure 14. Startup timing

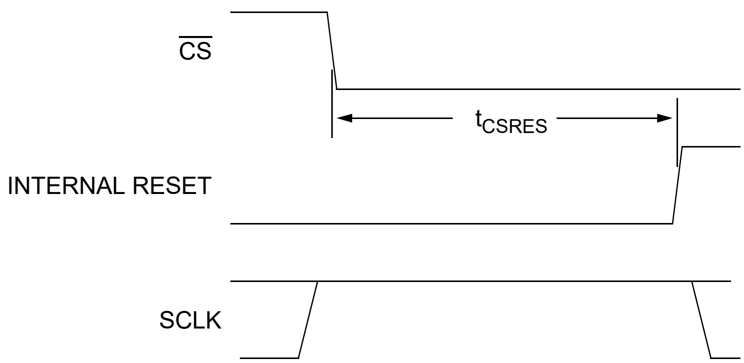


Figure 15. CS/RESET timing

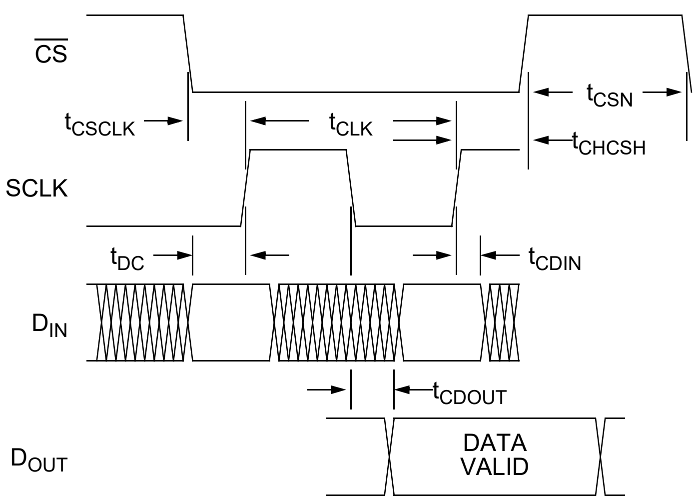
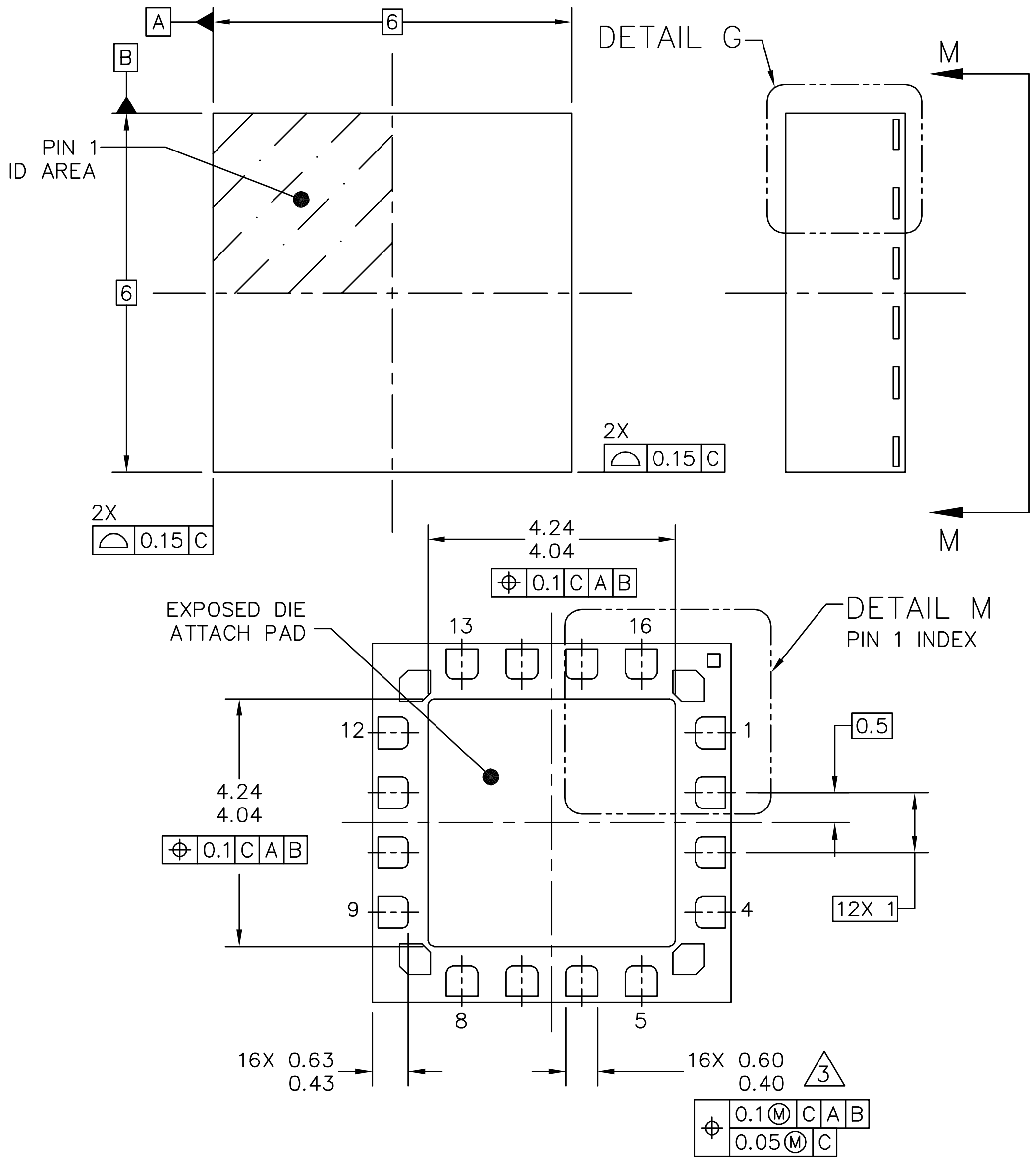


Figure 16. Serial interface timing

6 Package Dimension

The following documents provide a case outline drawing and information regarding printed wiring board mounting for the MMA6910KQ device. For the most current package revision, visit **www.freescale.com** and perform a keyword search using the "98A" listed below. The board mounting application note **AN3111** is also located on the Freescale website.



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TITLE: QUAD FLAT NON–LEADED PACKAGE (QFN) FOR SENSORS 16 TERMINAL, 1.0 PITCH (6 X 6 X 1.98)	DOCUMENT NO: 98ASA10571D	REV: C
	CASE NUMBER: 1477–02	10 SEP 2007
	STANDARD: NON–JEDEC	

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ISSUE C
CASE 1477-02
16-LEAD QFN

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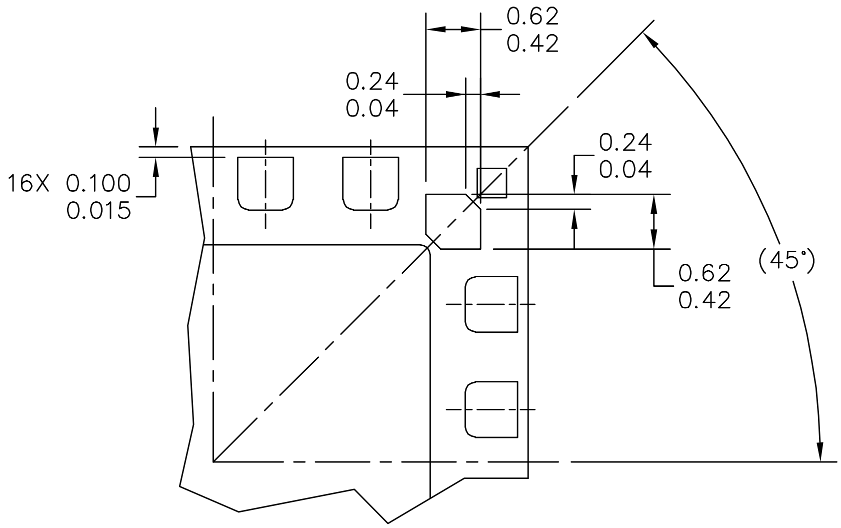
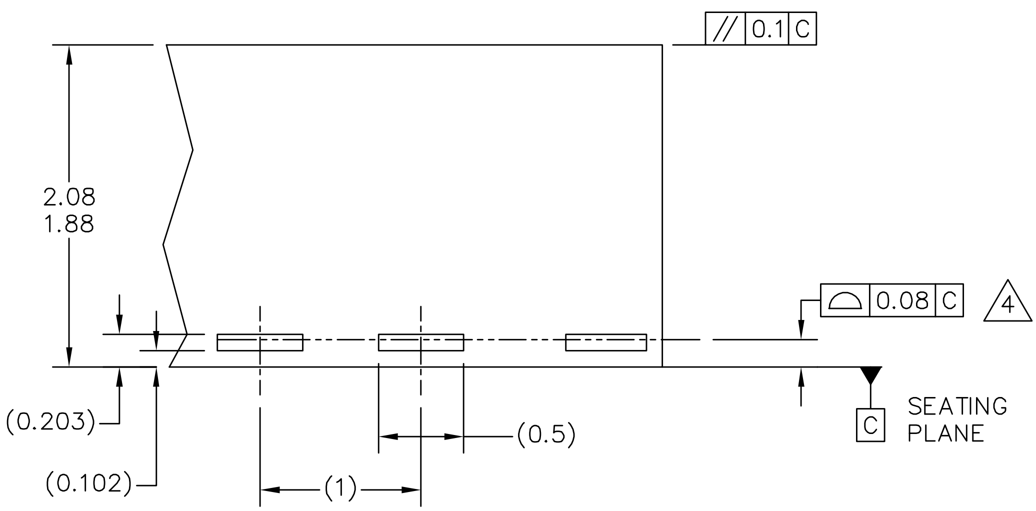


DETAIL M



DETAIL G
VIEW ROTATED 90° CW

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TITLE: QUAD FLAT NON-LEADED PACKAGE (QFN) FOR SENSORS 16 TERMINAL, 1.0 PITCH (6 X 6 X 1.98)	DOCUMENT NO: 98ASA10571D	REV: C PAGE 2 OF 3
	CASE NUMBER: 1477-02	10 SEP 2007
	STANDARD: NON-JEDEC	

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NOTES:

1. ALL DIMENSIONS ARE IN MILLMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25MM AND 0.30MM FROM TERMINAL TIP.

4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG, TERMINALS AND CORNER PADS.

5. RADIUS ON TERMINAL IS OPTIONAL.

6. MINIMUM METAL GAP SHOULD BE 0.2MM EXCEPT GAP BETWEEN CORNER PADS AND THE EXPOSED HEAT SLUG.

<table>
<tr><td colspan="2"></td><td>MECHANICAL OUTLINE</td><td colspan="2">PRINT VERSION NOT TO SCALE</td></tr>
<tr><td rowspan="3">TITLE:</td><td rowspan="3">QUAD FLAT NON-LEADED PACKAGE (QFN) FOR SENSORS 16 TERMINAL, 1.0 PITCH (6 X 6 X 1.98)</td><td colspan="2">DOCUMENT NO: 98ASA10571D</td><td>REV: C</td></tr>
<tr><td colspan="2">CASE NUMBER: 1477-02</td><td>10 SEP 2007</td></tr>
<tr><td colspan="3">STANDARD: NON-JEDEC</td></tr>
</table>

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Appendix A Digital Filter Characteristics

Response curves for filter options are provided in this appendix.

A.1 Sinc filter characteristics

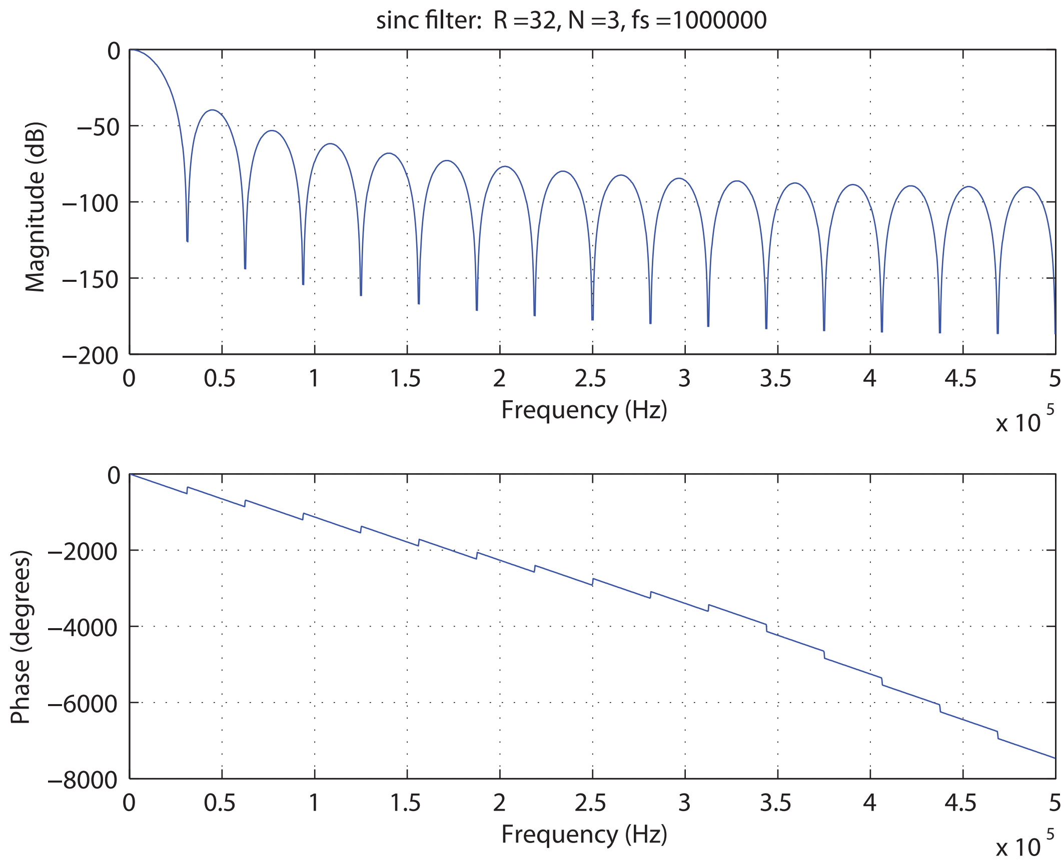

Figure 17. Sinc filter response

A.2 Low-pass filter characteristics

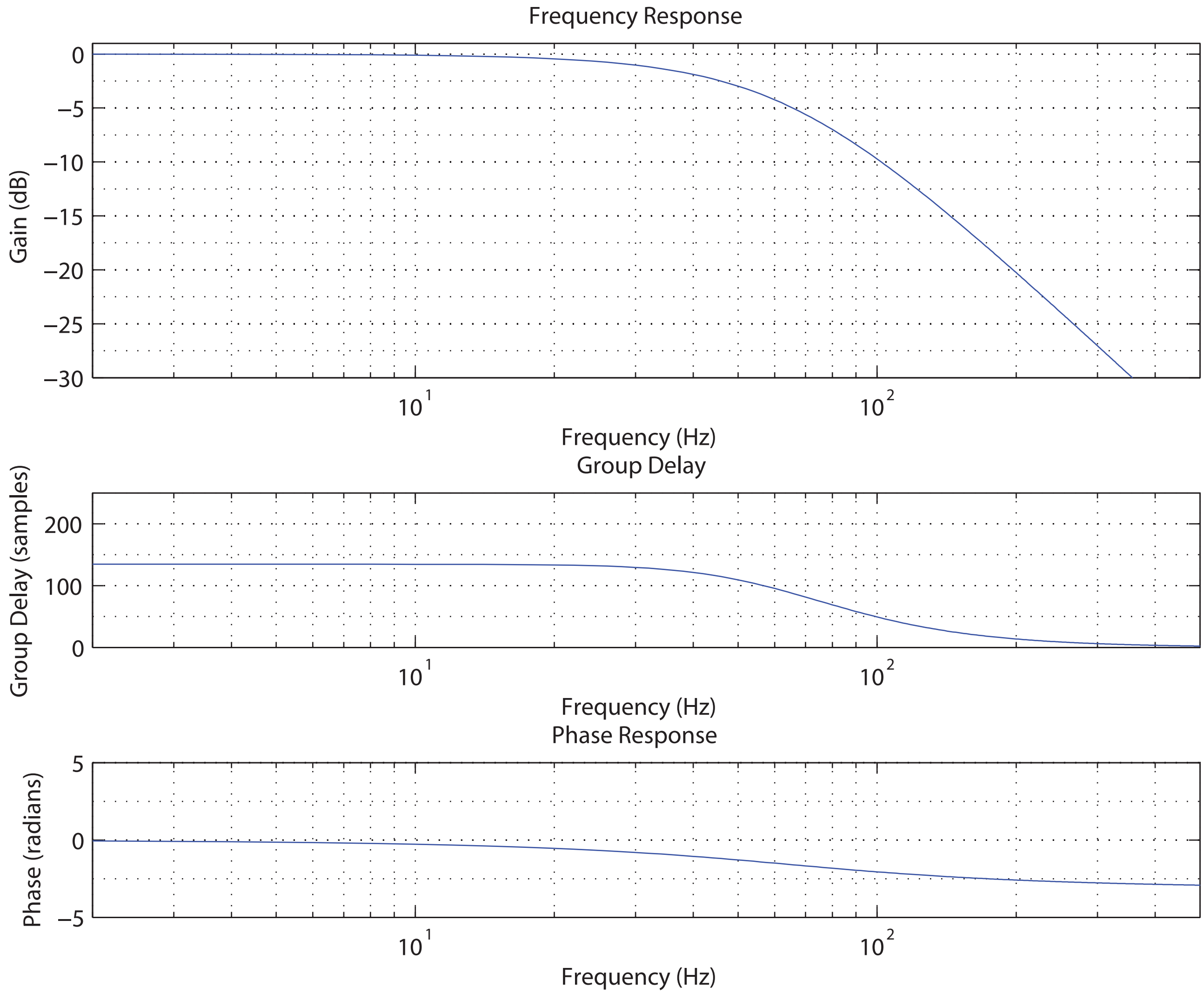

Figure 18. Low-pass filter, f_c = 50 Hz, poles = 2

7 Revision History

Table 21. Revision history

Revision number	Revision date	Description of changes
0	08/2012	• Initiated new data sheet.
1	08/2012	• Table 2: Corrected Addr $0A and $0B bits 7 and 6 from 0 and 1 to 1 and 0.
2	10/2015	• Removed Xtrinsic logo. • Updated shipping on ordering information for device MMA6910KQ from “Tubes” to “Trays”. • Section 2.1: Table 1, Changed row $0E, Bit 3 was HPFB to Unused. • Section 2.1.3: Table 4, Changed row $0E, Bit 3 was HPFB to Unused. • Section 2.1.3.4: Changed High-Pass Filter Bypass (HPFB) to Unused and updated paragraph of description. • Section 2.1.3.6: Removed sentence “When ST0 is set,...the high-pass filter frozen” and replaced with “The high-pass filter is disabled”. • Section 2.1.5.4: Deleted “Except when communication protocol is active,” from paragraph. • Section 2.12: First sentence, replaced “correction operations” with “compensation operations”. • Section 2.12.1: Deleted second paragraph. • Section 3.1.1.7: Removed “the expected number for the selected communications protocol” from first bullet and replaced with “16”. • Section 3.1.1.9: Deleted section (HOLD condition) • Section 3.1.1.9 (previously section 3.1.1.10) Deleted “condition, if a HOLD condition exists or self-test is activated” and replaced with “is enabled. Behavioral Conditions include the HOLD condition and Self-Test Activation”. • Section 4: Deleted first paragraph • Section 4.1, Deleted section (Normal operating mode) • Section 5.3: Electrical characteristics table, Startup reset threshold rows, moved figure 14 reference to V_{CC} only. Deleted Hysteresis characteristic row. Removed footnote 5, “Verified by Characterization. Conformance guaranteed to 20 ppm”. • Section 5.4: Corrected Serial interface timing row was “SCLK high to data out” to “SCLK low to data out”. • Appendix A: Updated figure title for figures 17 and 18, removed “t_C= 32 µs".

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10/2015