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Advance Information

MPC850/850SE PowerPC® Integrated Microprocessor Technical Summary

The MPC850 microprocessor is a versatile, one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It is a low-cost implementation of the MPC860 that provides an effective price/performance along with system enhancements for communications, such as universal serial bus (USB) support. The MPC850 integrates a high-performance embedded PowerPC core with a communication processor module (CPM) that uses a specialized RISC processor for communications. The CPM of the MPC850 supports six serial channels—one serial communication controller (SCC), one universal serial bus channel (USB), two serial management controllers (SMCs), one I^2C port, and one serial peripheral interface (SPI). The CPM of the MPC850SE (single ethernet) is the same except that USB support has been removed and the SCC has been optimized only to support ethernet. This two-processor architecture is more efficient than traditional architectures because the CPM off-loads peripheral tasks from the embedded PowerPC core.

Note that all information in this document applies to both MPC850 and MPC850SE, unless otherwise specified.

To locate any published errata or updates for this document, refer to the website at http://www.mot.com/SPS/RISC/netcomm.

1.1 Features

The following list summarizes the main features of the MPC850:

- Embedded PowerPC core provides 66 MIPS (using Dhrystone 2.1) or 115 K (Dhrystone 2.1) at 50 MHz
  - Single-issue, 32-bit version of the PowerPC core (fully compatible with the PowerPC architecture definition) with 32- x 32-bit fixed-point registers
  - Less than 180 mW (typical) at 25 MHz, 2.2-V internal, 3.3-V I/O boundary with microprocessor core, caches, memory management, and I/O in operation
  - Performs branch folding and branch prediction with conditional prefetch, but without conditional execution
  - 2-Kbyte instruction cache and 1-Kbyte data cache
  - Instruction and data caches are two-way, set associative, physical address, 4-word line burst, LRU replacement algorithm, lockable on-line granularity
  - Memory management units with 8-entry translation lookaside buffers (TLBs) and fully-associative instruction and data TLBs
  - Memory management units support multiple page sizes of 4 Kbytes, 16 Kbytes, 512 Kbytes, and 8 Mbytes (1-Kbyte protection granularity at the 4-Kbyte page size); 16 virtual address spaces and 8 protection groups
- Advanced on-chip emulation debug mode
- Data bus dynamic bus sizing for 8-, 16-, and 32-bit buses
  - Supports traditional 68-Kbyte big-endian, traditional x86 little-endian, and PowerPC little-endian memory systems
  - Twenty-six external address lines
- Completely static design (0- to 50-MHz operation)
- Communication processor module
  - Interfaces to PowerPC core through on-chip dual-access RAM and virtual (serial) DMA channels on a dedicated DMA accelerator
  - Programmable memory-to-memory and memory-to-I/O (including Flyby) DMA provided by virtual DMA support
  - Protocols supported by ROM or download microcode; and the single hardware serial communication controller include, but are not limited to, the digital portions of:
    - Ethernet/IEEE 802.3 (CS/CDMA) (applies to MPC850 and MPC850SE)

    The following protocols pertain only to the MPC850:

    - HDLC/SDLC™ and HDLC bus
    - Appletalk
    - Signaling system #7 (RAM microcode option)
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART (USART)
    - Binary synchronous communications (BiSync)
    - Totally transparent mode with/without CRC
    - Asynchronous HDLC

  - IrDA version 1.1 serial infrared
  - Basic rate ISDN (BRI) in conjunction with serial management controller channels
  - Primary rate ISDN
- 16- x 16-bit multiply-accumulate hardware (MAC)
  - One operation per clock. Two-clock latency, one-clock blockage.
  - MAC operates concurrently with other instructions
  - Uses DMA controller to burst data directly into register file without interaction from the PowerPC core
- 5-Kbyte dual-port RAM
- Ten serial DMA (SDMA) channels
- 32-bit, Harvard architecture, scalar RISC controller
- Communication-specific commands
- Supports continuous mode transmission and reception on all serial channels
- Each serial channel can have its own pins (nonmultiplexed serial interface mode)

- Four baud rate generators
  - Independent and can be connected to any serial communication controller or serial management controller
  - Allows changes during operation
  - Autobaud support option
- One serial communication controller (SCC)
  - Ethernet/IEEE 802.3 optional on the serial communication controller (full 10-Mbps support)
  - GeoPort support
  - HDLC bus implements an HDLC-based local area network
  - Universal asynchronous receiver transmitter
  - Synchronous UART
  - Synchronous BiSync
  - Serial infrared (IrDA) supporting a maximum of 4 Mbps
  - Totally transparent. Frame-based with optional cyclical redundancy check.
  - Maximum serial data rate of 22 Mbps
- One dedicated high-speed serial channel for the universal serial bus (USB) (pertains only to the MPC850)
  - Supports USB slave mode at a maximum of 12 Mbps with four USB endpoints: one for control and three for data
- Two serial management controllers. Only one has dedicated pins and the other can be connected to the time slot assigner.
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division multiplexed (TDM) channels

- One serial peripheral interface
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- One I^2C® port
  - Supports master and slave modes
  - Supports multimaster environments
- One time slot assigner
  - Allows serial communication controllers and serial management controllers to be used in multiplexed and/or nonmultiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, Frame Syncs, and clocking
  - Allows dynamic changes
  - Can be internally connected to four serial channels
- General-purpose timers
  - Two 16-bit timers or one 32-bit timer
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - Eight port pins with interrupt capability
  - Ten internal interrupt sources
  - Programmable highest-priority request
- Memory controller (eight banks)
  - Can be programmed to support almost any memory interface
  - Each bank can be a chip-select or $\overline{RAS}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM single in-line memory modules, static random-access memory, electrically programmable read-only memory, Flash EPROM
  - Four $\overline{CAS}$ lines, four $\overline{WE}$ lines, and one $\overline{OE}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes, 32 Kbyte to 256 Mbyte
  - Selectable write protection
  - On-chip bus arbitration supports external bus master
  - Special features for burst mode support

- System integration unit
  - Hardware bus monitor
  - Spurious interrupt monitor
  - Software watchdog
  - Periodic interrupt timer
  - Low-power stop mode
  - Clock synthesizer
  - PowerPC decrementer
  - PowerPC time base
  - Real-time clock
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Single socket PCMCIA-ATA interface
  - Master interface, release 2.1 compliant
  - Single PCMCIA socket
  - Eight memory or I/O windows can be allocated between sockets
- Low-power support
  - Full high: all units fully powered at high clock frequency
  - Full low: all units fully powered at low clock frequency
  - Doze: core functional units disabled except time base, decrementer, PLL, memory controller, real-time clock, and communication processor module in low-power standby
  - Sleep: all units disabled except real-time clock and periodic interrupt timer. PLL is active for fast wake-up
  - Deep sleep: all units disabled including PLL, but not the real-time clock and periodic interrupt timer
  - Low-power stop
  - Separate power supply input to operate internal logic at 2.2 V when operating at or below 25 MHz
  - Can be dynamically shifted between high frequency (3.3 V internal) and low frequency (2.2 V internal) operation
- Debug interface
  - Eight comparators. Four operate on instruction address, two operate on data address, and two operate on data
  - Supports =, ≠, <, and > conditions
  - Each watchpoint can generate a breakpoint internally
- 3.3-V operation with TTL compatibility on I/O pins
- 256-pin ball grid array (BGA)

1.2 Architecture Overview

The MPC850 integrates a high-performance embedded PowerPC core with high-performance, low-power peripherals and extends the Motorola family of microprocessors into cost-sensitive, high-volume communications and networking products.

The MPC850 adopts a dual-processor architecture providing a high-performance, general-purpose RISC integer processor, an embedded PowerPC core for application programming use, and a special-purpose 32-bit scalar RISC communication processor module. The peripherals are uniquely designed for communication requirements; they are capable of providing embedded signal processing functions for communications and user interface enhancements as well as the I/O support needed for high-speed digital communications. As shown in Figure 1, the MPC850 consists of three modules. Each module interfaces to the 32-bit internal bus.

- Embedded PowerPC core
- Communication processor module
- System interface unit

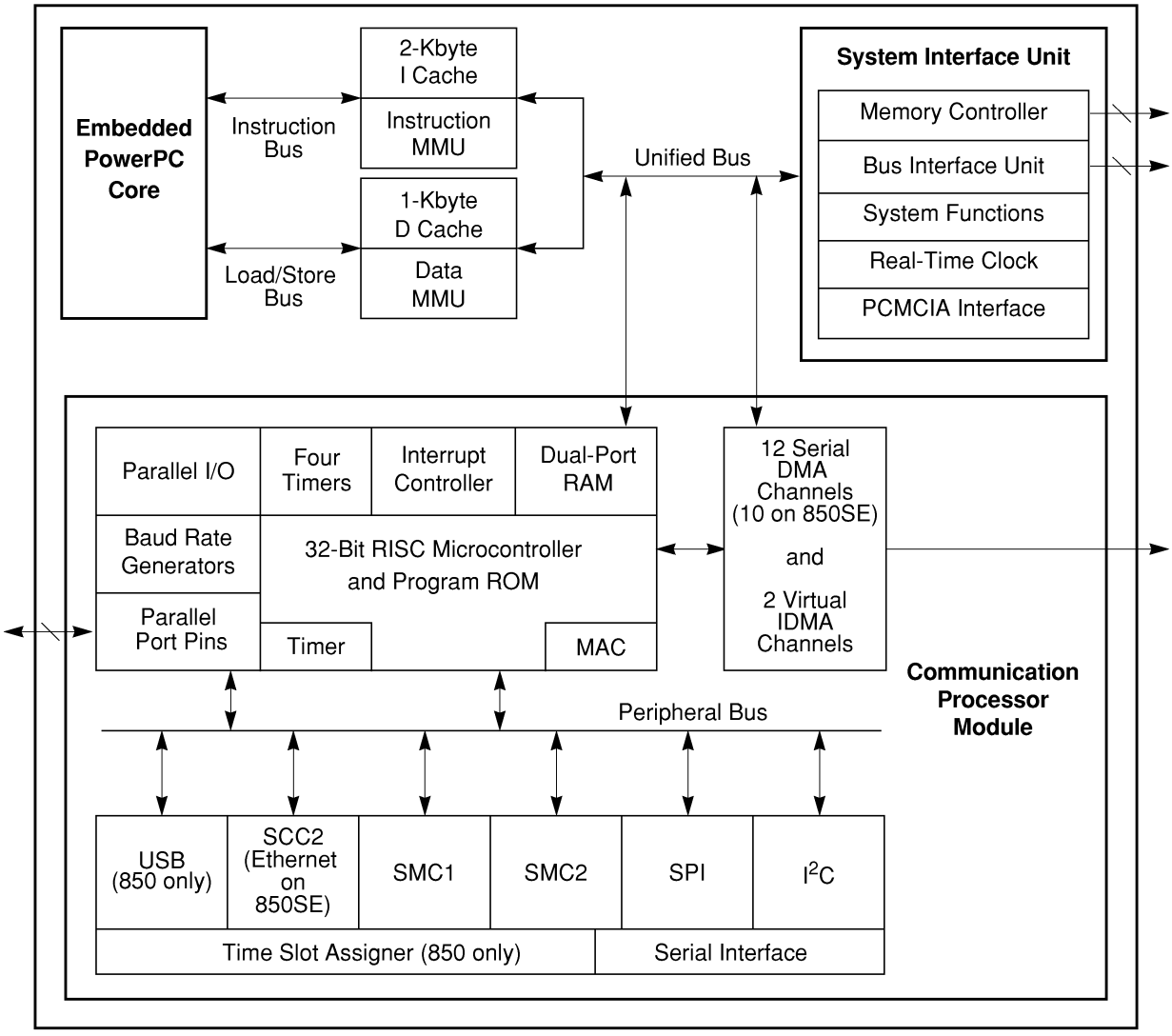

Figure 1. MPC850 Microprocessor Block Diagram

1.2.1 Embedded PowerPC Core

The PowerPC core is compliant with the PowerPC architecture definition. It has a fully-static design that consists of three functional blocks—integer block, hardware multiplier/divider, and load/store block. It executes all integer and load/store operations directly on the hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. Its interface to the internal and external buses is 32 bits. The core uses a two-instruction load/store queue, four-instruction prefetch queue, and a six-instruction history buffer. The core performs branch folding and branch prediction with conditional prefetch, but without conditional execution. The core can operate on 32-bit external operands with one bus cycle. The PowerPC integer block supports 32- x 32-bit fixed-point general-purpose registers. It can execute one integer instruction on each clock cycle. Each element in the integer block is only clocked when valid data is present in the data queue ready for operation, which reduces the amount of power consumed to the amount needed to perform an operation.

The PowerPC processor is integrated with the memory management units and 2-Kbyte instruction and 1-Kbyte data caches. The memory management units (MMUs) provide an 8-entry, fully-associative instruction and data TLB, with multiple page sizes of 4 Kbytes (1-Kbyte protection), 16 Kbytes, 512 Kbytes, and 8 Mbytes. It supports 16 virtual address spaces with eight protection groups. Three special registers are available as scratch registers to support software tablewalk and update.

The instruction cache is 2 Kbytes, two-way, set associative with physical addressing. It allows single-cycle access on hit with no added latency for miss. It has four words per line and supports burst linefill using an LRU replacement algorithm. The cache can be locked on a line basis for application critical routines. The data cache is 1 Kbyte, two-way, set associative with physical addressing. It allows single-cycle access on hit with one added clock latency for miss. It has four words per line and supports burst linefill using an LRU replacement algorithm. The cache can be locked on a line basis for application critical routines and can be programmed to support copy-back or write-through via the memory management unit. The inhibit mode can be programmed per MMU page.

The PowerPC processor with its instruction and data caches can deliver approximately 66 MIPS at 50 MHz (using Dhrystone 2.1) or 115 K Dhrystones, based on the assumption that it is issuing one instruction per cycle with a cache hit rate of 94%.

1.2.2 Communication Processor Module

The communication processor module (CPM) has features that allow the MPC850 to excel in communications and networking products. These features are divided into three blocks:

- Embedded DSP
- Communication processor
- Twelve serial DMA channels (ten on the 850SE) and two independent DMA channels

The embedded DSP function of the MPC850 allows the communication processor module to execute imaging algorithms in parallel with the PowerPC core for maximum performance and minimum power consumption. The DSP executes one 16 x16 MAC every cycle. It has preprogrammed filtering functions like IIR, FFT, and imaging functions for JPEG image compression and decompression. These functions are also used by modem and speech recognition programs.

The communication processor module provides the communication features of the MPC850. It includes a RISC processor with multiply accumulate (MAC) hardware, one serial communication controller (SCC), two serial management controllers (SMCs), one dedicated serial channel for the universal serial bus (USB), one interprocessor-integrated circuit (I^2C) port, one serial peripheral interface (SPI), 5-Kbyte dual-port RAM, an interrupt controller, a time-slot assigner, and four independent baud rate generators.

Twelve serial DMA channels on the MPC850 support the SCC, SMCs, USB channel, SPI, and I^2C. The MPC850SE, without USB support, has ten serial DMA channels. The IDMAs provide two channels of general-purpose DMA capability for each communication channel. They offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic. The RISC controller can access the IDMA registers directly in the buffer chaining modes.

1.2.3 System Interface Unit

Although the PowerPC core is always a 32-bit device internally, it can be configured to operate with an 8-, 16- or 32-bit data bus. Regardless of the choice of the system bus size, dynamic bus sizing is supported, which allows 8-, 16-, and 32-bit peripherals and memory to coexist on the 32-bit system bus. The system interface unit supports traditional 68-Kbyte big-endian memory systems, traditional x86 little-endian memory systems, and PowerPC little-endian memory systems. It also provides power management functions, reset control, a PowerPC decrementer, PowerPC time base, and real-time clock.

The memory controller supports up to eight memory banks with glueless interfaces to DRAM, SRAM, PSRAM, EPROM, Flash EPROM, SRDRAM, EDO and other peripherals with two-clock initial access to external SRAM and bursting support. It provides variable block sizes from 32 Kbytes to 256 Mbytes. The memory controller provides 0 to 15 wait states for each bank of memory and can use address type matching to qualify each memory bank access. It provides four byte-enable signals for varying width devices, one output enable signal, and one boot chip-select available at reset.

The DRAM interface supports 8-, 16-, and 32-bit ports. It uses a programmable state machine to support almost any memory interface. Memory banks can be defined in depths of 256 Kbytes, 512 Kbytes, 1 Mbyte, 2 Mbytes, 4 Mbytes, 8 Mbytes, 16 Mbytes, 32 Mbytes, or 64 Mbytes for all port sizes. In addition, the memory depth can be defined as 64 Kbytes and 128 Kbytes for 8-bit memory or 128 Mbytes and 256 Mbytes for 32-bit memory. The DRAM controller supports page mode access for successive transfers within bursts. The MPC850 supports a glueless interface to one bank of DRAM, while external buffers are required for additional memory banks. The refresh unit provides $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, a programmable refresh timer, refresh active during external reset, disable refresh modes, and stacking for a maximum of seven refresh cycles.

The PCMCIA-ATA interface is a master controller that is compliant with release 2.1. The interface supports one independent PCMCIA socket with external transceivers or buffers required. It provides eight memory or I/O windows that can be allocated to the socket. If the PCMCIA port is not being used as a card interface, it can be used as a general-purpose input with interrupt capability.

1.3 Power Management

The MPC850 supports a wide range of power management features including full-high, full-low, doze, sleep, deep-sleep, and low-power stop. In full-high mode, the MPC850 is fully powered with all internal units operating at the full speed of the processor. Full-low mode is the same as full-high, but operates at a lower frequency. There is a gear mode determined by a clock divider that allows the operating system to reduce the operational frequency of the processor.

Doze mode disables core functional units except the time base, decrementer, PLL, memory controller, real-time clock, and places the communication processor module in low-power standby mode. Sleep mode is the next lower power mode that disables everything except the real-time clock and periodic interrupt timer, thus leaving the PLL active for quick wake-up. The deep-sleep mode then disables the PLL for lower power, but slower wake-up. Low-power stop disables all logic in the processor except the minimum logic required to restart the device, and provides the lowest power consumption but requires the longest wake-up time.

1.4 System Debug Support

The MPC850 contains an advanced debug interface that provides superior debug capabilities without causing any degradation in the speed of operation. It supports six watchpoint pins that can be combined with eight internal comparators, four of which operate on the effective address on the address bus. The other four comparators are split—two comparators operate on the effective address on the data bus and two comparators operate on the data on the data bus. The MPC850 can compare using the =, ≠, <, and > conditions to generate watchpoints. Each watchpoint can then generate a breakpoint that can be programmed to trigger in a programmable number of events.

1.5 Differences between MPC860 and MPC850/850SE

The following list outlines how theMPC850/850SE integrated microprocessors differ from the MPC860.

- 256-lead plastic BGA package
- One SCC instead of four (MPC850)
- One ethernet channel vs. four SCCs (MPC850SE)
- One USB (12-Mbyte slave) port is added (MPC850)
- Smaller caches (2-Kbyte instruction cache and 1-Kbyte data cache)
- Smaller MMUs (eight entries instead of 32)
- Only one PCMCIA slot is supported
- Only one TDM port is supported (TDM_a)
- PIP (Centronics™ port) is not supported
- SMC2 is not connected to its own pins; it is usable only through TSA.

1.6 Ordering Information

Table 1 identifies the packages and operating frequencies available for the MPC850.

Table 1. MPC850 and MPC850SE Package/Frequency Availability

Package Type	Frequency (MHz)	Temperature	Order Number	
			MPC850	MPC850SE
Ball grid array (ZT suffix)	0–25	0° C to 70° C	XPC850ZT25	XPC850SEZT25
Ball grid array (ZT suffix)	0–40	0° C to 70° C	XPC850ZT40	XPC850SEZT40
Ball grid array (ZT suffix)	0–50	0° C to 70° C	XPC850ZT50	XPC850SEZT50
Ball grid array (CZT suffix)	TBD	–40° C to 85° C	—	TBD

The documents listed in Table 2 contain detailed information on the MPC850. These documents can be obtained from the Literature Distribution Centers at the addresses listed on the back page. Visit the website at http://www.mot.com/SPS/RISC/netcomm and http://www.mot.com/SPS/powerpc/ for more information.

Table 2. Documentation

Document Title	Order Number	Contents
MPC850 user's manual	TBD	Detailed information for design
PowerPC Microprocessors Family: The Programming Environments for 32-Bit Microprocessors	MPCFPE32B/AD	PowerPC programmer's reference and instruction set
The embedded PowerPC source	TBD	Independent vendor listing supporting software and development tools

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