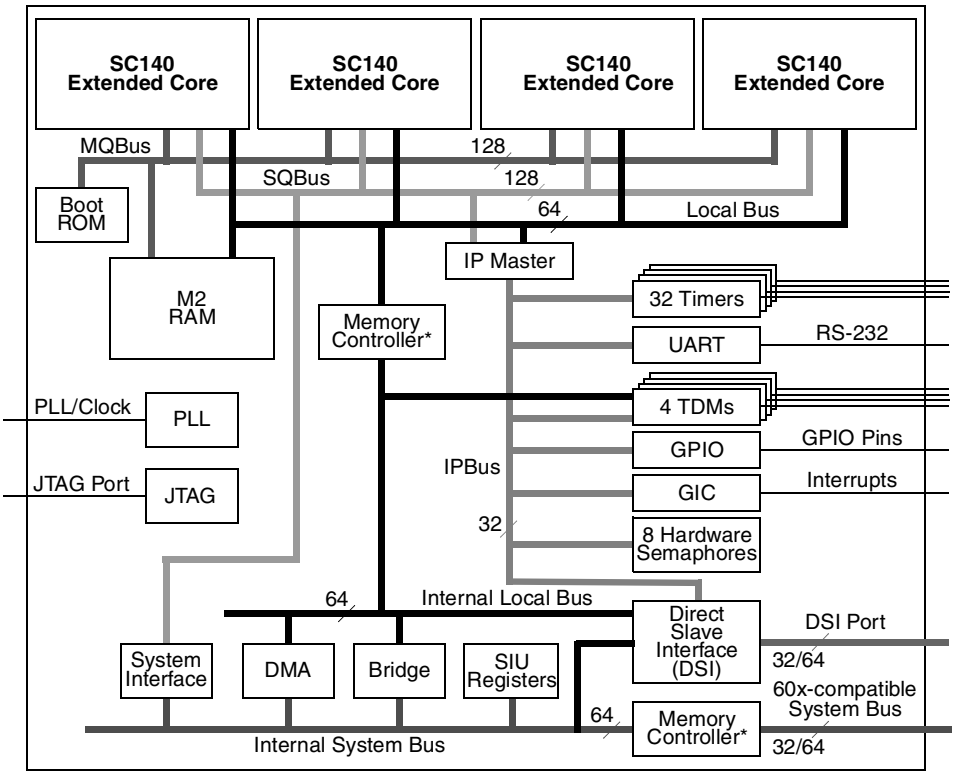
MSC8102

Quad Core 16-Bit Digital Signal Processor



*There is a single memory controller that controls access to both the local bus and the system bus.

Figure 1. MSC8102 Block Diagram

The raw processing power of this highly integrated system-on-a-chip device enables developers to create next-generation networking products that offer tremendous channel densities, while maintaining system flexibility, scalability, and upgradeability. The MSC8102 is offered in two core speed levels: 250 and 275 MHz.

What's New?

Rev. 12 includes the following changes:

- New **Section 2.5.2** adds start-up sequence timing.

The MSC8102 is a highly integrated system-on-a-chip that combines four StarCore™ SC140 extended cores with an RS-232 serial interface, four time-division multiplexed (TDM) serial interfaces, thirty-two general-purpose timers, a flexible system interface unit (SIU), and a multi-channel DMA engine. The four extended cores can deliver a total 4400 DSP MMACS performance at 275 MHz. Each core has four arithmetic logic units (ALUs), internal memory, a write buffer, and two interrupt controllers. The MSC8102 targets high-bandwidth highly computational DSP applications and is optimized for wireless transcoding and packet telephony as well as high-bandwidth base station applications. The MSC8102 delivers enhanced performance while maintaining low power dissipation and greatly reducing system cost.

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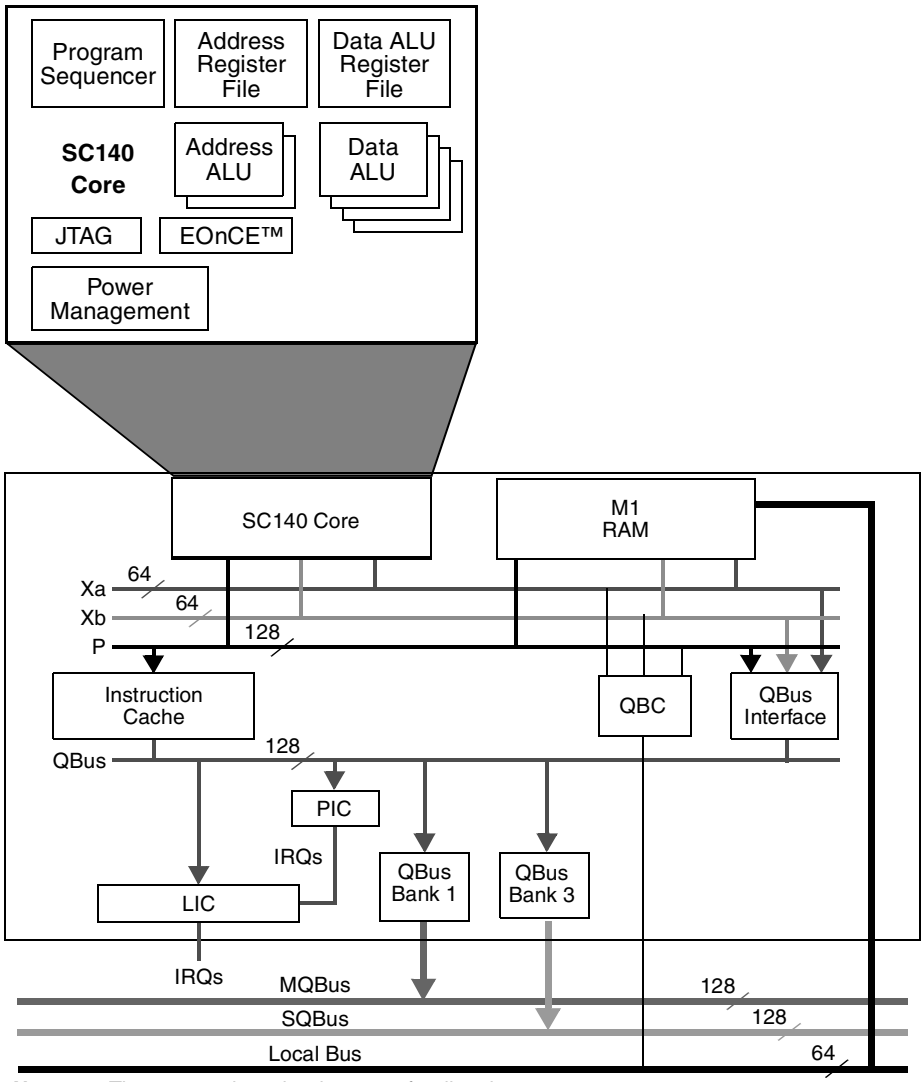
Data Sheet Conventions

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
“asserted”	Means that a high true (active high) signal is high or that a low true (active low) signal is low
“deasserted”	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.



Notes: 1. The arrows show the data transfer direction.
2. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

Figure 2. SC140 Extended Core Block Diagram

Features

The tables in this section list the features of the MSC8102 device.

Table 1. Extended SC140 Cores and Core Memories

Feature	Description
SC140 Core	Four SC140 cores: • Up to 4400 MMACS using 16 ALUs running at up to 275 MHz. • A total of 1436 KB of internal SRAM (224 KB per core). Each SC140 core provides the following: • Up to 1100 MMACS using an internal 275 MHz clock at 1.6 V. A MAC operation includes a multiply-accumulate command with the associated data move and pointer update. • 4 ALUs per SC140 core. • 16 data registers, 40 bits each. • 27 address registers, 32 bits each. • Hardware support for fractional and integer data types. • Very rich 16-bit wide orthogonal instruction set. • Up to six instructions executed in a single clock cycle. • Variable-length execution set (VLES) that can be optimized for code density and performance. • IEEE 1149.1 JTAG port. • Enhanced on-device emulation (EOnCE) with real-time debugging capabilities.
Extended Core	Each SC140 core is embedded within an extended core that provides the following: • 224 KB M1 memory that is accessed by the SC140 core with zero wait states. • Support for atomic accesses to the M1 memory. • 16 KB instruction cache, 16 ways. • A four-entry write buffer that frees the SC140 core from waiting for a write access to finish. • External cache support by asserting the global signal (GBL) when predefined memory banks are accessed. • Program Interrupt Controller (PIC). • Local Interrupt Controller (LIC).

Multi-Core Shared Memories	• M2 memory (shared memory):
	  • A 476 KB memory working at the core frequency.
	  • Accessible from the local bus
	  • Accessible from all four SC140 cores using the MQBus.
	• 4 KB bootstrap ROM.

M2-Accessible Multi-Core Bus (MQBus)	• A QBus protocol multi-master bus connecting the four SC140 cores to the M2 memory. • Data bus access of up to 128-bit read and up to 64-bit write. • Operation at the SC140 core frequency. • A central efficient round-robin arbiter controlling SC140 core access on the MQBus. • Atomic operation control of access to M2 memory by the four SC140 cores and the local bus.

Table 2. Phase-Lock Loop (PLL)

Feature	Description
Internal PLL	• Generates up to 275 MHz core clock and up to 91.67 MHz bus clocks for the 60x-compatible local and system buses and other modules. • PLL values are determined at reset based on configuration signal values.

Table 3. Buses and Memory Controller

Feature	Description
Dual-Bus Architecture	Can be configured to a 32-bit data system bus and a 64-bit data direct slave interface (DSI) or to a 64-bit data system bus and 32-bit data DSI.

Table 3. Buses and Memory Controller (Continued)

Feature	Description
60x-Compatible System Bus	• 64/32-bit data and 32-bit address 60x bus. • Support for multiple-master designs. • Four-beat burst transfers (eight-beat in 32-bit wide mode). • Port size of 64, 32, 16, and 8 controlled by the internal memory controller. • Bus can access external memory expansion or off-device peripherals, or it can enable an external host device to access internal resources. • Slave support, direct access by an external host to internal resources including the M1 and M2 memories. • On-device arbitration between up to four master devices.
Direct Slave Interface (DSI)	Provides a 32/64-bit wide slave host interface that operates only as a slave device under the control of an external host processor. • 21 bit address, 32/64-bit data. • Direct access by an external host to on-device resources, including the M1 and the M2 memories. • Synchronous and asynchronous accesses, with burst capability in the synchronous mode. • Dual or Single strobe modes. • Write and Read buffers improves host bandwidth. • Byte enable signals enables 1, 2, 4, and 8 byte write access granularity. • Sliding window mode enables access with reduced number of address pins. • Chip ID decoding enables using one $\overline{CS}$ signal for multiple DSPs. • Broadcast $\overline{CS}$ signal enables parallel write to multiple DSPs. • Big-endian, little-endian, and munged little-endian support.

Memory Controller	Flexible eight-bank memory controller:
	• Three user-programmable machines (UPMs), general-purpose chip-select machine (GPCM), and a page-mode SDRAM machine
	• Glueless interface to SRAM, 100 MHz page mode SDRAM, DRAM, EPROM, Flash memory, and other user-definable peripherals.
	• Byte enables for either 64-bit or 32-bit bus width mode.
	• Eight external memory banks (banks 0–7). Two additional memory banks (banks 9, 11) control IPBus peripherals and internal memories. Each bank has the following features:
	  • 32-bit address decoding with programmable mask.
	  • Variable block sizes (32 KB to 4 GB).
	  • Selectable memory controller machine.
	  • Two types of data errors check/correction: normal odd/even parity and read-modify-write (RMW) odd/even parity for single accesses.
	  • Write-protection capability.
	  • Control signal generation machine selection on a per-bank basis.
	  • Support for internal or external masters on the 60x-compatible system bus.
	  • Data buffer controls activated on a per-bank basis.
	  • Atomic operation.
	  • RMW data parity check (on 60x-compatible system bus only).
	  • Extensive external memory-controller/bus-slave support.
	  • Parity byte select pin, which enables a fast, glue less connection to RMW-parity devices (on 60x-compatible system bus only).
	  • Data pipeline to reduce data set-up time for synchronous devices.

Table 4. DMA Controller

Feature	Description

Multi-Channel DMA Controller	• 16 time-multiplexed unidirectional channels.
	• Services up to four external peripherals.
	• Supports $\overline{\text{DONE}}$ or $\overline{\text{DRACK}}$ protocol on two external peripherals.
	• Each channel group services 16 internal requests generated by eight internal FIFOs. Each FIFO generates:
	  • a watermark request to indicate that the FIFO contains data for the DMA to empty and write to the destination
	  • a hungry request to indicate that the FIFO can accept more data.
	• Priority-based time-multiplexing between channels using 16 internal priority levels
	• A flexible channel configuration:
	  • All channels support all features.
	  • All channels connect to the 60x-compatible system bus or local bus.
	• Flyby transfers in which a single data access is transferred directly from the source to the destination without using a DMA FIFO.

Table 5. Serial Interfaces

Feature	Description
Time-Division Multiplexing (TDM)	Up to four independent TDM modules, each with the following features: • Either totally independent receive and transmit, each having one data line, one clock line, and one frame sync line or four data lines, one clock and one frame sync that are shared between the transmit and receive. • Glueless interface to E1/T1 framers and MVIP, SCAS, and H.110 buses. • Hardware A-law/μ-law conversion • Up to 50 Mbps per TDM (50 MHz bit clock if one data line is used, 25 MHz if two data lines are used, 12.5 MHz if four data lines are used). • Up to 256 channels. • Up to 16 MB per channel buffer (granularity 8 bytes), where A/μ law buffer size is double (granularity 16 byte) • Receive buffers share one global write offset pointer that is written to the same offset relative to their start address. • Transmit buffers share one global read offset pointer that is read from the same offset relative to their start address. • All channels share the same word size. • Two programmable receive and two programmable transmit threshold levels with interrupt generation that can be used, for example, to implement double buffering. • Each channel can be programmed to be active or inactive. • 2-, 4-, 8-, or 16-bit channels are stored in the internal memory as 2-, 4-, 8-, or 16-bit channels, respectively. • The TDM transmitter sync signal (TxTSYN) can be configured as either input or output. • Frame sync and data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock. • Frame sync can be programmed as active low or active high. • Selectable delay (0–3 bits) between the Frame Sync signal and the beginning of the frame. • MSB or LSB first support.

Table 5. Serial Interfaces

Feature	Description

UART	• Two signals for transmit data and receive data.
	• No clock, asynchronous mode.
	• Can be serviced either by the SC140 DSP cores or an external host on the 60x-compatible system bus or on the DSI.
	• Full-duplex operation.
	• Standard mark/space non-return-to-zero (NRZ) format.
	• 13-bit baud rate selection.
	• Programmable 8-bit or 9-bit data format.
	• Separately enabled transmitter and receiver.
	• Programmable transmitter output polarity.
	• Two receiver walk-up methods:
	  • Idle line walk-up.
	  • Address mark walk-up.
	• Separate receiver and transmitter interrupt requests.
	• Eight flags, the first five can generate interrupt request:
	  • Transmitter empty.
	  • Transmission complete.
	  • Receiver full.
	  • Idle receiver input.
	  • Receiver overrun.
	  • Noise error.
	  • Framing error.
	  • Parity error.
	• Receiver framing error detection.
	• Hardware parity checking.
	• 1/16 bit-time noise detection.
	• Maximum bit rate 6.25 Mbps.
	• Single-wire and loop operations.

General-Purpose I/O (GPIO) port	• 32 bidirectional signal lines that either serve the peripherals or act as programmable I/O ports. • Each port can be programmed separately to serve up to two dedicated peripherals, and each port supports open-drain output mode.

Table 6. Miscellaneous Modules

Feature	Description
Timers	Two modules of 16 timers each. Each timer has the following features: • Cyclic or one-shot. • Input clock polarity control. • Interrupt request when counting reaches a programmed threshold. • Pulse or level interrupts. • Dynamically updated programmed threshold. • Read counter any time. Watchdog mode for the timers that connect to the device.
Hardware Semaphores	Eight coded hardware semaphores, locked by simple write access without need for read-modify-write mechanism.
Global Interrupt Controller (GIC)	• Consolidation of chip maskable interrupt and non-maskable interrupt sources and routing to $\overline{\text{INT\_OUT}}$, $\overline{\text{NMI\_OUT}}$, and to the cores. • Generation of 32 virtual interrupts (eight to each SC140 core) by a simple write access. • Generation of virtual $\overline{\text{NMI}}$ (one to each SC140 core) by a simple write access.

Table 7. Power and Packaging

Feature	Description
Reduced Power Dissipation	• Low power CMOS design. • Separate power supply for internal logic () and I/O (3.3 V). • Low-power standby modes. • Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent).
Packaging	• 0.8 mm pitch High Temperature Coefficient for Expansion Flip-Chip Ceramic Ball-Grid Array (CBGA (HCTE)). • 431-connection (ball). • 20 mm × 20 mm.

Table 8. Software Support

Feature	Description
Real-Time Operating System (RTOS)	The real-time operating system (RTOS) fully supports device architecture (multi-core, memory hierarchy, ICache, timers, DMA, interrupts, peripherals), as follows: • High-performance and deterministic, delivering predictive response time. • Optimized to provide low interrupt latency with high data throughput. • Preemptive and priority-based multitasking. • Fully interrupt/event driven. • Small memory footprint. • Comprehensive set of APIs. • Fully supports DMA controller, interrupts, and timer schemes.
Multi-Core Support	• Enables use of one instance of kernel code all four SC140 cores. • Dynamic and static memory allocation from local memory (M1) and shared memory (M2).
Distributed System Support	Enables transparent inter-task communications between tasks running inside the SC140 cores and the other tasks running in on-board devices or remote network devices: • Messaging mechanism between tasks using mailboxes and semaphores. • Networking support; data transfer between tasks running inside and outside the device using networking protocols. • Includes integrated device drivers for such peripherals as TDM, UART, and external buses.

Software Support	• Incorporates task debugging utilities integrated with compilers and vendors.
	• Board support package (BSP) for the application development system (ADS).
	• Integrated Development Environment (IDE):
	  • C/C++ compiler with in-line assembly. Enables the developer to generate highly optimized DSP code. It translates code written in C/C++ into parallel fetch sets and maintains high code density.
	  • Librarian. Enables the user to create libraries for modularity.
	  • C libraries. A collection of C/C++ functions for the developer's use.
	  • Linker. Highly efficient linker to produce executables from object code.
	  • Debugger. Seamlessly integrated real-time, non-intrusive multi-mode debugger that enables debugging of highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode.
	  • Simulator. Device simulation models, enables design and simulation before the hardware arrival.
	  • Profiler. An analysis tool using a patented Binary Code Instrumentation (BCI) technique that enables the developer to identify program design inefficiencies.
	  • Version control. CodeWarrior® includes plug-ins for ClearCase, Visual SourceSafe, and CVS.

Boot Options	• External memory. • External host. • UART. • TDM.

Table 9. Application Development System (ADS) Board

Feature	Description

MSC8102ADS	• Host debug through single JTAG connector supports both processors.
	• MSC8101 as the host with both devices on the board. The MSC8101 system bus connects to the DSI.
	• Flash memory for stand-alone applications.
	• Support for the following communications ports:
	  • 10/100Base-T.
	  • 155 Mbit ATM over Optical.
	  • T1/E1 TDM interface.
	  • H.110.
	  • Voice codec.
	  • RS-232.
	  • High-density (MICTOR) logic analyzer connectors to monitor signals
	  • 6U CompactPCI form factor.
	• Emulates DSP farm by connecting to three other ADS boards.

Product Documentation

The documents listed in **Table 10** are required for a complete description of the MSC8102 and are necessary to design properly with the part. Obtain documentation from a local Freescale distributor, Freescale Semiconductor sales office, or a Freescale Literature Distribution Center. For documentation updates, visit the Freescale DSP website shown on the last page of this document.

Table 10. MSC8102 Documentation

Name	Description	Order Number
MSC8102 Technical Data	MSC8102 features list and physical, electrical, timing, and package specifications	MSC8102
MSC8102 User's Guide	User information include system functionality, getting started tutorial, and programming topics	MSC8102UG
MSC8102 Reference Manual	Detailed functional description of the MSC8102 memory and peripheral configuration, operation, and register programming	MSC8102RM
StarCore™ SC140 DSP Core Reference Manual	Detailed description of the SC140 family processor core and instruction set	MNSC140CORE
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the MSC8102 product website

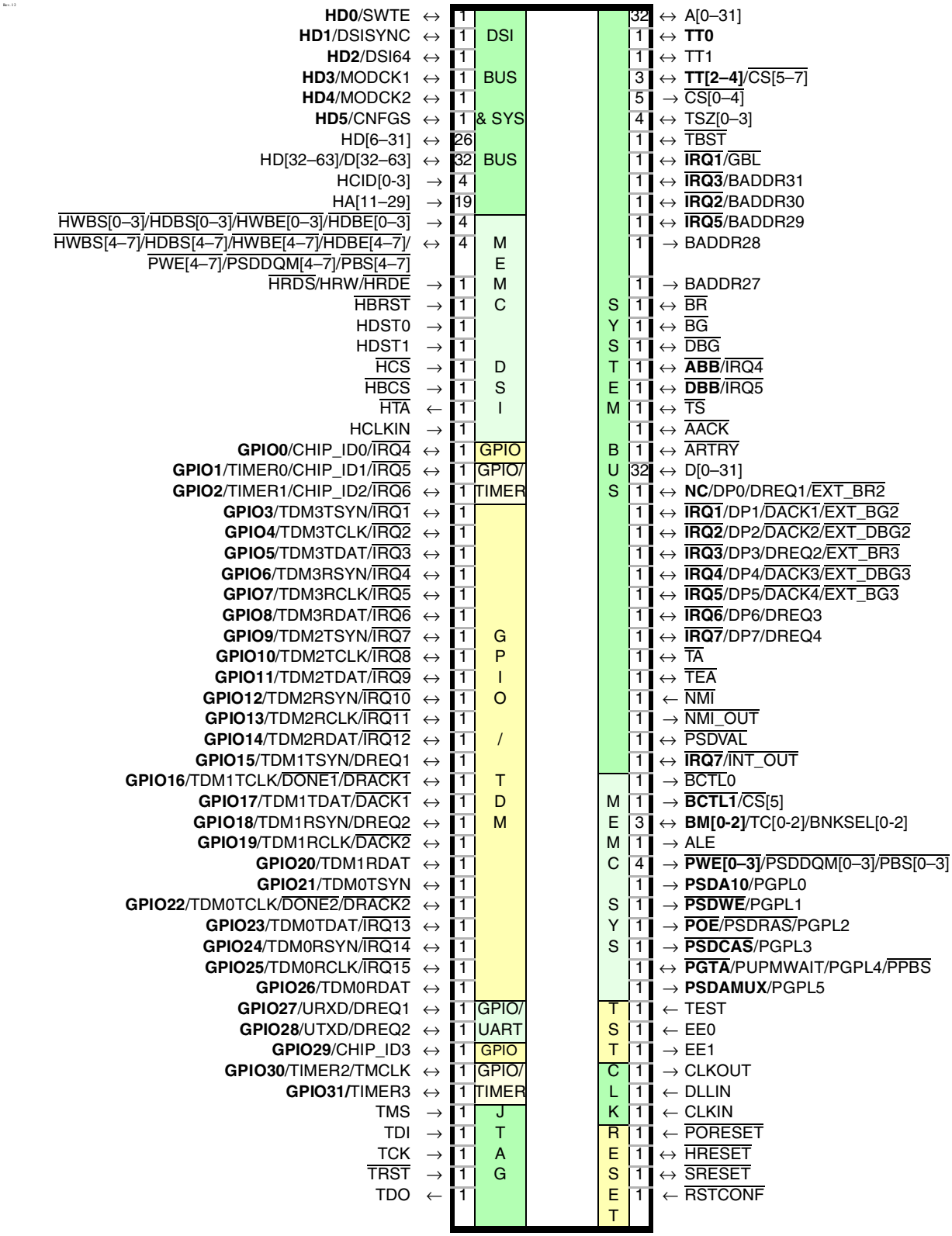
Signals/Connections 1

The MSC8102 external signals are organized into functional groups, as shown in **Table 1-1** and **Figure 1-1**.

Table 1-1 lists the functional groups, the number of signal connections in each group, and references the table that gives a detailed listing of multiplexed signals within each group. **Figure 1-1** shows MSC8102 external signals organized by function.

Table 1-1. MSC8102 Functional Signal Groupings

Functional Group	Number of Signal Connections	Detailed Description
Power (V_{DD}, V_{CC}, and GND)	158	**Table 1-2** on page 1-3
Clock	3	**Table 1-3** on page 1-3
Reset and Configuration	4	**Table 1-4** on page 1-3
DSI, System Bus, and Interrupts	210	**Table 1-5** on page 1-4
Memory Controller	16	**Table 1-6** on page 1-10
General-Purpose Input/Output (GPIO), Time-Division Multiplexed (TDM) Interface, Universal Asynchronous Receiver/ Transmitter (UART), and Timers	32	**Table 1-7** on page 1-12
EOnce and JTAG Test Access Port	7	**Table 1-8** on page 1-18
Reserved (denotes connections that are always reserved)	1	**Table 1-9** on page 1-19



Power signals include: V_{DD}, V_{DDH}, V_{CCSYN}, GND, and GND_{SYN}.

Figure 1-1. MSC8102 External Signals

1.1 Power Signals

Table 1-2. Power and Ground Signal Inputs

Signal Name	Description
V_{DD}	**Internal Logic Power** V_{DD} dedicated for use with the device core. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{DD} power rail.
V_{DDH}	**Input/Output Power** This source supplies power for the I/O buffers. The user must provide adequate external decoupling capacitors.
V_{CCSYN}	**System PLL Power** V_{CC} dedicated for use with the system Phase Lock Loop (PLL). The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
GND	**System Ground** An isolated ground for the internal processing logic and I/O buffers. This connection must be tied externally to all chip ground connections, except GND_{SYN}. The user must provide adequate external decoupling capacitors.
GND_{SYN}	**System PLL Ground** Ground dedicated for system PLL use. The connection should have an extremely low-impedance path to ground.

1.2 Clock Signals

Table 1-3. Clock Signals

Signal Name	Type	Signal Description
CLKIN	Input	**Clock In** Primary clock input to the MSC8102 PLL.
CLKOUT	Output	**Clock Out** The bus clock.
DLLIN	Input	**DLLIN** Synchronizes the internal clocks with an external device. **Note:** When the DLL is disabled, pull this pin low (GND).

1.3 Reset and Configuration Signals

Table 1-4. Reset and Configuration Signals

Signal Name	Type	Signal Description
$\overline{\text{PORESET}}$	Input	**Power-On Reset** When asserted, this line causes the MSC8102 to enter power-on reset state.
$\overline{\text{RSTCONF}}$	Input	**Reset Configuration**[1] Used during reset configuration sequence of the chip. A detailed explanation of its function is provided in the *MSC8102 Reference Manual*. This signal is sampled upon deassertion of $\overline{\text{PORESET}}$.
$\overline{\text{HRESET}}$	Input/ Output	**Hard Reset** When asserted as an input, this signal causes the MSC8102 to enter the hard reset state. When the device is in a hard reset state, it drives the signal as an open-drain output.
$\overline{\text{SRESET}}$	Input/ Output	**Soft Reset** When asserted as an input, this signal causes the MSC8102 to enter the soft reset state. When the device is in a soft reset state, it drives the signal as an open-drain output.
Note: When $\overline{\text{PORESET}}$ is deasserted, the MSC8102 also samples the following signals: • BM[0–2]—Selects the boot mode. • MODCK[1–2]—Selects the clock configuration. • SWTE—Enables the software watchdog timer. • DSISYNC, DSI64, CNFGS, and CHIP_ID[0–3]—Configures the DSI. Refer to **Table 1-5** for details on these signals.		

1.4 Direct Slave Interface, System Bus, and Interrupt Signals

The direct slave interface (DSI) is combined with the system bus because they share some common signal lines. Individual assignment of a signal to a specific signal line is configured through internal registers. **Table 1-5** describes the signals in this group.

Note: Although there are fifteen interrupt request (IRQ) connections to the core processors, there are multiple external lines that can connect to these internal signal lines. After reset, the default configuration enables only $\overline{\text{IRQ}}$[1–7], but includes two input lines each for $\overline{\text{IRQ}}$[1–3] and $\overline{\text{IRQ7}}$. The designer must select one line for each required interrupt and reconfigure the other external signal line or lines for alternate functions. Additional alternate IRQ lines and $\overline{\text{IRQ}}$[8–15] are enabled through the GPIO signal lines.

Table 1-5. DSI, System Bus, and Interrupt Signals

Signal Name	Type	Description
HD0 SWTE	Input/ Output Input	**Host Data Bus 0** Bit 0 of the DSI data bus. **Software Watchdog Timer Disable**. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD1 DSISYNC	Input/ Output Input	**Host Data Bus 1** Bit 1 of the DSI data bus. **DSI Synchronous** Distinguishes between synchronous and asynchronous operation of the DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD2 DSI64	Input/ Output Input	**Host Data Bus 2** Bit 2 of the DSI data bus. **DSI 64** Defines the width of the DSI and SYSTEM Data buses. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD3 MODCK1	Input/ Output Input	**Host Data Bus 3** Bit 3 of the DSI data bus. **Clock Mode 1** Defines the clock frequencies. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD4 MODCK2	Input/ Output Input	**Host Data Bus 4** Bit 4 of the DSI data bus. **Clock Mode 2** Defines the clock frequencies. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD5 CNFGS	Input/ Output Input	**Host Data Bus 5** Bit 5 of the DSI data bus. **Configuration Source** One signal out of two that indicates reset configuration mode. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
HD[6–31]	Input/Output	**Host Data Bus 6–31** Bits 6–31 of the DSI data bus.
HD[32–63] D[32–63]	Input/Output Input/Output	**Host Data Bus 32–63** Bits 32–63 of the DSI data bus. **System Bus Data 32–63** In write transactions, the bus master drives the valid data on this bus. In read transactions, the slave drives the valid data on this bus.

Table 1-5. DSI, System Bus, and Interrupt Signals (Continued)

Signal Name	Type	Description
HCID[0–3]	Input	**Host Chip ID 0–3** Carries the chip ID of the DSI. The DSI is accessed only if $\overline{\text{HCS}}$ is asserted and HCID[0–3] matches the Chip_ID, or if $\overline{\text{HBCS}}$ is asserted.
HA[11–29]	Input	**Host Bus Address 11–29** Used by external host to access the internal address space.
$\overline{\text{HWBS[0–3]}}$	Input	**Host Write Byte Strobes** (In Asynchronous dual mode) One bit per byte is used as a strobe for host write accesses.
$\overline{\text{HDBS[0–3]}}$	Input	**Host Data Byte Strobe** (in Asynchronous single mode) One bit per byte is used as a strobe for host read or write accesses
$\overline{\text{HWBE[0–3]}}$	Input	**Host Write Byte Enable** (In Synchronous dual mode) One bit per byte is used to indicate a valid data byte for host read or write accesses.
$\overline{\text{HDBE[0–3]}}$	Input	**Host Data Byte Enable** (in Synchronous single mode) One bit per byte is used as a strobe enable for host write accesses
$\overline{\text{HWBS[4–7]}}$	Input	**Host Write Byte Strobes** (In Asynchronous dual mode) One bit per byte is used as a strobe for host write accesses.
$\overline{\text{HDBS[4–7]}}$	Input	**Host Data Byte Strobe** (in Asynchronous single mode) One bit per byte is used as a strobe for host read or write accesses
$\overline{\text{HWBE[4–7]}}$	Input	**Host Write Byte Enable** (In Synchronous dual mode) One bit per byte is used to indicate a valid data byte for host write accesses.
$\overline{\text{HDBE[4–7]}}$	Input	**Host Data Byte Enable** (in Synchronous single mode) One bit per byte is used as a strobe enable for host read or write accesses
$\overline{\text{PWE[4–7]}}$	Output	**System Bus Write Enable** Outputs of the bus general-purpose chip-select machine (GPCM). These pins select byte lanes for write operations.
$\overline{\text{PSDDQM[4–7]}}$	Output	**System Bus SDRAM DQM** From the SDRAM control machine. These pins select specific byte lanes of SDRAM devices.
$\overline{\text{PBS[4–7]}}$	Output	**System Bus UPM Byte Select** From the UPM in the memory controller, these signals select specific byte lanes during memory operations. The timing of these pins is programmed in the UPM. The actual driven value depends on the address and size of the transaction and the port size of the accessed device.
$\overline{\text{HRDS}}$	Input	**Host Read Data Strobe** (In Asynchronous dual mode) Used as a strobe for host read accesses.
HRW	Input	**Host Read/Write Select** (in Asynchronous/Synchronous single mode) Host read/write select.
$\overline{\text{HRDE}}$	Input	**Host Read Data Enable** (In Synchronous dual mode) Indicates valid data for host read accesses.
$\overline{\text{HBRST}}$	Input	**Host Burst** The host asserts this pin to indicate that the current transaction is a burst transaction in synchronous mode only.
HDST0	Input	**Host Data structure 0** Defines the data structure of the host access in DSI little-endian mode.
HDST1	Input	**Host Data structure 1** Defines the data structure of the host access in DSI little-endian mode.
$\overline{\text{HCS}}$	Input	**Host Chip Select** DSI chip select. The DSI is accessed only if $\overline{\text{HCS}}$ is asserted and HCID[0–3] matches the Chip_ID.
$\overline{\text{HBCS}}$	Input	**Host Broadcast Chip Select** DSI chip select for broadcast mode. Enables more than one DSI to share the same host chip-select pin for broadcast write accesses.

Table 1-5. DSI, System Bus, and Interrupt Signals (Continued)

Signal Name	Type	Description
$\overline{\text{HTA}}$	Output	**Host Transfer Acknowledge** Upon a read access, indicates to the host when the data on the data bus is valid. Upon a write access, indicates to the host that the data on the data bus was written to the DSI write buffer.
HCLKIN	Input	**Host Clock Input** Host clock signal for DSI synchronous mode.
A[0–31]	Input/Output	**Address Bus** When the MSC8102 is in external master bus mode, these pins function as the system address bus. The MSC8102 drives the address of its internal bus masters and responds to addresses generated by external bus masters. When the MSC8102 is in internal master bus mode, these pins are used as address lines connected to memory devices and are controlled by the MSC8102 memory controller.
TT0	Input/Output	**Bus Transfer Type 0** The bus master drives this pins during the address tenure to specify the type of the transaction.
TT1	Input/Output	**Bus Transfer Type 1** The bus master drives this pins during the address tenure to specify the type of the transaction. Some applications use only the TT1 signal, for example, from MSC8102 to MSC8102 or MSC8102 to MSC8101 and *vice versa*. In these applications, TT1 functions as read/write signal.
TT[2–4] $\overline{\text{CS}}$[5–7]	Input/Output Output	**Bus Transfer Type 2–4** The bus master drives these pins during the address tenure to specify the type of the transaction. **Chip Select 5–7** Enables specific memory devices or peripherals connected to the system bus.
$\overline{\text{CS}}$[0–4]	Output	**Chip Select 0–4** Enables specific memory devices or peripherals connected to the system bus.
TSZ[0–3]	Input/Output	**Transfer Size 0–3** The bus master drives these pins with a value indicating the number of bytes transferred in the current transaction.
$\overline{\text{TBST}}$	Input/ Output	**Bus Transfer Burst** The bus master asserts this pin to indicate that the current transaction is a burst transaction (transfers eight words).
$\overline{\text{IRQ1}}$ $\overline{\text{GBL}}$	Input Output	**Interrupt Request 1**[1] One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. **Global**[1] When a master within the MSC8102 initiates a bus transaction, it drives this pin. Assertion of this pin indicates that the transfer is global and should be snooped by caches in the system.
$\overline{\text{IRQ3}}$ BADDR31	Input Output	**Interrupt Request 3**[1] One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. **Burst Address 31**[1] There are five burst address output pins, which are outputs of the memory controller. These pins connect directly to burstable memory devices without internal address incrementors controlled by the MSC8102 memory controller.
$\overline{\text{IRQ2}}$ BADDR30	Input Output	**Interrupt Request 2**[1] One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core. **Burst Address 30**[1] There are five burst address output pins, which are outputs of the memory controller. These pins connect directly to burstable memory devices without internal address incrementors controlled by the MSC8102 memory controller.

Table 1-5. DSI, System Bus, and Interrupt Signals (Continued)

Signal Name	Type	Description
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5**[1] One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
BADDR29	Output	**Bus Burst Address 29**[1] There are five burst address output pins, which are outputs of the memory controller. These pins connect directly to burstable memory devices without internal address incrementors controlled by the MSC8102 memory controller.
BADDR28	Output	**Burst Address 28** There are five burst address output pins, which are outputs of the memory controller. These pins connect directly to burstable memory devices without internal address incrementors controlled by the MSC8102 memory controller.
BADDR27	Output	**Burst Address 27** There are five burst address output pins, which are outputs of the memory controller. These pins connect directly to burstable memory devices without internal address incrementors controlled by the MSC8102 memory controller.
$\overline{\text{BR}}$	Input/Output	**Bus Request**[2] When an external arbiter is used, the MSC8102 asserts this pin as an output to request ownership of the bus. When the MSC8102 controller is used as an internal arbiter, an external master asserts this pin as an input to request bus ownership.
$\overline{\text{BG}}$	Input/ Output	**Bus Grant**[2] When the MSC8102 acts as an internal arbiter, it asserts this pin as an output to grant bus ownership to an external bus master. When an external arbiter is used, it asserts this pin as an input to grant bus ownership to the MSC8102.
$\overline{\text{DBG}}$	Input/ Output	**Data Bus Grant**[2] When the MSC8102 acts as an internal arbiter, it asserts this pin as an output to grant data bus ownership to an external bus master. When an external arbiter is used, it asserts this pin as an input to grant data bus ownership to the MSC8102.
$\overline{\text{ABB}}$	Input/Output	**Address Bus Busy**[1] The MSC8102 asserts this pin as an output for the duration of the address bus tenure. Following an $\overline{\text{AACK}}$, which terminates the address bus tenure, the MSC8102 deasserts $\overline{\text{ABB}}$ for a fraction of a bus cycle and then stops driving this pin. The MSC8102 does not assume bus ownership as long as it senses this pin is asserted as an input by an external bus master.
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{DBB}}$	Input/Output	**Data Bus Busy**[1] The MSC8102 asserts this pin as an output for the duration of the data bus tenure. Following a $\overline{\text{TA}}$, which terminates the data bus tenure, the MSC8102 deasserts $\overline{\text{DBB}}$ for a fraction of a bus cycle and then stops driving this pin. The MSC8102 does not assume data bus ownership as long as it senses that this pin is asserted as an input by an external bus master.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{TS}}$	Input/Output	**Bus Transfer Start** Assertion of this pin signals the beginning of a new address bus tenure. The MSC8102 asserts this signal when one of its internal bus masters begins an address tenure. When the MSC8102 senses that this pin is asserted by an external bus master, it responds to the address bus tenure as required (snoop if enabled, access internal MSC8102 resources, memory controller support).
$\overline{\text{AACK}}$	Input/ Output	**Address Acknowledge** A bus slave asserts this signal to indicate that it has identified the address tenure. Assertion of this signal terminates the address tenure.
$\overline{\text{ARTRY}}$	Input/ Output	**Address Retry** Assertion of this signal indicates that the bus master should retry the bus transaction. An external master asserts this signal to enforce data coherency with its caches and to prevent deadlock situations.

Table 1-5. DSI, System Bus, and Interrupt Signals (Continued)

Signal Name	Type	Description
D[0–31]	Input/ Output	**Data Bus Bits 0–31** In write transactions, the bus master drives the valid data on this bus. In read transactions, the slave drives the valid data on this bus.
Reserved	Input	The primary configuration selection (default after reset) is reserved.
DP0	Input/Output	**System Bus Data Parity 0** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 0 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 0 and D[0–7].
DREQ1	Input	**DMA Request 1** Used by an external peripheral to request DMA service.
$\overline{\text{EXT\_BR2}}$	Input	**External Bus Request 2** An external master asserts this pin to request bus ownership from the internal arbiter.
$\overline{\text{IRQ1}}$	Input	**Interrupt Request 1** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP1	Input/Output	**System Bus Data Parity** 1 The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 1 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 1 and D[8–15].
$\overline{\text{DACK1}}$	Output	**DMA Acknowledge 1** The DMA drives this output to acknowledge the DMA transaction on the bus.
$\overline{\text{EXT\_BG2}}$	Output	**External Bus Grant 2**[2] The MSC8102 asserts this pin to grant bus ownership to an external bus master.
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP2	Input/Output	**System Bus Data Parity 2** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 2 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 2 and D[16–23].
$\overline{\text{DACK2}}$	Output	**DMA Acknowledge 2** The DMA drives this output to acknowledge the DMA transaction on the bus.
$\overline{\text{EXT\_DBG2}}$	Output	**External Data Bus Grant 2**[2] The MSC8102 asserts this pin to grant data bus ownership to an external bus master.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP3	Input/Output	**System Bus Data Parity 3** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 3 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 3 and D[24–31].
DREQ2	Input	**DMA Request 2** Used by an external peripheral to request DMA service.
$\overline{\text{EXT\_BR3}}$	Input	**External Bus Request 3**[2] An external master should assert this pin to request bus ownership from the internal arbiter.

Table 1-5. DSI, System Bus, and Interrupt Signals (Continued)

Signal Name	Type	Description
IRQ4	Input	**Interrupt Request 4** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP4	Input/Output	**System Bus Data Parity 4** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 4 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 4 and D[32–39].
DACK3	Output	**DMA Acknowledge 3** The DMA drives this output to acknowledge the DMA transaction on the bus.
EXT_DBG3	Output	**External Data Bus Grant 3**[2] The MSC8102 asserts this pin to grant data bus ownership to an external bus master.
IRQ5	Input	**Interrupt Request 5** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP5	Input/Output	**System Bus Data Parity 5** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 5 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 5 and D[40–47].
DACK4	Output	**DMA Acknowledge 4** The DMA drives this output to acknowledge the DMA transaction on the bus.
EXT_BG3	Output	**External Bus Grant 3**[2] The MSC8102 asserts this pin to grant bus ownership to an external bus.
IRQ6	Input	**Interrupt Request 6** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP6	Input/Output	**System Bus Data Parity 6** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 6 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 6 and D[48–55].
DREQ3	Input	**DMA Request 3** Used by an external peripheral to request DMA service.
IRQ7	Input	**Interrupt Request 7** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
DP7	Input/Output	**System Bus Data Parity 7** The agent that drives the data bus also drives the data parity signals. The value driven on the data parity 7 pin should give odd parity (odd number of ones) on the group of signals that includes data parity 7 and D[56–63].
DREQ4	Input	**DMA Request 4** Used by an external peripheral to request DMA service.
TA	Input/Output	**Transfer Acknowledge** Indicates that a data beat is valid on the data bus. For single-beat transfers, TA assertion indicates the termination of the transfer. For burst transfers, TA is asserted eight times to indicate the transfer of eight data beats, with the last assertion indicating the termination of the burst transfer.
TEA	Input/Output	**Transfer Error Acknowledge** Assertion indicates a failure of the data tenure transaction.The masters within the MSC8102 monitor the state of this pin. The MSC8102 internal bus monitor can assert this pin if it identifies a bus transfer that does not complete.

Table 1-5. DSI, System Bus, and Interrupt Signals (Continued)

Signal Name	Type	Description
$\overline{\text{NMI}}$	Input	**Non-Maskable Interrupt** When an external device asserts this line, it generates an non-maskable interrupt in the MSC8102, which is processed internally (default) or is directed to an external host for processing (see $\overline{\text{NMI\_OUT}}$).
$\overline{\text{NMI\_OUT}}$	Output	**Non-Maskable Interrupt Output** An open-drain pin driven from the MSC8102 internal interrupt controller. Assertion of this output indicates that a non-maskable interrupt is pending in the MSC8102 internal interrupt controller, waiting to be handled by an external host.
$\overline{\text{PSDVAL}}$	Input/Output	**Port Size Data Valid** Indicates that a data beat is valid on the data bus. The difference between the $\overline{\text{TA}}$ pin and the $\overline{\text{PSDVAL}}$ pin is that the $\overline{\text{TA}}$ pin is asserted to indicate data transfer terminations, while the $\overline{\text{PSDVAL}}$ signal is asserted with each data beat movement. When $\overline{\text{TA}}$ is asserted, $\overline{\text{PSDVAL}}$ is always asserted. However, when $\overline{\text{PSDVAL}}$ is asserted, $\overline{\text{TA}}$ is not necessarily asserted. For example, if the DMA initiates a double word (2×64 bits) transaction to a memory device with a 32-bit port size, $\overline{\text{PSDVAL}}$ is asserted three times without $\overline{\text{TA}}$ and, finally, both pins are asserted to terminate the transfer.
$\overline{\text{IRQ7}}$	Input	**Interrupt Request 7** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
$\overline{\text{INT\_OUT}}$	Output	**Interrupt Output** Assertion of this output indicates that an unmasked interrupt is pending in the MSC8102 internal interrupt controller.

Notes:
1. See the System Interface Unit (SIU) chapter in the *MSC8102 Reference Manual* for details on how to configure these pins.
2. When used as the bus control arbiter, the MSC8102 can support up to three external bus masters. Each master uses its own set of Bus Request, Bus Grant, and Data Bus Grant signals ($\overline{\text{BR}}$/$\overline{\text{BG}}$/$\overline{\text{DBG}}$, $\overline{\text{EXT\_BR2}}$/$\overline{\text{EXT\_BG2}}$/$\overline{\text{EXT\_DBG2}}$, and $\overline{\text{EXT\_BR3}}$/$\overline{\text{EXT\_BG3}}$/$\overline{\text{EXT\_DBG3}}$). Each of these signal sets must be configured to indicate whether the external master is or is not a MSC8102 master device. See the Bus Configuration Register (BCR) description in the System Interface Unit (SIU) chapter in the *MSC8102 Reference Manual* for details on how to configure these pins. The second and third set of pins is defined by EXT_xxx to indicate that they can only be used with external master devices. The first set of pins ($\overline{\text{BR}}$/$\overline{\text{BG}}$/$\overline{\text{DBG}}$) have a dual function. When the MSC8102 is not the bus arbiter, these signals ($\overline{\text{BR}}$/$\overline{\text{BG}}$/$\overline{\text{DBG}}$) are used by the MSC8102 to obtain master control of the bus.

1.5 Memory Controller Signals

Refer to the Memory Controller chapter in the *MSC8102 Reference Manual* for details on configuring these signals.

Table 1-6. Memory Controller Signals

Signal Name	Type	Description
$\overline{\text{BCTL0}}$	Output	**System Bus Buffer Control 0** Controls buffers on the data bus. Usually used with $\overline{\text{BCTL1}}$. The exact function of this pin is defined by the value of SIUMCR[BCTLC].
$\overline{\text{BCTL1}}$	Output	**System Bus Buffer Control 1** Controls buffers on the data bus. Usually used with $\overline{\text{BCTL0}}$. The exact function of this pin is defined by the value of SIUMCR[BCTLC].
$\overline{\text{CS5}}$	Output	**System and Local Bus Chip Select 5** Enables specific memory devices or peripherals connected to MSC8102 buses.
BM[0–2]	Input	**Boot Mode 0–2** Defines the boot mode of the MSC8102. This signal is sampled on $\overline{\text{PORESET}}$ deassertion.
TC[0–2]	Input/Output	**Transfer Code 0–2** The bus master drives these pins during the address tenure to specify the type of the code.
BNKSEL[0–2]	Output	**Bank Select 0–2** Selects the SDRAM bank when the MSC8102 is in 60x-compatible bus mode.

Table 1-6. Memory Controller Signals (Continued)

Signal Name	Type	Description
ALE	Output	**Address Latch Enable** Controls the external address latch used in an external master bus.
PWE[0–3]	Output	**System Bus Write Enable** Outputs of the bus general-purpose chip-select machine (GPCM). These pins select byte lanes for write operations.
PSDDQM[0–3]	Output	**System Bus SDRAM DQM** From the SDRAM control machine. These pins select specific byte lanes of SDRAM devices.
PBS[0–3]	Output	**System Bus UPM Byte Select** From the UPM in the memory controller, these signals select specific byte lanes during memory operations. The timing of these pins is programmed in the UPM. The actual driven value depends on the address and size of the transaction and the port size of the accessed device.
PSDA10	Output	**System Bus SDRAM A10** From the bus SDRAM controller. The precharge command defines which bank is precharged. When the row address is driven, it is a part of the row address. When column address is driven, it is a part of column address.
PGPL0	Output	**System Bus UPM General-Purpose Line 0** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
PSDWE	Output	**System Bus SDRAM Write Enable** From the bus SDRAM controller. Should connect to SDRAM WE input.
PGPL1	Output	**System Bus UPM General-Purpose Line 1** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
POE	Output	**System Bus Output Enable** From the bus GPCM. Controls the output buffer of memory devices during read operations.
PSDRAS	Output	**System Bus SDRAM RAS** From the bus SDRAM controller. Should connect to SDRAM RAS input.
PGPL2	Output	**System Bus UPM General-Purpose Line 2** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
PSDCAS	Output	**System Bus SDRAM CAS** From the bus SDRAM controller. Should connect to SDRAM CAS input.
PGPL3	Output	**System Bus UPM General-Purpose Line 3** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
PGTA	Input	**System GPCM TA** Terminates external transactions during GPCM operation. Requires an external pull-up resistor for proper operation.
PUPMWAIT	Input	**System Bus UPM Wait** An external device holds this pin low to force the UPM to wait until the device is ready to continue the operation.
PGPL4	Output	**System Bus UPM General-Purpose Line 4** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.
PPBS	Output	**System Bus Parity Byte Select** In systems that store data parity in a separate chip, this output is used as the byte-select for that chip.

Table 1-6. Memory Controller Signals (Continued)

Signal Name	Type	Description
PSDAMUX	Output	**System Bus SDRAM Address Multiplexer** Controls the system bus SDRAM address multiplexer when the MSC8102 is in external master mode.
PGPL5	Output	**System Bus UPM General-Purpose Line 5** One of six general-purpose output lines from the UPM. The values and timing of this pin are programmed in the UPM.

1.6 GPIO, TDM, UART, and Timer Signals

The general-purpose input/output (GPIO), time-division multiplexed (TDM), universal asynchronous receiver/transmitter (UART), and timer signals are grouped together because they use a common set of signal lines. Individual assignment of a signal to a specific signal line is configured through internal registers. **Table 1-7** describes the signals in this group.

Table 1-7. GPIO, TDM, UART, and Timer Signals

Signal Name	Type	Description
GPIO0	Input/Output	**General-Purpose Input Output 0** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.
CHIP_ID0	Input	**Chip ID 0** Determines the chip ID of the MSC8102 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
GPIO1	Input/Output	**General-Purpose Input Output 1** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.
TIMER0	Input/Output	**Timer 0** Each signal is configured as either input to or output from the counter. See the *MSC8102 Reference* for configuration details.
CHIP_ID1	Input	**Chip ID 1** Determines the chip ID of the MSC8102 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
GPIO2	Input/Output	**General-Purpose Input Output 2** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual*.
TIMER1	Input/Output	**Timer 1** Each signal is configured as either input to or output from the counter. For the configuration of the pin direction, refer to the *MSC8102 Reference Manual*.
CHIP_ID2	Input	**Chip ID 2** Determines the chip ID of the MSC8102 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.
GPIO3	Input/Output	**General-Purpose Input Output 3** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM3TSYN	Input/Output	**TDM3 Transmit Frame Sync** Transmit frame sync for TDM 3.
IRQ1	Input	**Interrupt Request 1** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.

Table 1-7. GPIO, TDM, UART, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO4	Input/Output	**General-Purpose Input Output 4** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102* Reference Manual GPIO programming model.
TDM3TCLK	Input	**TDM3 Transmit Clock** Transmit Clock for TDM 3
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO5	Input/Output	**General-Purpose Input/Output 5** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM3TDAT	Input/Output	**TDM3 Serial Transmitter Data** The serial transmit data signal for TDM 3. As an output, it provides the DATA_D signal for TDM 3. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO6	Input/Output	**General-Purpose Input Output 6** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM3RSYN	Input/Output	**TDM3 Receive Frame Sync** The receive sync signal for TDM 3. As an input, this can be the DATA_B data signal for TDM 3.For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO7	Input/Output	**General-Purpose Input Output 7** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM3RCLK	Input/Output	**TDM3 Receive Clock** The receive clock signal for TDM 3. As an output, this can be the DATA_C data signal for TDM 3. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO8	Input/Output	**General-Purpose Input Output 8** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM3RDAT	Input/Output	**TDM3 Serial Receiver Data** The receive data signal for TDM 3. As an input, this can be the DATA_A data signal for TDM 3. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ6}}$	Input	**Interrupt Request 6** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.

Table 1-7. GPIO, TDM, UART, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO9	Input/Output	**General-Purpose Input Output 9** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM2TSYN	Input/Output	**TDM2 Transmit frame Sync** Transmit Frame Sync for TDM 2.
$\overline{\text{IRQ7}}$	Input	**Interrupt Request 7** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO10	Input/Output	**General-Purpose Input Output 10** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM2TCLK	Input	**TDM 2 Transmit Clock** Transmit Clock for TDM 2.
$\overline{\text{IRQ8}}$	Input	**Interrupt Request 8** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO11	Input/Output	**General-Purpose Input Output 11** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM2TDAT	Input/Output	**TDM2 Serial Transmitter Data** The transmit data signal for TDM 2. As an output, this can be the DATA_D data signal for TDM 2. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ9}}$	Input	**Interrupt Request 9** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO12	Input/Output	General-Purpose Input Output 12 One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM2RSYN	Input/Output	**TDM2 Receive Frame Sync** The receive sync signal for TDM 2. As an input, this can be the DATA_B data signal for TDM 2. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ10}}$	Input	**Interrupt Request 10** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO13	Input/Output	**General-Purpose Input Output 13** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM2RCLK	Input/Output	**TDM2 Receive Clock** The receive clock signal for TDM 2. As an input, this can be the DATA_C data signal for TDM 2. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ11}}$	Input	**Interrupt Request 11** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.

Table 1-7. GPIO, TDM, UART, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO14	Input/Output	**General-Purpose Input Output 14** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM2RDAT	Input/Output Input	**TDM2 Serial Receiver Data** The receive data signal for TDM 2. As an input, this can be the DATA_A data signal for TDM 2. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ12}}$	Input	**Interrupt Request 12** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO15	Input/Output	**General-Purpose Input Output 15** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM1TSYN	Input/Output	**TDM1 Transmit frame Sync** Transmit Frame Sync for TDM 1.
DREQ1	Input	**DMA Request 1** Used by an external peripheral to request DMA service.
GPIO16	Input/Output	**General-Purpose Input Output 16** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM1TCLK	Input	**TDM1 Transmit Clock** Transmit Clock for TDM 1.
$\overline{\text{DONE1}}$	Input/Output	**DMA Done 1** Signifies that the channel must be terminated. If the DMA generates $\overline{\text{DONE}}$, the channel handling this peripheral is inactive. As an input to the DMA, $\overline{\text{DONE}}$ closes the channel much like a normal channel closing. See the *MSC8102 Reference Manual* chapters on DMA and GPIO for information on configuring the $\overline{\text{DRACK}}$ or $\overline{\text{DONE}}$ mode and pin direction.
$\overline{\text{DRACK1}}$	Output	**DMA Data Request Acknowledge 1** Asserted by the DMA controller to indicate that the DMA controller has sampled the peripheral request.
GPIO17	Input/Output	**General-Purpose Input Output 17** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM1TDAT	Input/Output	**TDM1 Serial Transmitter Data** The transmit data signal for TDM 1. As an output, this can be the DATA_D data signal for TDM 1.For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
DACK1	Output	**DMA Acknowledge 1** The DMA controller drives this output to acknowledge the DMA transaction on the bus.
GPIO18	Input/Output	**General-Purpose Input Output 18** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM1RSYN	Input/Output	**TDM1 Receive Frame Sync** The receive sync signal for TDM 1. As an input, this can be the DATA_B data signal for TDM 1. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
DREQ2	Input	**DMA Request 2** Used by an external peripheral to request DMA service.

Table 1-7. GPIO, TDM, UART, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO19	Input/Output	**General-Purpose Input Output 19** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM1RCLK	Input/Output	**TDM1 Receive Clock** The receive clock signal for TDM 1. As an input, this can be the DATA_C data signal for TDM 1. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
DACK2	Output	**DMA Acknowledge 2** The DMA controller drives this output to acknowledge the DMA transaction on the bus.
GPIO20	Input/Output	**General-Purpose Input Output 20** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM1RDAT	Input/ Output	**TDM1 Serial Receiver Data** The receive data signal for TDM 1. As an input, this can be the DATA_A data signal for TDM 1. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
GPIO21	Input/Output	**General-Purpose Input Output 21** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM0TSYN	Input/Output	**TDM0 Transmit frame Sync** Transmit Frame Sync for TDM 0.
GPIO22	Input/Output	**General-Purpose Input Output 22** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM0TCLK	Input	**TDM 0 Transmit Clock** Transmit Clock for TDM 0.
$\overline{\text{DONE2}}$	Input/Output	**DMA Done 2** Signifies that the channel must be terminated. If the DMA generates DONE, the channel handling this peripheral is inactive. As an input to the DMA, DONE closes the channel much like a normal channel closing. **Note:** See the *MSC8102 Reference Manual* chapters on DMA and GPIO for information on configuring the $\overline{\text{DRACK}}$ or $\overline{\text{DONE}}$ mode and pin direction.
$\overline{\text{DRACK2}}$	Output	**DMA Data Request Acknowledge 2** Asserted by the DMA controller to indicate that the DMA controller has sampled the peripheral request.
GPIO23	Input/Output	**General-Purpose Input Output 23** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM0TDAT	Input/Output	**TDM0 Serial Transmitter Data** The transmit data signal for TDM 0. As an output, this can be the DATA_D data signal for TDM 0. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ13}}$	Input	**Interrupt Request 13** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.

Table 1-7. GPIO, TDM, UART, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO24	Input/Output	**General-Purpose Input Output 24** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM0RSYN	Input/Output	**TDM0 Receive Frame Sync** The receive sync signal for TDM 0. As an input, this can be the DATA_B data signal for TDM 0. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ14}}$	Input	**Interrupt Request 14** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO25	Input/Output	**General-Purpose Input Output 25** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM0RCLK	Input/Output	**TDM0 Receive Clock** The receive clock signal for TDM 0. As an input, this can be the DATA_C data signal for TDM 0. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
$\overline{\text{IRQ15}}$	Input	**Interrupt Request 15** One of fifteen external lines that can request a service routine, via the internal interrupt controller, from the SC140 core.
GPIO26	Input/Output	**General-Purpose Input Output 26** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TDM0RDAT	Input/Output	**TDM0 Serial Receiver Data** The receive data signal for TDM 0. As an input, this can be the DATA_A data signal for TDM 0. For configuration details, refer to the *MSC8102 Reference Manual* chapter describing TDM operation.
GPIO27	Input/Output	**General-Purpose Input Output 27** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
DREQ1	Input	**DMA Request 1** Used by an external peripheral to request DMA service.
URXD	Input	**UART Receive Data**
GPIO28	Input/Output	**General-Purpose Input Output 28** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
DREQ2	Input	**DMA Request 2** Used by an external peripheral to request DMA service.
UTXD	Output	**UART Transmit Data**
GPIO29	Input/Output	**General-Purpose Input Output 29** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
CHIP_ID3	Input	**Chip ID 3** Determines the chip ID of the MSC8102 DSI. It is sampled on the rising edge of $\overline{\text{PORESET}}$ signal.

Table 1-7. GPIO, TDM, UART, and Timer Signals (Continued)

Signal Name	Type	Description
GPIO30	Input/Output	**General-Purpose Input Output 30** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs.For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TIMER2	Input/Output	**Timer 2** Each signal is configured as either input to the counter or output from the counter. For the configuration of the pin direction, refer to the *MSC8102 Reference Manual*.
TMCLK	Input	**External TIMER Clock** An external timer can connect directly to the SIU as the SIU Clock.
GPIO31	Input/Output	**General-Purpose Input Output 31** One of 32 GPIO pins used as GPIO or as one of two dedicated inputs or one of two dedicated outputs. For details, refer to the *MSC8102 Reference Manual* GPIO programming model.
TIMER3	Input/ Output	**Timer 3** Each signal is configured as either input to or output from the counter. For the configuration of the pin direction, refer to the *MSC8102 Reference Manual*.

1.7 EOnCE Event and JTAG Test Access Port Signals

The MSC8102 uses two sets of debugging signals for the two types of internal debugging modules: EOnCE and the JTAG TAP controller. Each internal SC140 core has an EOnce module, but they are all accessed externally by the same two signals EE0 and EE1. The MSC8102 supports the standard set of Test Access Port (TAP) signals defined by IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture specification and described in **Table 1-8**.

Table 1-8. JTAG Test Access Port Signals

Signal Name	Type	Signal Description
EE0	Input	**EOnCE Event Bit 0** Used for putting the internal SC140 cores into Debug mode.
EE1	Output	**EOnCE Event Bit 1** Indicates that at least one on-chip SC140 core is in Debug mode.
TCK	Input	**Test Clock—**A test clock signal for synchronizing JTAG test logic.
TDI	Input	**Test Data Input—**A test data serial signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.
TDO	Output	**Test Data Output—**A test data serial signal for test instructions and data. TDO can be tri-stated. The signal is actively driven in the shift-IR and shift-DR controller states and changes on the falling edge of TCK.
TMS	Input	**Test Mode Select—**Sequences the test controller's state machine, is sampled on the rising edge of TCK, and has an internal pull-up resistor.
$\overline{\text{TRST}}$	Input	**Test Reset—**Asynchronously initializes the test controller, has an internal pull-up resistor, and must be asserted after power up.

1.8 Reserved Signals

Table 1-9. Reserved Signals

Signal Name	Type	Signal Description
TEST	Input	**Test** Used for manufacturing testing. You ***must*** connect this pin to GND.

Specifications 2

This chapter contains details on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8102 User's Guide* and *MSC8102 Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist. **Table 2-1** describes the maximum electrical ratings for the MSC8102.

Table 2-1. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core supply voltage	V_{DD}	–0.2 to 2.1	V
PLL supply voltage	V_{CCSYN}	–0.2 to 2.1	V
I/O supply voltage	V_{DDH}	–0.2 to 4.0	V
Input voltage	V_{IN}	(GND – 0.2) to 4.0	V
Maximum operating temperature	T_J	105	°C
Minimum operating temperature	T_A	–25	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 2-2.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 4.5**, , on page **4-6** includes a formula for computing the chip junction temperature (T_J).

2.2 Recommended Operating Conditions

Table 2-2 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2-2. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	V_{DD}	1.55 to 1.7	V
PLL supply voltage	V_{CCSYN}	1.55 to 1.7	V
I/O supply voltage	V_{DDH}	3.135 to 3.465	V
Input voltage	V_{IN}	–0.2 to V_{DDH}+0.2	V
Operating temperature range	T_J T_A	maximum: 105 minimum: –25	°C °C

2.3 Thermal Characteristics

Table 2-3 describes thermal characteristics of the MSC8102 for the FC-CBGA (HCTE) package.

Table 2-3. Thermal Characteristics for FC-CBGA (HCTE) Package

Characteristic	Symbol	FC-CBGA (HCTE) 20 × 20 mm[5]			Unit
		Natural Convection	100 ft/min (0.5 m/s) airflow	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$ or θ_{JA}	27	22	20	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$ or θ_{JA}	15	12	11	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$ or θ_{JB}	4.4			°C/W
Junction-to-case[5]	$R_{\theta JC}$ or θ_{JC}	0.3			°C/W

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and EIA/JESD51-2 with the single layer (1s) board horizontal.
3. Per JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

Section 4.5 describes these characteristics. The application note entitled *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601) describes the performance of the MSC8102 devices under standard thermal test conditions and when mounted in a component array. It also provides guidelines for evaluating board layouts that use MSC8102 devices.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8102. The measurements in **Table 2-4** assume the following system conditions:

- T_A = 25 °C
- V_{DD} = 1.55–1.7 V_{DC}
- V_{DDH} = 3.3 V ± 5% V_{DC}
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal V_{DDH} and V_{DD} or both V_{DDH} and V_{DD} must vary in the same direction (for example, both V_{DDH} and V_{DD} vary by +2 percent or both vary by –2 percent).

Table 2-4. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Input high voltage[1], all inputs except CLKIN	V_{IH}	2.0	3.0	3.465	V
Input low voltage[1]	V_{IL}	GND	0	0.4	V
CLKIN input high voltage	V_{IHC}	2.4	3.0	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0	0.4	V
Input leakage current, V_{IN} = V_{DDH}	I_{IN}	–1.0	0.09	1	µA
Tri-state (high impedance off state) leakage current, V_{IN} = V_{DDH}	I_{OZ}	–1.0	0.09	1	µA
Signal low input current, V_{IL} = 0.4 V[2]	I_L	–1.0	0.09	1	µA
Signal high input current, V_{IH} = 2.0 V[2]	I_H	–1.0	0.09	1	µA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0	0.4	V
Internal supply current: • In Wait mode — 250 MHz — 275 MHz • In Stop mode — 250 MHz — 275 MHz	 I_{DDW} I_{DDS} 	 — — — —	 203 222 88 95	 — — — —	 mA mA mA mA
Typical power consumption[3] at: • 250 MHz • 275 MHz	P 	 — —	 1.35 1.47	 — —	 W W

Notes:
1. See **Figure 2-1** for undershoot and overshoot voltages.
2. Not tested. Guaranteed by design.
3. The typical power was measured using an EFR code with the device running at room temperature (T_A = 25°C). No peripherals were enabled and ICache was not enabled. The source code was optimized to utilize all the ALUs and AGUs and all four cores. It was created using CodeWarrior® 2.5 by Metrowerks®. These values are provided as examples only. Power consumption is application dependent and varies widely. To assure proper board design with regard to thermal dissipation and proper operating temperatures, evaluate power consumption for your application and use the design guidelines in **Chapter 4** and in *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601).

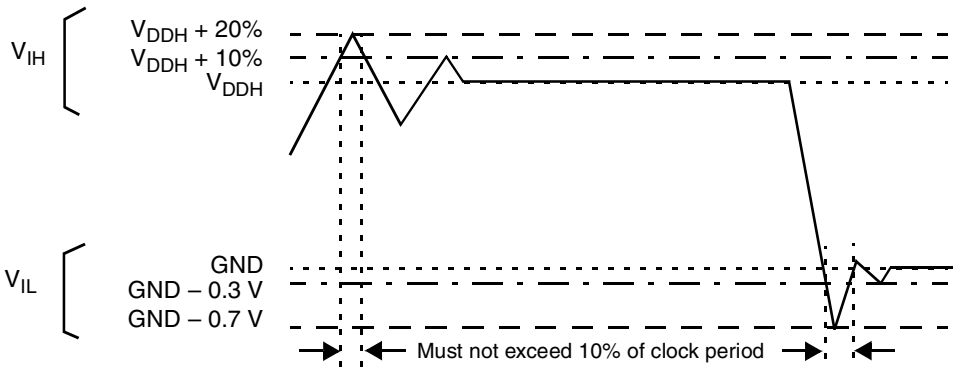


Figure 2-1. Overshoot/Undershoot Voltage for V_{IH} and V_{IL}

2.5 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. When designing systems such as DSP farms using the DSI, use a device loading of 4 pF per pin. AC timings are based on a 50 pF load, except where noted otherwise, and a 50 Ω transmission line. For any additional pF, add 0.07 ns for the delay and take the RC delay into consideration.

2.5.1 Output Buffer Impedances

Table 2-5. Output Buffer Impedances

Output Buffers	Typical Impedance (Ω)
System bus	35
Memory controller	35
Parallel I/O	55
Note: These are typical values at 65°C. The impedance may vary by ±25% depending on device process and operating temperature.	

2.5.2 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.5.3** describes the clocking characteristics. **Section 2.5.4** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8102 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence. See **Table 2-10** for timing.
- If possible, bring up the V_{DD} and V_{DDH} levels together. For designs with separate power supplies, bring up the V_{DDH} levels and then the V_{DD} levels (see **Figure 2-3** and **Figure 2-4**).
- CLKIN can start toggling after V_{DDH} reaches its nominal level, but it must toggle before V_{DD} reaches 0.5 V to guarantee correct device operation (see **Figure 2-2** and **Figure 2-4**).

The following figures show acceptable start-up sequence examples. **Figure 2-2** shows a sequence in which V_{DD} and V_{DDH} are raised together. **Figure 2-3** shows a sequence in which CLKIN starts toggling after V_{DDH} reaches its nominal level and before V_{DD} is applied. **Figure 2-4** shows a sequence in which V_{DD} is raised after V_{DDH} and CLKIN begins to toggle shortly before V_{DD} reaches the 0.5 V level.

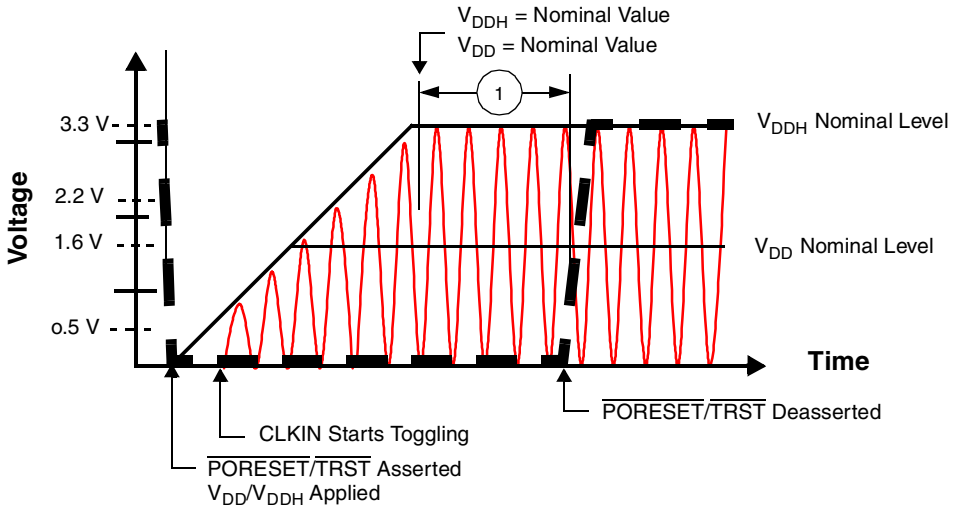


Figure 2-2. Start-Up Sequence with V_{DD} and V_{DDH} Raised Together

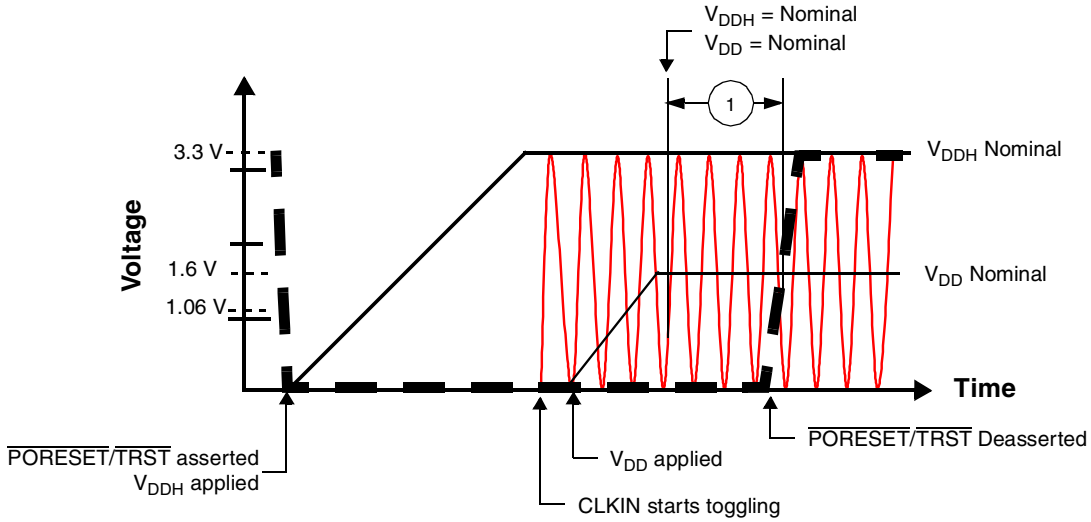


Figure 2-3. Start-Up Sequence with CLKIN Started After V_{DDH} and Before V_{DD}

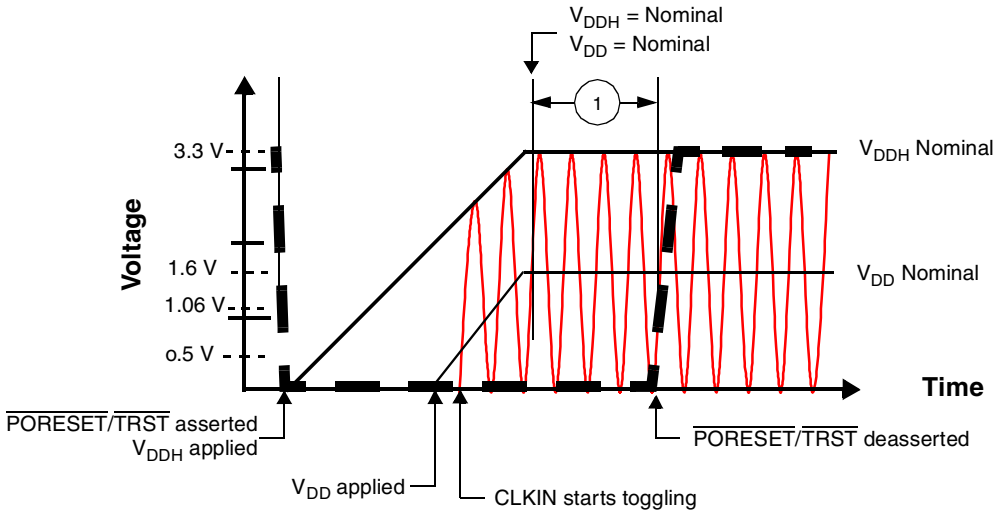


Figure 2-4. Start-Up Sequence with V_{DDH} Raised Before V_{DD} with CLKIN Started Before V_{DD} = 0.5 V

2.5.3 Clock and Timing Signals

The following sections include a description of clock signal characteristics. **Table 2-6** shows the maximum frequency values for internal (core, reference, bus, and DSI) and external (CLKOUT) clocks. The user must ensure that maximum frequency values are not exceeded.

Table 2-6. Maximum Frequencies

Characteristic	Maximum in MHz
Core frequency	250/275
Reference frequency (REFCLK)	83.3/91.7
Internal bus frequency (BLCK)	83.3/91.7
DSI clock frequency (HCLKIN)	if REFCLK ≤ 70 MHz, HCLKIN ≤CLKOUT if REFCLK > 70 MHz, HCLKIN ≤70 MHz
External clock output frequency (CLKOUT)	83.3/91.7
Note: The REFCLK is CLKOUT.	

Table 2-7. Clock Frequencies

Characteristics	Symbol	250 MHz Device		275 MHz Device	
		Min	Max	Min	Max
CLKIN frequency	F_{CLKIN}	33 MHz	75 MHz	33 MHz	75 MHz
DLLIN frequency	F_{DLLIN}	33 MHz	75 MHz	33 MHz	75 MHz
BCLK frequency	F_{BCLK}	33 MHz	75 MHz	33 MHz	75 MHz
Reference Clock (REFCLK) frequency	F_{REFCLK}	33 MHz	83.3 MHz	33 MHz	91.7 MHz
Output Clock (CLKOUT) frequency	F_{CLKOUT}	33 MHz	83.3 MHz	33 MHz	91.7 MHz
SC140 core clock frequency	F_{CORE}	165 MHz	250 MHz	165 MHz	275 MHz
Note: The rise and fall time of external clocks should be 5 ns maximum.					

Table 2-8. System Clock Parameters

Characteristic	Minimum	Maximum	Unit
Phase jitter between BCLK and DLLIN	—	0.5	ns
CLKIN frequency	33	75	MHz
CLKIN slope	—	5	ns
DLLIN slope	—	2	ns
CLKOUT frequency jitter[1]	—	(0.01 × F_{CLKOUT}) + F_{CLKIN} jitter	MHz
CLKOUT phase jitter (in DLLOFF mode)[2]	—	2	ns
Delay between CLKOUT and DLLIN[3]	—	5	ns

Notes:
1. Low CLKIN frequency causes poor PLL performance. Choose a F_{CLKIN} value high enough to keep the frequency after predivider (SPLLMFCLK) higher than 16.5 MHz.
2. Peak-to-peak.
3. Not tested. Guaranteed by design.

2.5.4 Reset Timing

The MSC8102 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- Bus monitor reset
- Host reset command through JTAG

All MSC8102 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 2-9** describes the reset sources.

Table 2-9. Reset Sources

Name	Direction	Description
Power-on reset ($\overline{\text{PORESET}}$)	Input	Initiates the power-on reset flow that resets the MSC8102 and configures various attributes of the MSC8102. On $\overline{\text{PORESET}}$, the entire MSC8102 device is reset. SPLL and DLL states are reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The clock mode (MODCK bits), reset configuration mode, boot mode, Chip ID, and use of either a DSI 64 bits port or a System Bus 64 bits port are configured only when $\overline{\text{PORESET}}$ is asserted.
External Hard reset ($\overline{\text{HRESET}}$)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC8102. While $\overline{\text{HRESET}}$ is asserted, $\overline{\text{SRESET}}$ is also asserted. $\overline{\text{HRESET}}$ is an open-drain pin. Upon hard reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The most configurable features are reconfigure. These features are defined in the 32-bit hard reset configuration word described in *Hard Reset Configuration Word* section of the *Reset* chapter in the *MSC8102 Reference Manual*.
External Soft reset ($\overline{\text{SRESET}}$)	Input/ Output	Initiates the soft reset flow. The MSC8102 detects an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8102 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin. Upon soft reset, $\overline{\text{SRESET}}$ is driven, the SC140 extended cores are reset, and system configuration is maintained.
Software watchdog reset	Internal	When the MSC8102 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
Bus monitor reset	Internal	When the MSC8102 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.
Host reset command through the TAP	Internal	When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated.

Table 2-10 summarizes the reset actions that occur as a result of the different reset sources.

Table 2-10. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)	
	External only	External or Internal (Software Watchdog or Bus Monitor)	External	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (refer to **Section 2.5.4.1** for details).	Yes	No	No	No
SPLL and DLL states reset	Yes	No	No	No
System reset configuration write through the DSI	Yes	No	No	No
System reset configuration write though the system bus	Yes	Yes	No	No
HRESET driven	Yes	Yes	No	No
SIU registers reset	Yes	Yes	No	No
IPBus Modules Reset (TDM, UART, timers, DSI, IPBus Master, GIC, HS, and GPIO)	Yes	Yes	Yes	Yes
SRESET driven	Yes	Yes	Yes	Depends on command
SC140 extended cores reset	Yes	Yes	Yes	Yes
MQBS reset	Yes	Yes	Yes	Yes

2.5.4.1 Power-On Reset (PORESET) Pin

Asserting PORESET initiates the power-on reset flow. PORESET and TRST should be asserted external during power-up. CLKIN may start toggling after V_{DDH} reaches the nominal level, but must start toggling before V_{DD} reaches 0.5 V.

2.5.4.2 Reset Configuration

The MSC8102 has two mechanisms for writing the reset configuration:

- Through the direct slave interface (DSI), or
- Through the system bus

When reset configuration written through the system bus, the MSC8102 uses as a configuration master or as a configuration slave. If a configuration slave is selected, but no special configuration word is written, a default configuration word is applied. Fourteen signal levels are sampled on PORESET deassertion to define the Reset Configuration mode and boot and operating conditions (see **Chapter 1** for signal descriptions):

- RSTCONF
- CNFGS
- DSISYNC
- DSI64
- CHIP_ID[0–3]
- BM[0–2]
- SWTE
- MODCK[1–2]

2.5.4.3 Reset Timing Tables

Table 2-11 and **Figure 2-5** describe the reset timing for a reset configuration write through the direct slave interface (DSI) or through the system bus.

Table 2-11. Timing for a Reset Configuration Write through the DSI or System Bus

No.	Characteristics	Expression	Min	Max	Unit
1	Required external $\overline{\text{PORESET}}$ duration minimum • CLKIN = 33 MHz • CLKIN = 75 MHz	16/CLKIN	 484.8 213.3	—	ns
2	Delay from deassertion of external $\overline{\text{PORESET}}$ to deassertion of internal $\overline{\text{PORESET}}$ • CLKIN = 33 MHz • CLKIN = 75 MHz	1024/CLKIN	 31.03 13.65		 µs µs
3	Delay from de-assertion of internal $\overline{\text{PORESET}}$ to SPLL lock • CLKIN = 33 MHz • CLKIN = 75 MHz	800/(CLKIN/PDF) (pre-division factor)	 48.5 32.0		 µs µs
4	Delay from SPLL lock to DLL lock. • DLL enabled REFCLK = 33 Mhz REFCLK = 75 Mhz • DLL disabled	 3073/REFCLK —	 93.12 40.97 0.0		 µs µs µs
5	• Delay from SPLL and DLL lock to $\overline{\text{HRESET}}$ de-assertion • DLL enabled REFCLK = 33 Mhz REFCLK = 75 Mhz • DLL disabled REFCLK = 33 Mhz REFCLK = 75 Mhz	 3585/REFCLK 512/REFCLK	 108.64 47.5 15.52 6.83		 µs µs µs µs
6	Delay from SPLL and DLL lock to $\overline{\text{SRESET}}$ de-assertion • DLL enabled REFCLK = 33 Mhz REFCLK = 75 Mhz • DLL disabled REFCLK = 33 Mhz REFCLK = 75 Mhz	 3588/REFCLK 515/REFCLK	 108.73 47.84 15.61 6.87		 µs µs µs µs
Note:	Timings are not tested, but are guaranteed by design.				

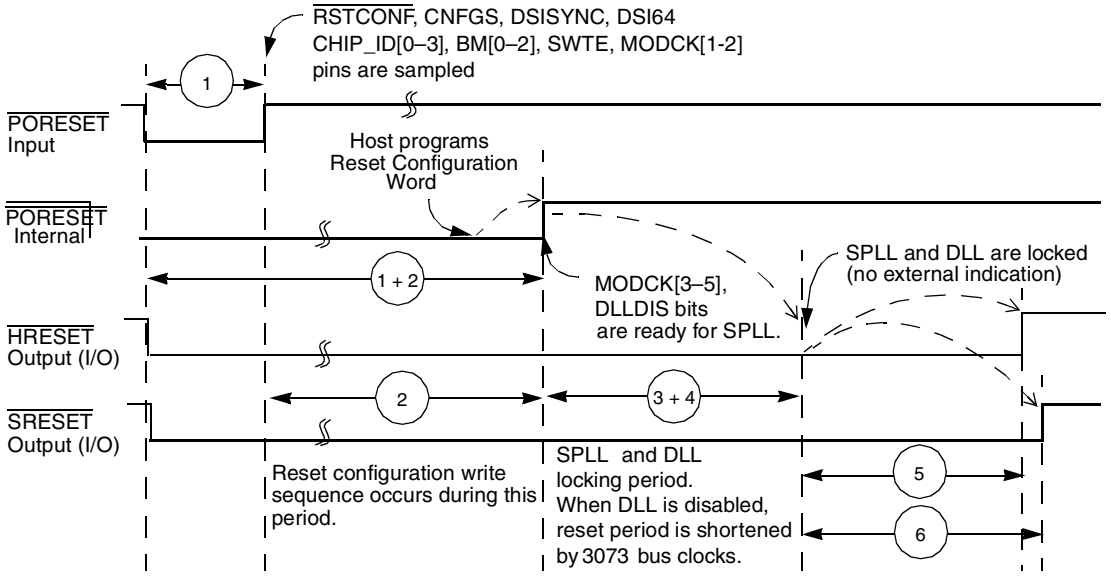


Figure 2-5. Timing Diagram for a Reset Configuration Write

2.5.5 System Bus Access Timing

2.5.5.1 Core Data Transfers

Generally, all MSC8102 bus and system output signals are driven from the rising edge of the reference clock (REFCLK). The REFCLK is either the DLLIN signal or, if DLL is disabled, the CLKOUT signal. Memory controller signals, however, trigger on four points within a REFCLK cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of REFCLK (and T3 at the falling edge), as **Figure 2-6** shows. **Figure 2-6** is a graphical representation of the internal ticks.

Figure 2-6. Internal Tick Spacing for Memory Controller Signals

The UPM machine and GPCM machine outputs change on the internal tick determined by the memory controller configuration. The AC specifications are relative to the internal tick. SDRAM machine outputs change only on the REFCLK rising edge.

Table 2-12. AC Timing for SIU Inputs

No.	Characteristic	Value[2]	Units
10	Hold time for all signals after the 50% level of the REFCLK rising edge	1	ns
11a	$\overline{\text{ARTRY}}/\overline{\text{ABB}}/\overline{\text{TS}}$ set-up time before the 50% level of the REFCLK rising edge	4.5	ns
11b	$\overline{\text{DBG}}/\overline{\text{DBB}}/\overline{\text{BG}}/\overline{\text{BR}}/\overline{\text{TC}}$ set-up time before the 50% level of the REFCLK rising edge	4.3	ns
11c	$\overline{\text{AACK}}$ set-up time before the 50% level of the REFCLK rising edge	5.0	ns
11d	$\overline{\text{TA}}/\overline{\text{TEA}}/\overline{\text{PSDVAL}}$ set-up time before the 50% level of the REFCLK rising edge • Pipeline mode • Non-pipeline mode	 3.7 5.0	 ns ns
12	Data bus set-up time before REFCLK rising edge in Normal mode • Pipeline mode • Non-pipeline mode	 2.3 4.9	 ns ns
13	Data bus set-up time before the 50% level of the REFCLK rising edge in ECC and PARITY modes • Pipeline mode • Non-pipeline mode	 2.6 7	 ns ns
14	DP set-up time before the 50% level of the REFCLK rising edge • Pipeline mode • Non-pipeline mode	 2.3 6.5	 ns ns
15a	Address bus set-up time before the 50% level of the REFCLK rising edge • Extra cycle mode (SIUBCR[EXDD] = 0) • No extra cycle mode (SIUBCR[EXDD] = 1)	 3.1 6.9	 ns ns
15b	Address attributes: TT/$\overline{\text{TBST}}$/TSIZ/$\overline{\text{GBL}}$ set-up time before the 50% level of the REFCLK rising edge • Extra cycle mode (SIUBCR[EXDD] = 0) • No extra cycle mode (SIUBCR[EXDD] = 1)	 5.5 7.6	 ns ns
16[1]	PUPMWAIT signal set-up time before the 50% level of the REFCLK rising edge	4.0	ns

Notes: 1. Synchronous operation. Asynchronous operation may have a higher set-up time.
2. Values are measured from the 50% TTL transition level relative to the 50% level of the REFCLK rising edge.

Table 2-13. AC Timing for SIU Outputs

No.	Characteristic	Value[1]		Units
		30 pF	50 pF	
30	Min delay from the 50% level of the REFCLK for all signals	1.0	1.0	ns
31	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$ max delay from the 50% level of the REFCLK rising edge • Pipeline mode • Non-pipeline mode	 6.0 6.5	 7.5 8.0	 ns ns
32a	Address bus max delay from the 50% level of the REFCLK rising edge • Multi-master mode (SIUBCR[EBM] = 1) • Single-master mode (SIUBCR[EBM] = 0)	 7.2 4.1	 8.7 5.6	 ns ns
32b	Address attributes: TT/TC/$\overline{\text{TBST}}$/TSIZ/$\overline{\text{GBL}}$ max delay from the 50% level of the REFCLK rising edge	5.8	7.3	ns
32c	BADDR max delay from the 50% level of the REFCLK rising edge	4.8	6.3	ns
33a	Data bus max delay from the 50% level of the REFCLK rising edge • Pipeline mode • Non-pipeline mode	 5.0 7.5	 6.5 9.0	 ns ns
33b	DP max delay from the 50% level of the REFCLK rising edge • Pipeline mode • Non-pipeline mode	 5.5 7.5	 7.0 9.0	 ns ns
34	Memory controller signals/ALE max delay from the 50% level of the REFCLK rising edge	5.9	7.4	ns
35a	$\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}/\overline{\text{DBB}}$ max delay from the 50% level of the REFCLK rising edge	5.5	7.0	ns
35b	$\overline{\text{AACK}}/\overline{\text{ABB}}/\overline{\text{TS}}/\overline{\text{CS}}$ max delay from the 50% level of the REFCLK rising edge	6.3	7.8	ns

Notes:
1. Values are measured from the 50% level of the REFCLK rising edge to the 50% signal level.
2. The maximum bus frequency depends on the mode:
   • In 60x-compatible mode connected to another MSC8102 device, the frequency is determined by adding the input and output longest timing values, which results in a frequency of 75 MHz for 30 pF output capacitance.
   • In single-master mode, the frequency depends on the timing of the devices connected to the MSC8102.

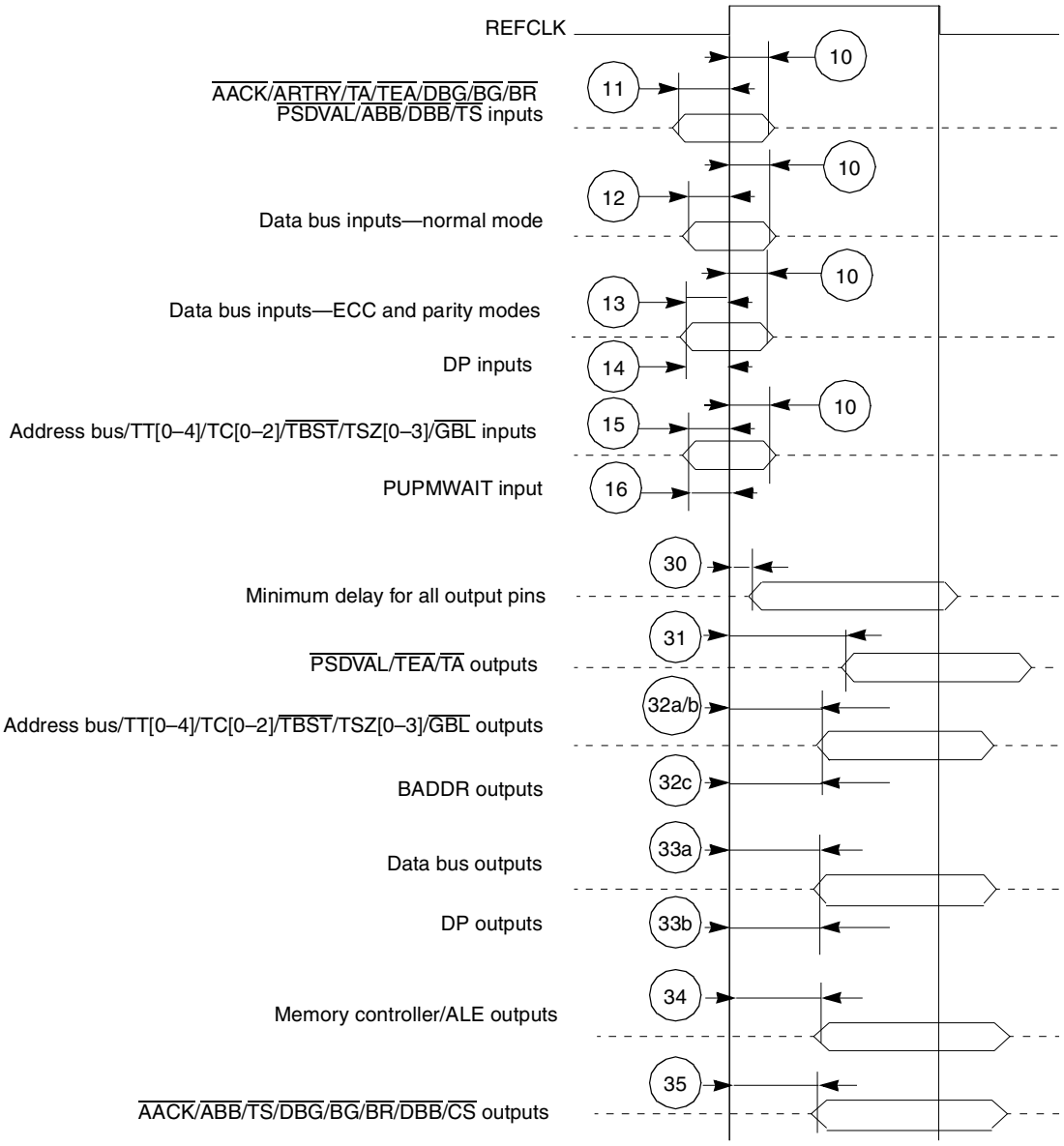


Figure 2-7. Bus Signal Timing

2.5.5.2 DMA Data Transfers

Table 2-14 describes the DMA signal timing.

Table 2-14. DMA Signals

No.	Characteristic	Minimum	Maximum	Units
37	DREQ set-up time before the 50% level of the falling edge of REFCLK	6	—	ns
38	DREQ hold time after the 50% level of the falling edge of REFCLK	0.5	—	ns
39	$\overline{\text{DONE}}$ set-up time before the 50% level of the rising edge of REFCLK	7	—	ns
40	$\overline{\text{DONE}}$ hold time after the 50% level of the rising edge of REFCLK	0.5	—	ns
41	$\overline{\text{DACK}}$/$\overline{\text{DRACK}}$/$\overline{\text{DONE}}$ delay after the 50% level of the REFCLK rising edge	0.5	9	ns

The DREQ signal is synchronized with REFCLK. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 2-14**. **Figure 2-8** shows synchronous peripheral interaction.

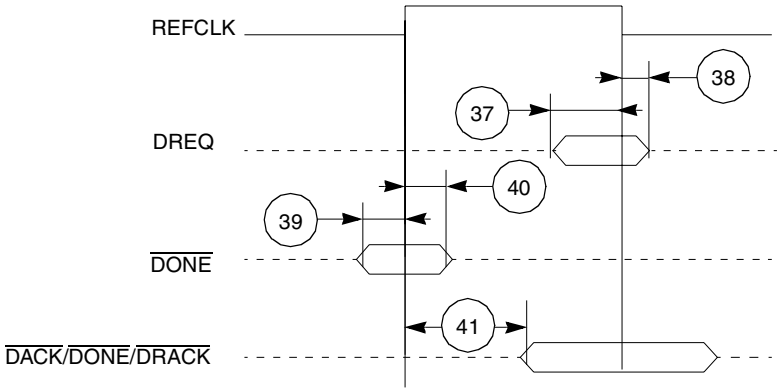


Figure 2-8. DMA Signals

2.5.6 DSI Timing

The timings in the following sections are based on a 30 pF capacitive load. See **Section 2.5.1**, *Output Buffer Impedances*, on page **2-4** for details.

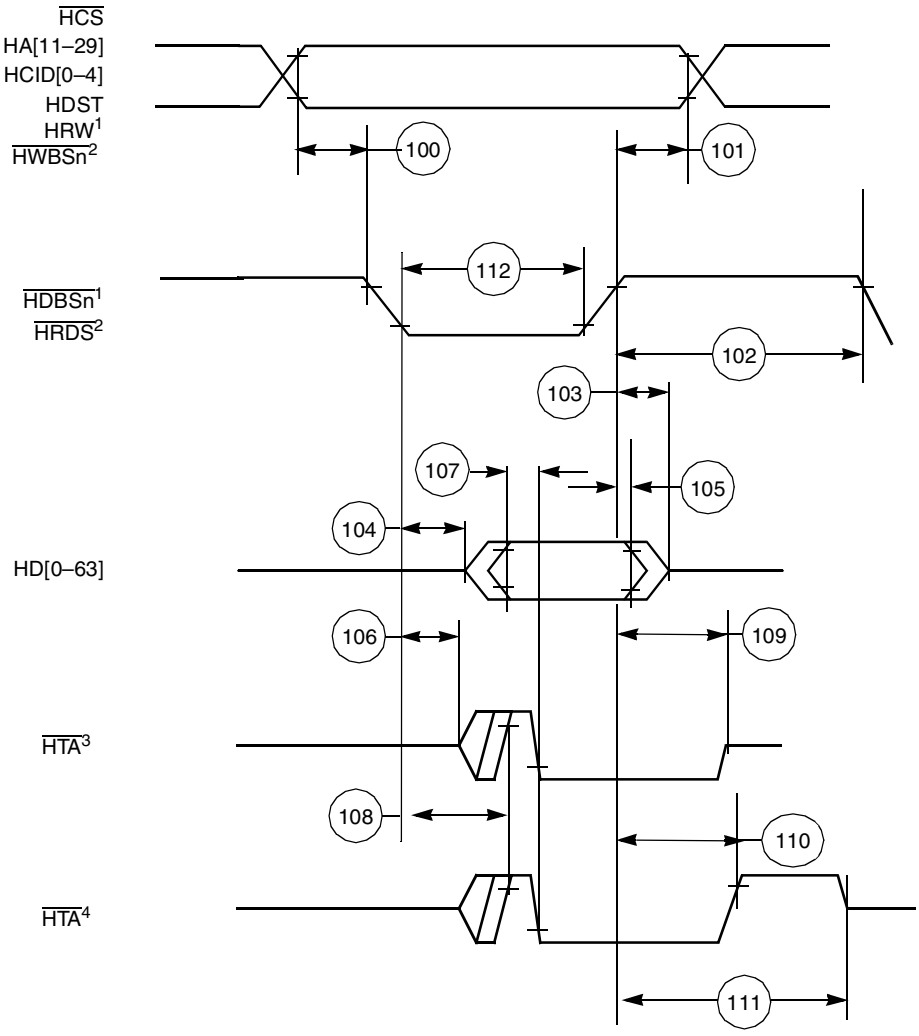
2.5.6.1 DSI Asynchronous Mode

Table 2-15. DSI Asynchronous Mode Timing

No.	Characteristics	Min	Max	Unit
100	Attributes[1] set-up time before strobe ($\overline{\text{HWBS[n]}}$) assertion	2.3	—	ns
101	Attributes[1] hold time after data strobe deassertion	2.0	—	ns
102	Read/Write data strobe deassertion width • DCR[HTAAD] = 1 — Consecutive access to the same DSI — Different device with DCR[HTADT] = 01 — Different device with DCR[HTADT] = 10 — Different device with DCR[HTADT] = 11 • DCR[HTAAD] = 0	 $1.8 + T_{REFCLK}$ $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$ $1.8 + T_{REFCLK}$	—	 ns ns ns ns ns
103	Read data strobe deassertion to output data high impedance	—	11.5	ns
104	Read data strobe assertion to output data active from high impedance	2.7	—	ns
105	Output data hold time after read data strobe deassertion	3.0	—	ns
106	Read/Write data strobe assertion to $\overline{\text{HTA}}$ active from high impedance	2.5	—	ns
107	Output data valid to $\overline{\text{HTA}}$ assertion	4.0	—	ns
108	Read/Write data strobe assertion to $\overline{\text{HTA}}$ valid[2]	—	7.5	ns
109	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance. (DCR[HTAAD] = 0, $\overline{\text{HTA}}$ at end of access released at logic 0)	—	7.5	ns
110	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ deassertion. (DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1)	—	7.2	ns
111	Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance. (DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1 • DCR[HTADT] = 01 • DCR[HTADT] = 10 • DCR[HTADT] = 11	—	 $5 + T_{REFCLK}$ $5 + (1.5 \times T_{REFCLK})$ $5 + (2.5 \times T_{REFCLK})$	 ns ns ns
112	Read/Write data strobe assertion width	$1.8 + T_{REFCLK}$	—	ns
201	Host data input set-up time before write data strobe deassertion	1.7	—	ns
202	Host data input hold time after write data strobe deassertion	3.2	—	ns

Notes:
1. *Attributes* refers to the following signals: $\overline{\text{HCS}}$, HA[11–29], HCID[0–4], HDST, HRW, $\overline{\text{HRDS}}$, and $\overline{\text{HWBSn}}$.
2. This specification is tested in dual strobe mode. Timing in single strobe mode is guaranteed by design.
3. All values listed in this table are tested or guaranteed by design.

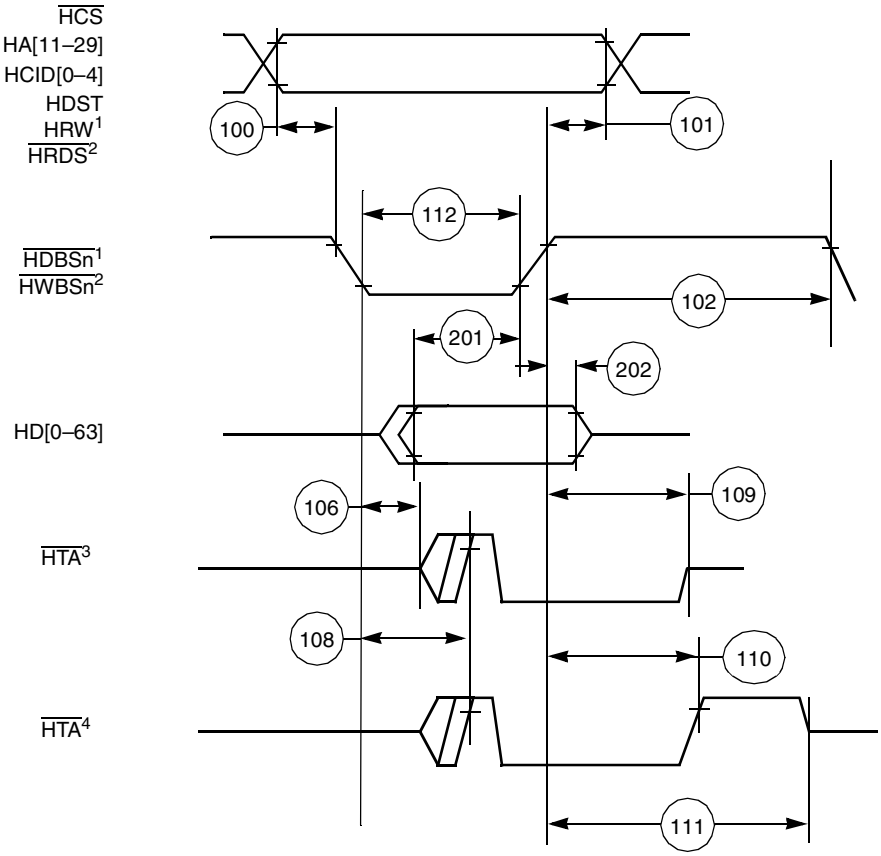
Figure 2-9 shows DSI asynchronous read signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 2-9. Asynchronous Single and Dual Modes Read Timing Diagram

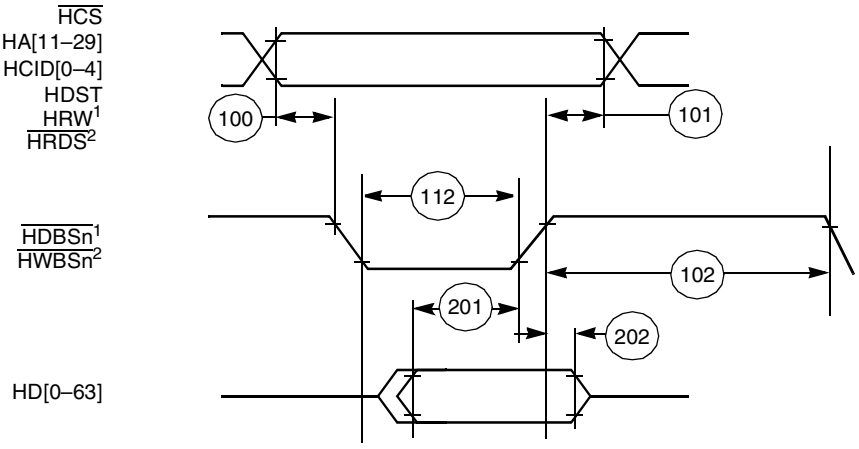
Figure 2-10 shows DSI asynchronous write signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 2-10. Asynchronous Single and Dual Modes Write Timing Diagram

Figure 2-11 shows DSI asynchronous broadcast write signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.

Figure 2-11. Asynchronous Broadcast Write Timing Diagram

2.5.6.2 DSI Synchronous Mode

Table 2-16. DSI Inputs—Synchronous Mode

Number	Characteristic	Expression	Minimum	Maximum	Units
120	HCLKIN Cycle Time[1]	HTC	14.3	55.6	ns
121	HCLKIN high pulse width	(0.5 ±0.1) × HTC	5.7	33.3	ns
122	HCLKIN Low pulse width	(0.5 ±0.1) × HTC	5.7	33.3	ns
123	HA[11–29] inputs set-up time	—	2.4	—	ns
124	HD[0–63] inputs set-up time	—	3.4	—	ns
125	HCID[0–4] inputs set-up time	—	3.3	—	ns
126	All other inputs set-up time	—	2.5	—	ns
127	All inputs hold time	—	2.2	—	ns
Notes: 1. Values are based on a frequency range of 18–70 MHz. See **Table 2-6** for HCLKIN limits.					

Table 2-17. DSI Outputs—Synchronous Mode

Number	Characteristic	Minimum	Maximum	Units
128	HCLKIN high to HD[0–63] output active	2.0	—	
129	HCLKIN high to HD[0–63] output valid	—	8.6	
130	HD[0–63] output hold time	1.8	—	
131	HCLKIN high to HD[0–63] output high impedance	—	9.4	
132	HCLKIN high to $\overline{\text{HTA}}$ output active	1.5	—	
133	HCLKIN high to $\overline{\text{HTA}}$ output valid	—	9.0	
134	$\overline{\text{HTA}}$ output hold time	1.7	—	
135	HCLKIN high to $\overline{\text{HTA}}$ high impedance	—	5.2	

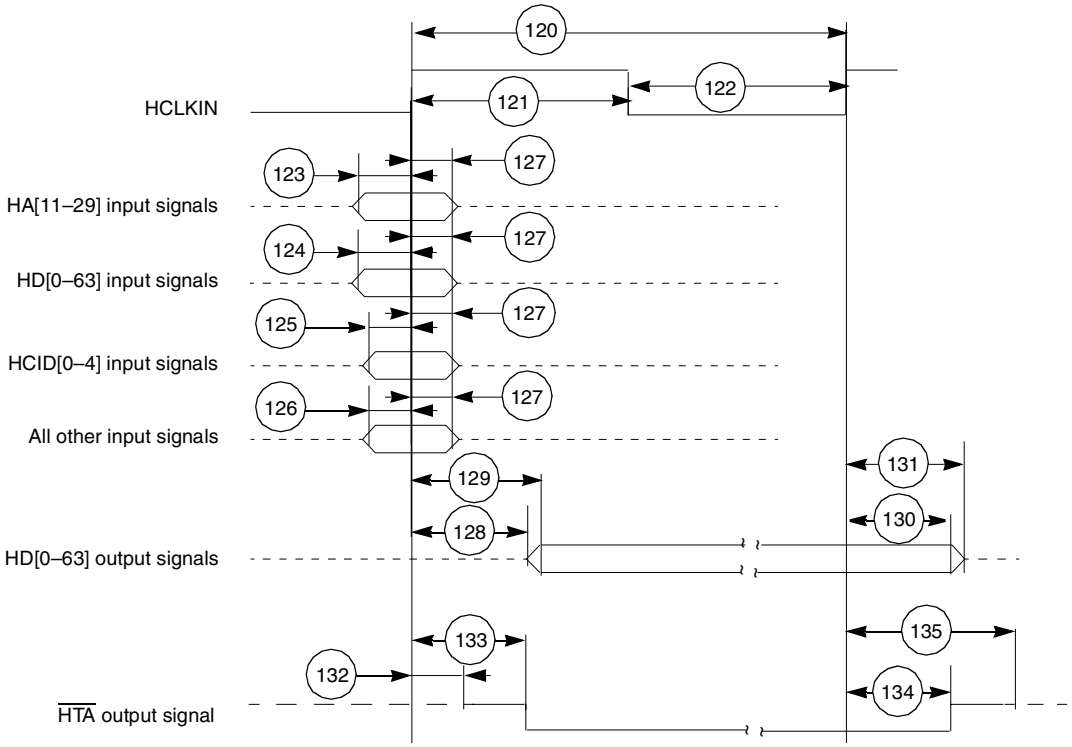


Figure 2-12. DSI Synchronous Mode Signals Timing Diagram

2.5.7 TDM Timing

Table 2-18. TDM Timing

Number	Characteristic	Expression	Minimum	Maximum	Units
300	TDMxRCLK/TDMxTCLK	TC[1]	20	—	ns
301	TDMxRCLK/TDMxTCLK high pulse width	(0.5 ± 0.1) × TC	8	—	ns
302	TDMxRCLK/TDMxTCLK Low pulse width	(0.5 ± 0.1) × TC	8	—	ns
303	TDM receive all input set-up time		2.5	—	ns
304	TDM receive all input hold time		2.5	—	ns
305	TDMxTCLK high to TDMxTDAT/TDMxRCLK output active[2,3]		3	—	ns
306	TDMxTCLK high to TDMxTDAT/TDMxRCLK output valid[2,3]		—	12	ns
307	All output hold time[2]		4	—	ns
308	TDMxTCLK high to TDmXTDAT/TDMxRCLK output high impedance[2,3]		—	11	ns
309	TDMxTCLK high to TDMXTSYN output valid[2]		—	11	ns
310	TDMxTSYN output hold time[2]		3.9	—	ns

Notes: 1. Values are based on a frequency range of 9–50 MHz.
2. Values are based on 30 pF capacitive load.
3. When configured as an output, TDMxRCLK acts as a second data link. See **Chapter 22** of the *MSC8102 Reference Manual* for details.

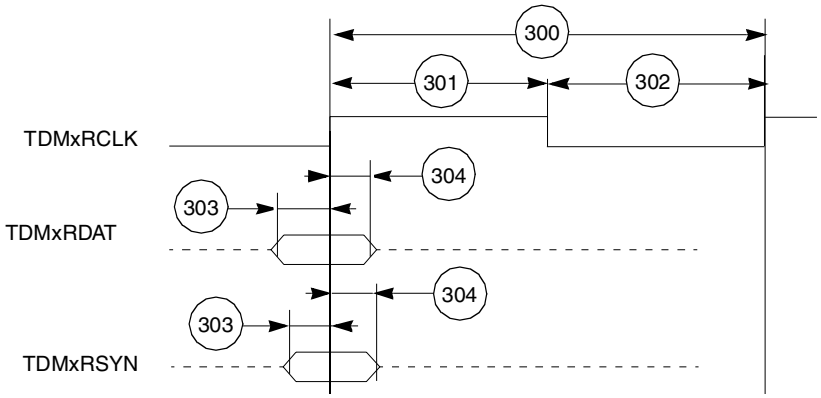


Figure 2-13. TDM Inputs Signals

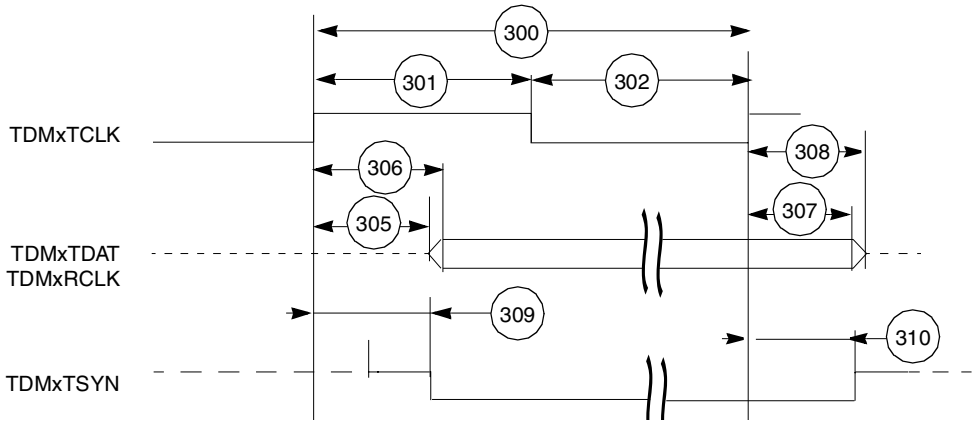


Figure 2-14. TDM Output Signals

2.5.8 UART Timing

Table 2-19. UART Timing

No.	Characteristics	Expression	Min	Max	Unit
400	URXD and UTXD inputs high/low duration	16 × T_{REFCLK}	160.0	—	ns
401	URXD and UTXD inputs rise/fall time			10	ns
402	UTXD output rise/fall time			10	ns

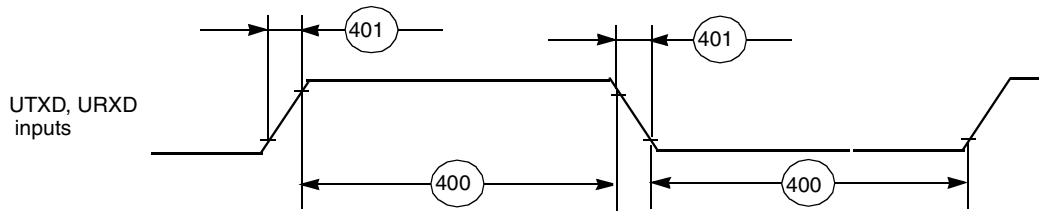


Figure 2-15. UART Input Timing

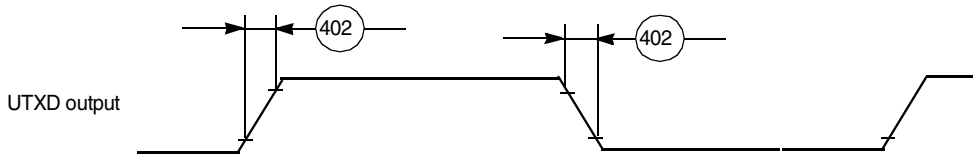


Figure 2-16. UART Output Timing

2.5.9 Timer Timing

Table 2-20. Timer Timing

No.	Characteristics	Min.	Max	Unit
500	TIMERx frequency	10.9	—	ns
501	TIMERx Input high period	4.0	—	ns
502	TIMERx output low period	4.0	—	ns
503	TIMERx propagations delay from its clock input	3.3	10.0	ns

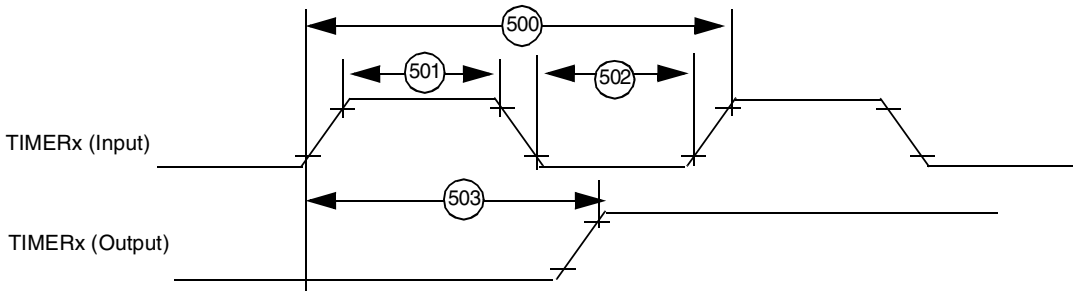


Figure 2-17. Timer Timing

2.5.10 GPIO Timing

Table 2-21. GPIO Timing

No.	Characteristics	Min	Max	Unit
601	REFCLK edge to GPIO out valid (GPIO out delay time)	—	8.5	ns
602	REFCLK edge to GPIO out not valid (GPIO out hold time)	1.5	—	ns
603	REFCLK edge to high impedance on GPIO out	—	5.4	ns
604	GPIO in valid to REFCLK edge (GPIO in set-up time)	4.5	—	ns
605	REFCLK edge to GPIO in not valid (GPIO in hold time)	0.5	—	ns

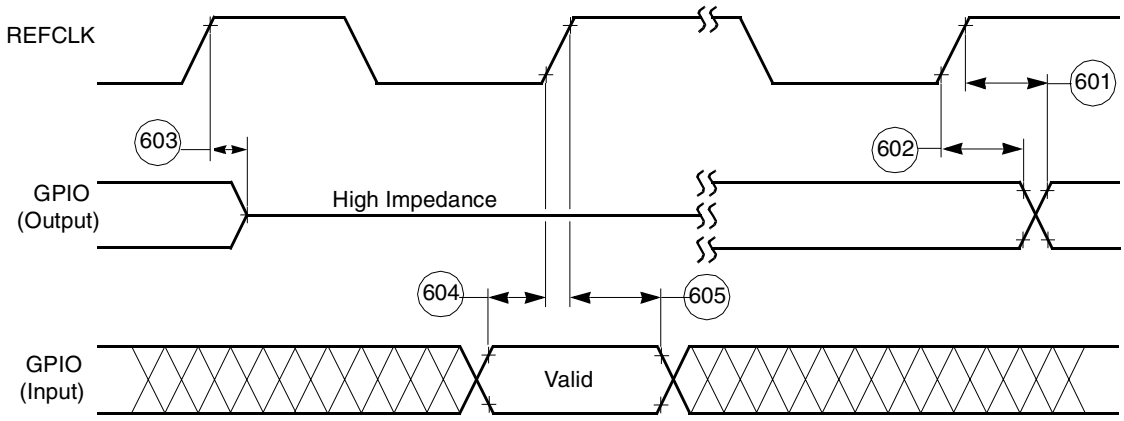


Figure 2-18. GPIO Timing

2.5.11 EE Signals

Table 2-22. EE Pin Timing

Number	Characteristics	Type	Minimum
65	EE0 (input)	Asynchronous	4 core clock periods
66	EE1 (output)	Synchronous to Core clock	1 core clock period

Notes: 1. The core clock is the SC140 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
2. Refer to **Table 1-4** on page 1-6 for detailed information about EE pin functionality.

Figure 2-19 shows the signal behavior of the EE pins.

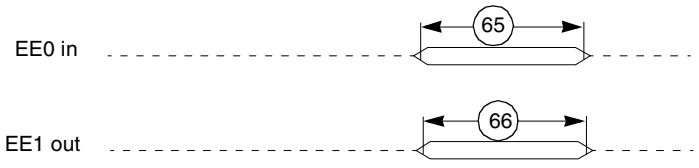


Figure 2-19. EE Pins Timing

2.5.12 JTAG Signals

Table 2-23. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
700	TCK frequency of operation (1/(T_C × 3); maximum 22 MHz)	0.0	22.0	MHz
701	TCK cycle time	45.0	—	ns
702	TCK clock pulse width measured at V_M = 1.6 V	21.0	—	ns
703	TCK rise and fall times	0.0	3.0	ns
704	Boundary scan input data set-up time	5.0	—	ns
705	Boundary scan input data hold time	24.0	—	ns
706	TCK low to output data valid	0.0	40.0	ns
707	TCK low to output high impedance	0.0	40.0	ns
708	TMS, TDI data set-up time	5.0	—	ns
709	TMS, TDI data hold time	25.0	—	ns
710	TCK low to TDO data valid	0.0	44.0	ns
711	TCK low to TDO high impedance	0.0	20.0	ns
712	$\overline{\text{TRST}}$ assert time	100.0	—	ns
713	$\overline{\text{TRST}}$ set-up time to TCK low	40.0	—	ns
Note:	All timings apply to OnCE module data transfers as the OnCE module uses the JTAG port as an interface.			

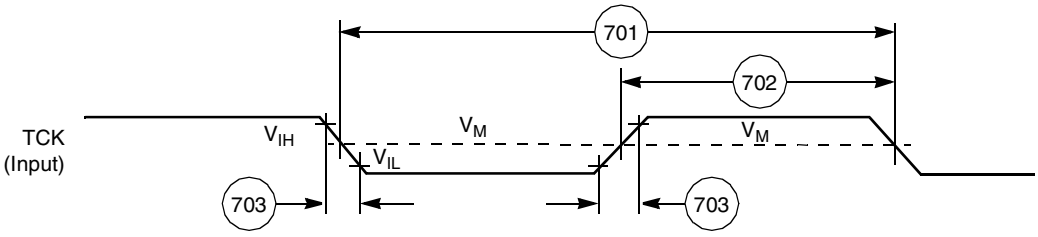


Figure 2-20. Test Clock Input Timing Diagram

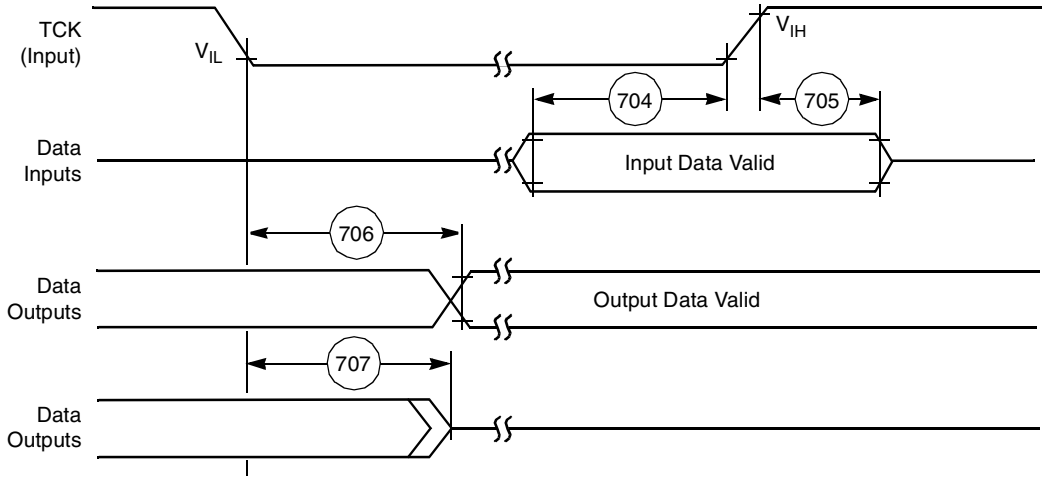


Figure 2-21. Boundary Scan (JTAG) Timing Diagram

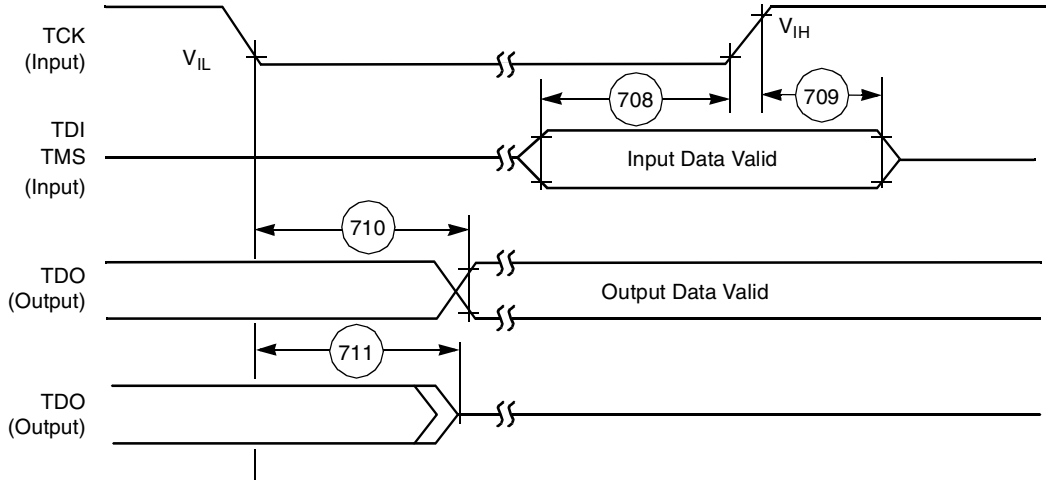


Figure 2-22. Test Access Port Timing Diagram

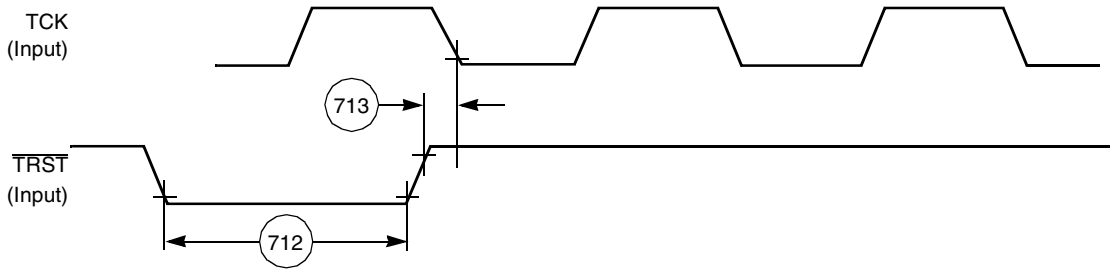


Figure 2-23. $\overline{\text{TRST}}$ Timing Diagram

Packaging 3

This chapter provides information on the MSC8102 package, including diagrams of the package pinouts and tables showing how the signals discussed in **Chapter 1** are allocated. The MSC8102 is available in a 431-pin High Temperature Coefficient for Expansion Flip Chip-Ceramic Ball Grid Array (FC-CBGA (HCTE)).

3.1 FC-CBGA (HCTE) Package Description

Figure 3-1 and **Figure 3-2** show top and bottom views of the FC-CBGA (HCTE) package, including pinouts. To conform to JDEC requirements, the package is based on a 23 × 23 position (20 × 20 mm) layout with the outside perimeter depopulated. Therefore, ball position numbering starts with B2. Signal names shown in the figures are typically the signal assigned after reset. Signals that are only used during power-on reset (SWTE, DSISYNC, DSI64, MODCK[1–2], CNFGS, and CHIP_ID[0–3]) are not shown in these figures if there is another signal assigned to the pin after reset. Also, there are several signals that are designated as IRQ lines immediately after reset, but represent duplicate IRQ lines that should be reconfigured by the user. To represent these signals uniquely in the figures, the second functions (BADDR[29–31], DP[1–7], and $\overline{\text{INT\_OUT}}$) are used.

Table 3-1 lists the MSC8102 signals alphabetically by signal name. Connections with multiple names are listed individually by each name. Signals with programmable polarity are shown both as signals which are asserted low (default) and high (that is, $\overline{\text{NAME}}$/NAME). **Table 3-2** lists the signals numerically by pin number. Each pin number is listed once with the various signals that are multiplexed to it. For simplicity, signals with programmable polarity are shown in this table only with their default name (asserted low).

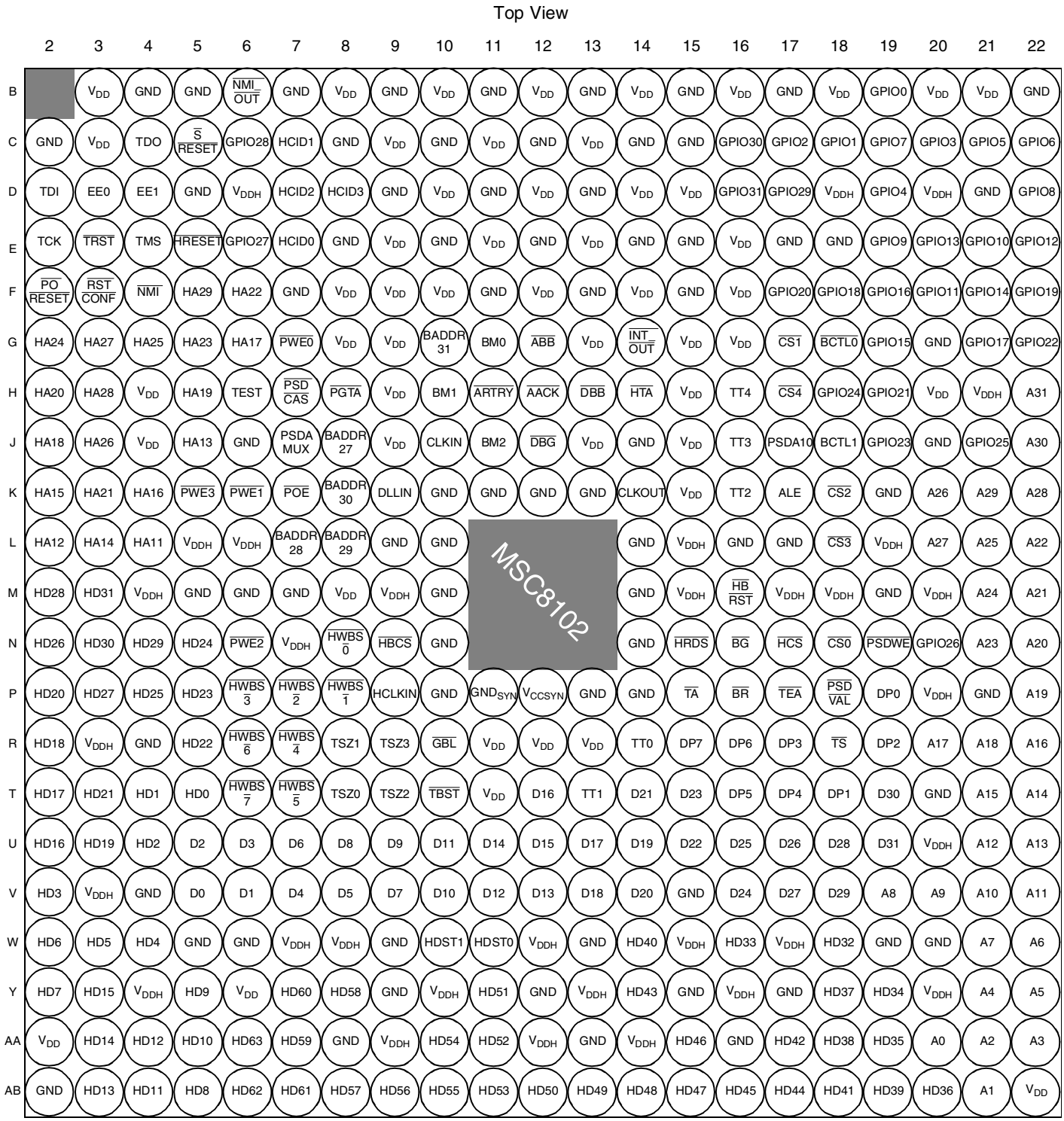


Figure 3-1. MSC8102 High Temperature Coefficient for Expansion Flip Chip Ceramic Ball Grid Array (High CTE FC-CBGA), Top View

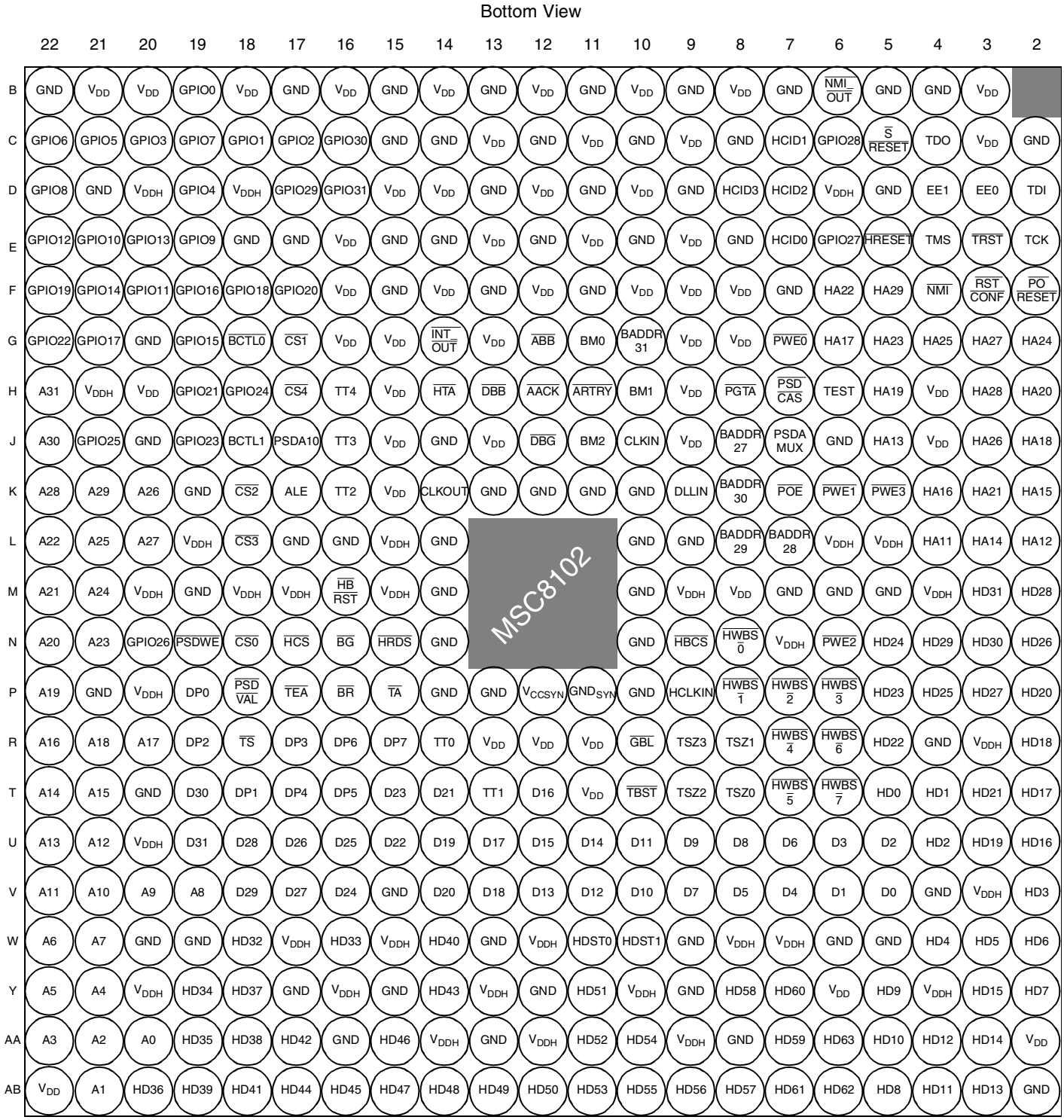


Figure 3-2. MSC8102 High Temperature Coefficient for Expansion Flip Chip Ceramic Ball Grid Array (High CTE FC-CBGA), Bottom View

Table 3-1. MSC8102 Signal Listing By Name

Signal Name	Location Designator	Signal Name	Location Designator
A0	AA20	BADDR27	J8
A1	AB21	BADDR28	L7
A2	AA21	BADDR29	L8
A3	AA22	BADDR30	K8
A4	Y21	BADDR31	G10
A5	Y22	$\overline{\text{BCTL0}}$	G18
A6	W22	$\overline{\text{BCTL1}}$	J18
A7	W21	$\overline{\text{BG}}$	N16
A8	V19	BNKSEL0	G11
A9	V20	BNKSEL1	H10
A10	V21	BNKSEL2	J11
A11	V22	BM0	G11
A12	U21	BM1	H10
A13	U22	BM2	J11
A14	T22	$\overline{\text{BR}}$	P16
A15	T21	CHIP_ID0	B19
A16	R22	CHIP_ID1	C18
A17	R20	CHIP_ID2	C17
A18	R21	CHIP_ID3	D17
A19	P22	CLKIN	J10
A20	N22	CLKOUT	K14
A21	M22	CNFGS	W3
A22	L22	$\overline{\text{CS0}}$	N18
A23	N21	$\overline{\text{CS1}}$	G17
A24	M21	$\overline{\text{CS2}}$	K18
A25	L21	$\overline{\text{CS3}}$	L18
A26	K20	$\overline{\text{CS4}}$	H17
A27	L20	$\overline{\text{CS5}}$	K16
A28	K22	$\overline{\text{CS5}}$	J18
A29	K21	$\overline{\text{CS6}}$	J16
A30	J22	$\overline{\text{CS7}}$	H16
A31	H22	D0	V5
$\overline{\text{AACK}}$	H12	D1	V6
$\overline{\text{ABB}}$	G12	D2	U5
ALE	K17	D3	U6
$\overline{\text{ARTRY}}$	H11	D4	V7

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
D5	V8	D41	AB18
D6	U7	D42	AA17
D7	V9	D43	Y14
D8	U8	D44	AB17
D9	U9	D45	AB16
D10	V10	D46	AA15
D11	U10	D47	AB15
D12	V11	D48	AB14
D13	V12	D49	AB13
D14	U11	D50	AB12
D15	U12	D51	Y11
D16	T12	D52	AA11
D17	U13	D53	AB11
D18	V13	D54	AA10
D19	U14	D55	AB10
D20	V14	D56	AB9
D21	T14	D57	AB8
D22	U15	D58	Y8
D23	T15	D59	AA7
D24	V16	D60	Y7
D25	U16	D61	AB7
D26	U17	D62	AB6
D27	V17	D63	AA6
D28	U18	$\overline{\text{DACK1}}$	G21
D29	V18	$\overline{\text{DACK1}}$	T18
D30	T19	$\overline{\text{DACK2}}$	F22
D31	U19	$\overline{\text{DACK2}}$	R19
D32	W18	$\overline{\text{DACK3}}$	T17
D33	W16	$\overline{\text{DACK4}}$	T16
D34	Y19	$\overline{\text{DBB}}$	H13
D35	AA19	$\overline{\text{DBG}}$	J12
D36	AB20	DLLIN	K9
D37	Y18	$\overline{\text{DONE1}}$	F19
D38	AA18	$\overline{\text{DONE2}}$	G22
D39	AB19	DP0	P19
D40	W14	DP1	T18

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
DP2	R19	GND	C10
DP3	R17	GND	C12
DP4	T17	GND	C14
DP5	T16	GND	C15
DP6	R16	GND	D5
DP7	R15	GND	D9
$\overline{\text{DRACK1}}$	F19	GND	D11
$\overline{\text{DRACK2}}$	G22	GND	D13
DREQ1	G19	GND	D21
DREQ1	P19	GND	E8
DREQ2	F18	GND	E10
DREQ2	R17	GND	E12
DREQ3	R16	GND	E14
DREQ4	R15	GND	E15
DSI64	U4	GND	E17
DSISYNC	T4	GND	E18
EE0	D3	GND	F7
EE1	D4	GND	F11
$\overline{\text{EXT\_BG2}}$	T18	GND	F13
$\overline{\text{EXT\_BG3}}$	T16	GND	F15
$\overline{\text{EXT\_BR2}}$	P19	GND	G20
$\overline{\text{EXT\_BR3}}$	R17	GND	J6
$\overline{\text{EXT\_DBG2}}$	R19	GND	J14
$\overline{\text{EXT\_DBG3}}$	T17	GND	J20
$\overline{\text{GBL}}$	R10	GND	K10
GND	B4	GND	K11
GND	B5	GND	K12
GND	B7	GND	K13
GND	B9	GND	K19
GND	B11	GND	L9
GND	B13	GND	L10
GND	B15	GND	L14
GND	B17	GND	L16
GND	B22	GND	L17
GND	C2	GND	M5
GND	C8	GND	M6

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
GND	M7	GPIO7	C19
GND	M10	GPIO8	D22
GND	M14	GPIO9	E19
GND	M19	GPIO10	E21
GND	N10	GPIO11	F20
GND	N14	GPIO12	E22
GND	P10	GPIO13	E20
GND	P13	GPIO14	F21
GND	P14	GPIO15	G19
GND	P21	GPIO16	F19
GND	R4	GPIO17	G21
GND	T20	GPIO18	F18
GND	V4	GPIO19	F22
GND	V15	GPIO20	F17
GND	W5	GPIO21	H19
GND	W6	GPIO22	G22
GND	W9	GPIO23	J19
GND	W13	GPIO24	H18
GND	W19	GPIO25	J21
GND	W20	GPIO26	N20
GND	Y9	GPIO27	E6
GND	Y12	GPIO28	C6
GND	Y15	GPIO29	D17
GND	Y17	GPIO30	C16
GND	AA8	GPIO31	D16
GND	AA13	HA11	L4
GND	AA16	HA12	L2
GND	AB2	HA13	J5
GND_{SYN}	P11	HA14	L3
GPIO0	B19	HA15	K2
GPIO1	C18	HA16	K4
GPIO2	C17	HA17	G6
GPIO3	C20	HA18	J2
GPIO4	D19	HA19	H5
GPIO5	C21	HA20	H2
GPIO6	C22	HA21	K3

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
HA22	F6	HD20	P2
HA23	G5	HD21	T3
HA24	G2	HD22	R5
HA25	G4	HD23	P5
HA26	J3	HD24	N5
HA27	G3	HD25	P4
HA28	H3	HD26	N2
HA29	F5	HD27	P3
$\overline{\text{HBCS}}$	N9	HD28	M2
$\overline{\text{HBRST}}$	M16	HD29	N4
HCID0	E7	HD30	N3
HCID1	C7	HD31	M3
HCID2	D7	HD32	W18
HCID3	D8	HD33	W16
HCLKIN	P9	HD34	Y19
$\overline{\text{HCS}}$	N17	HD35	AA19
HD0	T5	HD36	AB20
HD1	T4	HD37	Y18
HD2	U4	HD38	AA18
HD3	V2	HD39	AB19
HD4	W4	HD40	W14
HD5	W3	HD41	AB18
HD6	W2	HD42	AA17
HD7	Y2	HD43	Y14
HD8	AB5	HD44	AB17
HD9	Y5	HD45	AB16
HD10	AA5	HD46	AA15
HD11	AB4	HD47	AB15
HD12	AA4	HD48	AB14
HD13	AB3	HD49	AB13
HD14	AA3	HD50	AB12
HD15	Y3	HD51	Y11
HD16	U2	HD52	AA11
HD17	T2	HD53	AB11
HD18	R2	HD54	AA10
HD19	U3	HD55	AB10

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
HD56	AB9	IRQ2	K8
HD57	AB8	IRQ2	R19
HD58	Y8	IRQ3	C21
HD59	AA7	IRQ3	G10
HD60	Y7	IRQ3	R17
HD61	AB7	IRQ4	C22
HD62	AB6	IRQ4	G12
HD63	AA6	IRQ4	T17
HDBE4	R7	IRQ5	C19
HDBE5	T7	IRQ5	H13
HDBE6	R6	IRQ5	L8
HDBE7	T6	IRQ5	T16
HDBS4	R7	IRQ6	D22
HDBS5	T7	IRQ6	R16
HDBS6	R6	IRQ7	E19
HDBS7	T6	IRQ7	G14
HDST0	W11	IRQ7	R15
HDST1	W10	IRQ8	E21
HRDE	N15	IRQ9	F20
HRDS	N15	IRQ10	E22
HRESET	E5	IRQ11	E20
HRW	N15	IRQ12	F21
HTA	H14	IRQ13	J19
HWBS0	N8	IRQ14	H18
HWBS1	P8	IRQ15	J21
HWBS2	P7	MODCK1	V2
HWBS3	P6	MODCK2	W4
HWBS4	R7	NMI	F4
HWBS5	T7	NMI_OUT	B6
HWBS6	R6	PBPL3	H7
HWBS7	T6	PBS0	G7
INT_OUT	G14	PBS1	K6
IRQ1	C20	PBS2	N6
IRQ1	R10	PBS3	K5
IRQ1	T18	PBS4	R7
IRQ2	D19	PBS5	T7

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
PBS6	R6	SWTE	T5
PBS7	T6	TA	P15
PGPL0	J17	TBST	T10
PGPL1	N19	TC0	G11
PGPL2	K7	TC1	H10
PGPL4	H8	TC2	J11
PGPL5	J7	TCK	E2
PGTA	H8	TDI	D2
POE	K7	TDM0RCLK	J21
PORESET	F2	TDM0RDAT	N20
PPBS	H8	TDM0RSYN	H18
PSDA10	J17	TDM0TCLK	G22
PSDAMUX	J7	TDM0TDAT	J19
PSDCAS	H7	TDM0TSYN	H19
PSDDQM0	G7	TDM1RCLK	F22
PSDDQM1	K6	TDM1RDAT	F17
PSDDQM2	N6	TDM1RSYN	F18
PSDDQM3	K5	TDM1TCLK	F19
PSDDQM4	R7	TDM1TDAT	G21
PSDDQM5	T7	TDM1TSYN	G19
PSDDQM6	R6	TDM2RCLK	E20
PSDDQM7	T6	TDM2RDAT	F21
PSDRAS	K7	TDM2RSYN	E22
PSDVAL	P18	TDM2TCLK	E21
PSDWE	N19	TDM2TDAT	F20
PWE0	G7	TDM2TSYN	E19
PWE1	K6	TDM3RCLK	C19
PWE2	N6	TDM3RDAT	D22
PWE3	K5	TDM3RSYN	C22
PWE4	R7	TDM3TCLK	D19
PWE5	T7	TDM3TDAT	C21
PWE6	R6	TDM3TSYN	C20
PWE7	T6	TDO	C4
PUPMWAIT	H8	TEA	P17
RSTCONF	F3	TEST	H6
SRESET	C5	TIMER0	C18

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
TIMER1	C17	V_{DD}	E11
TIMER2	C16	V_{DD}	E13
TIMER3	D16	V_{DD}	E16
TMCLK	C16	V_{DD}	F8
TMS	E4	V_{DD}	F9
$\overline{\text{TRST}}$	E3	V_{DD}	F10
$\overline{\text{TS}}$	R18	V_{DD}	F12
TSZ0	T8	V_{DD}	F14
TSZ1	R8	V_{DD}	F16
TSZ2	T9	V_{DD}	G8
TSZ3	R9	V_{DD}	G9
TT0	R14	V_{DD}	G13
TT1	T13	V_{DD}	G15
TT2	K16	V_{DD}	G16
TT3	J16	V_{DD}	H4
TT4	H16	V_{DD}	H9
URXD	E6	V_{DD}	H15
UTXD	C6	V_{DD}	H20
V_{CCSYN}	P12	V_{DD}	J4
V_{DD}	B8	V_{DD}	J9
V_{DD}	B10	V_{DD}	J13
V_{DD}	B12	V_{DD}	J15
V_{DD}	B14	V_{DD}	K15
V_{DD}	B16	V_{DD}	M8
V_{DD}	B18	V_{DD}	R11
V_{DD}	B20	V_{DD}	R12
V_{DD}	B21	V_{DD}	R13
V_{DD}	C3	V_{DD}	T11
V_{DD}	C9	V_{DD}	Y6
V_{DD}	C11	V_{DD}	AA2
V_{DD}	C13	V_{DD}	B3
V_{DD}	D10	V_{DD}	AB22
V_{DD}	D12	V_{DDH}	D6
V_{DD}	D14	V_{DDH}	D18
V_{DD}	D15	V_{DDH}	D20
V_{DD}	E9	V_{DDH}	H21

Table 3-1. MSC8102 Signal Listing By Name (Continued)

Signal Name	Location Designator	Signal Name	Location Designator
V_{DDH}	L5	V_{DDH}	V3
V_{DDH}	L6	V_{DDH}	W7
V_{DDH}	L15	V_{DDH}	W8
V_{DDH}	L19	V_{DDH}	W12
V_{DDH}	M4	V_{DDH}	W15
V_{DDH}	M9	V_{DDH}	W17
V_{DDH}	M15	V_{DDH}	Y4
V_{DDH}	M17	V_{DDH}	Y10
V_{DDH}	M18	V_{DDH}	Y13
V_{DDH}	M20	V_{DDH}	Y16
V_{DDH}	N7	V_{DDH}	Y20
V_{DDH}	P20	V_{DDH}	AA9
V_{DDH}	R3	V_{DDH}	AA12
V_{DDH}	U20	V_{DDH}	AA14

Note: This table lists every signal name. Because many signals are multiplexed, an individual ball designator number may be listed several times.

Table 3-2. MSC8102 Signal Listing by Ball Designator

Locator Designator	Signal Name	Locator Designator	Signal Name
B3	V_{DD}	C20	GPIO3/TDM3TSYN/$\overline{IRQ1}$
B4	GND	C21	GPIO5/TDM3TDAT/$\overline{IRQ3}$
B5	GND	C22	GPIO6/TDM3RSYN/$\overline{IRQ4}$
B6	$\overline{NMI\_OUT}$	D2	TDI
B7	GND	D3	EE0
B8	V_{DD}	D4	EE1
B9	GND	D5	GND
B10	V_{DD}	D6	V_{DDH}
B11	GND	D7	HCID2
B12	V_{DD}	D8	HCID3
B13	GND	D9	GND
B14	V_{DD}	D10	V_{DD}
B15	GND	D11	GND
B16	V_{DD}	D12	V_{DD}
B17	GND	D13	GND
B18	V_{DD}	D14	V_{DD}
B19	GPIO0/CHIP_ID0	D15	V_{DD}
B20	V_{DD}	D16	GPIO31/TIMER3
B21	V_{DD}	D17	GPIO29/CHIP_ID3
B22	GND	D18	V_{DDH}
C2	GND	D19	GPIO4/TDM3TCLK/$\overline{IRQ2}$
C3	V_{DD}	D20	V_{DDH}
C4	TDO	D21	GND
C5	$\overline{SRESET}$	D22	GPIO8/TDM3RDAT/$\overline{IRQ6}$
C6	GPIO28/DREQ2/UTXD	E2	TCK
C7	HCID1	E3	$\overline{TRST}$
C8	GND	E4	TMS
C9	V_{DD}	E5	$\overline{HRESET}$
C10	GND	E6	GPIO27/DREQ1/URXD
C11	V_{DD}	E7	HCID0
C12	GND	E8	GND
C13	V_{DD}	E9	V_{DD}
C14	GND	E10	GND
C15	GND	E11	V_{DD}
C16	GPIO30/TIMER2/TMCLK	E12	GND
C17	GPIO2/TIMER1/CHIP_ID2	E13	V_{DD}
C18	GPIO1/TIMER0/CHIP_ID1	E14	GND
C19	GPIO7/TDM3RCLK/$\overline{IRQ5}$	E15	GND

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Locator Designator	Signal Name	Locator Designator	Signal Name
E16	V_{DD}	G12	$\overline{ABB}/\overline{IRQ4}$
E17	GND	G13	V_{DD}
E18	GND	G14	$\overline{IRQ7}/\overline{INT\_OUT}$
E19	GPIO9/TDM2TSYN/$\overline{IRQ7}$	G15	V_{DD}
E20	GPIO13/TDM2RCLK/$\overline{IRQ11}$	G16	V_{DD}
E21	GPIO10/TDM2TCLK/$\overline{IRQ8}$	G17	$\overline{CS1}$
E22	GPIO12/TDM2RSYN/$\overline{IRQ10}$	G18	$\overline{BCTL0}$
F2	$\overline{PORESET}$	G19	GPIO15/TDM1TSYN/DREQ1
F3	$\overline{RSTCONF}$	G20	GND
F4	$\overline{NMI}$	G21	GPIO17/TDM1TDAT/$\overline{DACK1}$
F5	HA29	G22	GPIO22/TDM0TCLK/$\overline{DONE2}$/$\overline{DRACK2}$
F6	HA22	H2	HA20
F7	GND	H3	HA28
F8	V_{DD}	H4	V_{DD}
F9	V_{DD}	H5	HA19
F10	V_{DD}	H6	TEST
F11	GND	H7	$\overline{PSDCAS}$/PBPL3
F12	V_{DD}	H8	$\overline{PGTA}$/PUPMWAIT/PGPL4/$\overline{PPBS}$
F13	GND	H9	V_{DD}
F14	V_{DD}	H10	BM1/TC1/BNKSEL1
F15	GND	H11	$\overline{ARTRY}$
F16	V_{DD}	H12	$\overline{AACK}$
F17	GPIO20/TDM1RDAT	H13	$\overline{DBB}/\overline{IRQ5}$
F18	GPIO18/TDM1RSYN/DREQ2	H14	$\overline{HTA}$
F19	GPIO16/TDM1TCLK/$\overline{DONE1}$/$\overline{DRACK1}$	H15	V_{DD}
F20	GPIO11/TDM2TDAT/$\overline{IRQ9}$	H16	TT4/$\overline{CS7}$
F21	GPIO14/TDM2RDAT/$\overline{IRQ12}$	H17	$\overline{CS4}$
F22	GPIO19/TDM1RCLK/$\overline{DACK2}$	H18	GPIO24/TDM0RSYN/$\overline{IRQ14}$
G2	HA24	H19	GPIO21/TDM0TSYN
G3	HA27	H20	V_{DD}
G4	HA25	H21	V_{DDH}
G5	HA23	H22	A31
G6	HA17	J2	HA18
G7	$\overline{PWE0}$/$\overline{PSDDQM0}$/$\overline{PBS0}$	J3	HA26
G8	V_{DD}	J4	V_{DD}
G9	V_{DD}	J5	HA13
G10	$\overline{IRQ3}$/BADDR31	J6	GND
G11	BM0/TC0/BNKSEL0	J7	PSDAMUX/PGPL5

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Locator Designator	Signal Name	Locator Designator	Signal Name
J8	BADDR27	L4	HA11
J9	V_{DD}	L5	V_{DDH}
J10	CLKIN	L6	V_{DDH}
J11	BM2/TC2/BNKSEL2	L7	BADDR28
J12	$\overline{\text{DBG}}$	L8	$\overline{\text{IRQ5}}$/BADDR29
J13	V_{DD}	L9	GND
J14	GND	L10	GND
J15	V_{DD}	L14	GND
J16	TT3/$\overline{\text{CS6}}$	L15	V_{DDH}
J17	PSDA10/PGPL0	L16	GND
J18	$\overline{\text{BCTL1}}$/$\overline{\text{CS5}}$	L17	GND
J19	GPIO23/TDM0TDAT/$\overline{\text{IRQ13}}$	L18	$\overline{\text{CS3}}$
J20	GND	L19	V_{DDH}
J21	GPIO25/TDM0RCLK/$\overline{\text{IRQ15}}$	L20	A27
J22	A30	L21	A25
K2	HA15	L22	A22
K3	HA21	M2	HD28
K4	HA16	M3	HD31
K5	$\overline{\text{PWE3}}$/$\overline{\text{PSDDQM3}}$/$\overline{\text{PBS3}}$	M4	V_{DDH}
K6	$\overline{\text{PWE1}}$/$\overline{\text{PSDDQM1}}$/$\overline{\text{PBS1}}$	M5	GND
K7	$\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/PGPL2	M6	GND
K8	$\overline{\text{IRQ2}}$/BADDR30	M7	GND
K9	DLLIN	M8	V_{DD}
K10	GND	M9	V_{DDH}
K11	GND	M10	GND
K12	GND	M14	GND
K13	GND	M15	V_{DDH}
K14	CLKOUT	M16	$\overline{\text{HBRST}}$
K15	V_{DD}	M17	V_{DDH}
K16	TT2/$\overline{\text{CS5}}$	M18	V_{DDH}
K17	ALE	M19	GND
K18	$\overline{\text{CS2}}$	M20	V_{DDH}
K19	GND	M21	A24
K20	A26	M22	A21
K21	A29	N2	HD26
K22	A28	N3	HD30
L2	HA12	N4	HD29
L3	HA14	N5	HD24

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Locator Designator	Signal Name	Locator Designator	Signal Name
N6	PWE2/PSDDQM2/PBS2	R2	HD18
N7	V_{DDH}	R3	V_{DDH}
N8	HWBS0	R4	GND
N9	HBCS	R5	HD22
N10	GND	R6	HWBS6/HDBS6/HWBE6/HDBE6/PWE6/ PSDDQM6/PBS6
N14	GND	R7	HWBS4/HDBS4/HWBE4/HDBE4/PWE4/ PSDDQM4/PBS4
N15	HRDS/HRW/HRDE	R8	TSZ1
N16	BG	R9	TSZ3
N17	HCS	R10	IRQ1/GBL
N18	CS0	R11	V_{DD}
N19	PSDWE/PGPL1	R12	V_{DD}
N20	GPIO26/TDM0RDAT	R13	V_{DD}
N21	A23	R14	TT0
N22	A20	R15	IRQ7/DP7/DREQ4
P2	HD20	R16	IRQ6/DP6/DREQ3
P3	HD27	R17	IRQ3/DP3/DREQ2/EXT_BR3
P4	HD25	R18	TS
P5	HD23	R19	IRQ2/DP2/DACK2/EXT_DBG2
P6	HWBS3	R20	A17
P7	HWBS2	R21	A18
P8	HWBS1	R22	A16
P9	HCLKIN	T2	HD17
P10	GND	T3	HD21
P11	GND_{SYN}	T4	HD1/DSISYNC
P12	V_{CCSYN}	T5	HD0/SWTE
P13	GND	T6	HWBS7/HDBS7/HWBE7/HDBE7/PWE7/ PSDDQM7/PBS7
P14	GND	T7	HWBS5/HDBS5/HWBE5/HDBE5/PWE5/ PSDDQM5/PBS5
P15	TA	T8	TSZ0
P16	BR	T9	TSZ2
P17	TEA	T10	TBST
P18	PSDVAL	T11	V_{DD}
P19	DP0/DREQ1/EXT_BR2	T12	D16
P20	V_{DDH}	T13	TT1
P21	GND	T14	D21
P22	A19	T15	D23

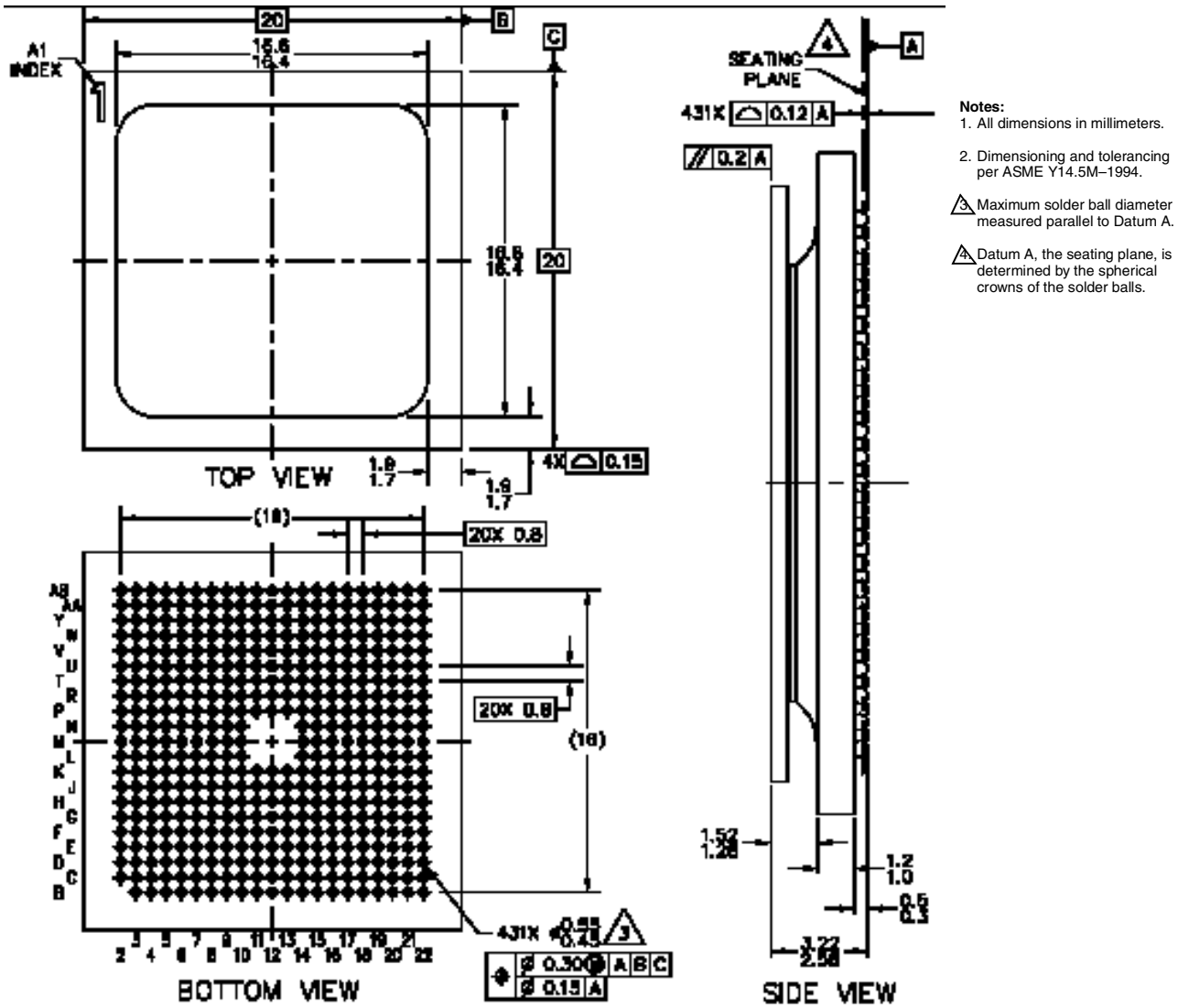
Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Locator Designator	Signal Name	Locator Designator	Signal Name
T16	$\overline{IRQ5}$/DP5/$\overline{DACK4}$/$\overline{EXT\_BG3}$	V12	D13
T17	$\overline{IRQ4}$/DP4/$\overline{DACK3}$/$\overline{EXT\_DBG3}$	V13	D18
T18	$\overline{IRQ1}$/DP1/$\overline{DACK1}$/$\overline{EXT\_BG2}$	V14	D20
T19	D30	V15	GND
T20	GND	V16	D24
T21	A15	V17	D27
T22	A14	V18	D29
U2	HD16	V19	A8
U3	HD19	V20	A9
U4	HD2/DSI64	V21	A10
U5	D2	V22	A11
U6	D3	W2	HD6
U7	D6	W3	HD5/CNFGS
U8	D8	W4	HD4/MODCK2
U9	D9	W5	GND
U10	D11	W6	GND
U11	D14	W7	V_{DDH}
U12	D15	W8	V_{DDH}
U13	D17	W9	GND
U14	D19	W10	HDST1
U15	D22	W11	HDST0
U16	D25	W12	V_{DDH}
U17	D26	W13	GND
U18	D28	W14	HD40/D40
U19	D31	W15	V_{DDH}
U20	V_{DDH}	W16	HD33/D33
U21	A12	W17	V_{DDH}
U22	A13	W18	HD32/D32
V2	HD3/MODCK1	W19	GND
V3	V_{DDH}	W20	GND
V4	GND	W21	A7
V5	D0	W22	A6
V6	D1	Y2	HD7
V7	D4	Y3	HD15
V8	D5	Y4	V_{DDH}
V9	D7	Y5	HD9
V10	D10	Y6	V_{DD}
V11	D12	Y7	HD60/D60

Table 3-2. MSC8102 Signal Listing by Ball Designator (Continued)

Locator Designator	Signal Name	Locator Designator	Signal Name
Y8	HD58/D58	AA16	GND
Y9	GND	AA17	HD42/D42
Y10	V_{DDH}	AA18	HD38/D38
Y11	HD51/D51	AA19	HD35/D35
Y12	GND	AA20	A0
Y13	V_{DDH}	AA21	A2
Y14	HD43/D43	AA22	A3
Y15	GND	AB2	GND
Y16	V_{DDH}	AB3	HD13
Y17	GND	AB4	HD11
Y18	HD37/D37	AB5	HD8
Y19	HD34/D34	AB6	HD62/D62
Y20	V_{DDH}	AB7	HD61/D61
Y21	A4	AB8	HD57/D57
Y22	A5	AB9	HD56/D56
AA2	V_{DD}	AB10	HD55/D55
AA3	HD14	AB11	HD53/D53
AA4	HD12	AB12	HD50/D50
AA5	HD10	AB13	HD49/D49
AA6	HD63/D63	AB14	HD48/D48
AA7	HD59/D59	AB15	HD47/D47
AA8	GND	AB16	HD45/D45
AA9	V_{DDH}	AB17	HD44/D44
AA10	HD54/D54	AB18	HD41/D41
AA11	HD52/D52	AB19	HD39/D39
AA12	V_{DDH}	AB20	HD36/D36
AA13	GND	AB21	A1
AA14	V_{DDH}	AB22	V_{DD}
AA15	HD46/D46		

3.2 FC-CBGA (HCTE) Package Mechanical Drawing



CASE 1453-02

Figure 3-3. MSC8102 Mechanical Information, 431-pin FC-CBGA (HCTE) Package

Design Considerations 4

This chapter includes design and layout guidelines for manufacturing boards using the MSC8102.

4.1 Power Supply Design and Layout Considerations

The input voltage must not exceed the I/O supply V_{DDH} by more than 2.5 V at any time, including during power-on reset. In turn V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 2.6 V at any time, including during power-on reset. V_{DD}/V_{CCSYN} must not exceed V_{DDH} by more than 0.4 V at any time, including during power-on reset.

Use the following guidelines for power-up and power-down sequences:

- Assert $\overline{\text{PORESET}}$ before applying power and keep the signal driven low until the power reaches the required minimum power levels. This can be implemented via a weak pull-down resistor.
- CLKIN can be held low or allowed to toggle during the beginning of the power-up sequence. However, CLKIN must start toggling before the deassertion of $\overline{\text{PORESET}}$ and after both power supplies have reached nominal voltage levels.
- To maintain the proper relationship and power-up sequence between the power levels, the recommendation is to use “bootstrap” diodes between the power rails, as shown in **Figure 4-1**.

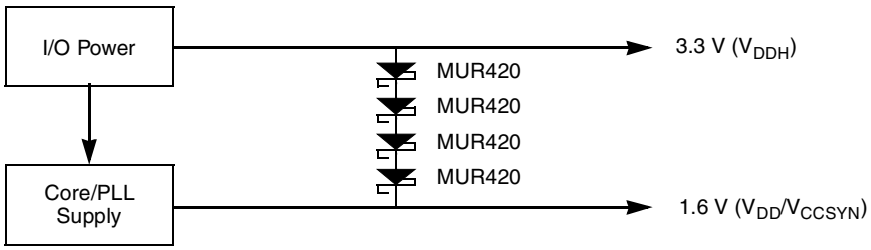


Figure 4-1. Bootstrap Diodes for Power-Up Sequencing

Select the bootstrap diodes such that a nominal V_{DD}/V_{CCSYN} is sourced from the V_{DDH} power supply until the V_{DD}/V_{CCSYN} power supply becomes active. In **Figure 4-1**, four MUR420 Schottky barrier diodes are connected in series; each has a forward voltage (V_F) of 0.6 V at high currents, so these diodes provide a 2.4 V drop, maintaining 0.9 V on the 1.6 V power line. Once the core/PLL power supply stabilizes at 1.6 V, the bootstrap diodes will be reverse biased with negligible leakage current. The V_F should be effective at the current levels required by the processor. Do not use diodes with a nominal V_F that drops too low at high current. **Figure 4-2** shows the recommended power decoupling circuit for the core power supply. The voltage regulator and the decoupling capacitors should supply the required device current without any drop in voltage on the device pins. The voltage on the package pins should not drop below 1.5 V even for a very short spikes. This can be achieved by using the following guidelines:

— For the core supply, use a voltage regulator rated at 1.6 V with nominal rating of at least 3 A. This rating does not reflect actual average current draw, but is recommended because it resists changes imposed by transient spikes and has better voltage recovery time than lower current rated supplies.

— Decouple the supply using low-ESR capacitors mounted as close as possible to the socket. **Figure 4-2** shows three capacitors in parallel to reduce the resistance. Three capacitors is a recommended minimum number. If possible, mount at least one of the capacitors directly below the MSC8102 device.

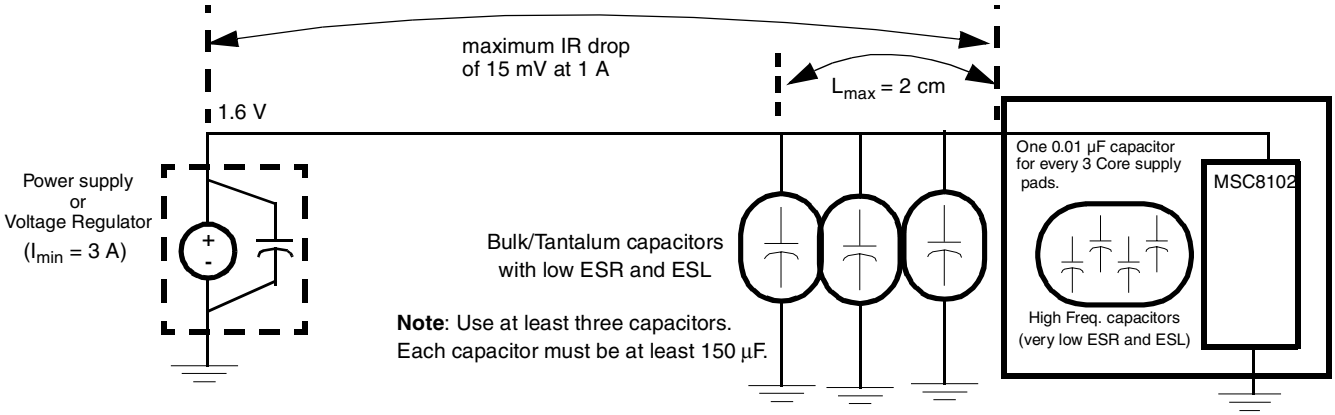


Figure 4-2. Core Power Supply Decoupling

Each V_{CC} and V_{DD} pin on the MSC8102 should be provided with a low-impedance path to the board power supply. Similarly, each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC}, V_{DD}, and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MSC8102 have fast rise and fall times. PCB trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PCB trace lengths of six inches are recommended. For the DSI control signals in Synchronous mode, make sure that the layout supports the DSI AC timing requirements and minimizes any signal crosstalk. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC}, V_{DD}, and GND circuits. Pull up all unused inputs or signals that will be inputs during reset.

Special care should be taken to minimize the noise levels on the PLL supply pins. There is one pair of PLL supply pins: V_{CCSYN}-GND_{SYN}. To ensure internal clock stability, filter the power to the V_{CCSYN} input with a circuit similar to the one in **Figure 4-3**. To filter as much noise as possible, place the circuit as close as possible to V_{CCSYN}. The 0.01-µF capacitor should be closest to V_{CCSYN}, followed by the 10-µF capacitor, the 10-nH inductor, and finally the 10-Ω resistor to V_{DD}. These traces should be kept short and direct. Provide an extremely low impedance path to ground

for GND_{SYN}. Bypass GND_{SYN} to V_{CCSYN} with a 0.01-µF capacitor as close as possible to the chip package. For best results, place this capacitor on the backside of the PCB aligned with the depopulated void on the MSC8102 located in the square defined by positions, L11, L12, L13, M11, M12, M13, N11, N12, and N13.

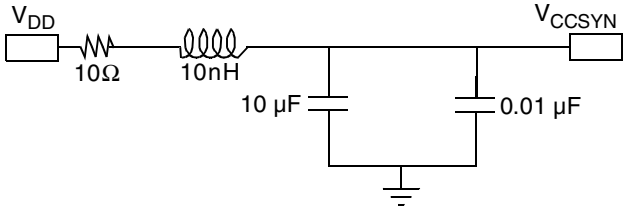


Figure 4-3. V_{CCSYN} Bypass

Note: See the *MSC8102 Design Checklist* (AN2506) for additional information.

4.2 Connectivity Guidelines

Unused output pins can be disconnected, and unused input pins should be connected to their non-active value, except for the following:

- If the DSI is unused (bit DDR[DSIDIS] is set), then $\overline{HCS}$ and $\overline{HBCS}$ must be tied to V_{DD} and all the rest of the DSI signals can be disconnected.
- When the DSI uses Synchronous mode, $\overline{HTA}$ must be pulled up. In asynchronous mode, $\overline{HTA}$ should be pulled either up or down depending on design requirements.
- $\overline{HDST}$ can be disconnected if the DSI is in Big-endian mode, or if the DSI is in Little-endian mode and DCR[DSRFA] bit is set.
- When the DSI is in 64-bit data bus mode and DCR[BEM] is cleared, $\overline{HWBS[1–3]}$/$\overline{HDBS[1–3]}$/$\overline{HWBE[1–3]}$/$\overline{HDBE[1–3]}$ and $\overline{HWBS[4–7]}$/$\overline{HDBS[4–7]}$/$\overline{HWBE[4–7]}$/$\overline{HDBE[4–7]}$/$\overline{PWE[4–7]}$/$\overline{PSDDQM[4–7]}$/$\overline{PBS[4–7]}$ must be tied to V_{DD}.
- When the DSI is in 32-bit data bus mode and DCR[BEM] is cleared, $\overline{HWBS[1–3]}$/$\overline{HDBS[1–3]}$/$\overline{HWBE[1–3]}$/$\overline{HDBE[1–3]}$ must be tied to V_{DD}.
- When the DSI is in Asynchronous mode, $\overline{HBRST}$ and HCLKIN should either be disconnected or tied to V_{DD}.
- When using the DSI in Synchronous mode, use special care when laying out the control signals. Test the layout to make sure that it supports the specified DSI AC timing values and minimizes signal cross-coupling.
- The following signals can be disconnected in single-master mode (BCR[EBM] is reset): $\overline{BG}$, $\overline{DBG}$, $\overline{EXT\_BG[2–3]}$, $\overline{EXT\_DBG[2-3]}$, $\overline{GBL}$ and $\overline{TS}$.
- The following signals must be pulled up: $\overline{HRESET}$, $\overline{SRESET}$, $\overline{ARTRY}$, $\overline{TA}$, $\overline{TEA}$, $\overline{PSDVAL}$, and $\overline{AACK}$.
- In single-master mode, $\overline{ABB}$ and $\overline{DBB}$ can be selected as $\overline{IRQ}$ inputs and be connected to the non-active value. In other modes, they must be pulled up.

- In single-master mode with the DLL disabled (that is, the DLLDIS bit in the Hard Reset Configuration Word is set), the following connections should be used:
  - Connect the oscillator output through a buffer to CLKIN.
  - Connect DLLIN to GND (pull low).
  - Connect CLKOUT through a zero-delay buffer to the slave device (for example, SDRAM) using the following guidelines:
    - The maximum delay between the slave and CLKOUT must not exceed 0.7 ns.
    - The maximum load on CLKOUT must not exceed 10 pF.
    - Use a zero-delay buffer with a jitter less than 0.3 ns.
- If the 60x-compatible system bus is not used and SIUMCR[PBSE] is set, you can disconnect $\overline{\text{PPBS}}$. Otherwise, pull the signal up.
- The following signals: SWTE, DSISYNC, DSI64, MODCK[1–2], CNFGS, CHIPID[0–3], RSTCONF and BM[0–2] are used to configure the MSC8102 and are sampled on the deassertion of the $\overline{\text{PORESET}}$ signal. Therefore, they should be tied to GND or V_{DD} either directly or through a pull-down or a pull-up resistor until the deassertion of the $\overline{\text{PORESET}}$ signal.
- You must pull up $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{DBG}}$, $\overline{\text{EXT\_BR[2–3]}}$, $\overline{\text{EXT\_BG[2–3]}}$, $\overline{\text{EXT\_DBG[2–3]}}$, and $\overline{\text{TS}}$ if the BCR[EBM] bit is set.
- When they are used, you must pull up $\overline{\text{INT\_OUT}}$ (if SIUMCR[INTODC] is cleared), $\overline{\text{NMI\_OUT}}$, and $\overline{\text{IRQxx}}$ (if not full drive).

Note: For details on configuration, see the *MSC8102 User's Guide* and *MSC8102 Reference Manual*.

4.3 Recommended Clock Connections for Single-Master Mode with DLL Off

Use the guidelines shown in **Figure 4-4** to connect CLKOUT to a slave device, such as an SDRAM. The zero-delay buffer can use internal or external feedback.

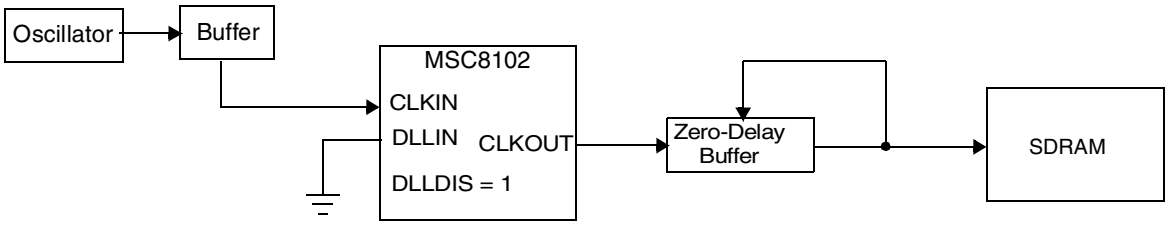


Figure 4-4. Example Clock Distribution In Single-Master Mode with DLL Disabled

Because the connection uses open loop timing between the internal and external clock (CLKOUT), the design must adhere to the following requirements:

- The maximum delay between the CLKOUT pin to the SDRAM must be less than 0.7 ns.
- The maximum external load on CLKOUT must not exceed 10 pF.
- The zero-delay buffer must have a jitter of less than 0.3 ns.

4.4 Power Considerations

The internal power dissipation consists of three components:

$$P_{INT} = P_{TCORE} + P_{SIU} + P_{BUSES} + P_{PERIPH}$$

The power dissipation depends on the operating frequency of the different portions of the chip. To determine the power dissipation at a given frequency, the following equations should be applied:

$P_{CORE}\ (f_c) = ((P_{CORE} - P_{LCO})/275) \times f_c + P_{LCO}$
$P_{TCORE}\ (f_c) = (P_{CORE} \times 4)$
$P_{SIU}\ (f_c) = ((P_{SIU} - P_{LSI})/91.67) \times f_c + P_{LSI}$
$P_{PERIPH}\ (f_c) = ((P_{PERIPH} - P_{LPE})/91.67) \times f_c + P_{LPE}$
$P_{BUSES}\ (f_c) = P_{BUSES}\ /91.67 \times f_c$
Where,
f_c is the operating frequency in MHz and all power numbers are in mW
P_{LCO} is the SC140 Core leakage power
P_{LSI} is the SIU leakage power
P_{LPE} is the peripheral leakage power

To determine a total power dissipation in a specific application, the following equation should be applied for each I/O output pin:

$$P = C \times V_{DDH}^2 \times f_s \times 10^{-3} \qquad \textbf{Equation 1}$$

Where:

P = power in mW
C = load capacitance in pF
f_s = output switching frequency in MHz.

4.5 Thermal Design Considerations

An estimation of the chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textbf{Equation 2}$$

where

T_A = ambient temperature near the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)
$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)
$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC8102 are listed in **Table 2-3**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm^2 with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip. You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case that is painted black. The MSC8102 device case surface is too shiny (low emissivity) to yield an accurate infrared temperature measurement. Use the following equation to determine T_J:

$$T_J = T_T + (\theta_{JA} \times P_D) \quad \textbf{Equation 3}$$

where

T_T = thermocouple (or infrared) temperature on top of the package (°C)
θ_{JA} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

Note: See *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601).

Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Order Number
MSC8102	1.6 V core 3.3 V I/O	High Temperature Coefficient for Expansion Flip Chip Ceramic Ball Grid Array (FC-CBGA (HCTE))	431	250	MSC8102M4000
				275	MSC8102M4400

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