NTA5332

NTAG 5 boost - NFC Forum-compliant I²C bridge for tiny devices

Rev. 1.1 — 2 October 2019
547511

Objective short data sheet
COMPANY PUBLIC

1 General description

NTAG 5 boost uses active load modulation (ALM) to deliver robust and reliable communication with NFC phones, bringing a new level of convenience to tiny devices.

NXP's NTAG 5 boost shrinks the NFC footprint while adding AES security, so designers can deliver ultra-compact devices for use in IoT, consumer, and industrial applications. It offers an NFC Forum-compliant contactless interface that delivers exceptional read range, giving tiny devices the ability to interact with the cloud and other NFC-enabled devices, including smartphones.

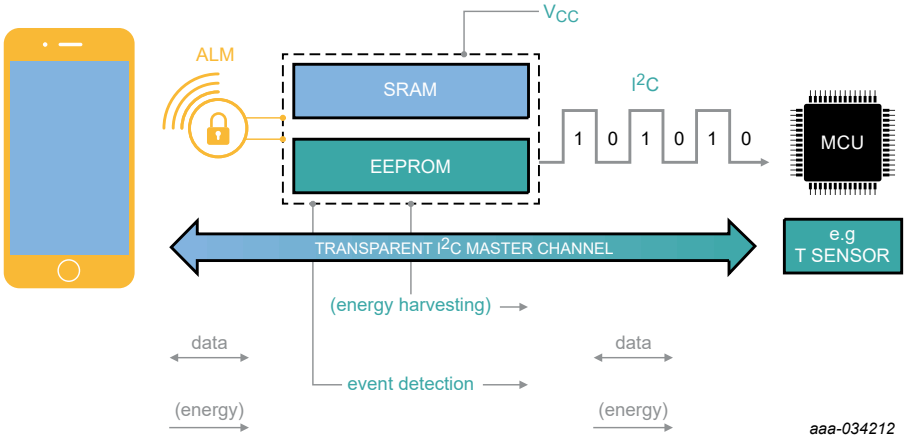


Figure 1. NTAG 5 boost overview

ALM allows construction of a compact yet highly reliable antenna, creating a significantly smaller footprint without compromising the read range. When operating in ALM mode, the read range is significantly longer than when operating in passive mode.

An energy-efficient design, equipped with a hard power-down mode and a standby current of less than 10 µA, ensures long battery life.

2048 bytes (16384 bits) of user memory can be divided into three areas, and each area can use a different protection level, varying from no protection to 32-/64-bit password protection or up to 128-bit AES-protected read/write access with mutual authentication. Different parties in the value chain can have their own dedicated memory areas for storing access data.

The NTAG 5 boost comes with pre-programmed proof-of-origin functionality to verify authenticity. The elliptic curve cryptography (ECC) based originality signature can be locked or reprogrammed by the customer.

With NTAG 5 boost, the device can connect to the cloud with a single tap. The connection uses an NFC Forum-compliant data exchange mechanism involving 256 bytes (2048 bits) SRAM to ensure highly interoperable data transfers.

2 Features and benefits

- Antenna size reduction by a factor of 40, same read range as in passive load modulation
- Long battery life due to low standby current and hard power-down
- Adjustable security levels up to mutual AES authentication
- Flexible split between three open and/or protected memory areas
- Ensured authenticity of product through value chain
- Interoperable data exchange according to NFC Forum standards
- Interoperable and high performance NFC interface
  - ISO/IEC 15693 and NFC Forum Type 5 Tag compliant
  - 64-bit Unique IDentifier
- Reliable and robust memory
  - 2048 bytes (16384 bits) user EEPROM on top of configuration memory
  - 256 bytes (2048 bits) SRAM for frequently changing data and pass-through mode
  - 40 years data retention
  - Write endurance of 1 000 000 cycles
- Configurable contact interface
  - I²C slave standard (100 kHz) and fast (400 kHz) mode
  - Transparent I²C master channel (for example, read sensors without an MCU)
  - One configurable event detection pin
  - Two GPIOs as multiplexed I²C lines
  - Two Pulse Width Modulation (PWM) channels as multiplexed GPIOs and/or ED pin
  - 1.62 V to 5.5 V supply voltage
- Scaleable security for access and data protection
  - Disable NFC interface temporarily
  - Disable I²C interface temporarily
  - NFC PRIVACY mode
  - Read-only protection as defined in NFC Forum Type 5 Tag Specification
  - Full, read-only, or no memory access based on 32-bit password from both interfaces
  - Optional 64-bit password protection from NFC perspective
  - 128-bit AES authentication as defined in ISO/IEC 15693
  - ECC-based reprogrammable originality signature
- Multiple fast data transfer mode
  - Pass-through mode with 256 byte SRAM buffer
  - Standardized data transfer mode (PHDC, TNEP)
- Low-power budget application support
  - Energy harvesting with configurable output voltage up to 30 mW
  - Low-power standby current <10 µA
  - Hard power down current <0.25 µA
- Very robust architecture
  - -40 °C to 85°C
- Extensive product support package
  - Feature specific application notes
  - Development board including software and source code
  - Hands-on training

3 Applications

- Use cases
  - Simple dynamic secure pairing
  - Commissioning
  - Parameterization
  - Diagnosis
  - Firmware download
  - Low BoM and low-power data acquisition for sensors
  - Calibration
  - Trimming
  - Authenticity check and data protection
  - Late "in the box" configuration
  - LED driver configuration
  - NFC Charging
- Applications
  - Lighting
  - Smart home
  - Hearable and Wearable
  - Consumer
  - Industrial
  - Gaming
  - Smart sensor
  - Smart metering

4 Quick reference data

Table 1. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
General							
f_i	input frequency	ISO/IEC 15693		13.553	13.56	13.567	MHz
Operating conditions							
T_{amb}	ambient temperature			-40	25	85	°C
V_{CC}	supply voltage	on pin V_{CC}		1.62	-	5.5	V
Current consumption							
I_{VCC}	V_{CC} supply current	V_{CC} = 1.8 V		-	150	-	µA
$I_{standby\ Vcc}$	standby current	V_{CC} = 5.5 V wake-up Active NFC level detector and I^2C		-	10	-	µA
Energy harvesting VOUT pad (passive mode)							
V_{out}	output voltage	load current <= configured output current		1.62	-	3.3	V
C_L	load capacitance	needs to come from calculation		-	1.1	-	µF

5 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
NTA53321G0FHK	XQFN16	NTAG 5 boost with I²C master/slave interface, AES authentication, ALM and 2048 bytes user EEPROM plastic, extremely thin quad flat package; no leads; 16 terminals	SOT1161-2
NTA53321G0FTT	TSSOP16	NTAG 5 boost with I²C master/slave interface, AES authentication, ALM and 2048 bytes user EEPROM plastic, thin shrink small outline package; 16 leads; 0.65 mm pitch; 5 mm x 4.4 mm x 1.1 mm body	SOT403-1
NTA53321G0FUA	Wafer	NTAG 5 boost; 8 inch wafer, 150 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format)	-

REMARK: Wafer specification addendum is available after exchange of a non-disclosure agreement (NDA)

6 Block diagram

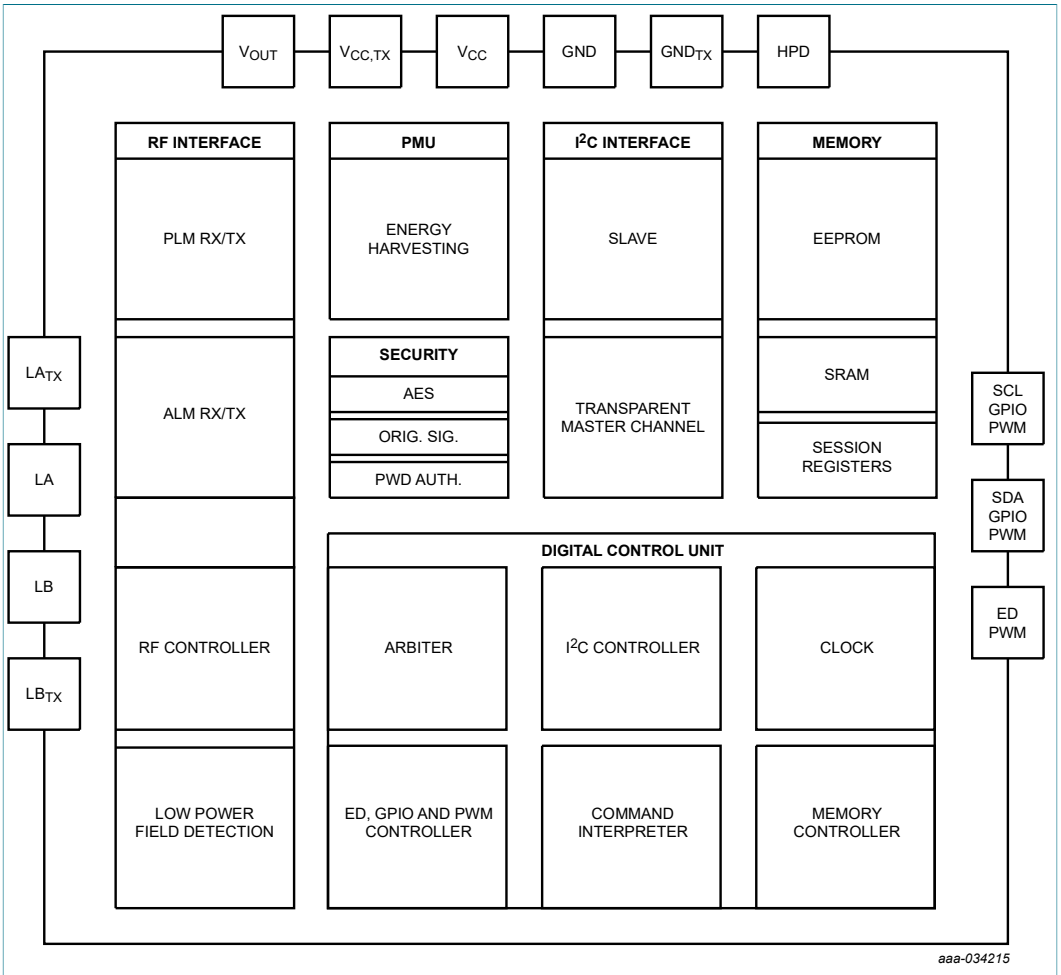
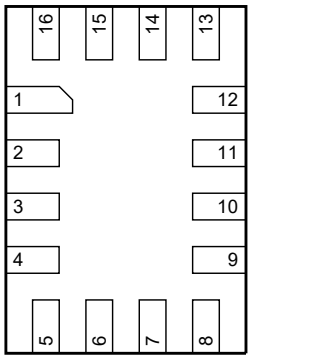


Figure 2. Block diagram NTAG 5 boost

7 Pinning Information



Transparent top view

Figure 3. Pin configuration for XQFN16 package

Table 3. Pin description for XQFN16

Pin	Symbol	Description	When unused
1	GND	Ground	connect to GND
2	GND_{TX}	Ground for ALM	connect to GND
3	$V_{CC,TX}$	External power supply for ALM	keep floating
4	N.C.	not connected	keep floating
5	N.C.	not connected	keep floating
6	SDA/GPIO1/PWM1	Multiplexed serial data I²C, GPIO1 and PWM1	keep floating
7	SCL/GPIO0/PWM0	Multiplexed serial clock I²C, GPIO0 and PWM0	keep floating
8	ED/PWM0	Multiplexed event detection and PWM0	keep floating
9	V_{CC}	External power supply	keep floating
10	HPD	Hard power down	keep floating
11	GND	Ground	connect to GND
12	V_{OUT}	Energy harvesting voltage output	keep floating
13	LB_{TX}	Antenna connection TX	keep floating
14	LB	Antenna connection	keep floating
15	LA	Antenna connection	keep floating
16	LA_{TX}	Antenna connection TX	keep floating

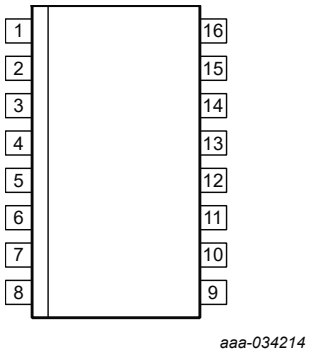


Figure 4. Pin configuration for TSSOP16 package

Table 4. Pin description for TSSOP16

Pin	Symbol	Description	When unused
1	LA	Antenna connection	keep floating
2	LA_{TX}	Antenna connection TX	keep floating
3	GND	Ground	connect to GND
4	GND_{TX}	Ground for ALM Ground	connect to GND
5	$V_{CC,TX}$	External power supply for ALM	keep floating
6	N.C.	not connected	keep floating
7	N.C.	not connected	keep floating
8	SDA/GPIO1/PWM1	Multiplexed serial data I²C, GPIO1 and PWM1	keep floating
9	SCL/GPIO0/PWM0	Multiplexed serial clock I²C, GPIO0 and PWM0	keep floating
10	ED/PWM0	Multiplexed event detection and PWM0	keep floating
11	V_{CC}	External power supply	keep floating
12	HPD	Hard power down	keep floating
13	GND	Ground	connect to GND
14	V_{OUT}	Energy harvesting voltage output	keep floating
15	LB_{TX}	Antenna connection TX	keep floating
16	LB	Antenna connection	keep floating

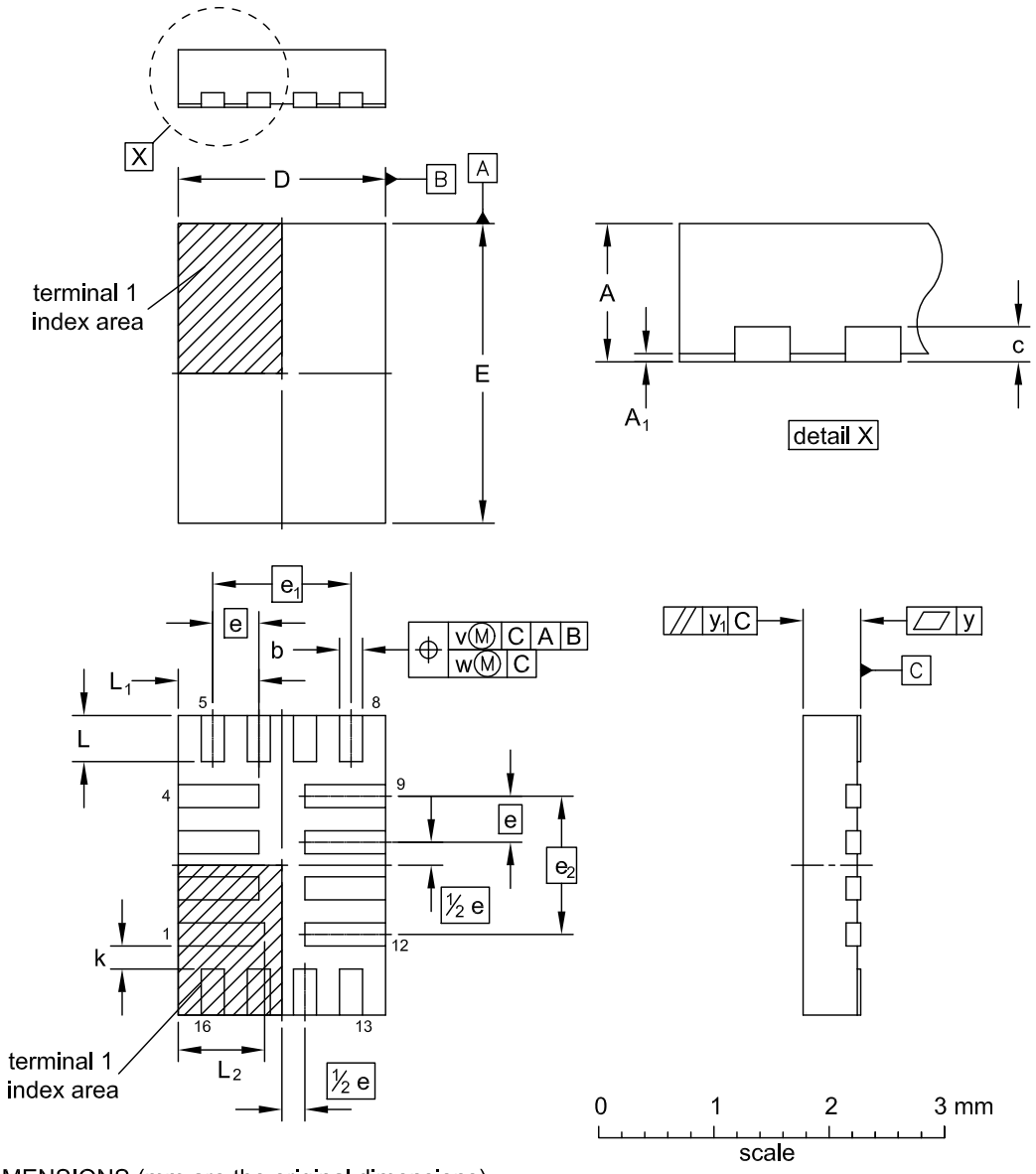
8 Limiting values

Table 5. Limiting values In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{stg}	storage temperature	all packages	-65	+150	°C
T_j	junction temperature		-	+95	°C
V_{ESD}	electrostatic discharge voltage	Charge Device Model [1]	-2	2	kV
		Human Body Model [2]	-2	2	kV
V_{CC}	supply voltage	on pin V_{CC}	-0.5	7.15	V
V_{CC}	supply voltage	on pin V_{CC_TX}	-0.5	7.15	V
V_i	input voltage	on pin SDA, SCL,ED, HPD	-0.5	7.15	V
$V_{I\ (RF)}$	RF input voltage	on pin LA/LB	-0.5	5.2	Vp
V_i	input voltage	on pin LA; LB is 0 V; sine wave of 13.56 MHz	-0.5	5.2	Vp
		on pin LB; LA is 0 V; sine wave of 13.56 MHz	-0.5	5.2	Vp
V_i	input voltage	on pin LA_TX, LB_TX	-0.5	4.7	V
$I_{i(max)}$	maximum input current	La/Lb; peak	-168	168	mA

[1] CDM: ANSI/ESDA/JEDEC JS-002
[2] HBM: ANSI/ESDA/JEDEC JS-001

9 Package outline



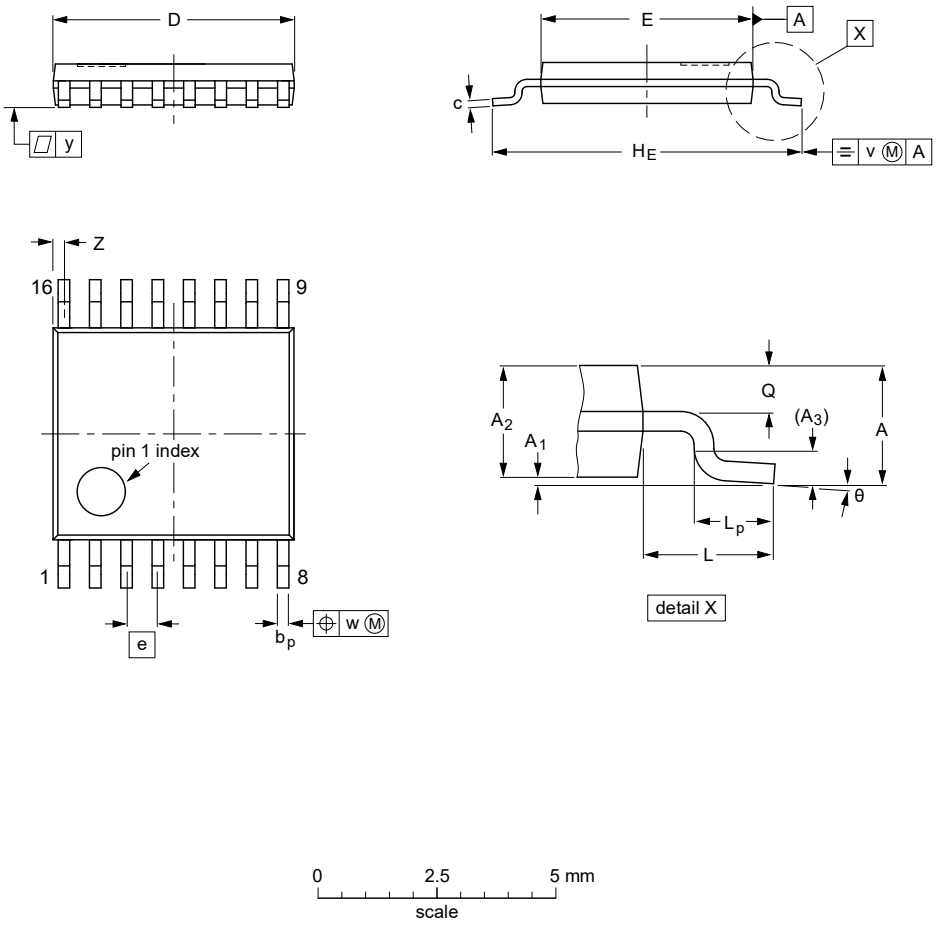
DIMENSIONS (mm are the original dimensions)

UNIT		$A^{(1)}$	A_1	b	c	$D^{(1)}$	$E^{(1)}$	e	e_1	e_2	k	L	L_1	L_2	v	w	y	y_1
mm	MAX	0.50	0.05	0.25		1.90	2.70					0.45	0.75	0.80				
	NOM			0.20	0.127	1.80	2.60	0.40	1.20	1.20	0.2	0.40	0.70	0.75	0.1	0.05	0.05	0.1
	MIN		0.00	0.15		1.70	2.50					0.35	0.65	0.70				

Notes
1. Plastic or metal protrusions of 0.075 maximum per side are not included.

Figure 5. Package outline XQFN16

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Figure 6. Package outline TSSOP16

10 Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

11 References

[1] NFC Forum specification, Type 5 Tag - Technical Specification Version 1.0 2018-04-27 [T5T] NFC Forum™
https://nfc-forum.org/product-category/specification/

[2] ISO/IEC 15693
https://www.iso.org/ics/35.240.15/x/

[3] UM10204 - I2C-bus specification and user manual
https://www.nxp.com/docs/en/user-guide/UM10204.pdf

12 Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTA5332_SDS v.1.1	20191002	Objective short data sheet		v.1.0
NTA5332_SDS v.1.0	20190528	Objective short data sheet		-
	• Initial version			

13 Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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