NTP5210

NTAG 5 switch - NFC Forum- compliant PWM and GPIO bridge

Rev. 1.1 — 2 October 2019 Objective short data sheet
547711 COMPANY PUBLIC

1 General description

Designed as an MCU replacement in various gaming and lighting applications, this NFC tag adds connectivity and increases flexibility while saving energy and lowering the bill of materials.

NXP's NTAG 5 switch lets designers eliminate the MCU in selected gaming and lighting applications and other cost sensitive designs, for added functionality, connectivity, and efficiency at a lower cost. Operating at 13.56 MHz, it is an NFC Forum-compliant contactless tag that can be read by any NFC-enabled device at close range and by an ISO/IEC 15693-enabled industrial reader over a longer range. Easy configuration supports a range of control functions, and the integrated originality check lets the user verify an end product's authenticity.

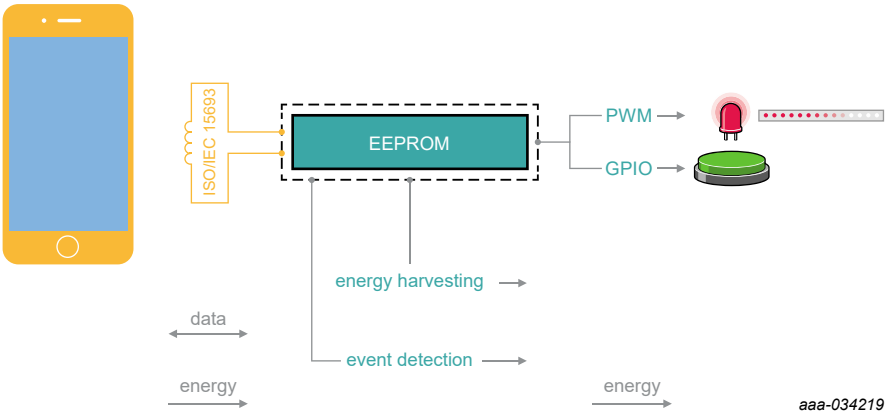


Figure 1. NTAG 5 switch overview

In some lighting and gaming applications, NTAG 5 switch enables simple and cost-effective designs without a microcontroller. It implements multiplexed pins, offering general-purpose I/O (GPIO) and pulse width modulation (PWM) as well as NFC field detection. The characteristics of the PWM or GPIO signal can be configured through the NFC interface. These features can be used to switch on/off and control motor speed or LED brightness.

Support for ISO/IEC 15693 lets the NTAG 5 switch communicate securely in two ways — with powerful industrial readers, at a range of up to 60 cm and with NFC-enabled devices within proximity range. This duality makes it possible for the device to be calibrated and parameterized automatically while in the factory and then, when put to use in the field, safely communicate with contactless devices such as NFCenabled smartphones.

The tag's 512 bytes of memory can be divided into three areas, and each area can use a different protection level, varying from no protection to 32-/64-bit, password-protected read/write access. Different parties in the value chain can have their own dedicated memory areas for storing access data.

The NTAG 5 switch comes with pre-programmed proof-of-origin functionality to verify authenticity. The elliptic curve cryptography (ECC) based originality signature can be locked or reprogrammed by the customer.

The NTAG 5 is a powerhouse, harvesting the energy from an NFC Reader, it can operate without a battery. Better yet, with its configurable output voltage, it can power a circuit, a sensor network and even charge a super capacitor wireless.

2 Features and benefits

- Reading distance with long-range reader > 60 cm (> 25 inches)
- Flexible operation with PWM/GPIO interface
- Flexible split between three open and/or protected memory areas
- Ensured authenticity of product through value chain
- Interoperable data exchange according to NFC Forum standards
- Energy-efficient design with reduced bill of material
- Interoperable and high performance NFC interface
  - ISO/IEC 15693 and NFC Forum Type 5 Tag compliant
  - 64-bit Unique IDentifier
- Reliable and robust memory
  - 512 bytes (4096 bits) user EEPROM on top of configuration memory
  - 40 years data retention
  - Write endurance of 1 000 000 cycles
- Configurable contact interface
  - One configurable event detection pin
  - Two GPIOs
  - Two Pulse Width Modulation (PWM) channels as multiplexed GPIOs and/or ED pin
  - 1.62 V to 5.5 V supply voltage
- Scaleable security for access and data protection
  - Disable NFC interface temporarily
  - NFC PRIVACY mode
  - Read-only protection as defined in NFC Forum Type 5 Tag Specification
  - Full, read-only, or no memory access based on 32-bit password
  - Optional 64-bit password protection
  - ECC-based reprogrammable originality signature
- Low-power budget application support
  - Energy harvesting with configurable output voltage up to 30 mW
  - Low-power standby current <6 µA
  - Hard power down current <0.25 µA
- Very robust architecture
  - -40 °C to 85°C
- Extensive product support package
  - Feature specific application notes
  - Development board including software and source code
  - Hands-on training

3 Applications

- Use cases
  - Calibration
  - Trimming
  - Authenticity check and data protection
  - Late "in the box" configuration
  - LED driver configuration
  - NFC Charging
- Applications
  - Lighting
  - Smart home
  - Hearable and Wearable
  - Consumer
  - Industrial
  - Gaming

4 Quick reference data

Table 1. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
General							
f_i	input frequency	ISO/IEC 15693		13.553	13.56	13.567	MHz
Operating conditions							
T_{amb}	ambient temperature			-40	25	85	°C
V_{CC}	supply voltage	on pin V_{CC}		1.62	-	5.5	V
Current consumption							
I_{VCC}	V_{CC} supply current	V_{CC} = 1.8 V		-	150	-	µA
Energy harvesting VOUT pad							
V_{out}	output voltage	load current <= configured output current		1.62	-	3.3	V
C_L	load capacitance	needs to come from calculation		-	1.1	-	µF

5 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
NTP52101G0JHK	XQFN16	NTAG 5 switch with GPIOs, PWM and 512 bytes user EEPROM plastic, extremely thin quad flat package; no leads; 16 terminals	SOT1161-2
NTP52101G0JTT	TSSOP16	NTAG 5 switch with GPIOs, PWM and 512 bytes user EEPROM plastic, thin shrink small outline package; 16 leads; 0.65 mm pitch; 5 mm x 4.4 mm x 1.1 mm body	SOT403-1
NTP52101G0JT	SO8	NTAG 5 switch with GPIOs, PWM and 512 bytes user EEPROM plastic, small outline package; 8 leads; 1.27 mm pitch; 4.9 mm x 3.9 mm x 1.75 mm body	SOT96-1
NTP52101G0FUA	Wafer	NTAG 5 switch; 8 inch wafer, 150 µm thickness, on film frame carrier, electronic fail die marking according to SECS-II format)	-

REMARK: Wafer specification addendum is available after exchange of a non-disclosure agreement (NDA)

6 Block diagram

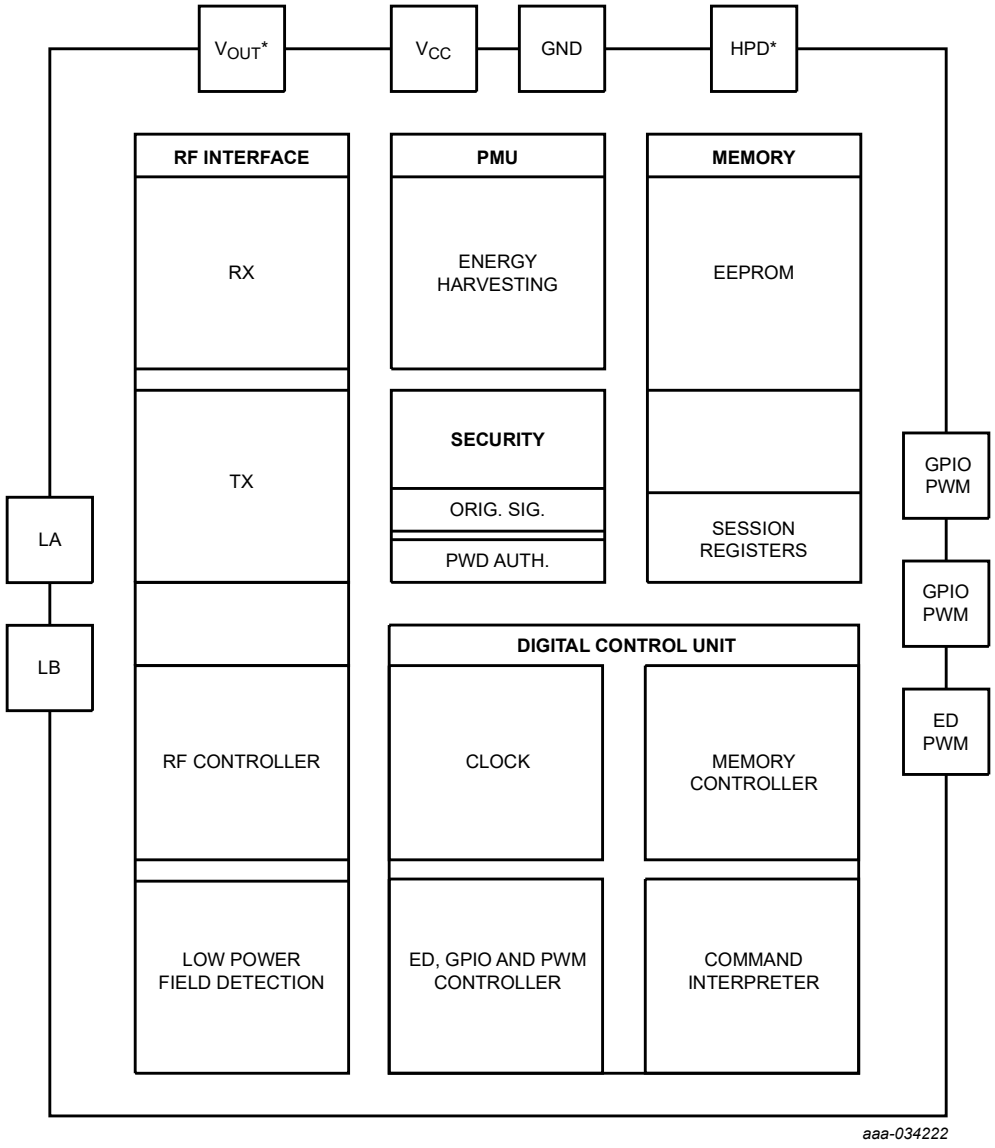
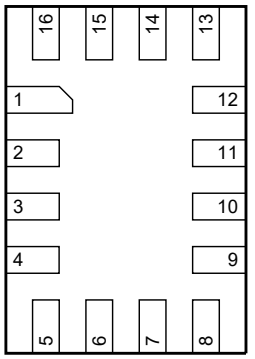


Figure 2. Block diagram NTAG 5 switch

[1]

[1] HPD and V_{OUT} are not available for SO8 package

7 Pinning Information



Transparent top view

Figure 3. Pin configuration for XQFN16 package

Table 3. Pin description for XQFN16

Pin	Symbol	Description	When unused
1	GND	Ground	connect to GND
2	GND	Ground	connect to GND
3	N.C.	not connected	keep floating
4	N.C.	not connected	keep floating
5	N.C.	not connected	keep floating
6	GPIO1/PWM1	Multiplexed GPIO1 and PWM1	keep floating
7	GPIO0/PWM0	Multiplexed GPIO0 and PWM0	keep floating
8	ED/PWM0	Multiplexed event detection and PWM0	keep floating
9	V_{CC}	External power supply	keep floating
10	HPD	Hard power down	keep floating
11	GND	Ground	connect to GND
12	V_{OUT}	Energy harvesting voltage output	keep floating
13	N.C.	not connected	keep floating
14	LB	Antenna connection	keep floating
15	LA	Antenna connection	keep floating
16	N.C.	not connected	keep floating

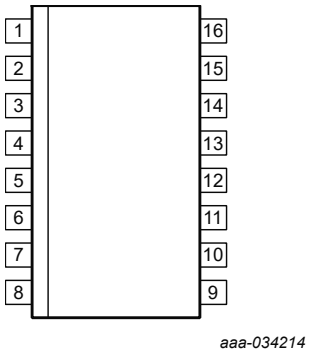


Figure 4. Pin configuration for TSSOP16 package

Table 4. Pin description for TSSOP16

Pin	Symbol	Description	When unused
1	LA	Antenna connection	keep floating
2	N.C.	not connected	keep floating
3	GND	Ground	connect to GND
4	GND	Ground	connect to GND
5	N.C.	not connected	keep floating
6	N.C.	not connected	keep floating
7	N.C.	not connected	keep floating
8	GPIO1/PWM1	Multiplexed GPIO1 and PWM1	keep floating
9	GPIO0/PWM0	Multiplexed GPIO0 and PWM0	keep floating
10	ED/PWM0	Multiplexed event detection and PWM0	keep floating
11	V_{CC}	External power supply	keep floating
12	HPD	Hard power down	keep floating
13	GND	Ground	connect to GND
14	V_{OUT}	Energy harvesting voltage output	keep floating
15	N.C.	not connected	keep floating
16	LB	Antenna connection	keep floating

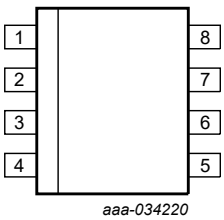


Figure 5. Pin configuration for SO8 package

Table 5. Pin description for SO8

Pin	Symbol	Description	When unused
1	GND	Ground	connect to GND
2	LA	Antenna connection	keep floating
3	LB	Antenna connection	keep floating
4	GND	Ground	connect to GND
5	GPIO1/PWM1	Multiplexed GPIO1 and PWM1	keep floating
6	GPIO0/PWM0	Multiplexed GPIO0 and PWM0	keep floating
7	ED/PWM0	Multiplexed event detection and PWM0	keep floating
8	V_{CC}	External power supply	keep floating

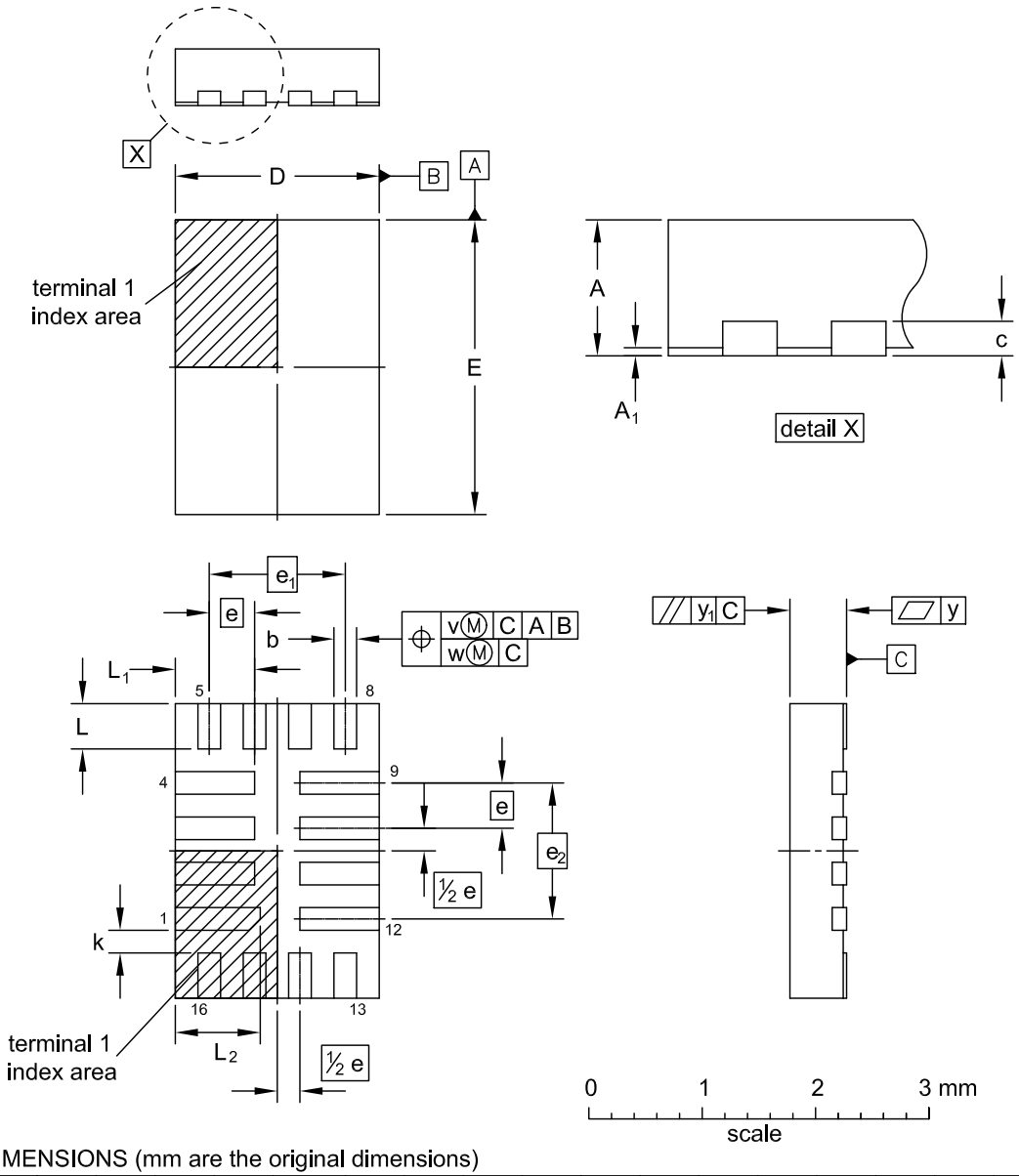
8 Limiting values

Table 6. Limiting values In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{stg}	storage temperature	all packages	-65	+150	°C
T_j	junction temperature		-	+95	°C
V_{ESD}	electrostatic discharge voltage	Charge Device Model [1]	-2	2	kV
		Human Body Model [2]	-2	2	kV
V_{CC}	supply voltage	on pin V_{CC}	-0.5	7.15	V
V_i	input voltage	on pin ED, HPD	-0.5	7.15	V
$V_{I\ (RF)}$	RF input voltage	on pin LA/LB	-0.5	5.2	Vp
V_i	input voltage	on pin LA; LB is 0 V; sine wave of 13.56 MHz	-0.5	5.2	Vp
		on pin LB; LA is 0 V; sine wave of 13.56 MHz	-0.5	5.2	Vp
$I_{i(max)}$	maximum input current	La/Lb; peak	-168	168	mA

[1] CDM: ANSI/ESDA/JEDEC JS-002
[2] HBM: ANSI/ESDA/JEDEC JS-001

9 Package outline



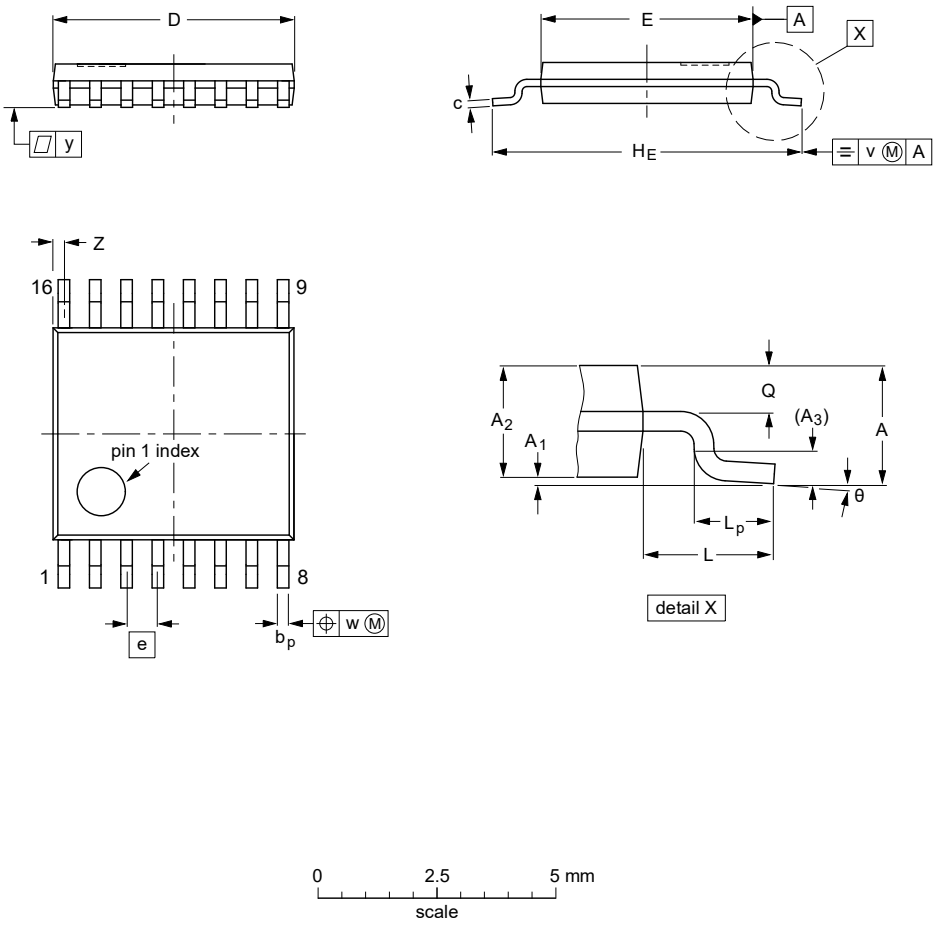
DIMENSIONS (mm are the original dimensions)

UNIT		$A^{(1)}$	A_1	b	c	$D^{(1)}$	$E^{(1)}$	e	e_1	e_2	k	L	L_1	L_2	v	w	y	y_1
mm	MAX	0.50	0.05	0.25		1.90	2.70					0.45	0.75	0.80				
	NOM			0.20	0.127	1.80	2.60	0.40	1.20	1.20	0.2	0.40	0.70	0.75	0.1	0.05	0.05	0.1
	MIN		0.00	0.15		1.70	2.50					0.35	0.65	0.70				

Notes
1. Plastic or metal protrusions of 0.075 maximum per side are not included.

Figure 6. Package outline XQFN16

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

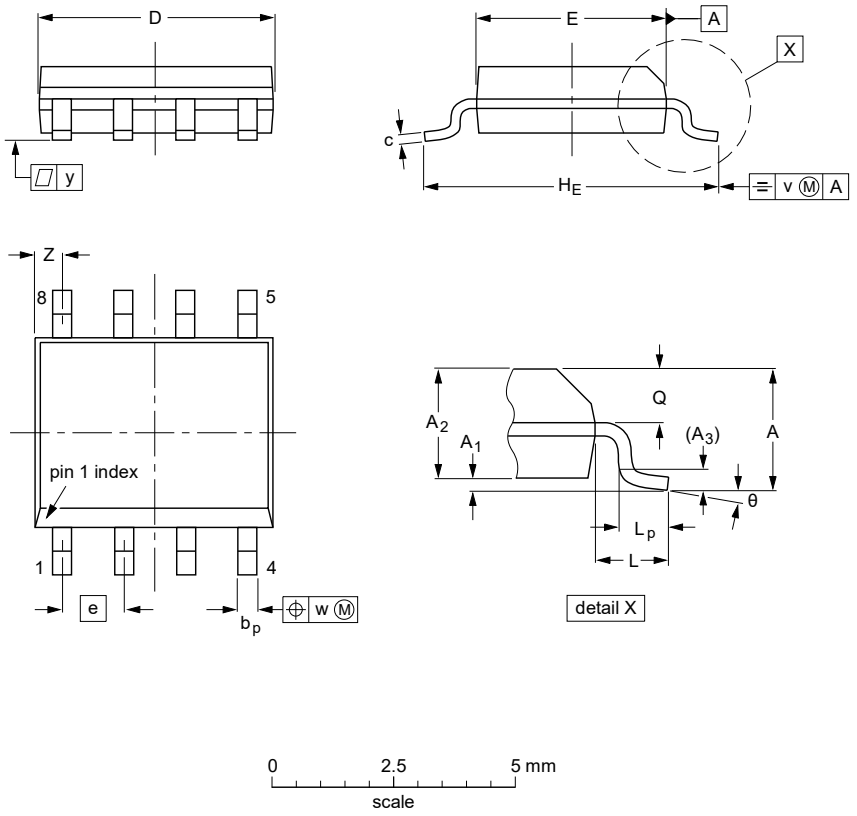
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Figure 7. Package outline TSSOP16

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Figure 8. Package outline SO8

10 Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

11 References

[1] NFC Forum specification, Type 5 Tag - Technical Specification Version 1.0 2018-04-27 [T5T] NFC Forum™
https://nfc-forum.org/product-category/specification/

[2] ISO/IEC 15693
https://www.iso.org/ics/35.240.15/x/

12 Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTP5210_SDS v.1.1	20191002	Objective short data sheet		v.1.0
NTP5210_SDS v.1.0	20190528	Objective short data sheet		-
	• Initial version			

13 Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Document number: 547711