NX20P3483UK

USB PD and Type-C high voltage sink/source combo switch with protection

Rev. 2 — 4 March 2019 Product data sheet

1. General description

The NX20P3483UK is a product with combined multiple power switches and an LDO for USB PD application. The device includes a bidirectional high voltage power switch which supports both 20V sink and 6V source; a 5V power switch for source and a 100mA LDO provides power supply for dead battery operation.

The high voltage power switch has 29V DC tolerance, and is able to sink up to 5A at maximum of 20V and source up to 3.4A at maximum of 6V. When it is configured as a high voltage sink switch, the path has overvoltage protection and reverse current protection features. While it is configured as high voltage source switch, the adjustable overcurrent limit circuit is integrated.

The 5V power switch has an adjustable overcurrent limit, “ideal diode” feature and short circuit protection. The maximum current capability is 3.4A. It supports fast role swap for USB PD3.0 application.

A VBUS discharge circuit is integrated according to USB PD VBUS discharging requirement. To minimize inrush current during normal startup, turn on slew rate control has been built in for all power switches. Over temperature protection is also equipped to automatically isolate the switch terminals when the device is overheated.

The device is controlled through an I^2C-bus interface, allowing the host to configure switches and program different specified parameters according to an I^2C register map.

The NX20P3483UK is offered with WLCSP42 package: 0.4mm pitch, 2.51 x 2.91 x 0.525mm, 0.4mm pitch.

2. Features and benefits

- Wide supply voltage range for VBUS from 2.8V to 20V
- System power supply V5V from 4.0V to 5.5V
- Chip power supply VDD from 2.7V to 5.5V
- VBUS to VCHG Switch
  - 28mΩ (typical) ultra low ON resistance
  - I_{SW} maximum 5A continuous current
  - Bidirectional operation: 20V sink switch from VBUS to VCHG with RCP and 6V source switch from VCHG to VBUS with overcurrent limit
  - Adjustable overcurrent limit for source configuration from 400mA to 3.4A by I^2C-bus interface
- V5V to VBUS switch
  - 38mΩ (typical) ultra low ON resistance

  - I_{SW} maximum 3.4A continuous current
  - Adjustable overcurrent limit from 400mA to 3.4A by I^2C-bus interface
- Integrated high voltage LDO with reverse voltage protection
- Built in slew rate control for all power switches for inrush current limit
- Supports 1MHz Fast Mode Plus I^2C-bus interface and four different I^2C slave addresses by ADDR pin
- Safety approvals
  - UL 62368-1, file no. 20181009- E470128
  - IEC 62368-1, file no. DK-77044-UL
- Protection circuitry
  - Over-Temperature Protection
  - Over-Voltage Protection
  - Under-Voltage Lockout
  - Reverse current protection
- Surge protection:
  - IEC61000-4-5 exceeds ±95V on VBUS
  - IEC61000-4-5 exceeds ±100V on VBUS with 4.7uF capacitor
- ESD protection
  - IEC61000-4-2 contact discharge exceeds kV on VBUS
  - IEC61000-4-2 air discharge exceeds 15kV on VBUS
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2kV on all pins
  - CDM ANSI/ESDA/JEDEC JS-002 exceeds 500V
- Operating ambient temperature −40°C to +85°C

3. Applications

- Notebook, Ultrabook and Desktop
- USB PD DFP, UFP and DRP
- Tablet and Smart phone

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX20P3483UK	–40 °C to +85 °C	WLCSP42	wafer level chip-scale package; 42 bumps; 2.91 mm x 2.51 mm x 0.525 mm body (backside coating included)	SOT1459-6

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NX20P3483UK	NX20P3483UKAZ	WLCSP42	reel dry pack, SMD, 7" Q1 standard product orientation	2000	T_{amb} = –40 °C to +85 °C

5. Marking

Table 3. Marking

Line	Content	Description
1	Pin 1 dot	Pin 1 dot
	3483UK	Product identification
2	XXXX	4 digit lot number before dot
	??	wafer ID
3	Z	wafer fab code (SSMC)
	t	Identification of assembly site (ASE-K)
	D	RoHS indicator (Dark green)
	YWW	Y: Last digits of year code of assembly, WW: week code of assembly
4	CCC-RRR	Die x-y coordinate

6. Functional diagram

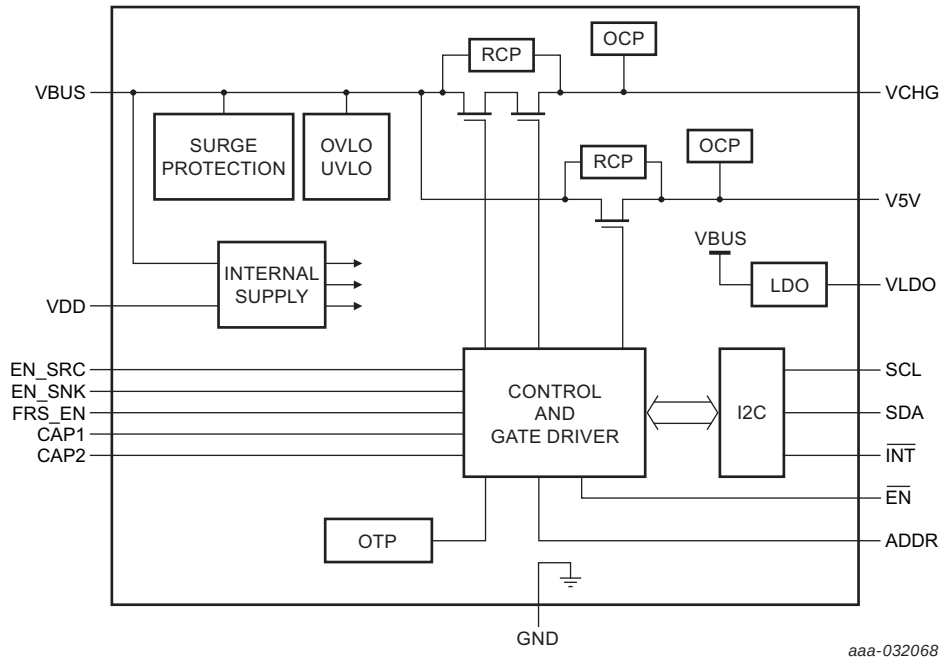


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

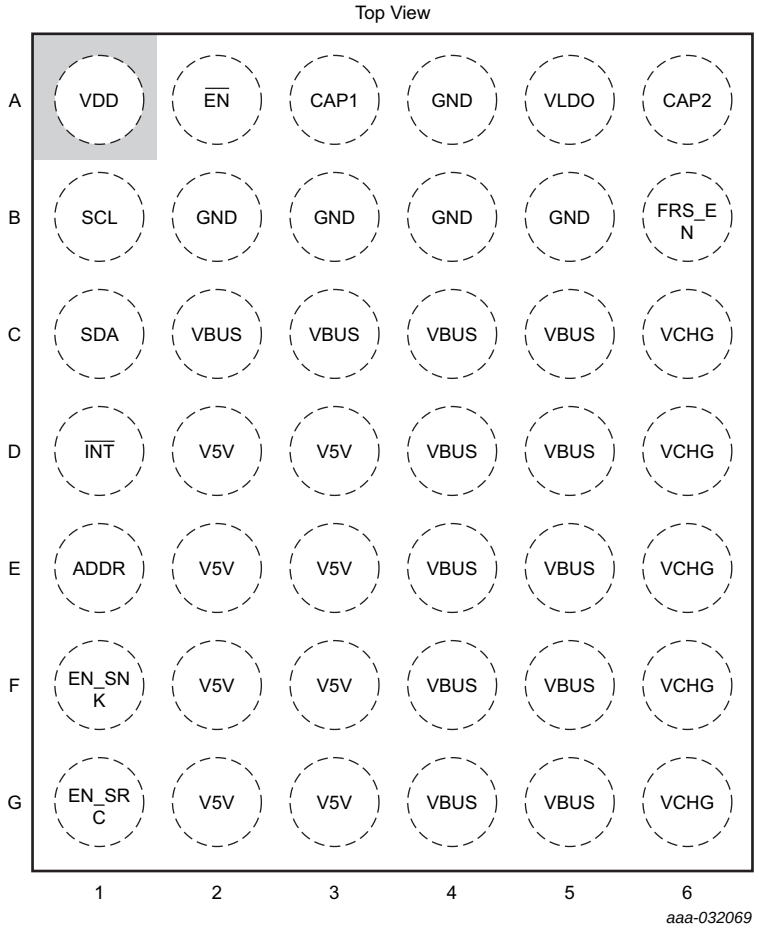


Fig 2. Pin map top view

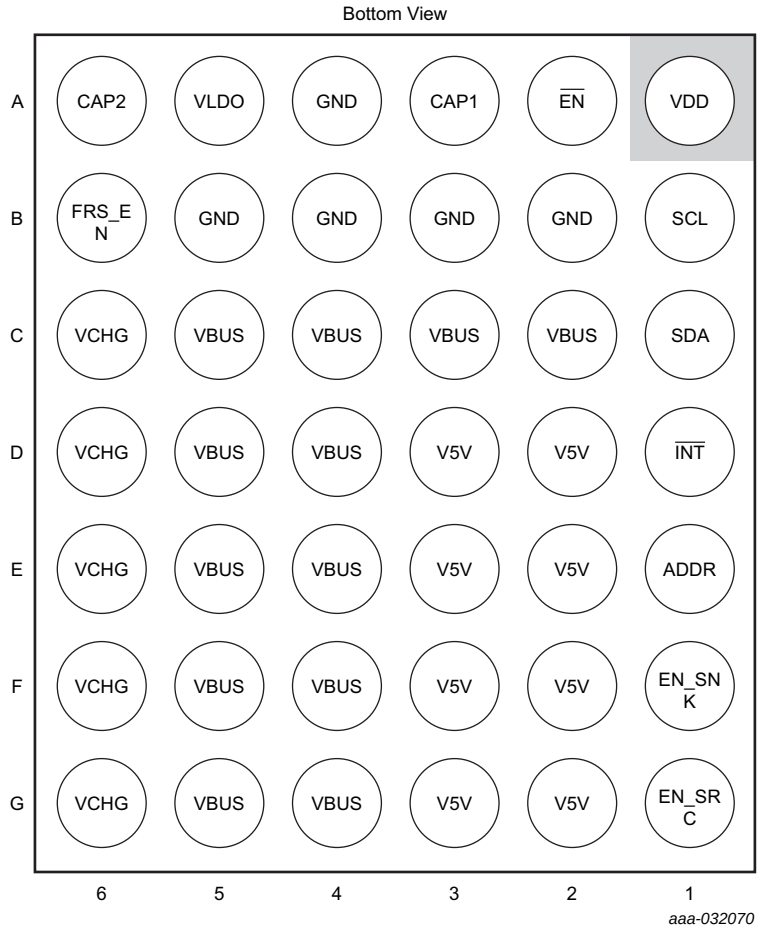


Fig 3. Pin map bottom view

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
VBUS	C2,C3,C4,C5,D4,D5, E4, E5, F4,F5,G4,G5	Power supply pin, Connects to TYPE-C Connector VBUS
VCHG	C6,D6, E6,F6,G6	connects to system charger input for USB PD voltage charging or output.
V5V	D2,E2,F2,G2, D3,E3,F3,G3	Power supply pin, 5V supply for the device and TYPE-C VBUS output
VDD	A1	Chip power supply, connects to system always ON 3.3V power rail or VBAT of 1S battery system
GND	A4,B3,B4,B5,B2	ground (0V)
FRS_EN	B6	Fast role swap enable pin, connects to TCPC fast role swap enable output pin
CAP1	A3	Internal power rail capacitance pin 1
CAP2	A6	Internal power rail capacitance pin 2
SDA	C1	I^2C Data input/output

Table 4. Pin description *...continued*

Symbol	Pin	Description
SCL	B1	I^2C Clock input
$\overline{INT}$	D1	open drain output; I^2C interrupt and chip alert
ADDR	E1	I^2C address select pin
EN_SNK	F1	Input enable pin for HVSNK power switch
EN_SRC	G1	Input enable pin for source power switch; the default enable is 5V_SRC power switch. It can be adjusted to enable HV_SRC power switch according to I^2C register
VLDO	A5	LDO output pin
$\overline{EN}$	A2	Enable pin for whole chip. Internal pull down resistor integrated

8. Functional description

8.1 Operation modes

NX20P3483UK can be supplied by VDD power from the system or VBUS power from USB port. Depending upon the power up sequence or availability of VDD and VBUS, the device works in dead battery mode or normal mode. The following sections describe the two modes in detail.

8.1.1 Dead Battery Mode

When VBUS powers up before VDD or VBUS is powered but VDD power is not valid (VDD <VDD UVLO), NX20P3483UK is forced to be in dead battery mode, regardless of the status of $\overline{EN}$, EN_SNK and EN_SRC pin. In this mode, NX20P3483UK automatically closes HV sink path to charge the battery. The VBUS OVLO in dead battery mode is fixed at 6.8V.

NX20P3483UK only exits from dead battery when the DB_EXIT bit is set as 1'b1 in register 0Bh by host and VDD is valid (>VDD UVLO). If the DB_EXIT is set as 1'b1 by host but VDD is less than UVLO, the device stays in dead battery mode and triggers an interrupt to notify host by setting DBEXIT_ERR in register 04h. In this mode, NX20P3483UK will not support source role and fast role swap.

In dead battery mode, the system can read and write to I^2C register, but NX20P3483UK will not take any action to respond to the control commands except for DB_EXIT bit. When NX20P3483UK exits from dead battery mode, the I^2C register is reset to the default value except for interrupt registers, and the device is controlled by EN_SNK and EN_SRC. If the HV sink path needs to be kept closed for charging after exiting dead battery mode, the EN_SNK pin should be asserted to HIGH 50us before system sets DB_EXIT bit as "1".

After NX20P3483UK exits from dead battery mode and VDD > VDD UVLO, if system sets DB_EXIT bit to "0" in register 0Bh; NX20P3483UK will not respond to it and keeps the current status.

While in normal mode, if VDD power is down and VDD < VDD ULVO, the device enters dead battery mode as well and resets DB_EXIT to "0".

8.1.2 Normal Modes

When VDD powers up before VBUS, VDD is powered but VBUS power is not valid (VBUS < VBUS UVLO) or when NX20P3483UK exits from dead battery mode, the device works in normal mode. The normal modes are controlled by $\overline{EN}$, EN_SNK or EN_SRC pins as shown in Table 5.

Table 5. Operation Modes

$\overline{EN}$	EN_SNK	EN_SRC	Operation mode
0	0	0	Standby mode
0	0	1	Source Mode: default enable 5V_SRC power switch. It can be configured to enable HV_SRC power switch through I^2C register

Table 5. Operation Modes *...continued*

$\overline{EN}$	EN_SNK	EN_SRC	Operation mode
0	1	0	HV Sink Mode: enable HV_SNK power switch
0	1	1	Forbidden, an error interrupt will be reported to system. The device keeps at the current status
1	x	x	Shutdown Mode

8.1.2.1 HV Sink Mode

In normal mode, when $\overline{EN}$ and EN_SRC are LOW and EN_SNK is HIGH, NX20P3483UK works in HV Sink mode. It turns on HV Sink path and takes power from VBUS to VCHG.

8.1.2.2 Source Mode

In normal mode, when $\overline{EN}$ and EN_SNK are LOW and EN_SRC is HIGH, NX20P3483UK works in Source mode. By default it turns on 5V Source path and supplies 5V power from V5V to VBUS.

The device supports fast role swap through the 5V Source path. If FRS_EN is set HIGH or FRS_AT bit is 1'b1 in register 0Bh, V5V is valid and EN_SRC=1, 5V source path is enabled with fast turn on feature. NX20P3483UK resumes the VBUS to vSafe5V in 100us.

NX20P3483UK can be configured to VCHG-VBUS Source path through I^2C-bus interface. When SRC_SEL bit of register 02h is 1'b1, the EN_SRC=HIGH enables VCHG-VBUS Source path power switch, which supplies voltage up to 6V from VCHG to VBUS by reverse boost of battery charger.

8.1.2.3 Standby mode

In normal mode, when $\overline{EN}$, EN_SNK and EN_SRC are LOW, NX20P3483UK is in standby mode. In this mode, most of internal circuits are turned off to save power. In order to react to system requests, the I^2C circuits are idle.

8.1.2.4 Shutdown mode

In normal mode, when $\overline{EN}$ is HIGH, NX20P3483UK is in shutdown mode. It is a low power mode to save system power consumption.

8.2 VBUS-VCHG Switch

The VBUS-VCHG path is a bidirectional high voltage capable switch. It can be configured to HV sink switch or source switch by I^2C-bus interface based on system requirement.

8.2.1 VBUS-VCHG HV Sink Mode

When EN_SNK is HIGH, VBUS-VCHG path works as a HV sink switch. It acts as a charging path to sink current from VBUS to VCHG. In this mode, the switch has adjustable overvoltage protection, reverse current protection from VCHG to VBUS and short circuit protection.

- Overvoltage protection

The overvoltage protection trip level can be programed by register 08h as shown in Table 6. Before the system sets NX20P3483UK to HV Sink mode, the OVLO threshold needs to be set if the threshold is not the reset default value, which is 6.8V.

Table 6. OVLO threshold setting by I²C register

Register Value OVP[2:0]	OVLO Threshold value
000	6V
001	6.8V (default)
010	10V
011	11.5V
100	14V
101	17V
110	23V
111	NA

When NX20P3483UK is in HV sink mode, the over-voltage lockout (OVLO) circuit disables the VBUS-VCHG power MOSFET. The OV_HVSNK in register 05h is set as “1” and an interrupt will be issued to notify the host. Once VBUS drops below V_{OVLO} and no other protection circuit is active, the power MOSFET resumes operation.

- Reverse current protection

The RCP circuit is integrated to prevent leakage from system to port. When the VCHG voltage exceeds the VBUS voltage by 10mV, the device will shutdown the power FET after 4ms de-glitch time. When VCHG voltage exceeds the VBUS voltage by 60mV, the device will shutdown the FET immediately without any de-glitch time. If RCP state is detected before enabling the power FET, the power FET will be kept in OFF state.

- Short circuit protection

The short circuit protection is integrated for this mode. When MOSFET is fully turned on and the current through it exceeds 10A, it turns off MOSFET to protect the device and system. An interrupt will be issued when short circuit protection is triggered by setting SC_HVSNK as “1” in register 05h. Once the short circuit condition is removed and no other protection circuit is active, the state of the MOSFET is controlled by I²C register bit again.

8.2.2 VCHG-VBUS HV Source Mode

When EN_SRC is HIGH and SRC_SEL bit is 1’b1 in register 02h, VCHG-VBUS path works as a source switch. It is a source path to supply external accessory up to 6V. In this mode, the switch has adjustable overcurrent limit, reverse current protection from VBUS to VCHG and short circuit protection. The VBUS is also protected with overvoltage protection circuit and the threshold can be adjusted according to Table 6. Before the system sets NX20P3483UK to HV Source mode, the OVLO threshold needs to be set.

- Adjustable overcurrent limit

The HV source mode offers overcurrent limit function. If the device senses I_{SW} exceeds I_{OCP} when enabled, OCP is triggered. It limits the output current to I_{OCP}, and an interrupt is issued to notify host by setting OC_HVSRC as “1” in register 05h. As a consequence, limiting the output current generates much higher power dissipation on the device, which could lead to over temperature protection (see Section 8.7).

The I_{OCP} can be adjusted by the register 09h according to Table 7 below.

Table 7. HV Source switch OCP threshold setting by I²C register

Register Value HVOCP[3:0]	HV Source Switch OCP Threshold Fine Tune value
0000	400mA
0001	600mA
0010	800mA
0011	1000mA
0100	1200mA
0101	1400mA
0110	1600mA (Default)
0111	1800mA
1000	2000mA
1001	2200mA
1010	2400mA
1011	2600mA
1100	2800mA
1101	3000mA
1110	3200mA
1111	3400mA

- Reverse current protection

The RCP circuit is integrated to prevent any reverse drive from VBUS to system. When the VBUS voltage exceeds the VCHG voltage by 15mV, the device will shutdown the power FET after 4ms de-glitch time; when VBUS voltage exceeds the VCHG voltage by 100mV, the device will shutdown the FET immediately without any de-glitch time. If RCP state is detected before enabling the power FET, the power FET will be kept in OFF state.

- Short circuit protection

The short circuit protection is integrated for this mode. When MOSFET is fully turned on and the current through it exceeds 7A, it turns off the MOSFET to protect the device and system. An interrupt will be issued when short circuit protection is triggered by setting SC_HVSRC as “1” in register 05h. Once the short circuit condition is removed and no other protection circuit is active, the state of the MOSFET is controlled by I²C register bit again.

8.3 V5V-VBUS 5V Source Switch

When EN_SRC is HIGH and SRC_SEL bit is 1’b0 in register 02h, the V5V-VBUS path is turned on and supplies the external accessary for 5V. The switch offers adjustable overcurrent limit, “ideal diode” feature, short circuit protection and overvoltage protection with fixed 6V OVLO trip level.

- Adjustable overcurrent limit

The 5V source switch has overcurrent limit feature. If the device senses I_{SW} exceeds I_{OCP} when enabled, OCP is triggered. It limits the output current to I_{OCP}, an interrupt is issued to notify host by setting OC_5VSRC as “1”. As a consequence, limiting the output current generates much higher power dissipation on the device, which could lead to over temperature protection (see Section 8.7).

The I_{OCP} can be adjusted by the register 0Ah according to Table 8 below.

Table 8. 5V Source switch OCP threshold setting by I^2C register

Register Value 5VOCP[3:0]	5V Source Switch OCP Threshold Fine Tune value
0000	400mA
0001	600mA
0010	800mA
0011	1000mA
0100	1200mA
0101	1400mA
0110	1600mA (Default)
0111	1800mA
1000	2000mA
1001	2200mA
1010	2400mA
1011	2600mA
1100	2800mA
1101	3000mA
1110	3200mA
1111	3400mA

- “Ideal diode” feature

The 5V source path integrates “ideal diode” feature. It operates like an ideal diode; whenever the VBUS voltage exceeds V5V voltage, the “ideal diode” feature turns off the path and prevents any reverse current from VBUS to V5V node. It protects the V5V lift by the reverse current when VBUS has a hot plug in the following conditions and limits the V5V voltage lift <400mV:

- VBUS<24V, plug in when 5V SRC switch is on
- C_{V5V} is in the range of 47uF - 100uF
- C_{BUS} is in the range of 4.7uF - 10uF

If the VBUS, C_{V5V}, and C_{BUS} are not in the range or conditions, they may have more reverse current and the VIN voltage lift depends on the conditions.

- Short circuit protection

The short circuit protection is integrated for 5V source path. When MOSFET is fully turned on and the current through it exceeds 7A, it turns off MOSFET to protect device and system. An interrupt will be issued when short circuit protection is triggered by setting OC_5VSRC as “1” in register 04h. Once the short circuit condition is removed and no other protection circuit is active, the state of the MOSFET is controlled by I^2C register bit again.

In the customer specific application case, the short circuit protection ensures the V5V voltage stays above 4.65V at the following short circuit testing.

- C_{IN} = 47μF, VBUS short to GND directly by a metal tweezer; the short resistor to ground is typically 40mΩ
- VIN connected to customer specified DC-DC

8.4 LDO Output

When NX20P3483UK is working at dead battery mode or HV sink mode, the integrated LDO is enabled and regulates the output voltage to 3.3V typically at VBUS>5V. It provides power to the downstream circuits when it is in dead battery mode or there is no battery. The current capability of the LDO is up to 100mA. The output capacitance of the LDO is 4.7μF, which should be connected as close as possible to VLDO pin.

When VBUS voltage drops below VLDO specified voltage in Table 26, the LDO is not turned off immediately but follows VBUS voltage drop and turns off when VBUS <V_{UVLO}.

When over temperature protection is triggered, the LDO is turned off by over temperature protection circuit. It can be turned off by LDO_SD bit in register 0Bh also for power saving.

8.5 Under-voltage lock-out

When VBUS and V5V exceeds UVLO threshold voltage, the device is in the modes defined in Table 5.

8.6 VBUS Discharge

In USB PD specifications, the VBUS voltage is required to be discharged to Vsafe5v and Vsafe0v when VBUS is detached or Hard Reset occurs. NX20P3483UK integrates VBUS discharge circuit and is controlled by VBUSDIS_EN in register 0Bh. The VBUS discharge function can be shut down by $\overline{EN}$ pin.

8.7 Over-temperature protection

When NX20P3483UK is conducting and the device temperature exceeds 140 °C, the over-temperature protection (OTP) circuit disables all the power switches and an interrupt will be sent to the host by setting OTP bit as “1” in register 04h. The power switches cannot be re-enabled in over-temperature protection. Once the device temperature decreases to below 120 °C, the device returns to normal operation.

8.8 I^2C Device Address

Following a START condition, the bus master must send the target slave address followed by a read (R/W = 1) or write (R/W = 0) operation bit. The slave address of the NX20P3483UK is shown in Figure 4. Slave address pin ADDR chooses one of four slave addresses. Table 9 shows all four slave addresses by connecting the ADDR pin to SCL, SDA, GND, or VDD.

Table 9. NX20P3483UK address map

ADDR	Device family high-order address bits					Variable portion of address		Address
	A6	A5	A4	A3	A2	A1	A0	
SCL	1	1	1	0	0	0	0	E0h
SDA	1	1	1	0	0	0	1	E2h
GND	1	1	1	0	0	1	0	E4h
VDD	1	1	1	0	0	1	1	E6h

The last bit of the first byte defines the reading from or writing to the NX20P3483UK. When setting to logic 1 a read is selected, while logic 0 selects a write operation.

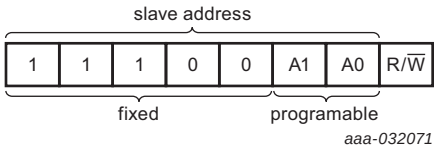


Fig 4. NX20P3483UK address

8.9 Register Map

The registers of NX20P3483UK are listed in Table 10.

Table 10. NX20P3483UK Register map

Addr (xxh)	Name	Type	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Device ID (reserved)	R	-	Vendor number					Revision number		
01h	Device Status	R	00h						Mode2	Mode1	Mode0
02h	Switch Control	R/W	00h	SRC_SEL	-	-	-	-	-	-	-
03h	Switch Status	R	00h	-	-	-	-	-	5VSRC_STS	HVSRC_STS	HVSNK_STS
04h	Interrupt1	C/R	00h	DBEXIT_ERR	-	-	OV_5VSRC	RCP_5VSRC	SC_5VSRC	OC_5VSRC	OTP
05h	Interrupt2	C/R	00h	EN_ERR	RCP_HVSNK	SC_HVSNK	OV_HVSNK	RCP_HVSRC	SC_HVSRC	OC_HVSRC	OV_HVSRC
06h	Interrupt1 Mask	R/W	00h	DBEXIT_ERR_MASK	-	-	OV_5VSRC_MASK	RCP_5VSRC_MASK	SC_5VSRC_MASK	OC_5VSRC_MASK	OTP_MASK
07h	Interrupt2 Mask	R/W	00h	EN_ERR_MASK	RCP_HVSNK_MASK	SC_HVSNK_MASK	OV_HVSNK_MASK	RCP_HVSRC_MASK	SC_HVSRC_MASK	OC_HVSRC_MASK	OV_HVSRC_MASK
08h	OVLO Threshold	R/W	01h	-	-	-	-	-	OVP2	OVP1	OVP0
09h	HV SRC OCP Threshold	R/W	0Bh	-	-	-	-	HVOCP3	HVOCP2	HVOCP1	HVOCP0
0Ah	5V SRC OCP Threshold	R/W	0Bh	-	-	-	-	5VOCP3	5VOCP2	5VOCP1	5VOCP0
0Bh	Device Control	R/W	00h	-	-	-	-	FRS_AT	DB_EXIT	VBUSDIS_EN	LDO_SD

8.9.1 Device ID Register (Address 00h)

Table 11. Device ID Register

Bit	Name	Type	Reset Value	Description
7:3	Vendor ID	R	00001	NXP Vendor ID 00001
2:0	Version ID	R	010	Device revision number revision 010

8.9.2 Device Status Register (Address 01h)

Table 12. Device Status Register

Bit	Name	Type	Reset Value	Description
7:3	Reserved	R	00h	default 00h
2:0	Mode[2:0]	R	04h	Device mode status according to section 8.1
				000 = Dead battery mode
				001=HV SNK mode
				010 = 5V SRC mode
				011 = HV SRC mode
				100 = Standby mode

8.9.3 Switch Control Register (Address 02h)

This register controls the EN_SRC turn on 5V SRC switch or HV SRC switch. It is required to set SRC_SEL bit before assert EN_SRC pin. The default value is 0h to turn on 5V SRC switch.

Table 13. Switch control Register

Bit	Name	Type	Reset Value	Description
7	SRC_SEL	R/W	0h	0h = 5V SRC for source path
				1h = HV SRC for source path
6:0	Reserved	R/W	0h	Default 0h

8.9.4 Switch Status Register (Address 03h)

This register reports the state of all the power switches of NX20P3483UK.

Table 14. Switch status Register

Bit	Name	Type	Reset Value	Description
7:3	Reserved	R	0h	Default 0h
2	5VSRC_STS	R	0h	0h = 5V source switch is off
				1h = 5V source switch is on
1	HVSRC_STS	R	0h	0h = HV source switch is off
				1h = HV source switch is on
0	HVSNK_STS	R	0h	0h = HV sink switch is off
				1h = HV sink switch is on

8.9.5 Interrupt1 Register (Address 04h)

The Interrupt1 register contains flags indicating error flags, 5V source switch fault conditions and a chip level over temperature flag. An event will be latched and only the first occurrence triggers an interrupt (if not masked). Reoccurring events will not change the flags' status or trigger an additional interrupt. The event registers are automatically cleared by reading.

Table 15. Interrupt1 Register

Bit	Name	Type	Reset Value	Description
7	DBEXIT_ERR	C/R	0h	Exit dead battery error, please refer to section 8.1.2
				0: No exit dead battery error
				1: Exit dead battery error occurs
6:5	Reserved	C/R	0h	0h = Default
4	OV_5VSRC	C/R	0h	5V Source switch overvoltage protection
				0: No overvoltage fault
				1: overvoltage fault triggered
3	RCP_5VSRC	C/R	0h	5V Source switch RCP
				0: No reverse current fault
				1: Reverse current fault triggered
2	SC_5VSRC	C/R	0h	5V Source switch short circuit protection
				0: No short circuit fault
				1: Short circuit protection fault triggered
1	OC_5VSRC	C/R	0h	5V Source switch overcurrent limit
				0: No overcurrent fault
				1: over circuit limit triggered
0	OTP	C/R	0h	Chip Over temperature protection
				0: No over temperature fault
				1: over temperature protection fault triggered

8.9.6 Interrupt2 Register (Address 05h)

The Interrupt2 register contains flags indicating HV source and HV sink switch fault conditions. An event will be latched and only the first occurrence triggers an interrupt (if not masked). Reoccurring events will not change the flags' status or trigger an additional interrupt. The event registers are automatically cleared by reading.

Table 16. Interrupt2 Register

Bit	Name	Type	Reset Value	Description
7	EN_ERR	C/R	0h	EN_SNK and EN_SRC both high error fault
				0: EN_SNK and EN_SRC are not both high
				1: EN_SNK and EN_SRC are both high

Table 16. Interrupt2 Register

Bit	Name	Type	Reset Value	Description
6	RCP_HVSNK	C/R	0h	HV Sink switch RCP
				0: No reverse current fault
				1: Reverse current fault triggered
5	SC_HVSNK	C/R	0h	HV Sink switch short circuit protection
				0: No short circuit fault
				1: Short circuit protection fault triggered
4	OV_HVSNK	C/R	0h	HV Sink switch overvoltage protection
				0: No overvoltage fault
				1: Overvoltage fault triggered
3	RCP_HVSRC	C/R	0h	HV Source switch RCP
				0: No reverse current fault
				1: Reverse current fault triggered
2	SC_HVSRC	C/R	0h	HV Source switch short circuit protection
				0: No short circuit fault
				1: Short circuit protection fault triggered
1	OC_HVSRC	C/R	0h	HV Source switch overcurrent limit
				0: No overcurrent fault
				1: overcurrent limit triggered
0	OV_HVSRC	C/R	0h	HV Source switch overvoltage protection
				0: No overvoltage fault
				1: Overvoltage fault triggered

8.9.7 Interrupt1 Mask Register (Address 06h)

The Interrupt1 Mask register enables the masking (disabling) of the different available interrupt signals of register Interrupt1.

Table 17. Interrupt1 Register

Bit	Name	Type	Reset Value	Description
7	DBEXIT_ERR_MASK	C/R	0h	Dead battery exit error interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt
6:5	Reserved	C/R	0h	0h = Default
4	OV_5VSRC_MASK	C/R	0h	5V Source switch overvoltage protection interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt
3	RCP_5VSRC_MASK	C/R	0h	5V Source switch RCP interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt

Table 17. Interrupt1 Register

Bit	Name	Type	Reset Value	Description
2	SC_5VSRC_MASK	C/R	0h	5V Source switch short circuit protection interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt
1	OC_5VSRC_MASK	C/R	0h	5V Source switch overcurrent protection interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt
0	OTP_MASK	C/R	0h	Chip Over temperature protection interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt

8.9.8 Interrupt2 Mask Register (Address 07h)

The Interrupt2 Mask register enables the masking (disabling) of the different available interrupt signals of register Interrupt2.

Table 18. Interrupt2 Register

Bit	Name	Type	Reset Value	Description
7	EN_ERR_MASK	C/R	0h	EN_SNK and EN_SNK both HIGH error interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt
6	RCP_HVSNK_MASK	C/R	0h	HV Sink switch RCP interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt
5	SC_HVSNK_MASK	C/R	0h	HV Sink switch short circuit protection interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt
4	OV_HVSNK_MASK	C/R	0h	HV Sink switch overvoltage protection interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt
3	RCP_HVSRC_MASK	C/R	0h	HV Source switch RCP interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt
2	SC_HVSRC_MASK	C/R	0h	HV Source switch short circuit protection interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt

Table 18. Interrupt2 Register

Bit	Name	Type	Reset Value	Description
1	OC_HVSRC_MASK	C/R	0h	HV Source switch overcurrent protection interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt
0	OV_HVSRC_MASK	C/R	0h	HV Source switch overvoltage protection interrupt mask
				0: Can trigger the interrupt
				1: Cannot trigger the interrupt

8.9.9 OVLO threshold Register (Address 08h)

This is the register to set the OVLO threshold, please refer to Section 8.2.1.

Table 19. OVLO threshold Register

Bit	Name	Type	Reset Value	Description
7:3	Reserved	R/W	0h	0h=default
3:0	OVP[2:0]	R/W	01h	OVLO threshold setting bits. Reset default OVLO threshold is 6.8V.

8.9.10 HV source switch OCP threshold Register (Address 09h)

This is the register to set the HV source switch OCP trip level threshold, please refer to Section 8.2.2.

Table 20. HV source switch OCP threshold register

Bit	Name	Type	Reset Value	Description
7:4	Reserved	R/W	0h	0h=default
3:0	HVOCP[3:0]	R/W	06h	HV source switch setting bits

8.9.11 5V source switch OCP threshold Register (Address 0Ah)

This is the register to set the 5V source switch OCP trip level threshold, please refer to Section 8.3.

Table 21. 5V source switch OCP threshold register

Bit	Name	Type	Reset Value	Description
7:4	Reserved	R/W	0h	0h=default
3:0	5VOCP[3:0]	R/W	06h	5V source switch setting bits

8.9.12 Device control Register (Address 0Bh)

The register controls device status for exiting dead battery mode, enabling VBUS discharge circuit and shutting down LDO.

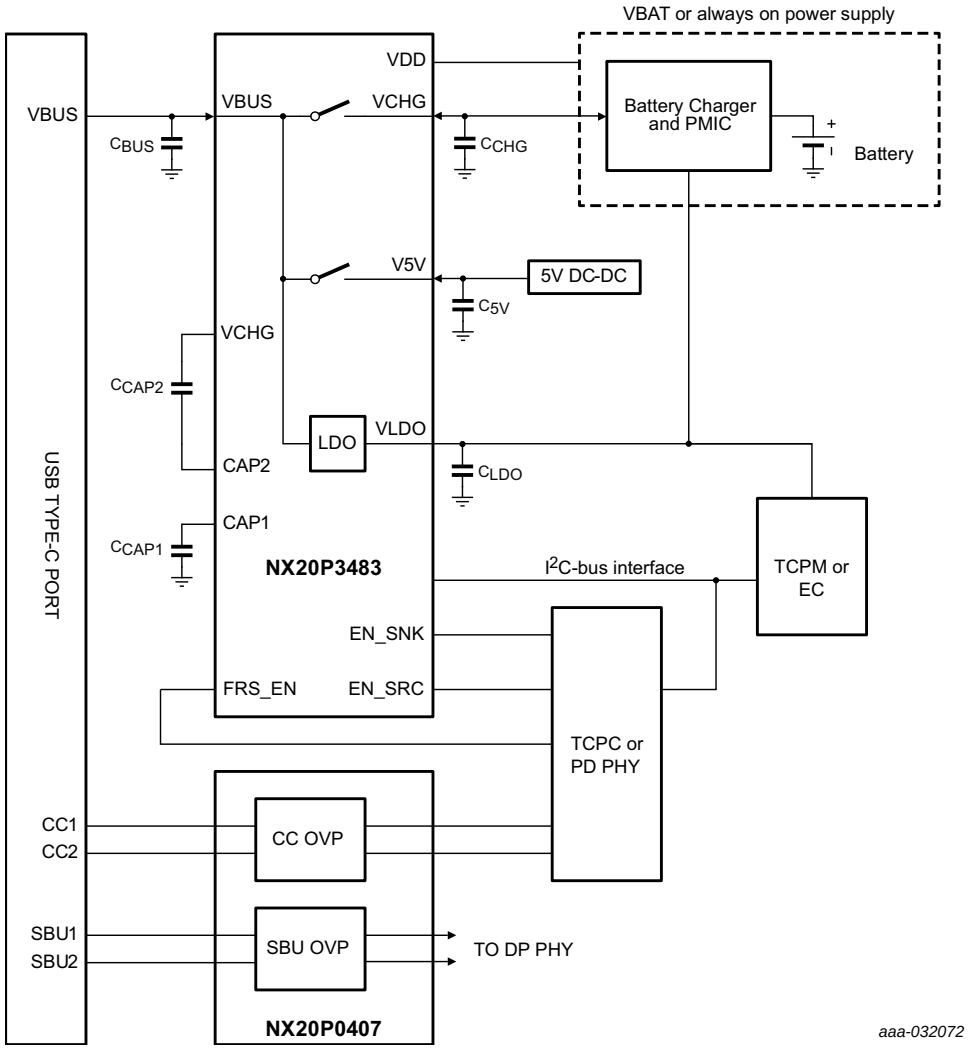
Table 22. Device control Register

Bit	Name	Type	Reset Value	Description
7:4	Reserved	R/W	0h	0h=default
3	FRS_AT	R/W	0h	Activate fast role swap
				0: Fast role swap capability is not activated
				1: Fast role swap capability is activated
2	DB_EXIT	R/W	0h	Exit dead battery mode
				0: keeps in dead battery mode
				1: Exit dead battery mode
1	VBUSDIS_EN	R/W	0h	VBUS discharge enable bit
				0: VBUS discharge circuit disabled
				1: VBUS discharge circuit enabled
0	LDO_SD	R/W	0h	LDO Shut down control bit
				0: LDO is enabled
				1: LDO is shutdown

9. Application diagram

The NX20P3483UK is typically used on a USB PD port in a portable, battery operated device. It provides HV sink path for charging from VBUS to VCHG, 5V source path for Type C 5V output to accessory and HV source path for USB PD output to accessory. Besides the power paths, a 3.3V LDO is integrated to supply TCPM or EC in dead battery operation. The device can be controlled by I²C-bus interface by TCPM or system chip.

The device is fully compliant with normal USB PD PHY and TCPC+TCPM structure.



1. The capacitances C_{BUS},C_{CHG},C_{5V} and C_{LDO} should be as close as possible to NX20P3483UK
2. The recommended capacitance value for C_{LDO} is 4.7uF
3. The minimum required capacitance value for C_{CHG} is 10uF
4. The minimum required capacitance value for C_{BUS} is 4.7uF
5. The minimum required capacitance value for C_{5V} is 47uF
6. C_{CAP1} and C_{CAP2} are the capacitors for internal power rail, the recommend C_{CAP1} is 1nF 16V capacitor and C_{CAP2} is 10nF 25V capacitor

Fig 5. NX20P3483UK application diagram

10. Limiting values

Table 23. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	VBUS; VCHG		–0.5	+29	V
		V5V; VDD		–0.5	+6.0	V
		$\overline{EN}$; SCL; SDA; FRS_EN	[1]	–0.5	+6.0	V
		EN_SNK; EN_SRC	[1]	–0.5	+29	V
V_O	output voltage	$\overline{INT}$; VLDO		–0.5	+6.0	V
		CAP1		–0.5	+12	V
		CAP2	[2]	-0.5	+20	V
I_{IK}	input clamping current	$\overline{EN}$; V_I < –0.5 V;		–50	-	mA
I_{SW}	High voltage Power switch continuous current	V_{SW} > –0.5 V		-	5	A
	5V power switch continuous current	V_{SW} > –0.5 V		-	3.5	A
$T_{j(max)}$	maximum junction temperature			–40	+125	°C
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb}=25°C	[3]	-	2.02	W

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] Though the CAP2 maximum rating is specified as 20V, CAP2 is a floating source refer to VCHG. If CAP2 is forced by an external power source, the maximum difference between VCHG and CAP2 should be less than 6V.

[3] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed in conjunction with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 25 °C and the use of a two layer PCB.

11. Recommended operating conditions

Table 24. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	VBUS;		2.8	20	V
		VCHG; as voltage input of source switch from VCHG to VBUS		4.0	6.0	V
		VDD		2.7	5.5	V
		V5V		4.0	5.5	V
		$\overline{EN}$; SCL; SDA; FRS_EN		0	5.5	V
		EN_SNK; EN_SRC		0	5.5	V
V_O	Output voltage	VLDO; $\overline{INT}$		0	5.5	V
		CAP1		0	10	V
		CAP2		VCHG-5V	VCHG	V
I_{SW}	High voltage switch current	T_{amb} = –40 °C to +85 °C		0	5	A
	5V source switch current	T_{amb} = –40 °C to +85 °C		0	3	A
T_{amb}	ambient temperature			–40	+85	°C

12. Thermal characteristics

Table 25. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	49.4	K/W

[1] $R_{th(j-a)}$ is dependent upon board layout. To minimize $R_{th(j-a)}$, ensure all pins have a solid connection to larger copper layer areas. In multi-layer PCBs, the second layer should be used to create a large heat spreader area below the device. Avoid using solder-stop varnish under the device.

13. Static characteristics

Table 26. Static characteristics

At recommended operating conditions and VDD=3.3V; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
General Specifications								
V_{IH}	HIGH-level input voltage	$\overline{EN}$, EN_SNK, EN_SRC, FRS_EN pins;	1.2	-	-	1.2	-	V
V_{IL}	LOW-level input voltage	$\overline{EN}$, EN_SNK, EN_SRC, FRS_EN pins;	-	-	0.4	-	0.4	V
I_I	Input pin leakage current	$\overline{EN}$, FRS_EN pins; V_I=0V	-	0.1	-	-1	1	µA
		$\overline{EN}$, FRS_EN pins; V_I=5V	-	5	-	3	8	µA
		EN_SNK, EN_SRC pins; V_I=0V	-	0.1	-	-1	1	µA
		EN_SNK, EN_SRC pins; V_I=5V	-	5	-	3	8	µA
C_I	input capacitance	$\overline{EN}$, FRS_EN pin; $V_{I(VDD)}$ = 5V	-	4.5	-	-	-	pF
		EN_SNK, EN_SRC pins; $V_{I(VDD)}$ = 5V	-	8	-	-	-	pF
R_{pd}	pull-down resistance	$\overline{EN}$ pin;	-	1	-	-	-	MΩ
$I_{q\_VDD\_HVSINK}$	VDD quiescent current	$\overline{EN}$ = 0 V; HV sink mode, VDD=3.3V, VBUS=5V	-	1	-	-	5	µA
		$\overline{EN}$ = 0 V; HV sink mode, VDD=5V, VBUS=5V	-	155	-	-	225	µA
$I_{q\_VBUS\_HVSINK}$	VBUS quiescent current	$\overline{EN}$ = 0 V; HV sink mode, VDD=3.3V, VBUS=5V	-	205	-	-	300	µA
		$\overline{EN}$ = 0 V; HV sink mode, VDD=5V, VBUS=5V	-	50	-	-	75	µA
$I_{q\_VDD\_HVSRC}$	VDD quiescent current	$\overline{EN}$ = 0 V; HV source mode, VDD=3.3V, VCHG=5V, I_{LOAD}= 0A	-	1	-	-	5	µA
		$\overline{EN}$ = 0 V; HV source mode, VDD=5V, VCHG=5V, I_{LOAD}= 0A	-	210	-	-	275	µA
$I_{q\_VBUS\_HVSRC}$	VCHG quiescent current	$\overline{EN}$ = 0 V; HV source mode, VDD=3.3V, VCHG=5V, I_{LOAD}= 0A	-	360	-	-	500	µA
		$\overline{EN}$ = 0 V; HV source mode, VDD=5V, VCHG=5V, I_{LOAD}= 0A	-	150	-	-	225	µA
$I_{q\_VDD\_5VSRC}$	VDD quiescent current	$\overline{EN}$ = 0 V; HV source mode, VDD=3.3V, V5V=5V, I_{LOAD}= 0A	-	1	-	-	5	µA
		$\overline{EN}$ = 0 V; HV source mode, VDD=5V, V5V=5V, I_{LOAD}= 0A	-	130	-	-	190	µA
$I_{q\_V5V\_5VSRC}$	V5V quiescent current	$\overline{EN}$ = 0 V; HV source mode, VDD=3.3V, V5V=5V, I_{LOAD}= 0A	-	1.25	-	-	1.62	mA
		$\overline{EN}$ = 0 V; HV source mode, VDD=5V, V5V=5V, I_{LOAD}= 0A	-	1.12	-	-	1.5	mA

Table 26. Static characteristics *...continued*

At recommended operating conditions and VDD=3.3V; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
$I_{q\_standby}$	VDD quiescent	$\overline{EN}$ = 0V; No switch in operation, VDD=3.3V	-	7.5	-	-	24	µA
		$\overline{EN}$ = 0V; No switch in operation, VDD=5V	-	8.5	-	-	25	µA
$I_{q\_shutdown}$	VDD quiescent	$\overline{EN}$ = 5V;	-	1.8	-	-	4	µA
V_{VBUS_UVLO}	under-voltage lockout release voltage	VBUS Rising; $\overline{EN}$ = 0 V	-	2.6	-	2.45	2.75	V
		VBUS Falling;	-	2.5	-			V
V_{VDD_UVLO}	under-voltage lockout release voltage	VDD Rising; $\overline{EN}$ = 0 V	-	2.5	-	2.35	2.65	V
		VDD Falling;	-	2.4	-			V
V_{V5V_UVLO}	under-voltage lockout release voltage	V5V Rising; $\overline{EN}$ = 0 V	-	3.6	-	3.4	3.8	V
		V5V Falling;	-	3.5	-			V
V_{VHCG_UVLO}	under-voltage lockout release voltage	VCHG Rising; $\overline{EN}$ = 0 V	-	3.6	-	3.4	3.8	V
		VCHG Falling;	-	3.5	-			V
V_{VLDO}	LDO output voltage	VBUS=5V; I_{LOAD}=100mA	-	3.3	-	3.0	3.6	V
HV SNK Switch Specifications								
$V_{OVLO\_HVSNK\_ACC}$	Overvoltage lockout voltage accuracy	VBUS Rising; $\overline{EN}$ = 0 V; For all OVLO level set by Table 6	-5	-	5	-5	5	%
$V_{hys(OVLO)}$	Overvoltage lockout hysteresis voltage	VBUS Falling; $\overline{EN}$ = 0 V; For all OVLO level set by Table 6	-	2	-	1	3	%
V_{RCP_HVSNK}	HV SNK RCP trig level	$V_{RCP\_HVSNK} = V_{(VCHG)} - V_{(VBUS)}$	-	10	-	6	14	mV
V_{RCPS_HVSNK}	HV SNK Severe RCP trig level	$V_{RCP\_HVSNK} = V_{(VCHG)} - V_{(VBUS)}$	-	60	-	40	80	mV
$I_{S(OFF)\_HVSNK}$	VBUS OFF state leakage	HV SNK Switch OFF; VBUS=5V	-	5	-	-	10	µA
		HV SNK Switch OFF; VBUS=20V	-	15	-	-	30	µA
	VCHG OFF state leakage	HV SNK Switch OFF; VCHG=5V	-	1	-	-	5	µA
		HV SNK Switch OFF; VCHG=20V	-	4	-	-	16	µA
$I_{S(ON)\_HVSNK}$	RCP Leakage current	$\overline{EN}$ = 0 V; HVSNK switch is enabled; VCHG=5V; VBUS=0V	-	1	-	-	5	µA
I_{SCP_HVSNK}	HV SNK Switch short protection	HVSNK switch is enabled	-	10	-	8	-	A
HV SRC Switch Specifications								
$I_{OCP\_HVSRC\_ACC}$	HV SRC Switch overcurrent protection accuracy	V_{VCHG}=4V to 6v; $\overline{EN}$ = 0 V; I_{OCP}>1A	-10	-	10	-10	10	%
		V_{VCHG}=4V to 6V; $\overline{EN}$ = 0 V; I_{OCP}<1A	-20	-	20	-20	20	%

Table 26. Static characteristics *...continued*

At recommended operating conditions and VDD=3.3V; voltages are referenced to GND (ground = 0 V).

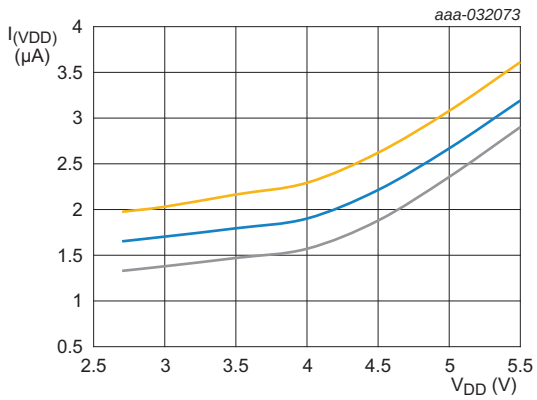
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{RCP_HVSRC}	HV SRC RCP trig level	$V_{RCP\_HVSRC} = V_{(VBUS)} - V_{(VCHG)}$	-	15	-	8	21	mV
V_{RCPS_HVSRC}	HV SRC Severe RCP trig level	$V_{RCP\_HVSRC} = V_{(VBUS)} - V_{(VCHG)}$	-	100	-	70	130	mV
$I_{S(OFF)\_HVSRC}$	VBUS OFF state leakage	HV SRC Switch OFF; VBUS=5V	-	5	-	-	10	µA
		HV SRC Switch OFF; VBUS=20V	-	15	-	-	30	µA
	VCHG OFF state leakage	HV SRC Switch OFF; VCHG=5V	-	1	-	-	5	µA
$I_{S(ON)\_HVSRC}$	RCP Leakage current	$\overline{EN}$ = 0 V; HVSRC switch is enabled; VCHG=0V; VBUS=5V	-	1	-	-	5	µA
I_{SCP_HVSRC}	HV SRC Switch short protection	HVSRC switch is enabled and at normal operation	-	10	-	7	-	A
		HVSRC switch is enabled and after OCP triggered	-	6.5	-	4.5	-	A
5V SRC Switch Specifications								
$I_{OCP\_5VSRC\_ACC}$	5V SRC Switch overcurrent protection accuracy	V_{V5V}=4V to 5.5V; $\overline{EN}$ = 0 V; I_{OCP}>1A	-	-	-	-10	10	%
		V_{V5V}=4V to 5.5V; $\overline{EN}$ = 0 V; I_{OCP}>1A	-	-	-	-20	20	%
V_{RCP_5VSRC}	5V SRC RCP trig level	$V_{RCP\_5VSRC} = V_{(VBUS)} - V_{(V5V)}$	-	10	-	6	14	mV
V_{RCPS_5VSRC}	5V SRC Severe RCP trig level	$V_{RCP\_5VSRC} = V_{(VBUS)} - V_{(V5V)}$	-	60	-	40	80	mV
$I_{S(OFF)\_5VSRC}$	VBUS OFF state leakage	5V SRC Switch OFF; VBUS=5V	-	5	-	-	10	µA
		5V SRC Switch OFF; VBUS=20V	-	15	-	-	30	µA
	V5V OFF state leakage	5V SRC Switch OFF; V5V=5V	-	1	-	-	5	µA
$I_{S(ON)\_5VSRC}$	RCP Leakage current	$\overline{EN}$ = 0 V; 5VSRC switch is enabled; V5V=0V; VBUS=5V	-	1	-	-	5	µA
I_{SCP_5VSRC}	5V SRC Switch short protection	5VSRC switch is enabled and at normal operation	-	7	-	5	-	A
		5VSRC switch is enabled and after OCP triggered	-	6	-	4.5	-	A
I^2C-bus Interface Specifications								
V_{IH}	HIGH-level input voltage	SCL, SDA; VDD= 2.7V to 5.5V	1.2	-	-	1.2	-	V
V_{IL}	LOW-level input voltage	SCL, SDA; VDD= 2.7V to 5.5V	-	-	0.4	-	0.4	V
V_{OL}	LOW-level output voltage	$\overline{INT}$ pin; VDD= 2.7V to 5.5V; I_{load} = 1mA	-	-	0.4	-	0.4	V

Table 26. Static characteristics *...continued*

At recommended operating conditions and VDD=3.3V; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
f_{CLK_I2C}	I^2C bus clock frequency		0	-	1	0	1	MHz
Thermal Protection								
$T_{th(otp)}$	over temperature shutdown threshold temperature	VDD=2.7V to 5.5V	-	140	-	-	-	°C
$T_{th(otp)hys}$	hysteresis of over temperature protection threshold temperature	VIN=2.7V to 5.5V	-	20	-	-	-	°C

13.1 Graphs



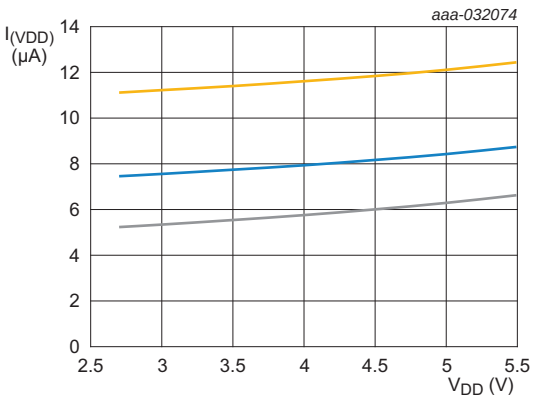
$V_{I(EN)}$ =3.3V;

(1) T_{amb}=-40°C

(2) T_{amb}=25°C

(3) T_{amb}=85°C

Fig 6. VDD shutdown quiescent current



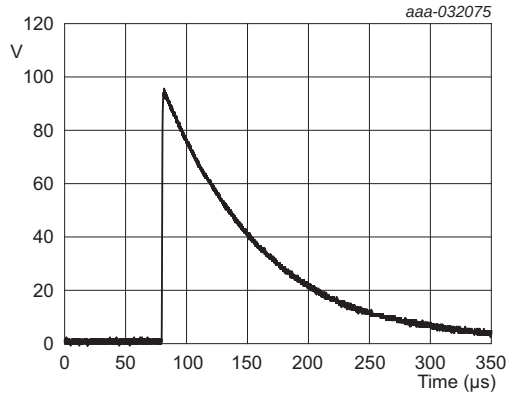
$V_{I(EN)}$ =0V; $V_{I(EN\_SNK)}$ = 0V; $V_{I(EN\_SRC)}$ = 0V

(1) T_{amb}=-40°C

(2) T_{amb}=25°C

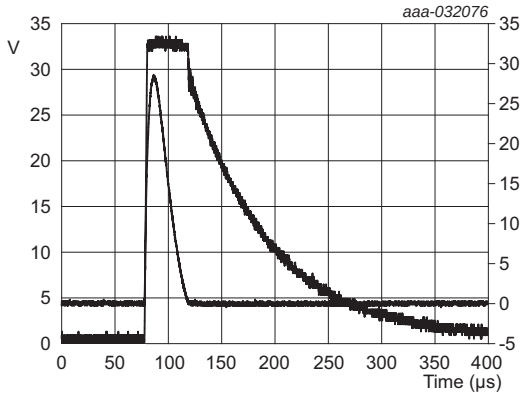
(3) T_{amb}=85°C

Fig 7. VDD standby quiescent current



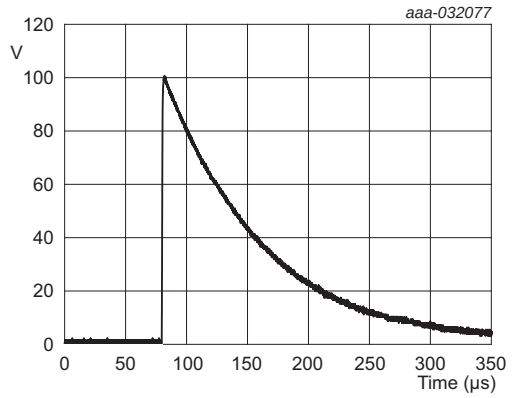
IEC61000-4-5

Fig 8. 95V surge without device



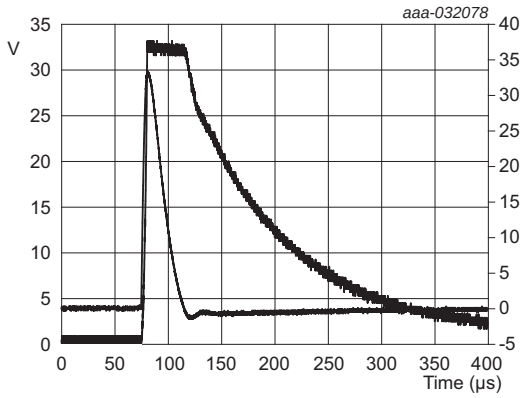
Without capacitor on VBUS

Fig 9. 95V surge with device



IEC61000-4-5

Fig 10. 100V surge without device



With 4.7uF on VBUS

Fig 11. 100V surge with device

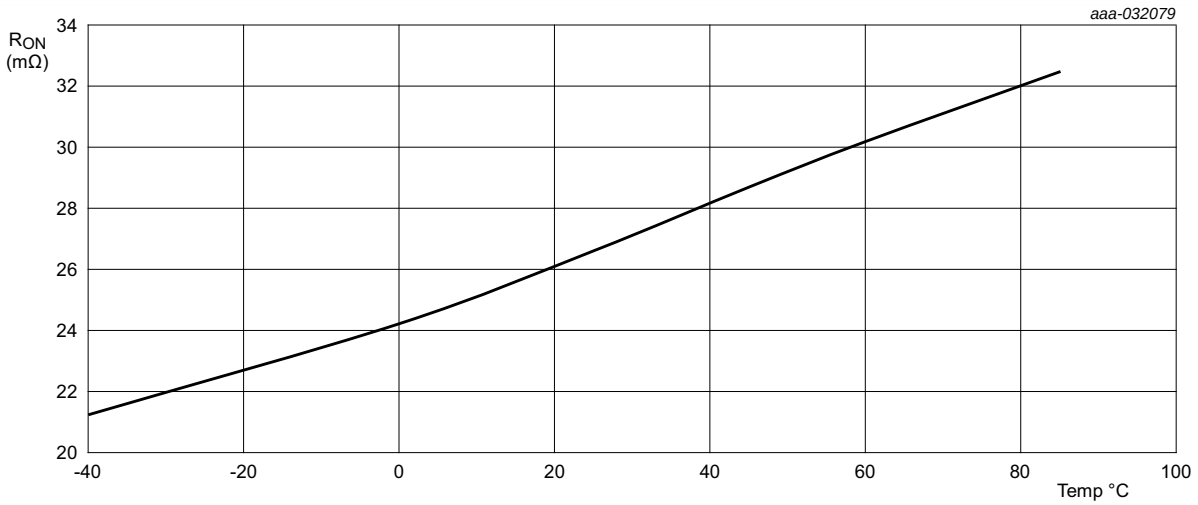
13.2 ON resistance

Table 27. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
R_{ON_HVSNK}	ON resistance	I_{LOAD} = 1 A							
		$V_{I(VBUS)}$ = 5.0 V		-	28	32	-	42	mΩ
		$V_{I(VBUS)}$ = 20 V		-	28	32	-	42	mΩ
R_{ON_HVSRC}	ON resistance	I_{LOAD} = 1 A							
		$V_{I(VCHG)}$ = 5.0 V		-	28	32	-	42	mΩ
R_{ON_5VSRC}	ON resistance	I_{LOAD} = 1 A							
		$V_{I(V5V)}$ = 5.0 V		-	38	43	-	57	mΩ

13.3 ON resistance graphs



X = T_{amb}, Y = Ron;

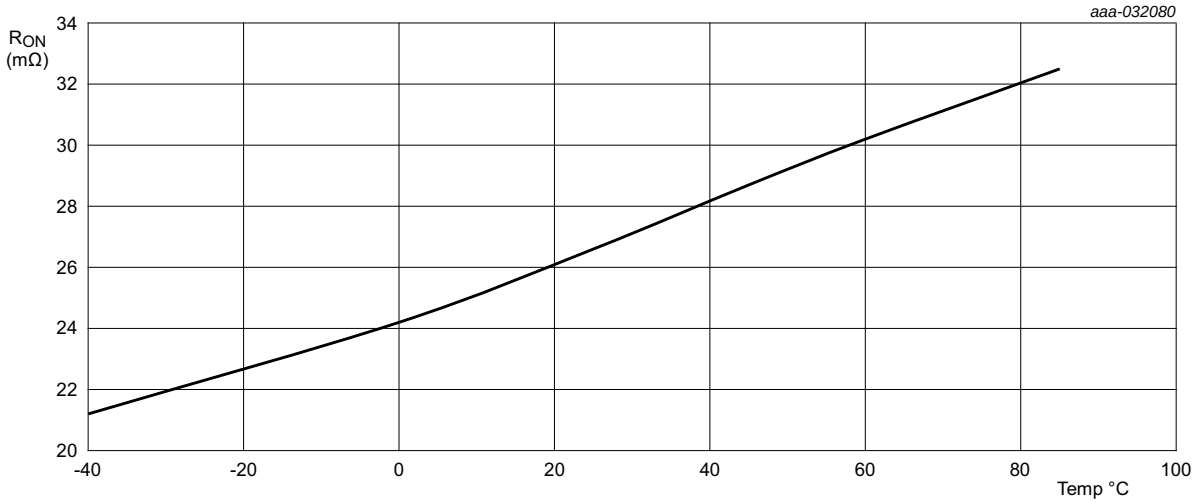
(1) VBUS=5V

(2) VBUS=9V

(3) VBUS=12V

(4) VBUS=20V

Fig 12. HV Sink switch typical ON resistance versus temperature

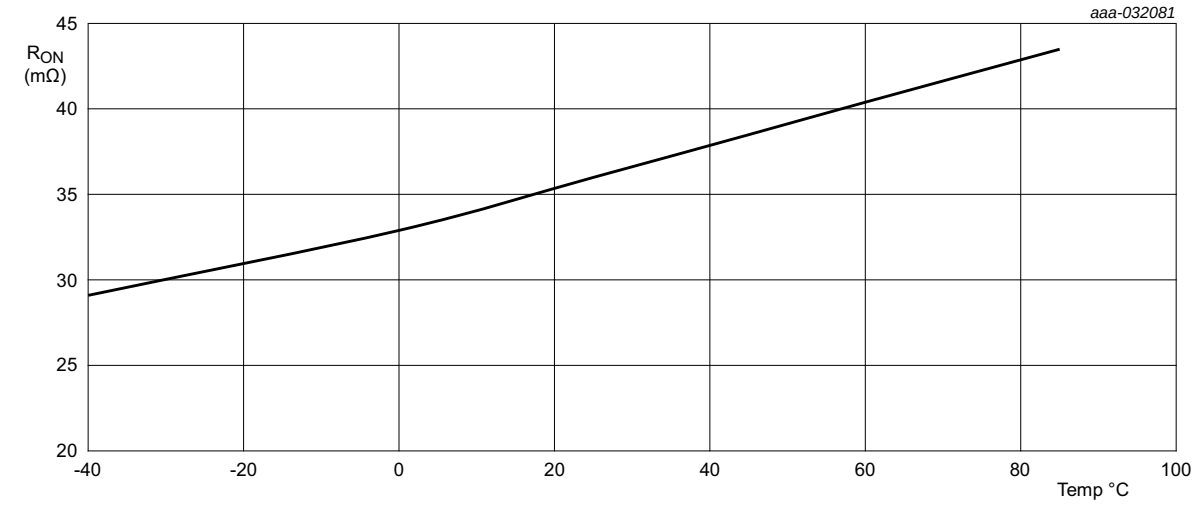


X = T_{amb}, Y = Ron

(1) VCHG=5V

(2) VCHG=6V

Fig 13. HV Source switch typical ON resistance versus temperature



X = T_{amb}, Y = Ron

(1) V5V=5V

Fig 14. 5V Source switch typical ON resistance versus temperature

14. Dynamic characteristics

Table 28. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 16.

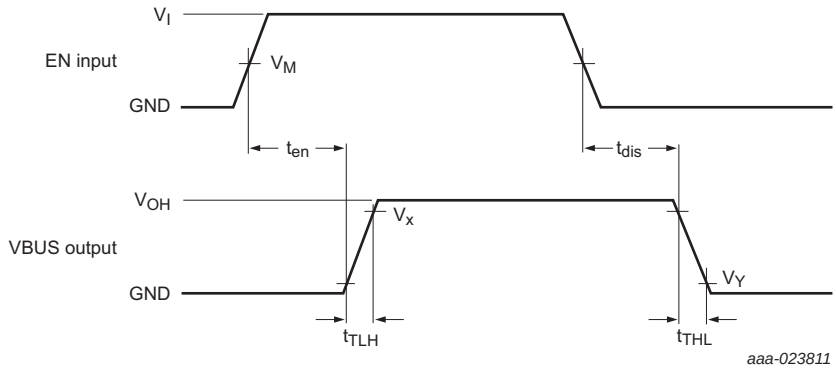
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
HV SNK Switch specifications								
t_{DEB_HVSNK}	HV SNK Switch De-bounce time	Time from V_{UVLO}<VBUS<V_{OVLO} to $V_{(VCHG)}$ = 10% of $V_{(VBUS)}$	-	15	-	-	-	ms
t_{TLH_HVSNK}	HV SNK Switch VCHG rise time	$V_{(VCHG)}$ from 10% to 90% $V_{(VBUS)}$; C_{Load} = 22µF; R_{Load} = 100Ω						
		$V_{I(VIN)}$ = 5V	-	1.8	-	-	2.7	ms
		$V_{I(VIN)}$ = 20V	-	2.3	-	-	3.5	ms
$t_{dis(OVP)}$	OVLO turn off time	From $V_{(VBUS)}$>V_{OVLO} to $V_{(VCHG)}$ = 80% of $V_{(VIN)}$; R_{Load} = 100Ω; C_{Load} = 0 µF; $V_{I(VBUS)}$ = 20V; VIN rise >2V/us	-	30	-	-	100	ns
t_{dis_HVSNK}	HV SNK Switch Disable time	From $\overline{EN}$ to $V_{(VBUS)}$ = 90% of $V_{(VIN)}$; $V_{I(VIN)}$ = 5V; C_{Load} = 0µF; R_{Load} = 100Ω	-	5	-	3	7	µs
$t_{dis(RCPS)\_HVSNK}$	HV SNK Switch Severe RCP Disable time	From HV Sink Severe RCP to switch turn off	-	3.5	-	3	4	µs
t_{degl_HVSNK}	HV SNK Switch RCP de-glitch time	Time from V_{UVLO}<VIN<V_{OVLO} to $V_{(VCHG)}$ = 10% of $V_{(VIN)}$	-	4	-	-	-	ms
t_{SCP_HVSNK}	Short circuit protection response time	VBUS=5V; Time from short circuit happened to switch turn off	-	2.5	-	-	-	µs
HV SRC Switch specifications								
t_{EN_HVSRC}	HV SRC Switch Enable time	EN_SRC= HIGH to $V_{(VBUS)}$ = 10% of $V_{(VCHG)}$; C_{Load} = 10µF; R_{Load} = 100Ω	-	5	-	-	9	ms
t_{TLH_HVSRC}	HV SRC Switch VBUS rise time	$V_{(VBUS)}$ from 10% to 90% $V_{(VCHG)}$; C_{Load} = 10µF; R_{Load} = 100Ω						
		$V_{I(VCHG)}$ = 5V	-	1.8	-	-	2.7	ms
t_{dis_HVSRC}	HV SRC Switch Disable time	EN_SRC=LOW to $V_{(VBUS)}$ = 90% of $V_{(VCHG)}$; $V_{I(VCHG)}$ = 5V; C_{Load} = 0µF; R_{Load} = 100Ω	-	5	-	3	7	µs
$t_{dis(RCPS)\_HVSRC}$	HV SRC Switch Severe RCP Disable time	From HV source severe RCP to switch turn off	-	1	-	-	2	us
$t_{degl\_RCP\_HVSRC}$	HV SRC Switch RCP de-glitch time	Time from V_{UVLO}<VCHG<V_{OVLO} to $V_{(VCHG)}$ = 10% of $V_{(VIN)}$	-	4	-	-	-	ms
$t_{degl\_OCP\_HVSRC}$	HV SRC Switch OCP de-glitch time	De-glitch Time from overcurrent to OC_HVSRC interrupt	-	8	-	-	-	ms

Table 28. Dynamic characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 16.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{SCP_HVSRC}	Short circuit protection response time	VCHG=5V; Time from short circuit happened to switch turn off	-	1	-	-	-	µs
5V SRC Switch specifications								
t_{EN_5VSRC}	5V SRC Switch Enable time	EN_SRC=HIGH to $V_{(VBUS)}$ = 90% of $V_{(V5V)}$; C_{Load} = 10µF; R_{Load} = 100Ω						
		Non Fast role swap mode	-	2.8	-	-	-	ms
		Fast role swap mode	-	60	-	-	90	µs
t_{TLH_5VSRC}	5V SRC Switch VCHG rise time	$V_{(VBUS)}$ from 10% to 90% $V_{(V5V)}$; C_{Load} = 10µF; R_{Load} = 100Ω						
		Non Fast role swap mode	-	1.3	-	-	-	ms
		Fast role swap mode	-	50	-	-	80	µs
t_{dis_5VSRC}	5V SRC Switch Disable time	EN_SRC=LOW to $V_{(VBUS)}$ = 90% of $V_{(V5V)}$; $V_{I(V5V)}$ = 5V; C_{Load} = 0µF; R_{Load} = 100Ω	-	5	-	3	7	µs
$t_{dis(RCPS)\_5VSRC}$	5V SRC Switch RCP Disable time	From VBUS>V5V+50mV to switch turn off	-	1	-	-	1.5	µs
$t_{degl\_RCP\_5VSRC}$	5V SRC Switch RCP de-glitch time	Time from V_{UVLO}<VBUS<V_{OVLO} to $V_{(VCHG)}$ = 10% of $V_{(VIN)}$	-	4	-	-	-	ms
$t_{degl\_OCP\_5VSRC}$	5V SRC Switch OCP de-glitch time	De-glitch Time from overcurrent to OC_5VSRC interrupt	-	8	-	-	-	ms
t_{SCP_5VSRC}	Short circuit protection response time	V5V=5V; Time from short circuit happened to switch turn off	-	0.5	-	-	-	µs
$t_{VBUSDISCHARGE}$	Time taken for VIN discharge	VDD= 3.3V; Load Capacitance = 10µF VBUS pin going down below Vsafe0V after VBUS detached and switch disabled	-	-	-	-	650	ms
		VDD= 3.3V; Load Capacitance = 10µF VBUS pin going down below Vsafe5V (when initial voltage is >5V) after VBUS detached and switch disabled	-	-	-	-	275	ms

14.1 Waveform and test circuits



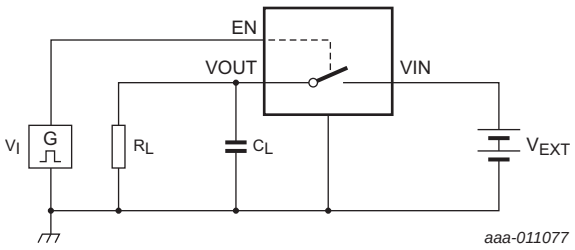
Measurement points are given in Table 29.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 15. Switching times and rise and fall times

Table 29. Measurement points

Supply voltage	$\overline{EN}$ Input	Output	
$V_{I(VIN)}$	V_M	V_X	V_Y
5.0 V; 20.0V	0.5 × $V_{I(EN)}$	0.9 × V_{OH}	0.1 × V_{OH}



Test data is given in Table 30.

Definitions test circuit:

R_L = Load resistance.

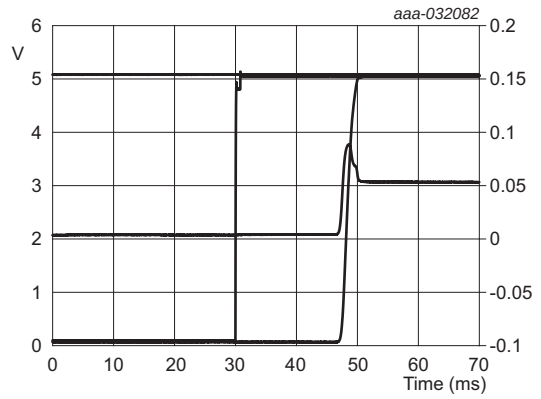
C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 16. Test circuit for measuring switching times

Table 30. Test data

Supply voltage	$\overline{EN}$ Input	Load	
V_{EXT}	$V_{I(EN)}$	C_L	R_{LOAD}
5.0 V; 20.0V	0 to $V_{I(VIN)}$	22 µF	100 Ω

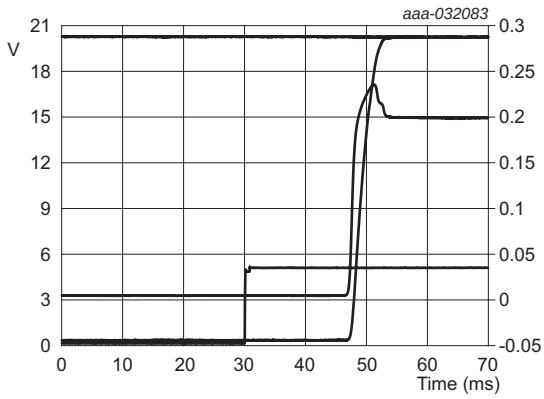


$V_{I(VBUS)}$ = 5 V; R_L = 100Ω; CL = 22uF

(1) $V_{O(VCHG)}$

(2) $I_{(VIN)}$

Fig 17. HV sink switch turn on timing and inrush current at 5V

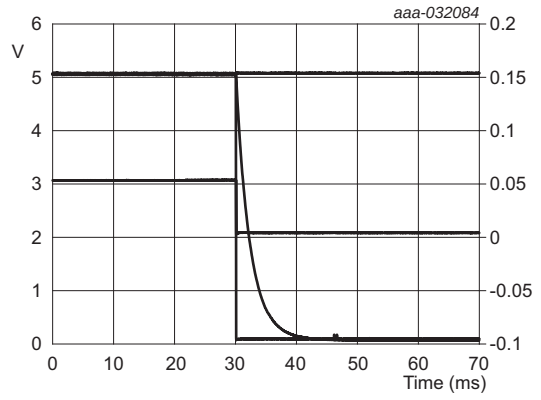


$V_{I(VBUS)}$ = 20V; R_L = 100Ω; CL = 22uF

(1) $V_{O(VCHG)}$

(2) $I_{(VIN)}$

Fig 18. HV sink switch turn on timing and inrush current at 20V

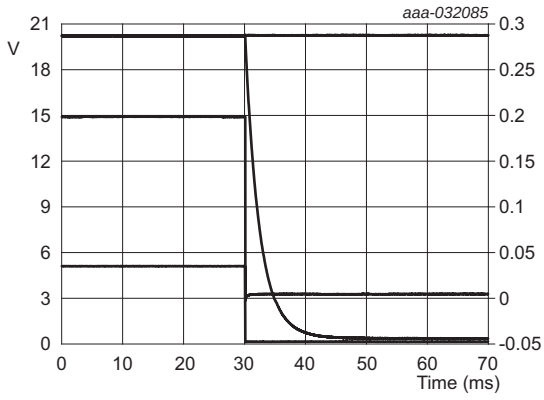


$V_{I(VBUS)}$ = 5 V; R_L = 100Ω; CL = 22uF

(1) $V_{O(VCHG}$

(2) $I_{(VIN)}$

Fig 19. HV sink switch turn off timing at 5V

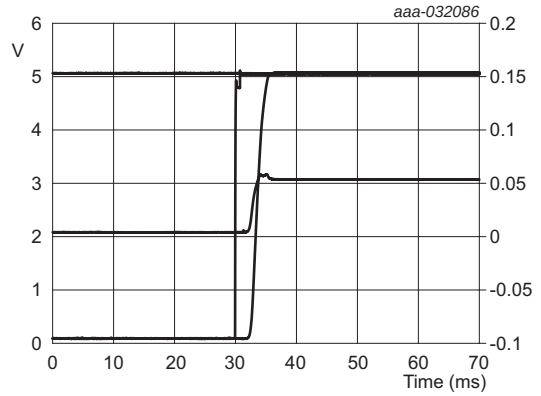


$V_{I(VBUS)}$ = 5 V; R_L = 100Ω; CL = 22uF

(1) $V_{O(VCHG)}$

(2) $I_{(VIN)}$

Fig 20. HV sink switch turn off timing at 20V

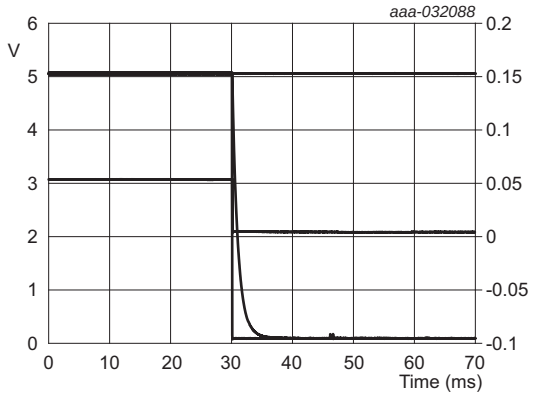


$V_{I(VCHG)}$ = 5 V; R_L = 100Ω; CL = 10uF; Ioc=1.6A

(1) $V_{O(VBUS)}$

(2) $I_{(VIN)}$

Fig 21. HV source switch turn on timing and inrush current at 5V

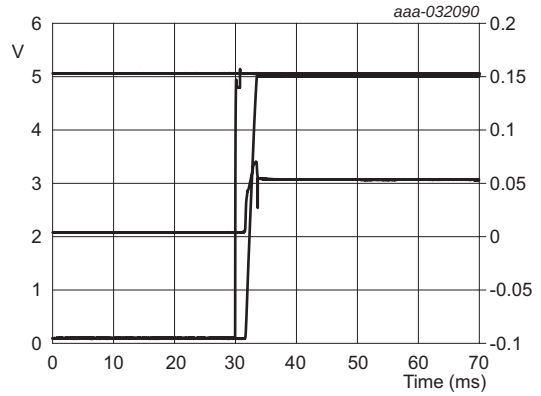


$V_{I(VCHG)}$ = 5 V; R_L = 100Ω; CL = 10uF; Ioc=1.6A

(1) $V_{O(VBUS)}$

(2) $I_{(VIN)}$

Fig 22. HV source switch turn off timing at 5V

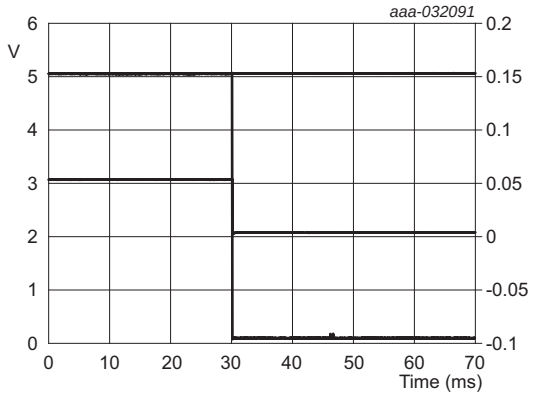


$V_{I(V5V)}$ = 5 V; R_L = 100Ω; CL = 10uF; Ioc=1.6A

(1) $V_{O(VBUS)}$

(2) $I_{(VIN)}$

Fig 23. 5V source switch turn on timing and inrush current

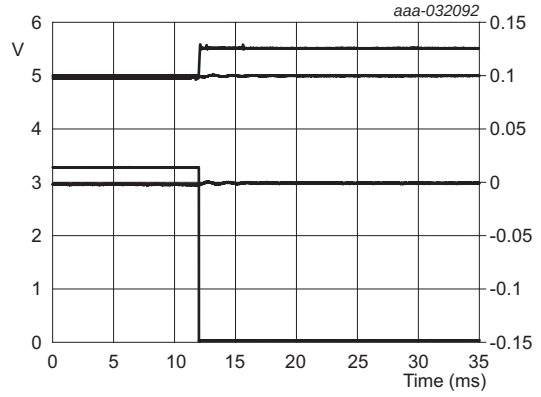


$V_{I(V5V)}$ = 5 V; R_L = 100Ω; CL = 10uF; Ioc=1.6A

(1) $V_{O(VBUS)}$

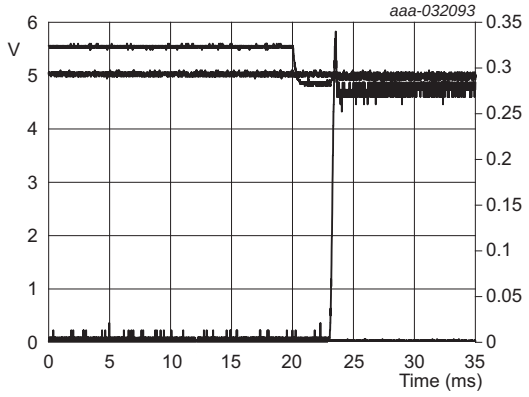
(2) $I_{(VIN)}$

Fig 24. 5V source switch turn off timing



$V_{I(V5V)}$ = 5 V

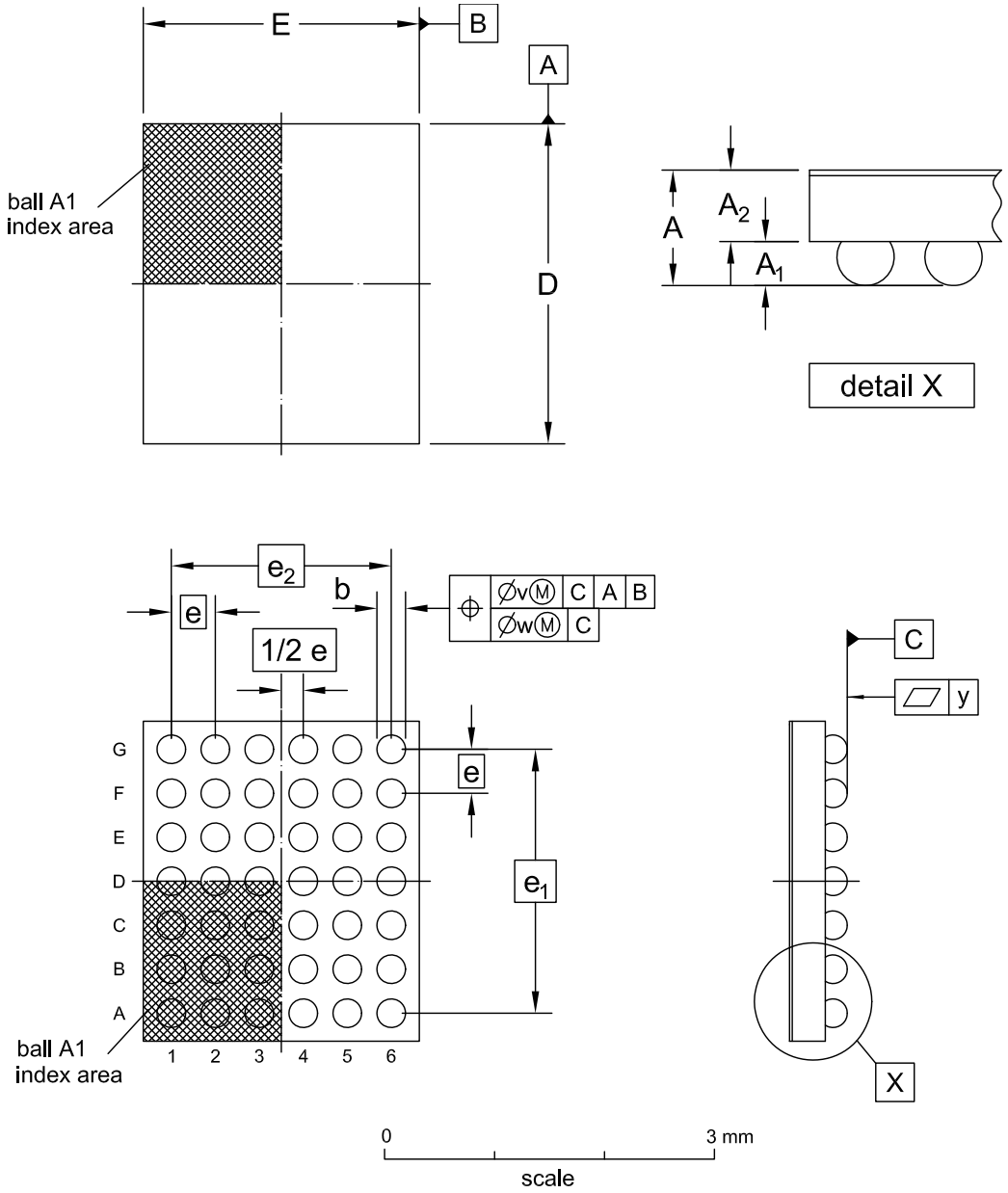
Fig 25. 5V source switch RCP response



$V_{I(V5V)}$ = 5 V

Fig 26. 5V source switch RCP recovery

15. Package outline



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	MAX.	0.565	0.23	0.350	0.29	2.94	2.54	0.4	2.4	2.0	0.05	0.02	0.03
	NOM.	0.525	0.20	0.325	0.26	2.91	2.51						
	MIN.	0.485	0.17	0.300	0.23	2.88	2.48						

NOTE: Backside coating 25 um

Fig 27. Package outline SOT1459-6 (WLCSP42)

16. Packing information

16.1 SOT1459-6 (WLCSP42); reel dry pack, SMD, 7" Q1 standard product orientation ordering code (12NC) ending 012

16.1.1 Dimensions and quantities

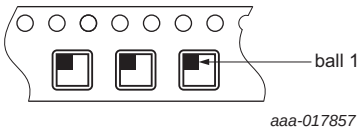
Table 31. Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box
180 × 12	2000	1

[1] d = reel diameter; w = tape width.

[2] Packing quantity dependent on specific product type.
View ordering and availability details at NXP order portal, or contact your local NXP representative.

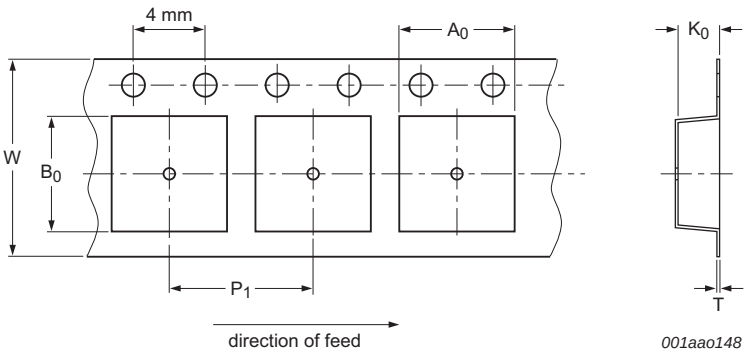
16.1.2 Product orientation



Ball 1 is in quadrant 1

Fig 28. Product orientation in carrier tape

16.1.3 Carrier tape dimensions



Not drawn to scale.

Fig 29. Carrier tape dimensions

Table 32. Carrier tape dimensions
In accordance with IEC 60286-3.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
2.71 ± 0.05	3.11 ± 0.05	0.72 ± 0.05	0.25 ± 0.02	8.0 ± 0.10	12 +.30/-.10

17. Abbreviations

Table 33. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
CDM	Charged Device Model
HBM	Human Body Model
USB	Universal Serial Bus
VOIP	Voice over Internet Protocol

18. Revision history

Table 34. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX20P3483UK v.2.0	20190304	Product data sheet	-	NX20P3483UK v.1.0
Modifications:	• Updated Section 2 “Features and benefits”			
NX20P3483UK v.1.0	20181026	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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21. Contents

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