NXH3670UK

Ultra-low power 2.4 GHz BLE transceiver for audio streaming

Rev. 3.1 — 25 July 2019 Product data sheet

Document information

Information	Content
Keywords	Ultra low-power, 2.4 GHz, Wireless, Audio transceiver, Embedded MCU, Hearables
Abstract	The NXH3670UK constitutes a highly integrated, single chip ultra low-power 2.4 GHz wireless transceiver with embedded MCU, targeted at wireless audio streaming for hearables, wireless headsets and headphones.

1 General description

The NXH3670UK constitutes a highly integrated, single chip ultra-low power 2.4 GHz wireless transceiver with embedded MCU, targeted at wireless audio streaming for hearables, wireless headsets and headphones.

The NXH3670UK chip integrates the following key functionalities – among others:

- A 2.4 GHz RF transceiver and digital modem supporting up to 2 Mbits/s
- Supporting BLE GFSK modulation 1 Mbps and 2 Mbps
- A low-power 16 MHz/32 MHz crystal oscillator and on-chip oscillators
- An RF MAC for supporting the lower protocol layers
- A Cortex-M0 subsystem for system control and higher protocol layers
- An AES-128 security coprocessor
- Audio interfaces and audio processing accelerators
- A CoolFlux DSP for audio processing
- Multiple user interfaces for control, data, debug and test

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.
Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

CAUTION

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction.
The IC must be protected against light. The protection must be applied to all sides of the IC..

Unless otherwise specified:

- Typical values are at room temperature (25 °C) with nominal supply voltages of 1.2 V.
- Minimum/Maximum values are valid over operating temperature and voltage range as specified in Table 27.

2 Features and benefits

- Transceiver charactersitics
  - 2.36 GHz to 2.5 GHz carrier frequency
  - BLE 1 Mbps and 2 Mbps PHY modes
  - 2 MHz channels in 1 Mbps and 2 Mbps modes
- Receiver characteristics:
  - Sensitivity −90 dBm in BLE 2 Mbps modulation mode
  - Sensitivity −94 dBm in BLE 1 Mbps modulation mode
  - Frequency offset correction up to ±300 kHz.
  - RSSI measurement with ±3 dB accuracy
- Transmitter characteristics:
  - Programmable TX output power of −10 dBm to +4 dBm in 2 dB steps
- Synthesizer characteristics:
  - Fully integrated PLL, no external loop filter components
- Integrated power management:
  - Low voltage supply 1.2 V
  - Integrated supply generation for sensitive radio blocks
  - Integrated supply generation for digital and memories
  - Flexible low-power states
- Clock generation:
  - Integrated low-power crystal oscillator
  - Support for 16 MHz or 32 MHz crystals with ±60 ppm accuracy and crystal trimming
  - On chip oscillators, including ultra low-power oscillator
- Low current consumption:
  - Sleep current < 63 µA
  - Continuous RX current < 3.7 mA
  - Continuous TX current < 7.3 mA (0 dBm output power)
- MCU subsystem:
  - ARM Cortex-M0 up to 16 MHz in low-power mode and 84 MHz in high-performance mode
  - Flexible DMA engine
  - Serial debug interface
- Control/Data interfaces:
  - SPI slave
  - UART
  - GPIOs
- RF MAC:
  - Dedicated RF MAC accelerator
  - AES security coprocessor
  - Packet processing
  - Timers
  - CRC, whitening
- Audio interfaces and processing
  - I^2S interface
  - G.722/ADPCM codec accelerator

  - CoolFlux DSP up to 16 MHz in low-power mode and 84 MHz in high-performance mode
  - Asynchronous sample rate converter (ASRC)
  - Latency control
- Flexible boot mode support
  - Host-assisted boot mode
- Certified for Bluetooth specification version 5.0
- WLCSP package < 7.25 mm^2 (maximum die size after sawing) with 34 bumps
- Low number of external passive components
- Pb-free and compliant with RoHS Directive 2011/65/EU (RoHS 2)
- Operating temperature -20 °C to +85 °C

3 Applications

The main application target is gaming headsets, wireless headsets and headphones.

Thanks to its support for audio, control and data, the NXH3670UK can be used in many applications where ultra-low power and small size are required.

Additional typical applications are mobile phone accessories and computer peripherals.

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
NXH3670UK	WLCSP34	waver level chip-scale package; 34 bumps; 2.45 × 2.87 × 0.38 mm	SOT1403-1

5 Block diagram

Figure 1 shows an overview of the NXH3670UK architecture. The NXH3670UK consists of the following subsystems:

- RF radio:
  - An RF radio transceiver
  - Digital RF modem and calibration logic
- Wireless link controller:
  - A clock shop for dividing, multiplexing and calibrating clocks
  - An ARM Cortex running up to 16 MHz in low-power mode and 84 MHz in high-performance mode:
    - ROM for program
    - RAM for program and data
    - DMA engine
  - A flexible RF MAC for the lower protocol layers:
    - An RF MAC controller interfacing to the radio
    - Packet transmit and receive
    - CRC/whitening/assembly/dis-assembly accelerators
    - Timers
    - An AES security coprocessor
  - Audio processing unit:
    - Latency control unit
    - Dual context G.722/ADPCM codec
    - Sample rate converter
    - A CoolFlux audio DSP with associated memories and DMA engine
  - Interfaces:
    - General-purpose IOs
    - A debug and test UART
    - An SPI slave
    - An audio port supporting I2S modes
  - Timers
  - A watchdog timer
  - A random number generator
- Power Management Unit (PMU):
  - Voltage regulators
  - Power-on reset (POR)
  - Brownout detection (BOD)
  - Power management and reset controller, sleep timer, persistent register file
- A 16 MHz/32 MHz crystal oscillator and various internal oscillators
- A versatile IO switch matrix

These subsystems are described in more detail in Section 7.

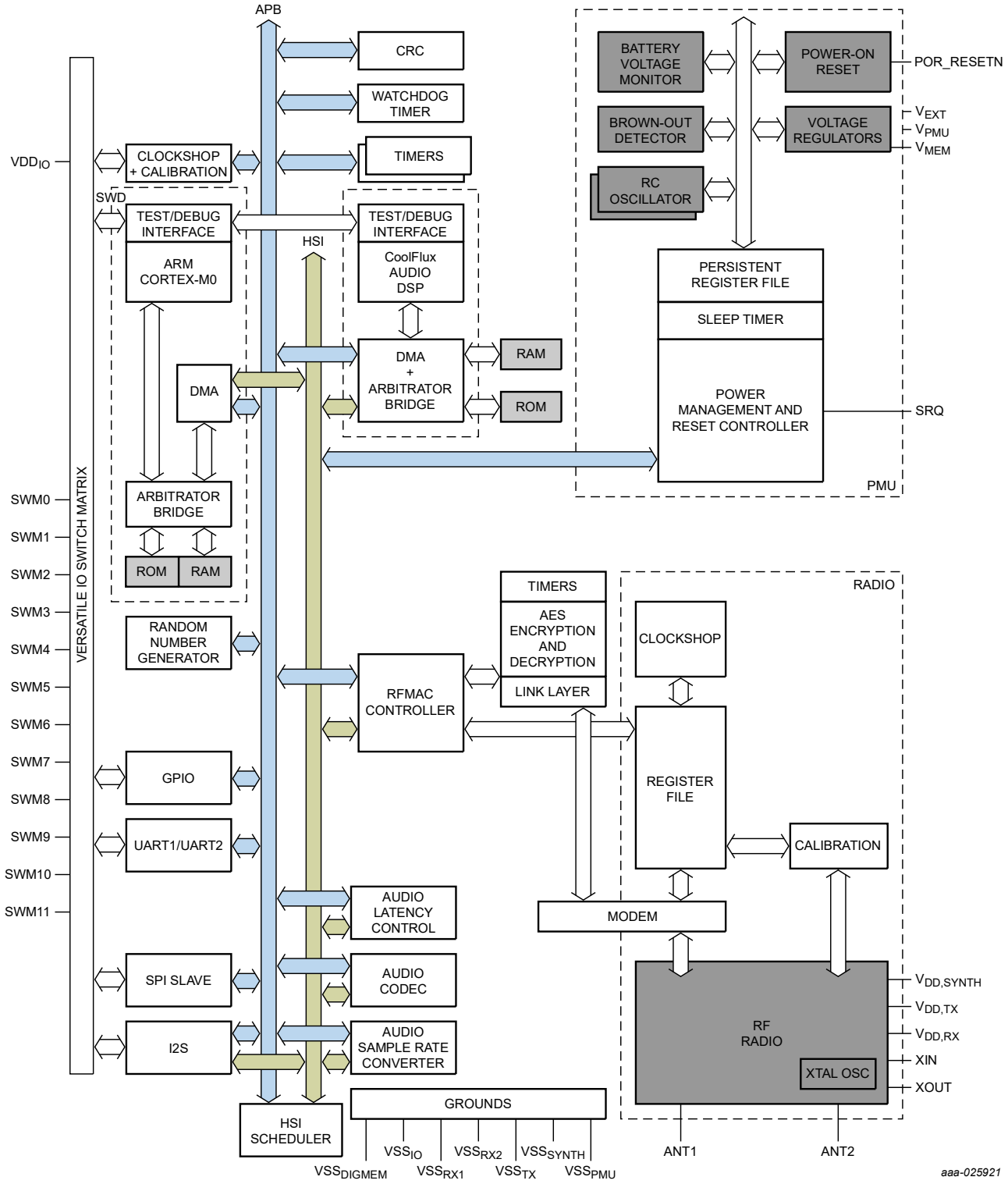


Figure 1. NXH3670UK block diagram

6 Package and pinning information

This chapter provides an overview on the NXH3670UK package and pinning.

6.1 Package

Figure 2 shows the NXH3670UK bump layout

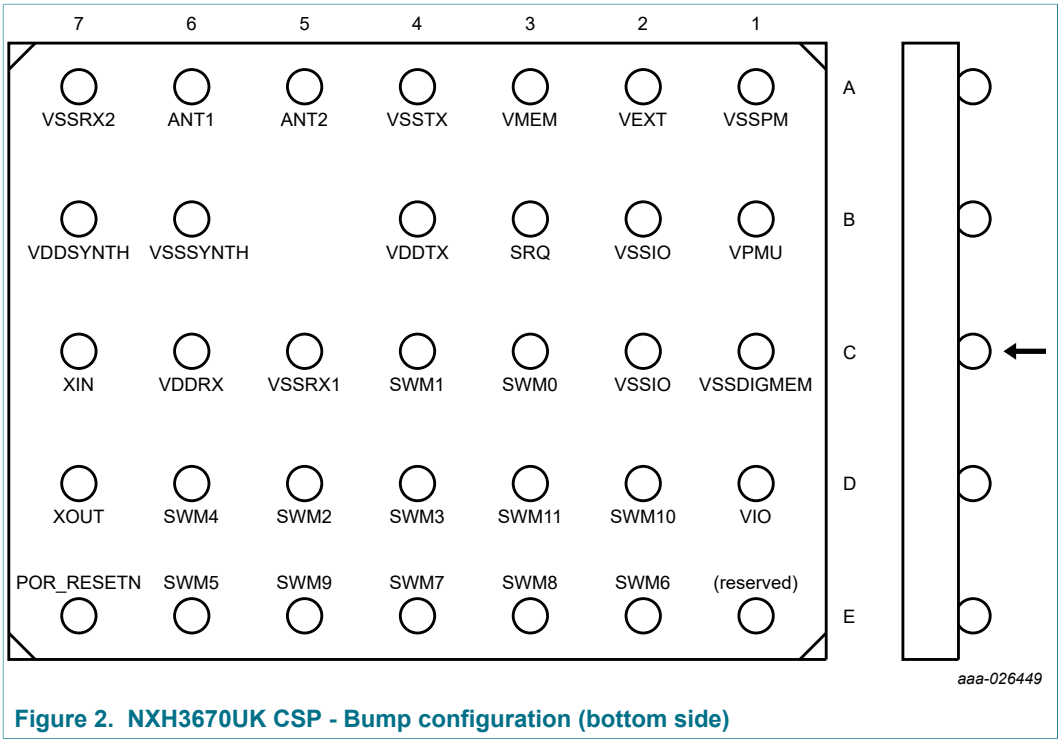


Figure 2. NXH3670UK CSP - Bump configuration (bottom side)

6.2 Pinning

The following table lists the bump assignments, usage and associated pad type. The different types are:

- PWR: supply bump
- GND: ground bump
- RF: RF signal bump
- A: analog bump
- DIO: digital IO bump

At start-up, all digital IOs are set in 3-state input mode.

Table 2. NXH3670UK bumping

Bump	Symbol	Type	Description
Supply			
A2	V_{EXT}	PWR	external power supply
D1	V_{IO}	PWR	IO bumps power supply
A3	V_{MEM}	PWR	To be used for external decoupling of internal supply node. Do not use to supply external circuit (externally connected to V_{EXT})
B1	V_{PMU}	PWR	supply of the analog part of the PMU (externally connected to V_{EXT})
B4	$V_{DD,TX}$	PWR	RF TX power supply (externally connected to V_{EXT})
C6	$V_{DD,RX}$	PWR	RF RX power supply (externally connected to V_{EXT})
B7	$V_{DD,SYNTH}$	PWR	RF synthesizer power supply (externally connected to V_{EXT})
Ground			
C1	$V_{SS,DIGMEM}$	GND	ground for the digital core and memories
C5	$V_{SS,RX1}$	GND	ground for the radio receiver
A7	$V_{SS,RX2}$	GND	ground for the radio receiver
A4	$V_{SS,TX}$	GND	ground for the radio transmitter
B6	$V_{SS,SYNTH}$	GND	ground for the radio synthesizer
A1	$V_{SS,PMU}$	GND	ground for the PMU
C2	$V_{SS,IO}$	GND	ground for the digital IO pads and ESD structures
B2	$V_{SS,IO}$	GND	ground for the digital IO pads and ESD structures
Radio			
A6	ANT1	RF	balanced antenna connection terminal 1
A5	ANT2	RF	balanced antenna connection terminal 2
XOSC			
C7	XIN	A	crystal oscillator input terminal
D7	XOUT	A	crystal oscillator output terminal
IO-SWM			
C3	SWM0	DIO	general-purpose digital IO
C4	SWM1	DIO	general-purpose digital IO
D5	SWM2	DIO	general-purpose digital IO
D4	SWM3	DIO	general-purpose digital IO
D6	SWM4	DIO	general-purpose digital IO
E6	SWM5	DIO	general-purpose digital IO
E2	SWM6	DIO	general-purpose digital IO

Bump	Symbol	Type	Description
E4	SWM7	DIO	general-purpose digital IO
E3	SWM8	DIO	general-purpose digital IO
E5	SWM9	DIO	general-purpose digital IO
D2	SWM10	DIO	general-purpose digital IO
D3	SWM11	DIO	general-purpose digital IO
Miscellaneous			
E7	POR_ RESETN	DIO	reset pin; active LOW, referenced to VBAT
B3	SRQ	DI	service request; to be used by host to change power states.
E1	-	-	(reserved)

7 Functional description

7.1 RF radio transceiver

7.1.1 Features

The RF radio transceiver implements the complete physical layer of a 2.4 GHz ultra low-power RF wireless link. It includes:

- RF functions, power & timing management
- Integrated analog RF front-end with combined Rx/Tx interface
- Symbol demodulation and timing/frequency recovery blocks
- Gaussian frequency shift keying (GFSK) with the following modulation parameters:
  - BLE 2 Mbps mode
    - h = 0.5
    - BT = 0.5
    - 2 Mbps throughput mode
  - BLE 1 Mbps mode
    - h = 0.5
    - BT = 0.5
    - 1 Mbps throughput mode
- Accurate received signal strength indicator (RSSI)
- Integrated frequency synthesizer
- Automatic gain control
- Programmable transmit power
- Trimming and calibration during chip production, removing the need for trimming in the application
- Continuous wave (CW) transmit for test mode

The RF radio transceiver consists of 3 functional blocks:

- The synthesizer, which generates the RF carrier
- The receiver
- The transmitter

The specifications for each of these blocks are described in Section 7.1.2, Section 7.1.3, and Section 7.1.4. They are guaranteed on NXH3670UK reference board schematics and layout.

In-band specifications are referred to RF antenna bumps.

Out-of-band specifications include band-pass filtering of reference board.

7.1.2 Synthesizer specification

Table 3 summarizes the key specifications of the RF synthesizer.

Table 3. Synthesizer specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_c	Carrier frequency	2360	-	2500	MHz
$f_{c,res}$	Carrier frequency resolution	-	1	-	MHz
$f_{ch,2Mbps}$	Non-overlapping channel spacing (2 Mbps and 1 Mbps modes)	-	2	-	MHz
T_{PLL}	PLL turn-on/hop settling time	-	50	-	µs
T_{txrx}	TX/RX turn around time using same channel	-	40	-	µs

7.1.3 Transmitter specification

Table 4 to Table 6 contain the detailed specifications of the RF transmitter.

Table 4. Transmitter generic specifications

Symbol	Parameter	Min	Typ	Max	Unit
P_{RF}	lowest TX output power range	-	−10	-	dBm
	highest TX output power range	-	+4	-	dBm
ΔP_{RF}	TX output power: programming step size	-	2	-	dBm
P_{tol}	output power tolerance at 0 dBm[1]	-	±1.5	-	dBm
Z_{OUT}	output impedance - balanced	-	99-j42	-	Ω
$P_{2,harm}$	power in 2nd harmonic: all rates at 0 dBm	-	-	−30	dBm
	power in 2nd harmonic: all rates at 4 dBm	-	-	−25	dBm
$P_{3,harm}$	power in 3rd harmonic: all rates at 0 dBm	-	-	−30	dBm
	power in 3rd harmonic: all rates at 4 dBm	-	-	−25	dBm
$P_{4,harm}$	power in 4th harmonic: all rates at 0 dBm	-	-	−30	dBm
	power in 4th harmonic: all rates at 4 dBm	-	-	−30	dBm
P_{spur}	spurious emissions (all output levels and rates)[2]				
	30 MHz to1000 MHz	-	-	−36	dBm
	1 GHz to12.75 GHz	-	-	−30	dBm
	47 MHz to 74 MHz	-	-	−54	dBm
	87.5 MHz to 108 MHz	-	-	−54	dBm
	174 MHz to 230 MHz	-	-	−54	dBm
	470 MHz to 862 MHz	-	-	−54	dBm
$P_{spur0dBm}$	spurious emissions for P_{out} < 0 dBm, 2.0 GHz to 3.0 GHz	-	−60	−45	dBm

Symbol	Parameter	Min	Typ	Max	Unit
Δh_{2Mbps}	frequency deviation accuracy (2 Mbps − 0 dBm)	-	±3	±7[3]	%
Δh_{1Mbps}	frequency deviation accuracy (1 Mbps − 0 dBm)	-	±3	±7[3]	%

[1] Measured at 25 °C, full supply voltage range, tested with lab supply. Assuming perfect matching.
[2] Complies with EN 300 440 -1 V1.6.1, EN 300 328 V1.8.1, FCC CFR 47 part 15, ARIB STD-66, RSS-210
[3] Maximum value over temperature and for a supply exceeding 1.05 V

Table 5. Transmitter mode 2 Mbps BLE specifications

Symbol	Parameter	Min	Typ	Max	Unit
BW_{A2Mbps}	20 dB bandwidth	-	2.06	-	MHz
$ACPR_{A2Mbps}$	Adjacent Channel Power Ratio	-	-	−30	dBc
$AACPR_{A2Mbps}$	Alternate Adjacent Channel Power Ratio	-	-	−50	dBc

Table 6. Transmitter mode 1 Mbps BLE specifications

Symbol	Parameter	Min	Typ	Max	Unit
BW_{BLE}	20 dB bandwidth	-	1.030	-	MHz
$ACPR_{BLE}$	Adjacent Channel Power Ratio	-	-	−30	dBc
$AACPR_{BLE}$	Alternate Adjacent Channel Power Ratio	-	-	−50	dBc

7.1.4 Receiver specifications

Table 7 to Table 9 contain the detailed specifications of the RF radio receiver.

The following conventions are chosen:

- Maximum input power $P_{in,max}$ is given for a BER of 10^{-3}
- RX sensitivity $P_{RX,*}$ is defined for a BER of 10^{-3} for all modes

BER of 10^{-3} corresponds to a PER of 30.8 % since a packet length of 46 bytes is used according to the BLE RF PHY test specification

- Co-channel interference $C/I_{CO,*}$ and ACS (C/I) are measured with a wanted signal at −67 dBm and one interferer having the same modulation as the wanted signal. The measurement is done according to the BLE RF PHY test spec for all different modes
- IMD is measured with a wanted signal at −64 dBm and 2 interferers having the same power. The closest interferer is a CW signal and the other interferer has the same modulation as the wanted signal. The largest power of the interfering signals for which the wanted signal fulfills the sensitivity criterion is reported. The measurement is done according to the BLE RF PHY test spec for all different modes.

Table 7. Receiver generic specifications

Symbol	Parameter	Min	Typ	Max	Unit
$P_{in,max}$	maximum input power	-	−10	-	dBm
LO_{leak}	LO leakage	-	−70	-	dBm
OBB	out of band blocking[1]				
	30 MHz to 2000 MHz	-	0	-	dBm
	2003 MHz to 2399 MHz	-	−10	-	dBm
	2484 MHz to 2997 MHz	-	−10	-	dBm
	3000 MHz to 12.75 GHz	-	+10	-	dBm
$RSSI_{dyn}$	RSSI dynamic range	−90	-	−10	dBm
$RSSI_{tol}$	RSSI tolerance	−3	-	+3	dBm
$RSSI_{res}$	RSSI resolution (monotonically)	-	-	3	dBm
IR	image Rejection, C/I[2]	-	−28	-	dB
$P_{spur,RX}$	spurious emissions RX - 25 MHz to 1 GHz	-	-	−57	dBm
	spurious emissions RX - above 1 GHz	-	-	−47	dBm
Z_{in}	input impedance	-	99-j42	-	Ω

[1] As defined by BLE standard (Bluetooth spec 4.0 – Volume 6 – Part A – section 4.3).
[2] Measured at 0.1 % BER, desired signal 3 dB above sensitivity. Image frequency is 2 MHz below the RF frequency in 1 Mbps mode and 3 MHz above the RF frequency in 2 Mbps mode.

Table 8. Receiver mode 2 Mbps BLE specifications

Symbol	Parameter	Min	Typ	Max	Unit
$P_{Rx,2Mbps}$	RX sensitivity	-	−90	-	dBm
$C/I_{CO,2Mbps}$	co-channel C/I	-	8	-	dB
$ACS_{1,2Mbps}$	C/I at 2 MHz	-	−4	-	dB
$ACS_{2,2Mbps}$	C/I at 4 MHz	-	−28	-	dB
$ACS_{N,2Mbps}$	C/I at Δf ≥ 10 MHz	-	−45	-	dB
IMD_{2Mbps}	CW at 6 MHz/8 MHz/10 MHz	-	−36	-	dBm

Table 9. Receiver mode 1 Mbps BLE specifications

Symbol	Parameter	Min	Typ	Max	Unit
$P_{Rx,BLE}$	RX Sensitivity	-	−94	-	dBm
$C/I_{CO,BLE}$	co-channel C/I	-	8	-	dB
$ACS_{1,BLE}$	C/I at 1 MHz	-	−2	-	dB
$ACS_{2,BLE}$	C/I at 2 MHz	-	−28	-	dB
$ACS_{N,BLE}$	C/I at Δf ≥ 10 MHz	-	−45	-	dB
IMD_{BLE}	CW at 3 MHz/4 MHz/5 MHz	-	−36	-	dBm

7.2 Wireless link controller

The sections below are intended to give a summary of the functionality implemented in the wireless link controller.

7.2.1 On-chip buses

7.2.1.1 Advanced peripheral bus (APB)

Both the ARM Cortex-M0 and the CoolFlux audio DSP are masters on the APB. This bus is intended for configuration and status reporting.

The host can access all peripherals on the APB through the software API.

7.2.1.2 HSI data bus

The High-speed interface (HSI) scheduler enables peripherals to access the HSI Data bus using a fixed schedule. The HSI data bus provides scheduled bus access with two-way handshaking between the source and destination peripheral.

7.2.2 ARM Cortex-M0 MCU subsystem

The ARM Cortex-M0 MCU subsystem consists of:

- An ARM Cortex-M0
- 128 kB ROM
- 96 kB RAM
- HSI/APB bridge
- 8 DMA channels; interfacing between the Cortex-M0 memories and the HSI data bus
- A test and debug SWD interface, configurable on SWM

The ARM Cortex-M0 is designed to run at a frequency up to 84 MHz. The maximum operating frequency is however dependent on the core voltage, allowing to trade off between high frequency and low current consumption.

The ARM Cortex-M0 is intended to control the overall system and execute the firmware for higher protocol layers. the RF MAC controller typically handles the lower protocol layers.

Table 10. ARM Cortex-M0 memories

Memory	Value
RAM size	24 K × 32 bit [96 kB]
ROM size	32 K × 32 bit [128 kB]

Table 11. ARM Cortex-M0 configuration

Parameter	Value
Endianness	little endian
Debug port	Serial Wire (SW-DBG)

7.2.3 SPI slave

The SPI slave hardware module provides the interface through which an external host can communicate as master with the wireless link controller. The SPI slave adheres to the 4-wire SPI specification, supporting operation mode 0.

The SPI slave includes:

- 2 buffers (RX and TX) of 72 bytes each:
  - RX buffer: used to transmit message from external host to Cortex-M0
  - TX buffer: used to transmit message from Cortex-M0 to external host
- Flow control settings and status to manage the packet transfers

To allow the controller to request an SPI transfer, a signaling line (GPIO) from the controller to the host can be used.

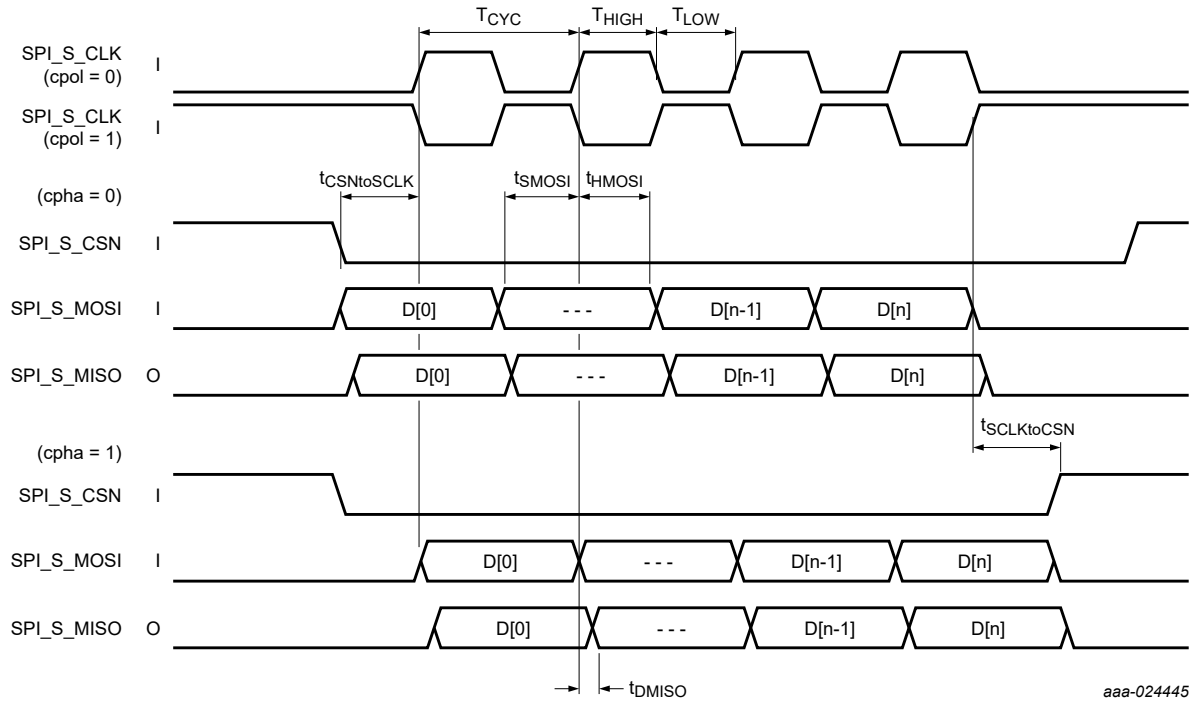


Figure 3. SPI slave timing

Write operations of NXH3670UK SPI slave interface can be done with a clock frequency of 16 MHz. However, for read operations in the final application, the MISO output delay can impact the performances.

Table 12. SPI slave timing for V_{IO} = 0.90 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{CYC}	clock cycle time	V_{IO} = 0.90 V, C_{out} = 15 pF	62.5	-	-	ns
T_{HIGH}	clock HIGH time as a percentage of T_{CYC}		45	-	55	%
T_{LOW}	clock LOW time as a percentage of T_{CYC}		45	-	55	%
t_{SMOSI}	MOSI setup time		12.5	-	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{HMOSI}	MOSI hold time		12.5	-	-	ns
t_{DMISO}	MISO output delay	V_{IO} = 0.90 V, C_{out} = 15 pF, drive strength = HIGH	-	-	45	ns
$t_{CSNtoSCLK}$	chip select LOW to clock		15	-	-	ns
$t_{SCLKtoCSN}$	clock to chip select HIGH		15	-	-	ns

Table 13. SPI slave timing for V_{IO} = 1.20 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{CYC}	clock cycle time	V_{IO} = 1.20 V, C_{out} = 15 pF	62.5	-	-	ns
T_{HIGH}	clock HIGH time as a percentage of T_{CYC}		45	-	55	%
T_{LOW}	clock LOW time as a percentage of T_{CYC}		45	-	55	%
t_{SMOSI}	MOSI setup time		12.5	-	-	ns
t_{HMOSI}	MOSI hold time		12.5	-	-	ns
t_{DMISO}	MISO output delay	V_{IO} = 1.20 V, C_{out} = 15 pF, drive strength = HIGH	-	-	30	ns
$t_{CSNtoSCLK}$	chip select LOW to clock		15	-	-	ns
$t_{SCLKtoCSN}$	clock to chip select HIGH		15	-	-	ns

Table 14. SPI slave timing for V_{IO} = 1.80 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{CYC}	clock cycle time	V_{IO} = 1.80 V, C_{out} = 15 pF	62.5	-	-	ns
T_{HIGH}	clock HIGH time as a percentage of T_{CYC}		45	-	55	%
T_{LOW}	clock LOW time as a percentage of T_{CYC}		45	-	55	%
t_{SMOSI}	MOSI setup time		12.5	-	-	ns
t_{HMOSI}	MOSI hold time		12.5	-	-	ns
t_{DMISO}	MISO output delay	V_{IO} = 1.80 V, C_{out} = 15 pF, drive strength = HIGH	-	-	26	ns
$t_{CSNtoSCLK}$	chip select LOW to clock		15	-	-	ns
$t_{SCLKtoCSN}$	clock to chip select HIGH		15	-	-	ns

Table 15. SPI slave timing for V_{IO} = 2.50 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{CYC}	clock cycle time	V_{IO} = 2.50 V, C_{out} = 15 pF	62.5	-	-	ns
T_{HIGH}	clock HIGH time as a percentage of T_{CYC}		45	-	55	%
T_{LOW}	clock LOW time as a percentage of T_{CYC}		45	-	55	%
t_{SMOSI}	MOSI setup time		12.5	-	-	ns
t_{HMOSI}	MOSI hold time		12.5	-	-	ns
t_{DMISO}	MISO output delay	V_{IO} = 2.50 V, C_{out} = 15 pF, drive strength = HIGH	-	-	25	ns
$t_{CSNtoSCLK}$	chip select LOW to clock		15	-	-	ns
$t_{SCLKtoCSN}$	clock to chip select HIGH		15	-	-	ns

7.2.4 UARTs

The two UART interfaces are not mapped by default on SWM IOs. They are made available externally under control of API.

They are used for debug and testing purposes and are not available for interfacing with a Host. They can for instance be used by the ARM Cortex-M0 or the CoolFlux audio DSP for logging purposes.

More information about configuration parameters of UART interfaces can be found in Table 16.

Table 16. UART configuration parameters

Property	Value
character width	8 bit
stop bits	1 bit
parity	no parity
flow control	no flow control
baud rate	888888

7.2.5 GPIOs

The NXH3670UK supports General-purpose input output (GPIO) functionality. The GPIO functionality is not available by default, but the ARM Cortex-M0 core has access to it via the switch matrix configuration.

Every SWM bump that is not used as a host interface can be used as a GPIO function, with following features:

- Enable as input or output
- Enable the generation of an interrupt on an event on the GPIO:
  - Generate an interrupt on a rising edge on the GPIO
  - Generate an interrupt on a falling edge on the GPIO
- Read data from the GPIO
- Write data to the GPIO

7.2.6 I^2S (dataport)

The I^2S or dataport is used for audio transmission between the NXH3670UK and a host or a codec. The interface uses four lines as shown in Table 17.

Table 17. I^2S Signal names

Signal name	Description
I2S_WS	word select line I2S_WS, indicating the channel (LEFT or RIGHT) being transmitted in I^2S mode.
I2S_CLK	clock line I2S_CLK, specifying the bit rate
I2S_SI	input data line
I2S_SO	output data line

The following configuration options are available:

- Slave mode supports 48 kHz
- Word length (common value for both input and output channels): 16 bit or 32 bit (16 bit sample is left aligned, other bits are omitted)

7.2.7 Clock shop

The clock shop modules provide the necessary clocks for the ARM Cortex-M0 and all the other modules in the wireless link controller. Each module has its own clock or clocks, generated by the clock shop. Each clock individually has the following settings:

- Clock source
- Enable/disable
- Division factor

For the clocks to be reprogrammed in a safe way (such that no spikes occur on the clock signal), the parameters have to be programmed in a certain order. For all clocks, it is recommended to disable the clock before changing the divider setting. The ARM Cortex-M0 clock itself is a special case, since it cannot be switched off or the system would lock up. For this reason, the parameter updates for this block are synchronized with the running clock during update.

Clock switching is glitch free for modules that require clock switching in active mode. These modules are:

- The ARM Cortex-M0
- The HSI bus
- The ADPCM/G.722 CODECs
- The CoolFlux audio DSP

The clock shop can be programmed via software API by the ARM Cortex-M0.

The clock shop module also contains a calibration function. This function can be used to adjust the internal RC oscillator frequencies by comparing them with the 16 MHz/32 MHz crystal oscillator clock.

7.2.8 Timers

The NXH3670UK contains two identical hardware timer modules. Each timer module is a 16- bit interval timer with 3 independent capture/compare registers.

7.2.9 Audio processing

The wireless link controller contains the following modules for audio processing: G.722/ ADPCM codec instance, sample rate converter, audio latency control instance, and the CoolFlux audio DSP.

7.2.9.1 G.722/ADPCM codec

The audio codec hardware module has the following specifications:

- 2 contexts, each context can independently encode/decode an audio stream
- Two supported modes:
  - Subband ADPCM according to ITU-T G.722 mode 1
  - Low-latency single band ADPCM

Typical sample rate of G.722/ADPCM compression is 16 kHz but it can be used up to 48 kHz.

7.2.9.2 Latency control

The latency control hardware module controls the end-to-end audio latency across the wireless link to a programmable value. This control is especially important for synchronous streams (for example left/right audio channel) where it is mandatory to achieve the same audio latency. The latency control hardware module contains timers and an NCO, which are steered to maintain the configured audio latency.

7.2.9.3 CoolFlux audio DSP

The CoolFlux audio DSP is a hardware audio accelerator used to implement audio functions such as audio compression/decompression standards, equalization and audio mixing. It is designed to work typically at 16 MHz or a lower frequency, but can run at a frequency up to 84 MHz in the configuration where an external regulator is used.

A test and debug interface, available on SWM IO through configuration is also provided.

The CoolFlux audio DSP subsystem is connected to the HSI data bus through a DMA engine, which can handle up to 8 independent queues. This DMA engine can reach the program memory and both X and Y data memories.

The CoolFlux audio DSP can access the APB bus via the APB memory bridge, through an APB arbiter. Conversely, the Cortex-M0 has access to CoolFlux IO register map, also via the APB memory bridge.

The CoolFlux DSP program images are loaded from an external device (e.g. EEPROM) by the boot loader running on the Cortex-M0. The loading is performed through the DMA interface, while holding the DSP in reset.

Amount of X and Y memories is configurable at startup from a fixed pool of ROM and RAM.

Table 18 indicates the sizes of the different memories:

Table 18. CoolFlux memories

Memory	Value
P-RAM size	8 K × 32 bit [32 kB]
P-ROM size	16 K × 32 bit [64 kB]
RAM pool (X and Y) size	20 K × 24 bit [60 kB]
ROM pool (X and Y) size	10 K× 24 bit [30 kB]

7.2.10 Random number generator (RNG)

The Random number generator (RNG) is a true random number generator to be used for security purposes. It takes multiple clock sources as input to provide a random number on request.

7.2.11 RF HWMAC accelerator

The RF HWMAC accelerator implements the medium access control (MAC) layer of the radio. The MAC consists of:

- RFMAC controller
- Configuration interface toward the RF modem and RF radio
- DMA engine with 4 channels for interfacing with HSI bus and Cortex-M0
- Radio data path
  - Up to 4 configuration banks for TX and 4 configuration banks for RX
  - Packet assembly, disassembly (address, header, payload)
  - CRC accelerator
  - Whitening accelerator
  - AES security accelerator
    - Off-line encryption/decryption of payload data using API control
    - On-the-fly encryption/decryption of BLE payload data
  - Accurate timers for packet timing

7.2.11.1 External PA control

The following signals, available through the switch matrix, provide external PA support:

- PA enable
- RX enable

7.2.12 Versatile IO switch matrix

This module allows connection of the various functional signals to a limited set of actual chip IO pins. The switch matrix pad voltage is referenced to VIO.

During reset (POR_ RESETN), SWM pins are in 3-state.

The following table gives an overview of the functionalities that are multiplexed on each of the SWM pins:

Table 19. Versatile switch matrix

Pin	Default	Configuration A[1]	Configuration B[1]	Configuration C[1]	Configuration D[1]
SWM00	SPI_S_MISO (output)	SPI_S_MISO (output)	SPI_S_MISO (output)	SPI_S_MISO (output)	SPI_S_MISO (output)
SWM01	SPI_S_MOSI (input)	SPI_S_MOSI (input)	SPI_S_MOSI (input)	SPI_S_MOSI (input)	SPI_S_MOSI (input)
SWM02	SPI_S_CLK (input)	SPI_S_CLK (input)	SPI_S_CLK (input)	SPI_S_CLK (input)	SPI_S_CLK (input)
SWM03	SPI_S_CSN (output)	SPI_S_CSN (output)	SPI_S_CSN (output)	SPI_S_CSN (output)	SPI_S_CSN (output)
SWM04	SPI_S_INT (output)	SPI_S_INT (output)	SPI_S_INT (output)	SPI_S_INT (output)	SPI_S_INT (output)
SWM05[2]	(tristate)	(tristate)	(tristate)	I2S_SO (output)	(tristate)
SWM06[2]	(tristate)	I2S_SI (input)	I2S_SI (input)	I2S_SI (input)	UART_RXD (input)
SWM07[2]	(tristate)	I2S_SO (output)	I2S_SO (output)	UART_TXD (output)	UART_TXD (output)
SWM08[2]	(tristate)	UART_TXD (output)	EXT_RXEN(CRX) (output)	EXT_RXEN(CRX) (output)	EXT_RXEN(CRX) (output)
SWM09[2]	(tristate)	UART_RXD (input)	EXT_PAEN(CTX) (output)	EXT_PAEN(CTX) (output)	EXT_PAEN(CTX) (output)
SWM10[2]	(tristate)	I2S_CLK (input)	I2S_CLK (input)	I2S_CLK (input)	(tristate)
SWM11[2]	(tristate)	I2S_WS (input)	I2S_WS (input)	I2S_WS (input)	(tristate)
SRQ	SPI_S_SRQ (input)	SPI_S_SRQ (input)	SPI_S_SRQ (input)	SPI_S_SRQ (input)	SPI_S_SRQ (input)

[1] The configuration of A,B,C, or D is performed by the host controller with an HCI SPI command just after booting the NXH3670.
[2] SWM pins 5 to 11 are only enabled after the host controller triggers the function with an HCI SPI command.

Section 9.2 explains the default positions of SPI master and SPI slave during boot mode.

7.2.13 Power management unit (PMU)

7.2.13.1 General

The PMU module supports the following operating modes:

- Operation on external power regulator (1.2 V)

It provides regulated power supplies from the external voltage to supply:

- Radio subsystem
- Digital and memories

Under control of firmware, the PMU is able to optimize current consumption in each use case by enabling and controlling the supply of only the hardware blocks necessary for the use case.

The PMU also contains state machine that allows support of different low-power modes (see Section 9) and wake-up functionality. The wake-up can be triggered from the following sources:

- POR
- Low-power timer
- SRQ (service request) pin

In addition, it contains functionality for battery voltage monitoring, Power-on reset (POR) and to detect power dips (BOD). It also includes a persistent register file for configuration and trimming that is kept in all power modes.

7.2.13.2 Power-on reset (POR)

A Power-on reset (POR) circuit ensures proper startup of the chip. It comprises:

- A detector responsive to the presence (ramp-up) of the supply voltage VEXT
- A 50 ms delay circuit to stretch the POR signal. This delay is called TPOR. This delay is to ensure proper start-up of the chip after insertion of a new battery which can cause the battery to bounce.

The POR module is always enabled. A reset generated by the POR module resets the complete IC, including the PMU.

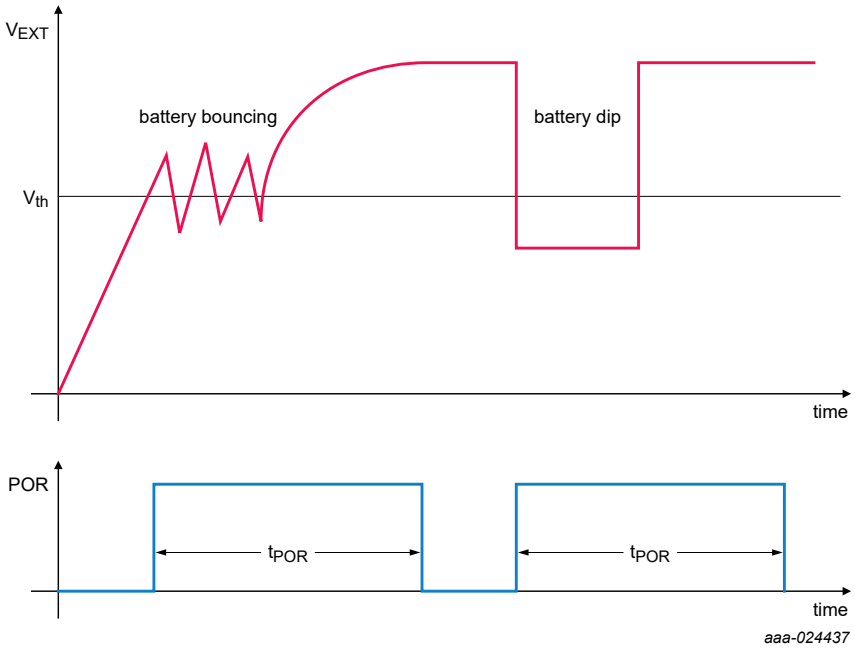


Figure 4. Battery bouncing/dip + Power-on-reset

When V_{EXT} drops below V_{POR}, the power-on reset circuit drives the RESETN signal LOW weakly to generate a clean reset signal to reset the PMU. The PMU prolongs the reset for t_{POR} to reset the rest of the chip. When not active, the power-on reset circuit is driving the RESETN signal weakly HIGH (see Figure 5).

An external device can override the power-on reset circuit and trigger a reset by driving the RESETN signal LOW. It is not allowed to drive the RESETN signal HIGH or to put an external pull resistor on the RESETN signal. A HIGH on RESETN prevents correct operation of the power-on reset circuit.

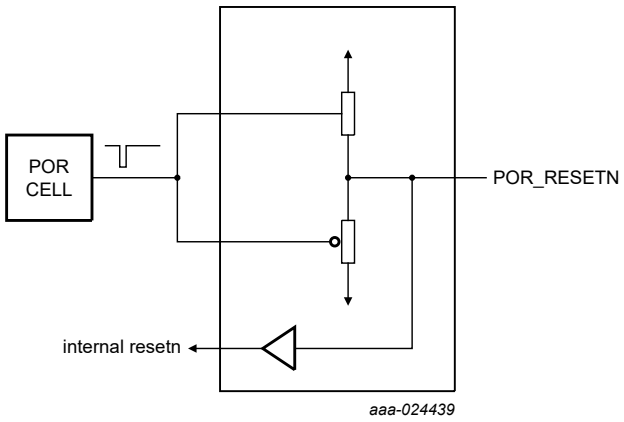


Figure 5. Details of POR_RESETN pad

Table 20. POR

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{POR}	POR stretching time		34	50	102	ms
V_{TH}	POR threshold	minimum V_{EXT} = 0.8 V, maximum V_{EXT} = 1.45 V	0.68	0.8	0.89	V

7.2.13.3 Brownout detection (BOD)

In addtion to the POR protecting the power domain which is continuously on, the NXH3670UK also has Brownout detection (BOD) for internal supplies. The brownout threshold voltage can be programmed. Each brownout detector generates a signal that can force a POR.

The goal of the BOD cells is to protect the circuit against malfunctioning in case of dips on the supply voltage.

7.2.13.4 Persistent registers

The PMU also contains persistent registers. These registers are directly supplied from V_{EXT} so that their value is retained even when all other digital supplies are off.

These registers contain values that must be retained to allow restart from some low-power modes. The values that are stored here are configuration parameters and trimming values.

7.2.13.5 Clock generation

The NXH3670UK typically derives its internal clocks from a 16 MHz/32 MHz crystal oscillator. In some modes, in order to save power or to generate faster clock, the chip can also generate clocks from internal oscillators. LPOs at 16 MHz and 20 MHz, HFOs at 44 MHz and 84 MHz and ULPO/LJO at 400 kHz oscillators are provided. The internal oscillators can be trimmed from the crystal oscillator clock.

7.2.13.6 Crystal oscillator

An external crystal must be connected to the crystal oscillator pins (XIN, XOUT) in order to generate a clock for the NXH3670UK. Both 16 MHz and 32 MHz crystals are supported but internally the clock is 16 MHz.

The oscillator is provided with on chip capacitors to remove the need for external load capacitors. A fraction of these capacitors is trimmable in order to adjust the frequency accuracy. The trimming is done through firmware during PCB assembly to get to the desired accuracy for the application.

The crystal oscillator is not enabled until the Cortex boots up; the control of the crystal remains under control of the firmware.

If a 16 MHz/32 MHz clock is already present in the application, this clock can be provided to the NXH3670UK through the XIN bump, provided this clock supports the required characteristics to sustain RF performances (see Table 23).

If other devices want to slave from the NXH3670UK crystal, the crystal signal must be taken from the XIN bump. Constraints for this configuration can be found in Table 24.

Table 21. 16 MHz crystal oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{XTAL}	crystal frequency		-	16	-	MHz
Δf_{XTAL}	crystal frequency tolerance [1]	untrimmed, including temperature and aging	−60	-	+60	ppm
C_L	crystal load capacitance		8	10	12	pF
C_0	crystal static capacitance		-	1.5	7	pF
R_{L-16}	crystal series resistance - 16 MHz		-	-	200	Ω
L_{S-16}	equivalent crystal serial inductance - 16 MHz		-	-	90	mH
T_{XTAL}	crystal oscillator settling time [2]		0.8	1.5	2.5	ms
$f_{noise16M}$	phase noise characteristics for 16 MHz crystal frequency	offset from carrier at 10 kHz	-	−130	-	dBc/Hz
		offset from carrier at 100 kHz	-	−136	-	dBc/Hz

[1] To support 250 kbps/1 Mbps data rate in NxH-C mode, a ±50 ppm accuracy is needed.
[2] Settling time depends on crystal parameters. Typical value based on 8 pF/60 mH/100 Ω.

Table 22. 32 MHz crystal oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{XTAL}	crystal frequency		-	32	-	MHz
Δf_{XTAL}	crystal frequency tolerance [1]	untrimmed, including temperature and aging	−60	-	+60	ppm
C_L	crystal load capacitance		6	10	12	pF
C_0	crystal static capacitance		-	1.5	7	pF
R_{L-32}	crystal series resistance - 32 MHz		-	-	100	Ω
L_{S-32}	equivalent crystal serial inductance - 32 MHz		-	-	45	mH
T_{XTAL}	crystal oscillator settling time [2]		0.8	1.5	2.5	ms
$f_{noise32M}$	phase noise characteristics for 32 MHz crystal frequency	offset from carrier at 10 kHz	-	−124	-	dBc/Hz
		offset from carrier at 100 kHz	-	−130	-	dBc/Hz

[1] To support 250 kbps/1 Mbps data rate in NxH-C mode, a ±50 ppm accuracy is needed. (BLE specification requirement)
[2] Settling time depends on crystal parameters. Typical value based on 8 pF/30 mH/100 Ω.

Table 23. 16 MHz/32 MHz Input clock characteristics when external crystal is provided to XIN

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLK}	crystal frequency		-	16/32	-	MHz
Δf_{CLK}	accuracy		−20	-	+20	ppm
V_{PP}	input clock amplitude	peak to peak voltage (sine wave)	500	-	800	mV
$f_{noise16M}$	phase noise characteristics for 16 MHz crystal frequency	offset from carrier at 10 kHz	-	−130	-	dBc/Hz
		offset from carrier at 100 kHz	-	−136	-	dBc/Hz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{noise32M}$	phase noise characteristics for 32 MHz crystal frequency	offset from carrier at 10 kHz	-	−124	-	dBc/Hz
		offset from carrier at 100 kHz	-	−130	-	dBc/Hz

Table 24. 16 MHz/32 MHz clock characteristics when external host loads from XIN

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{CLK}	crystal frequency			-	16/32	-	MHz
C_L	XIN pin load			-	-	5[1]	pF
V_{PP}	output clock amplitude	peak-to-peak volage (sine wave)	[2]	-	200	-	mV

[1] Depending on used crystal
[2] Output amplitude is configurable by firmware. The swing has impact on current consumption and phase noise. Full swing is needed in order to meet radio performance.

7.2.14 One-Time Programmable (OTP) memory

The OTP holds trimming values for the PMU and RF. Programming of those bits is done during chip production.

8 Debugging and testing facilities

8.1 UART

The NXH3670UK features a complete UART interface which both the ARM Cortex-M0 and the CoolFlux DSP can use. More information about configuration parameters of UART interfaces can be found in Table 16.

As well as this complete UART interface, the CoolFlux DSP has a dedicated TX-only UART for logging purposes

UARTs are available on SWM IOs according to Table 19.

9 Start-up and power modes

9.1 Booting procedure

9.1.1 Power supply sequence

To prevent leakage current via I/Os of NXH3670UK and undefined state of the SWMs, V_{IO} should not be enabled before V_{EXT}. V_{IO} is enabled preferably at the same time as or later than V_{EXT}.

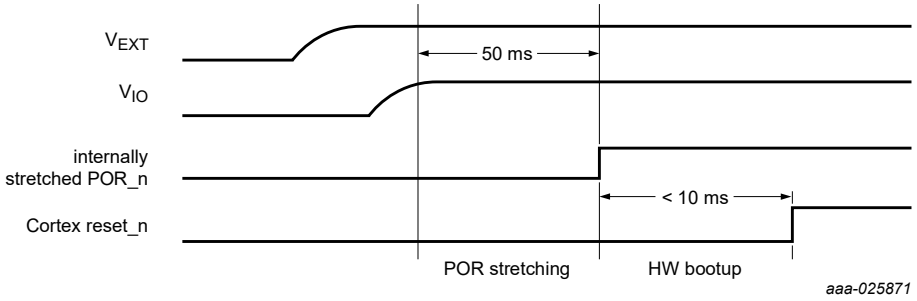


Figure 6. Power supply sequence

9.1.2 Boot loader

The boot loader is the default ROM code which is executed by the Cortex M0 after a POR. The boot loader brings the IC in the ‘active user mode’ as shown in Figure 7. The boot loader in SPI Command Handler exposes command over SPI in order to load an image.

More information of the functionality can be found in Section 9.2.

Detailed boot loader commands can be found in the "NXH3670UK boot loader" document (Ref. 2).

9.1.3 Boot time

The boot time depends on several factors that are system and user application specific:

- Size of the firmware to be downloaded
- Speed of the SPI interface
- Maximum current allowed by the application (possibly limiting the speed of the SPI interface)

There is also a fixed time at start-up before the real boot procedure can start. This time includes POR reset, configuration, and start-up of the supplies and the clock. This time is less than 60 ms, considering a POR delay of 50 ms.

9.2 State diagram

Figure 7 shows how the NXH3670UK starts up and switches between different states. The sections below describe the different states and how the system switches between them. The different states are:

- Reset
- Init
- SPI command handler
- Active user mode
- SLEEP

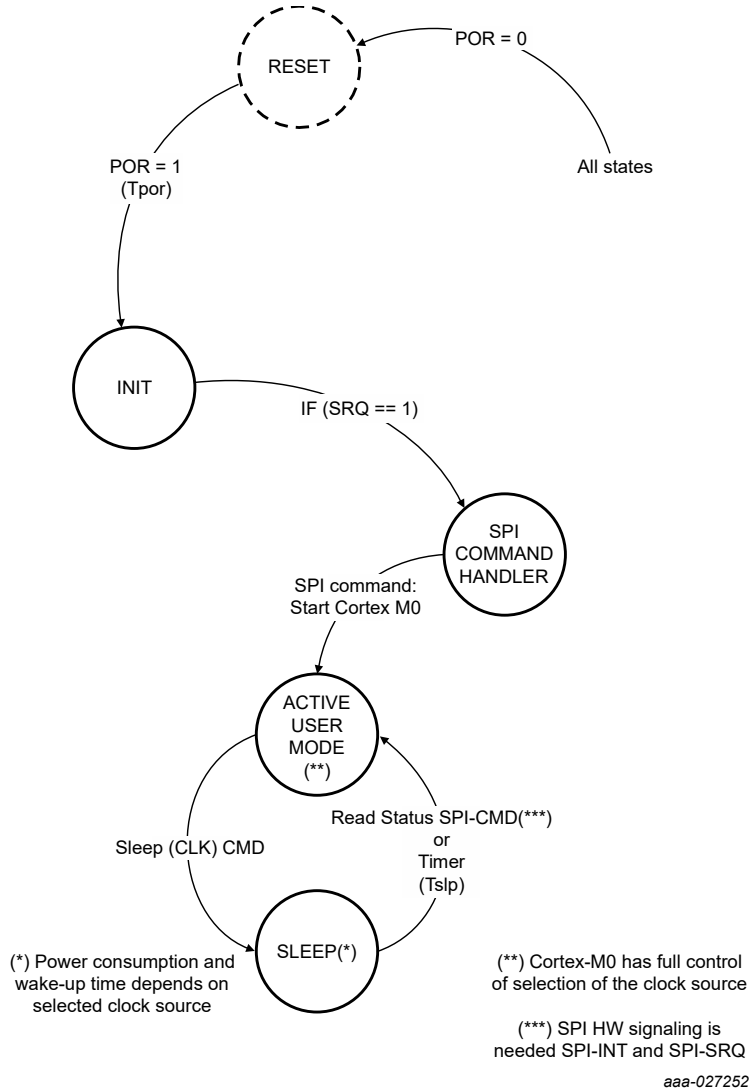


Figure 7. NXH3670UK start-up and power modes

9.2.1 Reset (undefined)

This state is the default state of the chip when the battery is inserted. The full chip is OFF, with the core kept in a stable state by the POR cell.

All the functions in the chip are off or disabled. Only the POR cell is active.

This state can be entered from all other state for different reasons:

- Battery voltage going below the minimum level
- BOD event (impact of BOD event is configurable by API after start-up)
- Firmware generated reset

As a POR state transition can be generated from all states, it is not repeated as possible state transition in the sections below.

When the power-on reset cell has settled, the chip can start up and enter the INIT state.

9.2.2 Init

The init state configures the NXH3670UK for correct operation. This state can only be entered from the reset state. The battery voltage is measured and the PMU configures the different supply generation blocks to the right settings. The trimming and functional configuration settings are loaded from OTP. To keep the current consumption low in this state, most of the digital logic remains inactive.

The Cortex works from the on-chip 16 MHz LPO oscillator clock in the Init state.

The NXH3670UK checks the status of the SRQ (service request) input pin.

- If SRQ = logic 0, the NXH3670UK stays in the init state
- If SRQ = logic 1, the NXH3670UK enters the SPI command handler state

9.2.3 SPI command handler

During this state, the MCU system is started and the boot loader firmware is executed from ROM to enable firmware download.

The NXH3670UK is slave of the host and download is started and executed through SPI commands

The following steps are performed:

- SPI slave interface is enabled by default using:
  - SMW00: SPI_S_MISO
  - SMW01: SPI_S_MOSI
  - SMW02: SPI_S_CLK
  - SMW03: SPI_S_CS
- Based on a set of SPI commands, the host can download an image into the ARM Cortex-M0 memory
- When the firmware download is completed, the NXH3670UK moves to active user mode state upon receiving an SPI command

Following functionality is provided to the host controller based on SPI commands:

- Read & Write ARM memory:
  The host is able to read and write ARM memory.
- Read & Write CoolFlux memory:
  The host is able to read and write CoolFlux program and data memory.
- Initialize/Disable CoolFlux:
  The host can enable and disable the CoolFlux DSP.
- Start application:
  The host is able to force the boot loader to start execution from a given ARM-program-memory location.
- Get version:
  The host can retrieve the version of the boot loader and the hardware.
- Reset command:
  The host can trigger a reset of the device.
- Reinitialize SWM:
  The host can reconfigure the SWM.

9.2.4 Active user mode

In this state, the NXH3670UK can activate all blocks and run all necessary activities for the application. RF transmission and reception, audio processing, link control, SPI transfers are all done in active user mode state

Generally, the system only stays in this mode during the real period of activity. When this activity is finished, it switches to the sleep state. However, even in this mode the current consumption is minimized by stopping the clock and the supply to the blocks which are not active.

This state can be entered from the SPI command handler state after firmware download or from the sleep state when the chip wakes up.

The system can enter the sleep state based on a dedicated MCU command.

In the active user mode state, the SPI_S_SRQ and SPI_S_INT must be used for signaling from the host to the NXH3670UK.

9.2.5 Sleep

The sleep state is the low-power mode state. To reduce current consumption, this state is used as much as possible between periods of activity of the chip. It allows the quickest restart as the full state of the chip is kept.

In this state, the digital logic that must retain its state is kept supplied. All the unnecessary clocks are stopped and the MCU are in idle state. Typically, the system runs on ULPO or LJO[1] but the firmware can decide to keep other clocks active (e.g. the XTAL clock). Because the current consumption depends on the clocks and blocks that are requested to stay active by the MCU, it is variable in this state. However, most of the time the leakage of the digital logic and the clock generation determines the current consumption.

This state is entered from the active user mode state through a Cortex MCU sleep command.

The system can go back to the active user mode state based on interrupt, typically coming from an SPI read status command or a timer event.

1 Applications using ULPO/LJO as sleep timer clock must consider the drift in frequency caused by a change in temperature or VEXT supply.

10 Current consumption

Table 25 shows the NXH3670UK current consumption for different modes of operation. The conditions for the current values are given in the table. For the low-power modes and for the radio modes, the current is typically constant. For the use cases, the value given is an average of the current consumption over multiple periods of RF activity.

All values are measured on reference board for typical process at 1.2 V and 25 °C. They do not include the current from V_{IO} as it depends on activity, switch matrix configuration, and application board load.

The NXH3670UK uses the high-performance (HP) mode.

Table 25. Current consumption

Mode/Use case	Conditions	HP	Unit
SLEEP	ULPO active and Cortex retention	63	µA
	LJO active and Cortex retention (incremental) LJO frequency is 650 kHz	10	µA
	CoolFlux memory retention (incremental)	10	µA
XTAL oscillator 32 MHz	Murata XRCMD32M000FXP52R0 crystal (recommended). Includes RF band gap and XTAL LDO	115	µA
Start-up	maximum current during start-up, from POR to the active user mode state	< 4	mA
Active	Cortex active baseline current. XTAL oscillator not included	950[1]	µA
	audio subsystem baseline (incremental)	155	µA
	CoolFlux memory active (incremental)	110	µA
Cortex	processor and memory only, excluding leakage and static clock tree consumption. Radio and audio inactive.		
	WFI	17	µA/MHz
	while-1 loop	76	µA/MHz
CoolFlux	processor and memory only, excluding leakage and static clock tree consumption.		
	idle	8	µA/MHz
	SBC encoding	61	µA/MHz
Audio HW	dataport in 16 kHz – coder – decoder – ASRC – dataport out. Not including V_{IO} current (use case dependent). (excluding leakage and static clock tree consumption)	90	µA
Radio activation		404	µA
	after that XTAL settles	0.162	ms

Mode/Use case	Conditions	HP	Unit
Radio RX	ramp-up current including RFMAC and RFPHY but not Cortex. All radio modes	1.25	mA
	ramp-up time	0.12	ns
	active current including RFMAC and RFPHY but not Cortex, All radio modes	4.0	mA
Radio TX	ramp-up current including RFMAC and RFPHY but not Cortex. All radio modes	1.25	mA
	ramp-up time	0.12	ms
	active current at −10 dBm, including RFMAC and RFPHY but not Cortex. All radio modes, Ideal load presented to RF antenna bumps	3.7	mA
	active current at 0 dBm, including RFMAC and RFPHY but not Cortex. All radio modes. Ideal load presented to RF antenna bumps	7.2	mA
	active current at 4 dBm, including RFMAC and RFPHY but not Cortex. All radio modes. Ideal load presented to RF antenna bumps	13.4	mA

[1] This number includes static power consumption of the 84 MHz FRO

11 Limiting values

Table 26. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{EXT,MAX}$	supply voltage	applying to all supplies connected to the V_{EXT}		−0.5	+1.5566	V
$V_{IO,MAX}$	IO Pad voltage	fail-safe operation between minimum and maximum values.		−0.3	+2.7	V
P_{TOT}	total power consumption			-	1	W
T_{JUNCT}	junction temperature			−40	+125	°C
T_{STO}	storage temperature			−40	+150	°C
RH	operating humidity range		[1]	-	95	%
V_{ES}	electrostatic handling voltage	human body model (HBM)[2]				
		all pins		-	2000[3]	V
		charged device model (CDM)[4]				
		all pins		-	500[5]	V

[1] MSL - Moisture Sensitivity Level - JEDEC J-STD-20D - maximum level 3 (168 hours floor life at ≤ 30 °C and 60 % relative humidity)

[2] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor (human body model) compliant with JESD22-A115-AJS-001-2014 norm.

[3] JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process

[4] Only applied to integrated component, Compliant with JESD22-C101-AC101F norm.

[5] JEDEC document JEP157 states that 500 V HBM allows safe manufacturing with a standard ESD control process

12 Electrical characteristics

Table 27. Electric and environmental characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{AMB}	operating temperature range			−20	+25	+85	°C
V_{EXT}	external regulator	maximum current is limited to 9 mA for digital and 6 mA for memories.		1.14	1.2	1.26	V
V_{NOISE}	external supply voltage noise	from external supply, up to 20 kHz		-	-	150	mVpp
V_{IO}	IO supply voltage	$V_{IO} \geq V_{EXT}$					
V_{IL}	input level LOW	percentage of V_{IO}; SWM pads		-	-	30	%
V_{IH}	input level HIGH	percentage of V_{IO}; SWM pads		70	-	-	%
V_{OL}	output level LOW	percentage of V_{IO}; at I_{OL} = 2 mA		-	-	20	%
V_{OH}	output level HIGH	percentage of V_{IO}; at I_{OH} = 2 mA		80	-	-	%
I_{OL}	output drive capability LOW	API selectable speed mode: low, nominal, high; maximum 8 SSO		-	-	2	mA
I_{OH}	output drive capability HIGH	API selectable speed mode: low, nominal, high; maximum 8 SSO		-	-	2	mA
R_{pull}	pull-up resistor IO pins	tolerance < 20 %		-	50	-	kΩ
V_{t+}	Schmitt trigger rising threshold			0.7	-	-	V_{IO}
V_{t-}	Schmitt trigger falling threshold			-	-	0.3	V_{IO}
V_{HYS}	hysteresis voltage			0.1 * V_{IO}	0.15 * V_{IO}	-	V
t_r	IO rise time; V_{IO} = 1.2 V − 1 SSO; C_L = 62 pF[1]	low-speed mode		-	24	-	ns
		nominal-speed mode		-	12	-	ns
		high-speed mode		-	6	-	ns
t_f	IO fall time; V_{IO} = 1.8 V − 1 SSO; C_L = 62 pF[1]	low-speed mode		-	16	-	ns
		nominal-speed mode		-	12	-	ns
		high-speed mode		-	6	-	ns
C_p	bump capacitance	all digital IO pads		-	4	-	pF
C_L	load capacitance		[2]	-	15	100	pF

[1] Measured on reference board under typical conditions.
[2] High bump load may impact the speed of some interfaces.

13 Application information

To enable high-performance mode, all following application diagrams use external regulated supplies.

The NXH3670UK is delivered with precompiled binaries which are booted from the host controller (KL27 on SDK board or other). Based on the host API, the host controller controls these binaries over the SPI interface (see the SDK documentation for more information). These binaries constitute a complete application including power handling, radio configuration (e.g. pairing), and audio processing up to the I^2S interface.

13.1 Headset application diagram

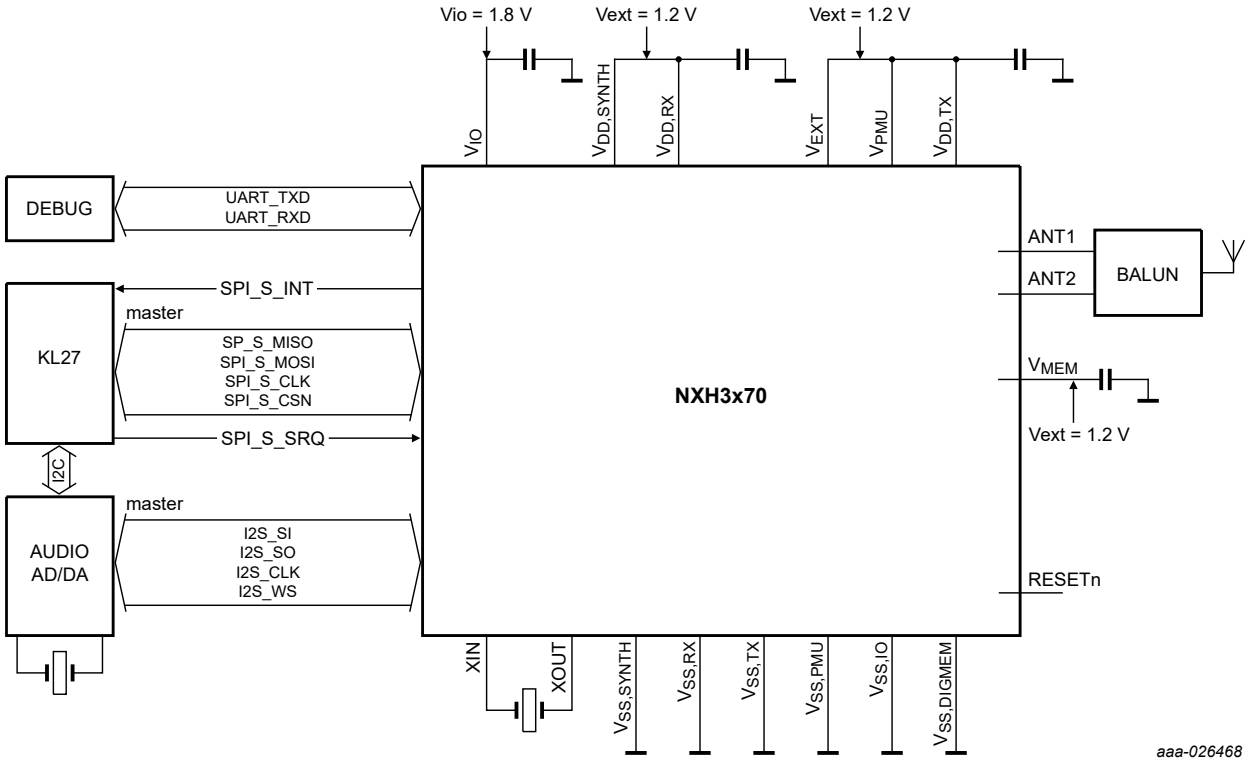


Figure 8. Headset application diagram

13.2 Dongle application diagram

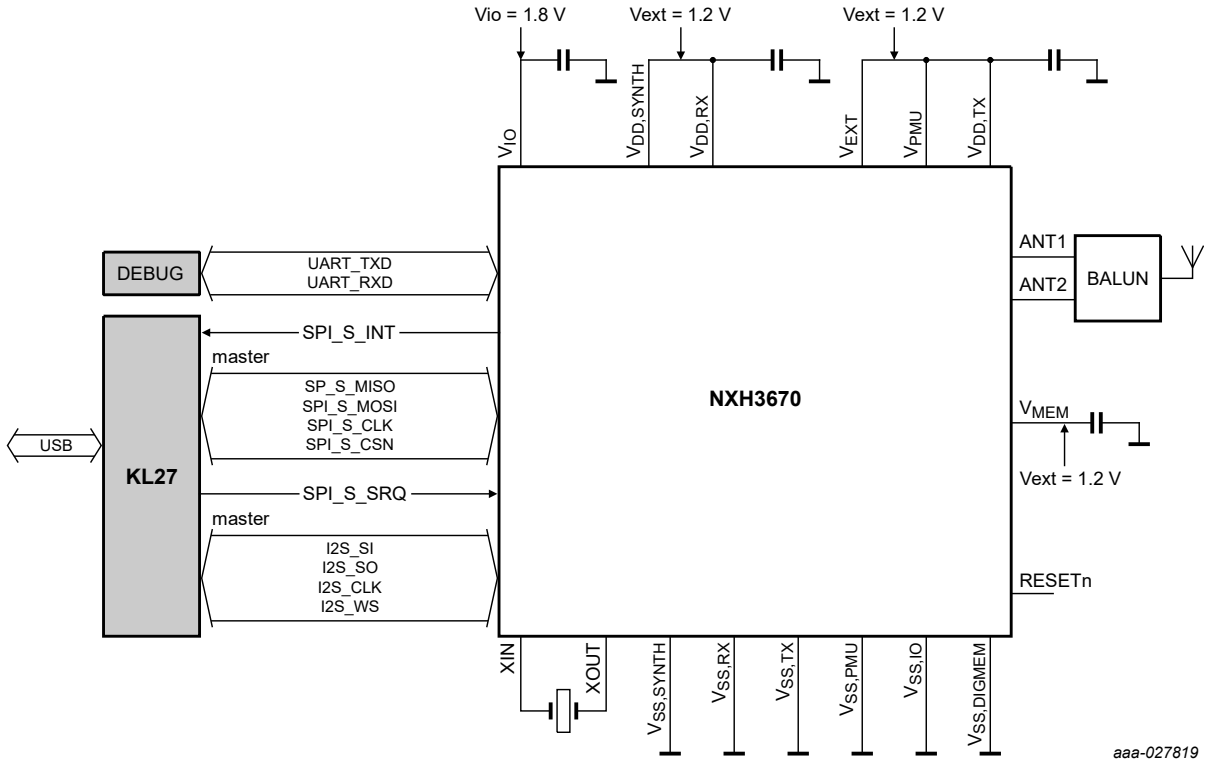


Figure 9. Dongle application diagram

13.3 External decoupling capacitors

The NXH3670UK design minimizes the requirement for external decoupling. All decoupling capacitors use 0201 package.

Table 28. Specification of decoupling capacitors

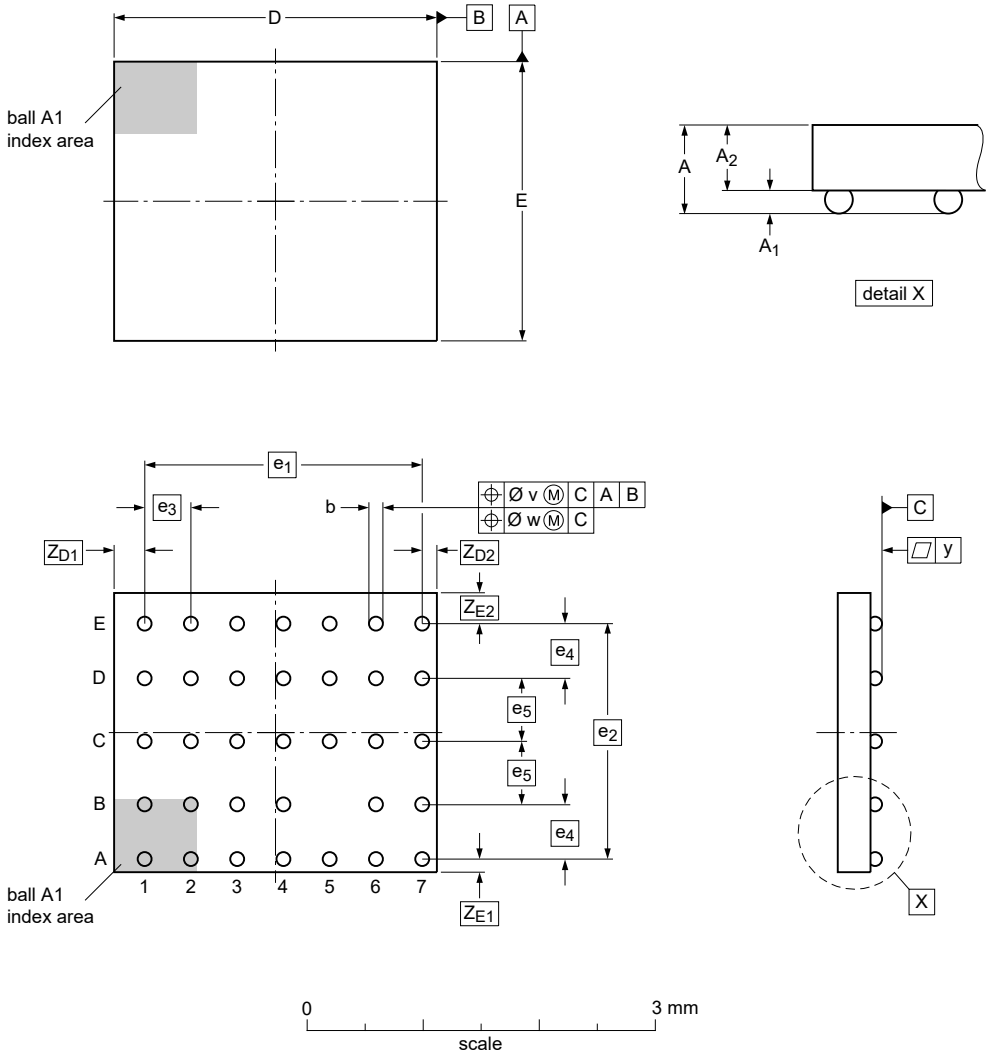
Supply	Typical value	Description
V_{PMU} $V_{DD,TX}$ V_{EXT}	470 nF	common battery voltage decoupling
$V_{DD,SYNTH}$ $V_{DD,RX}$	470 nF	common battery voltage decoupling
V_{IO}	470 nF	IO supply decoupling
V_{MEM}	470 nF	common battery voltage decoupling

13.4 PCB reliability

To ensure that board level reliability requirements are met, the application PCB must use underfill. It is the responsibility of the customer to validate board level reliability in the end application.

14 Package outline

WLCSP34: wafer level chip-scale package; 34 bumps; 2.45 x 2.87 x 0.38 mm **SOT1403-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e_1	e_2	e_3	e_4	e_5	Z_{D1}	Z_{D2}	Z_{E1}	Z_{E2}	v	w	y
	max	0.41	0.115	0.305	0.140	2.90	2.48												
mm	nom	0.38	0.100	0.280	0.125	2.87	2.45	2.4	2.034	0.40	0.47	0.547	0.315	0.155	0.127	0.29	0.15	0.05	0.02
	min	0.35	0.085	0.255	0.110	2.84	2.42												

sot1403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1403-1						~~15-10-26~~ 16-08-08

Figure 10. Package outline SOT1403-1 (WLCSP34)

Bump material is Sn + Ag 1.8 %

15 Handling information

See Ref. 1 for detailed instructions on handling, soldering and mounting WLCSP packaged devices.

16 Packaging information

Default packing for the NXH3670UK devices is tape and reel according to T1 taping orientation as depicted below.

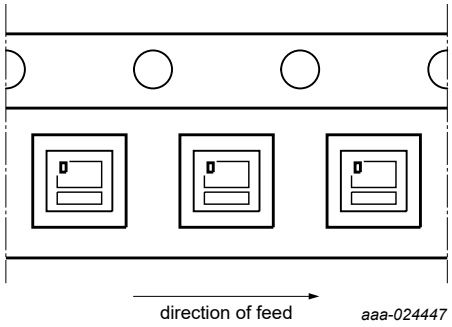


Figure 11. Tape and reel product orientation

17 Abbreviations

Table 29. Abbreviations

Abbreviation	Description
ACK	acknowledge
ADC	analog-to-digital converter
ADPCM	adaptive differential pulse code modulation
AES	Advanced Encryption Standard
APB	advanced peripheral bus
API	application program interface
ASIC	application specific integrated circuit
ASRC	asynchronous sample rate converter
BLE	bluetooth low energy
BOD	brownout detect
CDM	charged device model
CRC	cyclic redundancy check
CS	chip select
CSP	chip scale package
DAC	digital-to-analog converter
DS	data sheet
DMA	direct memory access
DSP	digital signal processor
DTU	data transfer unit
EEPROM	electrically erasable programmable read-only memory
FIFO	first-in-first-out
FPGA	field programmable gate array
GCC	GNU compiler collection
GFSK	gaussian frequency shift keying
GMSK	gaussian minimum shift keying
GPIO	general-purpose input output
HAL	hardware abstraction layer
HBM	human body model
HCI	host controller interface
HI	hearing instrument
HSI	high-speed interface
I2S	integrated interchip sound
ISR	interrupt service routine
ISV	independent software vendor

Abbreviation	Description
JTAG	joint test action group
LFSR	linear feedback shift register
LDO	low drop out regulator
LJO	low jitter oscillator
MAC	medium access controller
MIS	medium integrity check
MISO	master-in-slave-out
MOSI	master-out-slave-in
NCO	numerically controlled oscillator
NVM	non-volatile memory
OS	operating system
OSAL	operating system abstraction layer
OPT	one time programmable
PCM	pulse code modulation
PHY	physical layer (of the radio subsystem)
PMC	power management controller
PMU	power management unit
PPM	parts per million
RDM	radio daughter module
RAM	random access memory
RF	radio frequency
RSSI	received signal strength indicator
SCL	serial clock
SDK	software development kit
SPI	serial peripheral interface
SR	service request
SSO	simultaneously switching outputs
SWB	software board
SWD	serial wire debug
SWM	switch matrix
UART	universal asynchronous receiver/transmitter
UBM	underbump Mmtallization
ULPO	ultra-low power oscillator
USB	universal serial bus
WLCSP	wafer level chip scale package

18 References

[1] **AN11761 application note** — Flip-chip Rev. 3.0; 2016, NXP Semiconductors

[2] **AN11953 application note** — NXH3670UK Boot loader; 2017, NXP Semiconductors

19 Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXH3670UK v.3.1	20190725	Product data sheet	-	NXH3670UK v.3
Modifications:	Section 7.2.6 "I^2S (dataport) has been updated; 32 bit wordlength added.			
NXH3670UK v.3	20181029	Product data sheet	-	NXH3670UK v.2
Modifications:	• Section 7.2.6 "I^2S (dataport) has been updated. • Section 7.2.12 "Versatile IO switch matrix" has been updated. • Section 9.2.3 "SPI command handler" has been updated. • Section 9.2.4 "Active user mode" has been updated. • Section 13 "Application information" has been updated • Section 17 "Abbreviations" has been updated.			
NXH3670UK v.2	20180302	Product data sheet	-	NXH3670UK v.1
NXH3670UK v.1	20171127	Product data sheet	-	-

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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