TEA1999TK/2

GreenChip synchronous rectifier controller

Rev. 3 — 13 September 2018 **Product data sheet**

1 General description

The TEA1999TK is a member of a new generation of Synchronous Rectifier (SR) controller ICs for switched mode power supplies with adaptive gate drive for maximum efficiency at any load.

The TEA1999TK is a dedicated controller IC for synchronous rectification on the secondary side of flyback converters. It incorporates the sensing stage and driver stage for driving the SR MOSFET, which is rectifying the output of the secondary transformer winding.

The TEA1999TK can generate its own supply voltage for battery charging applications with low output voltage or for applications with high-side rectification.

The TEA1999TK is fabricated in a Silicon-On-Insulator (SOI) process.

2 Features and benefits

2.1 Efficiency features

- Adaptive gate drive for maximum efficiency at any load
- Typical supply current in no-load operation below 250 μA

2.2 Application features

- Operates in an output voltage range between 26 V and 0 V
- Drain sense pin capable of handling input voltages up to 120 V
- Self-supplying for operation with low output voltage
- Self-supplying for high-side rectification without the use of an auxiliary winding
- Operates with standard and logic level SR MOSFETs
- Supports USB BC, QuickCharge, and smart charging applications
- HVSON8 package

2.3 Control features

- Adaptive gate drive for fast turn-off at the end of conduction
- UnderVoltage LockOut (UVLO) with active gate pull-down
- Blanking input for low and high switching frequency
- Enable input for CCM operation and for disabling at start-up or shorted output

3 Applications

The TEA1999TK is intended for flyback power supplies. In such applications, it can drive the external synchronous rectifier MOSFET, which replaces the diode for the rectification of the voltage on the secondary winding of the transformer.

It can be used in all power supplies that require a high efficiency, like:

- Chargers
- Adapters
- Flyback power supplies with very low and/or variable output voltage

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1999TK/2	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 mm × 3 mm × 0.85 mm	SOT782-1

5 Marking

Table 2. Marking code

Type number	Marking code
TEA1999TK/2	E1999

6 Block diagram

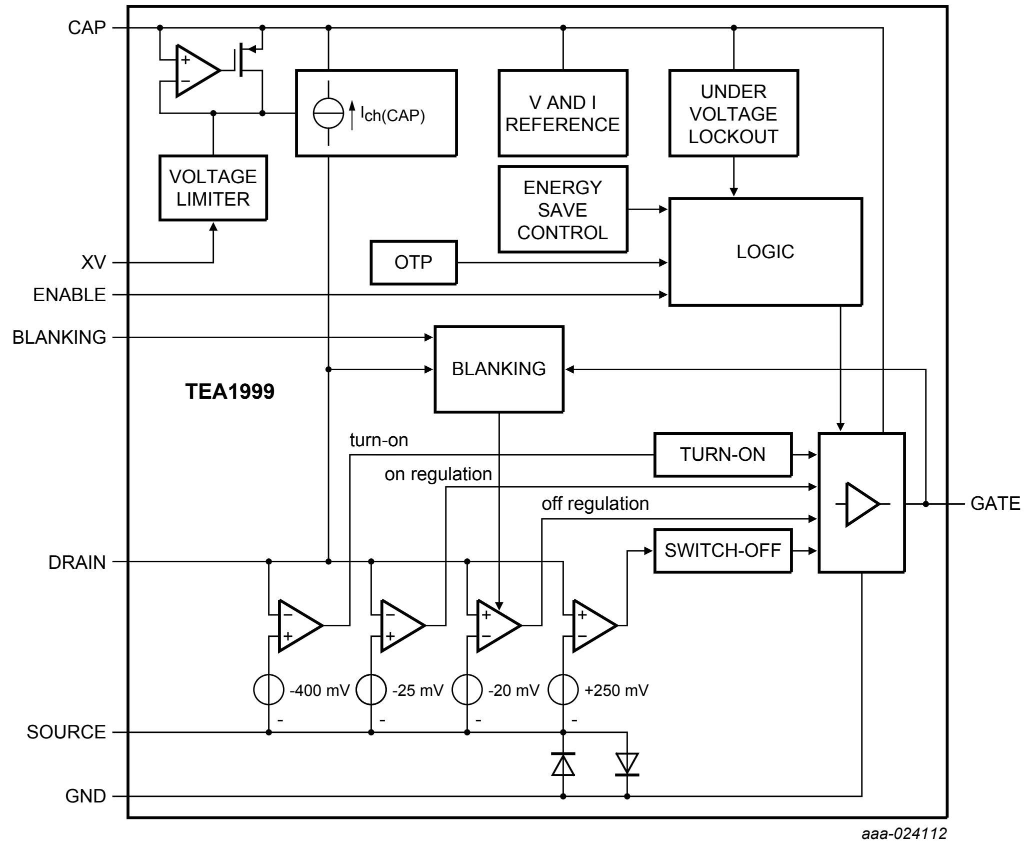


Figure 1. TEA1999TK block diagram

7 Pinning information

7.1 Pinning

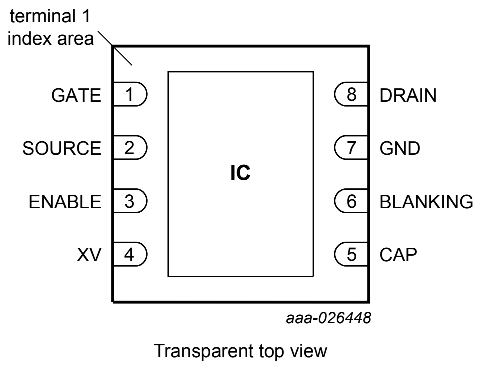


Figure 2. TEA1999TK pin configuration (SOT782-1)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GATE	1	gate driver output for SR MOSFET
SOURCE	2	source sense input of SR MOSFET
ENABLE	3	enable input for SR operation
XV	4	external supply input
CAP	5	capacitor input for internal supply voltage
BLANKING	6	blanking input for minimum active time selection
GND	7	ground
DRAIN	8	drain sense input of SR MOSFET

8 Functional description

8.1 Introduction

The TEA1999TK is a controller IC for Synchronous Rectification (SR) in flyback applications. It can drive the external synchronous rectifier MOSFET for the rectification of the voltage on the secondary winding of the transformer. Figure 3 shows a typical configuration.

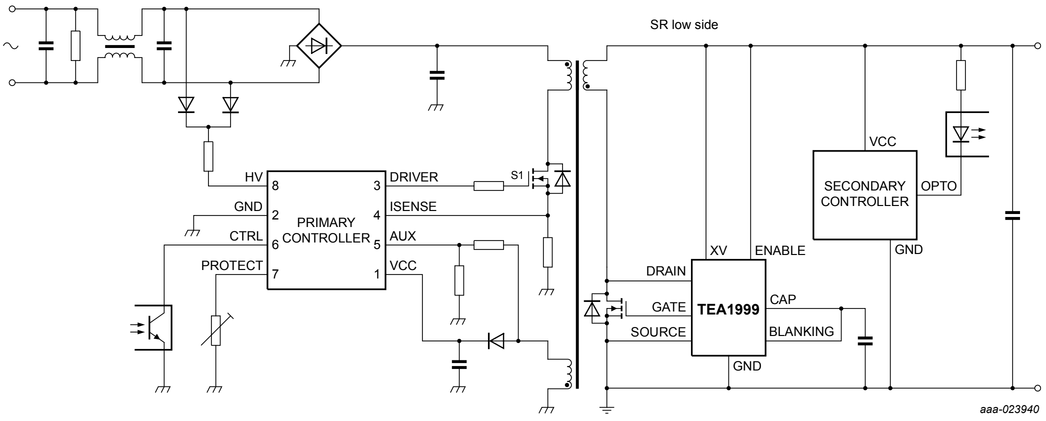


Figure 3. TEA1999TK configuration with low-side rectification

8.2 Start-up and UnderVoltage LockOut (UVLO; CAP and XV pins)

The capacitor on the CAP pin supplies the TEA1999TK. At a low CAP voltage (< 3.7 V), the capacitor is charged via the DRAIN pin with a limited start-up current of typically 15 mA. When the CAP voltage exceeds 3.7 V, the DRAIN pin or the XV pin can charge the capacitor. When the XV voltage < 4.7 V, the capacitor is charged via the DRAIN pin with a typical charge current of 125 mA. When the XV voltage ≥ 4.7 V, the capacitor is charged via the XV pin and an internal regulator. The regulator reduces the voltage difference between the XV and CAP pins to a level below 100 mV.

When the voltage on the CAP pin exceeds $V_{start(CAP)}$ (3.7 V typical), the IC leaves the UVLO state and activates the synchronous rectifier circuitry. When the voltage drops below 3.6 V (typical), the UVLO state is re-entered and the SR MOSFET gate driver output is actively kept low.

8.3 Drain sense (DRAIN pin)

The drain sense pin is an input pin capable of handling input voltages up to 120 V. At positive drain sense voltages, the gate driver is in off-mode with the gate driver pulled down (pin GATE). At negative drain sense voltages, the IC enables the Synchronous Rectification (SR) by sensing the drain source differential voltage.

8.4 Synchronous rectification (DRAIN and SOURCE pins)

The IC senses the voltage difference between the drain sense (DRAIN pin) and the source sense (SOURCE pin) connections. This drain source differential voltage of the SR MOSFET is used to drive the gate of the SR MOSFET.

When this absolute voltage difference is higher than $V_{act(drv)}$, the corresponding gate driver output turns on the external SR MOSFET. When the external SR MOSFET is switched on, the absolute voltage difference between the drain and the source sense connections drops to below $V_{act(drv)}$. The regulation phase follows the turn-on phase.

In the regulation phase, the IC regulates the difference between the drain and the source sense inputs to an absolute level of 25 mV. When the absolute difference exceeds 25 mV ($V_{reg(drv)}$), the gate driver output increases the gate voltage of the external SR MOSFET until the 25 mV level is reached. The SR MOSFET does not switch off at low current. To avoid that the device switches off because of ringing, a minimum on-time of 1.5 μs ($t_{tact(sr)(min)}$) is integrated.

When the absolute difference < 20 mV, the gate driver output decreases the gate voltage of the external SR MOSFET. The voltage waveform on the gate of the SR MOSFET follows the waveform of the current through the SR MOSFET. When the current through the SR MOSFET reaches zero, the SR MOSFET is switched off quickly.

After SR MOSFET switch-off, the drain voltage increases. When the drain voltage exceeds 250 mV, a low ohmic gate pull-down of 3 Ω keeps the gate of the SR MOSFET switched off.

8.5 Gate driver (GATE pin)

The gate driver circuit charges the gate of the external SR MOSFET during the rising part of the current. The driver circuit discharges the gate during the falling part of the current. The gate driver has a source capability of typically 0.70 A. It has a sink capability of typically 0.50 A. The source and sink capabilities allow fast turn-on and fast turn-off of the external SR MOSFET.

The maximum output voltage of the driver is limited to the voltage on the CAP pin. The maximum output voltage ranges between 4.7 V and 10 V, depending on the voltage on the CAP pin. The high output gate voltage drives all MOSFET brands to the minimum on-state resistance. In applications where the IC is supplied with 5 V, the maximum output voltage of the driver is 4.90 V, and logic level SR MOSFETs can be used.

The IC is self-supplying in applications with high-side rectification or in battery charging applications with an output voltage < 4.7 V. When the XV pin is connected to ground for driving standard SR MOSFETs, the driver is regulated to 10 V. When the XV pin is connected to the converter output for driving logic-level SR MOSFETs, the driver is regulated to the voltage on the XV pin with a minimum of 4.7 V.

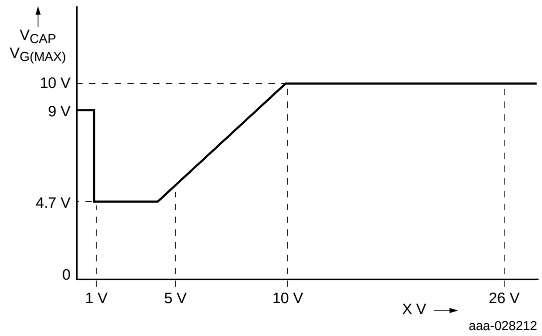


Figure 4. Maximum gate voltage ($V_{G(max)}$)

During start-up conditions ($V_{CAP} < V_{start(CAP)}$) and UVLO, the driver output voltage is actively pulled low.

When the XV voltage exceeds 10 V, the CAP voltage and $V_{G(max)}$ are limited to typically 10.7 V. The XV voltage is allowed to increase until the 26 V limit is reached.

8.6 Source sense (SOURCE pin)

The IC is equipped with an additional source sense pin (SOURCE). This pin is used for measuring the drain-to-source voltage of the external SR MOSFET. Voltage differences on PCB tracks because of parasitic inductance in combination with large dI/dt values, can cause errors. To minimize these errors, the source sense input must be connected as close as possible to the SOURCE pin of the external SR MOSFET.

8.7 Overtemperature protection (GATE pin)

Overtemperature protection is triggered when the output of the gate driver:

- Has a load that is too high
- Is short-circuited to ground
- Is short-circuited to the SOURCE pin

The OTP circuit is triggered at 165 °C. It actively pulls down the gate driver output. When the temperature has decreased to 145 °C, the circuit resumes normal operation.

8.8 Enable input (ENABLE pin)

The enable input can be used for enabling and disabling the SR driver.

Disabling the SR driver can be desired during start-up or during a short-circuit of the output.

The enable input can be used for turning off the SR in CCM operation.

If the output voltage is higher than 2 V, input connect to the XV pin enables the SR operation. Pulling the input to ground disables the driver.

An open input enables the SR operation by an internal 1 μA pull-up current.

8.9 Blanking input (BLANKING pin)

The blanking input can set the minimum active time ($t_{act(sr)(min)}$).

An open pin or a pin connected to the CAP pin can be used for a long blanking time (1.5 μs) for applications with a switching frequency of up to 150 kHz.

A pin connected to ground can be used for a short blanking time (0.8 μs) for applications with a switching frequency of up to 300 kHz.

9 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 2); positive currents flow into the chip. Voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the other ranges are not violated.

Symbol	Parameter	Conditions		Min	Max	Unit
Voltages						
V_{XV}	voltage on pin XV			−0.4	+26	V
$V_{sense(DRAIN)}$	sense voltage on pin DRAIN			−0.8	+120	V
$V_{sense(SOURCE)}$	sense voltage on pin SOURCE			−0.4	+0.4	V
V_{ENABLE}	voltage on pin ENABLE			−0.4	+26	V
$V_{BLANKING}$	voltage on pin BLANKING			−0.4	V_{CAP}	V
General						
P_{tot}	total power dissipation	T_{amb} = 90 °C		-	1	W
T_{stg}	storage temperature			−55	+150	°C
T_j	junction temperature			−40	+150	°C
ElectroStatic Discharge (ESD)						
V_{ESD}	electrostatic discharge voltage	class 2				
		human body model	[1]	-	2000	V
		charged device model		-	500	V
		machine model	[2]	-	200	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
[2] Equivalent to discharging a 200 pF capacitor through a 10 Ω series resistor and a 0.75 μH inductor.

10 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{XV}	voltage on pin XV		0	-	21	V
V_{DRAIN}	voltage on pin DRAIN	peak voltage in switching application	8	-	120	V

11 Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC test board	57	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	JEDEC test board	48	K/W

12 Characteristics

Table 7. Characteristics

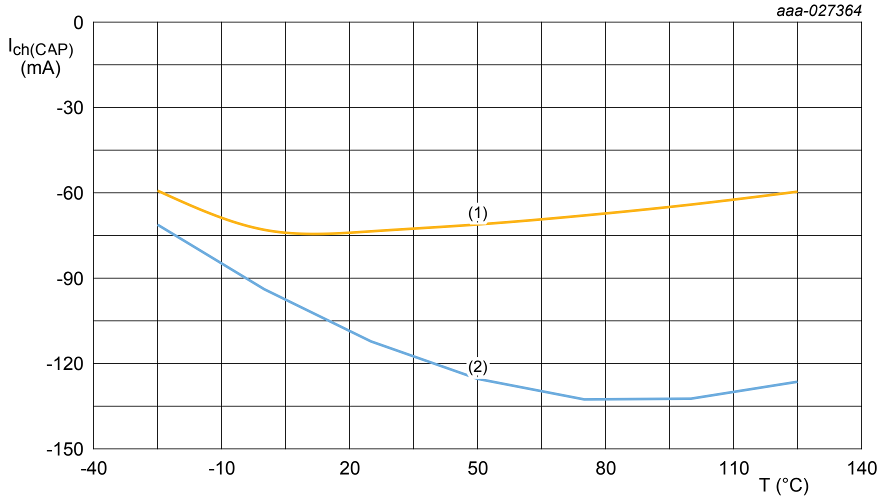
−25 °C < T_j < +125 °C; V_{xv} = 5 V; ENABLE connected to XV; BLANKING connected to CAP; C_{CAP} = 1 μF; C_{GATE} = 10 nF (capacitor between the GATE and the GND pins); all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage management (XV and CAP pins)						
$V_{start(CAP)}$	start voltage on pin CAP	V_{XV} = 0 V	3.5	3.7	3.9	V
$V_{stop(CAP)}$	stop voltage on pin CAP	V_{XV} = 0 V	3.4	3.6	3.8	V
$I_{start(CAP)}$	start current on pin CAP	V_{XV} = 5 V; V_{CAP} = 0 V; V_{DRAIN} = 12 V	−24	−15	−8	mA
$I_{ch(CAP)}$	charge current on pin CAP	power save operation				
		V_{XV} = 0 V; V_{CAP} = 8 V; V_{DRAIN} = 12 V; T_j = 25 °C	−120	−80	−50	mA
		V_{XV} = 2 V; V_{CAP} = 4 V; V_{DRAIN} = 12 V; T_j = 25 °C	−160	−110	−50	mA
$V_{I(CAP)}$	input voltage on pin CAP	V_{XV} = 0 V; V_{DRAIN} = 15 V	9.0	9.4	9.8	V
		V_{XV} = 2 V; V_{DRAIN} = 12 V	4.5	4.6	4.8	V
		V_{XV} = 5 V	4.8	4.9	5.0	V
		V_{XV} = 10 V	9.8	9.9	10.0	V
		V_{XV} = 26 V	10.3	10.7	11.1	V
$I_{I(XV)}$	input current on pin XV	power save operation; V_{DRAIN} = 5.5 V; T_j = 25 °C	200	240	280	μA
		normal operation; without gate charge; V_{DRAIN} step from 5.5 V to −250 mV; T_j = 25 °C	1.0	1.2	1.4	mA
$t_{act(pwrsave)}$	power-save activation time		70	100	130	μs
Synchronous rectification sense input (DRAIN and SOURCE pins)						
$V_{act(drv)}$	driver activation voltage	V_{SOURCE} = 0 V; T_j = 25 °C	−510	−470	−430	mV
$V_{reg(drv)}$	driver regulation voltage	V_{SOURCE} = 0 V; T_j = 25 °C	−30	−25	−20	mV
V_{swoff}	switch-off voltage	V_{SOURCE} = 0 V	180	250	320	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(act)(drv)}$	driver activation delay time	V_{SOURCE} = 0 V; normal operation; time for step-on V_{DRAIN} (2 V to −0.5 V) to rising of V_G at 10 % of end value	-	40	-	ns
$t_{d(deact)(drv)}$	driver deactivation delay time	V_{SOURCE} = 0 V; normal operation; time for step-on V_{DRAIN} (−50 mV to 2 V) to falling of V_G at 90 % of begin value	-	40	-	ns
$t_{act(sr)(min)}$	minimum synchronous rectification active time	V_{SOURCE} = 0 V; normal operation; time for step-on V_{DRAIN} (−700 mV to +100 mV) to falling of V_G at 90 % of begin value; without gate charge	1.1	1.4	1.8	μs
		V_{SOURCE} = 0 V; normal operation; time for step-on V_{DRAIN} (−700 mV to +100 mV) to falling of V_G at 90 % of begin value; without gate charge; $V_{BLANKING}$ = 0 V	0.5	0.7	0.9	μs
Gate driver (GATE pin)						
I_{source}	source current	peak.current; V_{XV} = 5 V; V_{ds} = −0.5 V; V_G = 0 V	-	-0.70	-	A
I_{sink}	sink current	regulation current; V_{XV} = 5 V; V_{ds} = 0 V; V_G = 3 V	-	100	-	mA
		peak current; V_{XV} = 5 V; V_{ds} = 0.5 V; V_G = 4 V	-	0.50	-	A
$R_{pd(G)}$	gate pull-down resistance	V_{DRAIN} = 0.5 V; I_G = 100 mA; V_{XV} = 5 V; T_j = 25 °C	2.6	3.2	4.0	Ω
$V_{G(max)}$	maximum gate voltage	V_{XV} = 0 V	9.0	9.4	9.8	V
		V_{XV} = 2 V	4.45	4.60	4.75	V
		V_{XV} = 5 V	4.8	4.9	5.0	V
		V_{XV} = 10 V	9.8	9.9	10.0	V
		V_{XV} = 26 V	10.3	10.7	11.1	V
Enable function (ENABLE pin)						
$V_{th(en)}$	enable threshold voltage		1.1	1.6	2.0	V
$V_{th(dis)}$	disable threshold voltage		1.0	1.5	1.9	V
$t_{d(en)}$	enable delay time	turn-on delay	-	85	-	ns
$t_{d(dis)}$	disable delay time	turn-off delay	-	100	-	ns
Temperature protection						
$T_{otp(act)}$	activation overtemperature protection temperature		155	165	175	°C
$T_{otp(hys)}$	overtemperature protection trip hysteresis		-	20	-	°C

12.1 Temperature curves

12.1.1 Charge current (CAP pin)

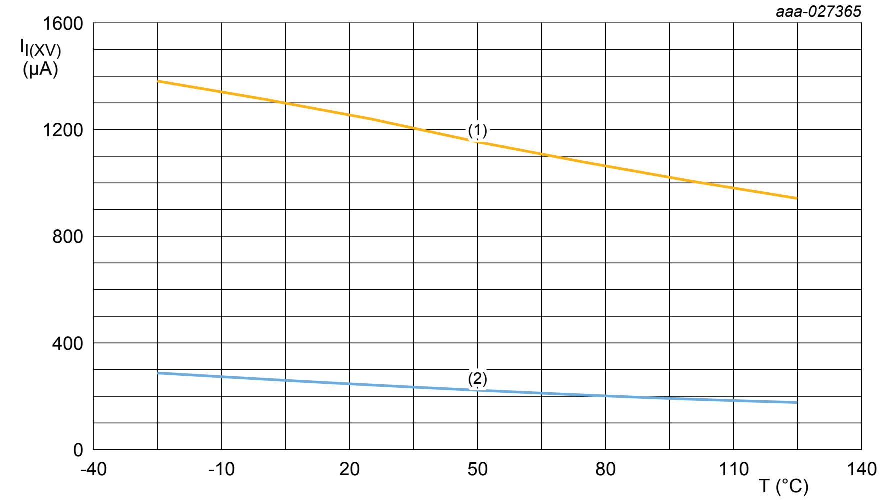


(1) $I_{ch(CAP)}$ at V_{CAP} = 8 V; V_{XV} = 0 V

(2) $I_{ch(CAP)}$ at V_{CAP} = 4 V; V_{XV} = 2 V

Figure 5. $I_{ch(CAP)}$ as a function of temperature

12.1.2 Operating current (XV pin)



(1) $I_{I(XV)}$ - normal operation

(2) $I_{I(XV)}$ - power save operation

Figure 6. $I_{I(XV)}$ as a function of temperature

12.1.3 Driver regulation voltage

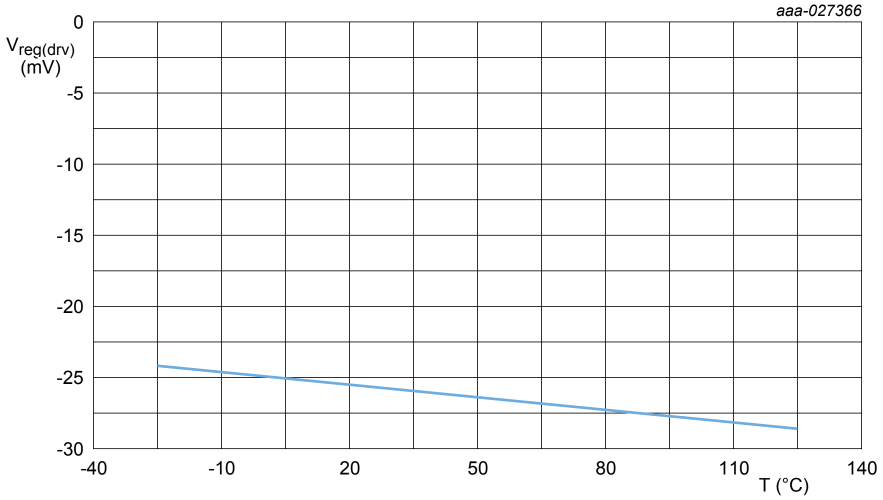


Figure 7. $V_{reg(drv)}$ as a function of temperature

12.1.4 Gate pull-down resistance

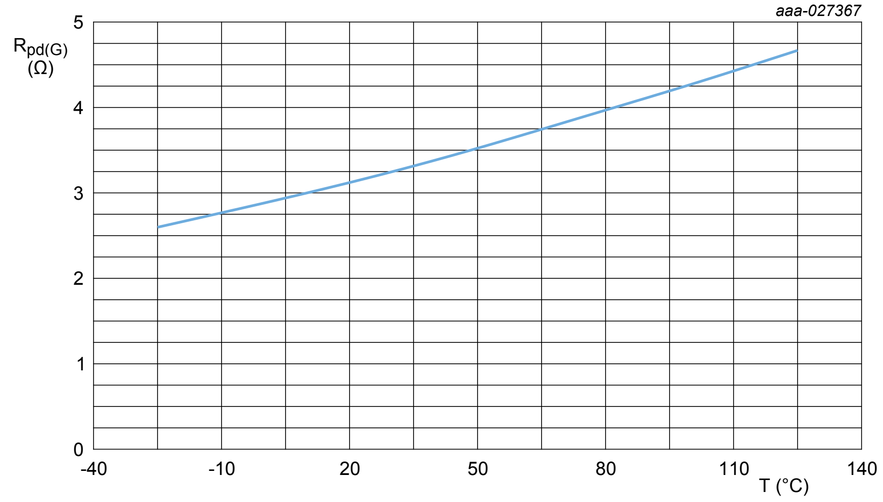


Figure 8. $R_{pd(G)}$ as a function of temperature

12.1.5 Switch-off voltage

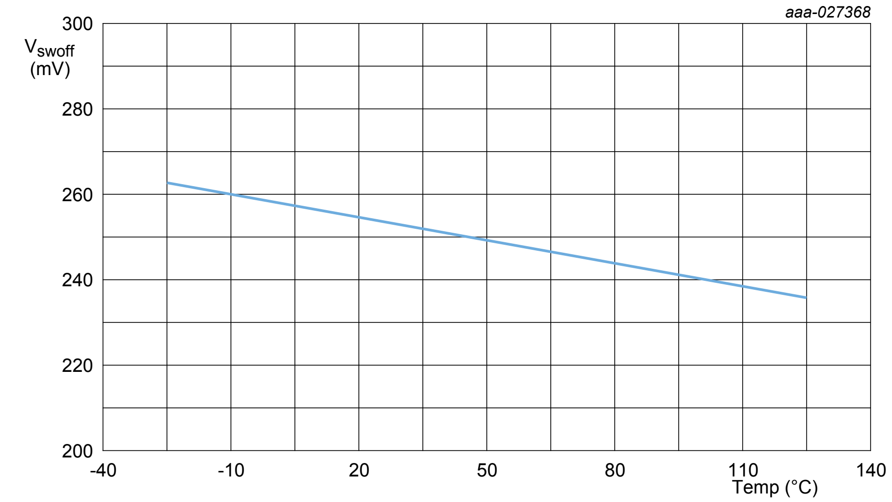
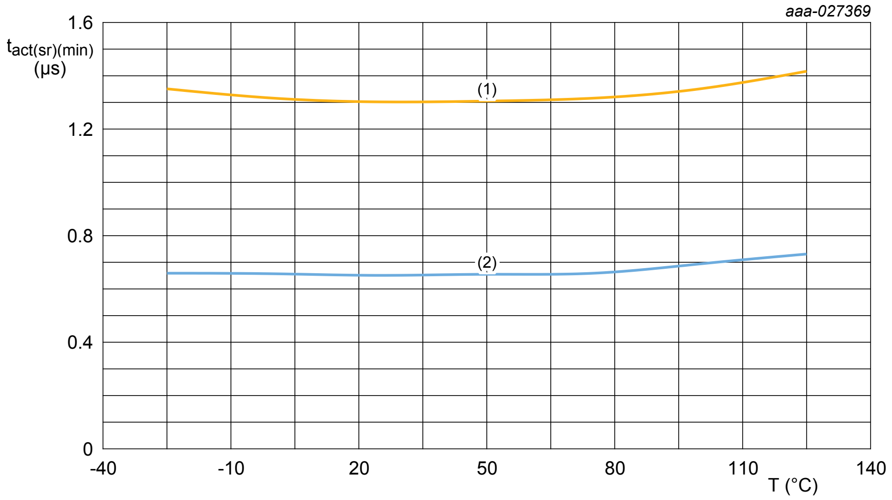


Figure 9. V_{swoff} as a function of temperature

12.1.6 Minimum synchronous rectification active time



(1) Blanking connected to CAP

(2) $V_{blanking}$ = 0 V

Figure 10. $t_{act(sr)(min)}$ as a function of temperature

13 Application information

A flyback switched mode power supply with the TEA1999TK consists of a primary side controller with a primary switch, a transformer, and an output stage. To obtain low conduction loss rectification, an SR MOSFET is used in the output stage. The SR MOSFET can be placed low-side (see Figure 3) or can be placed high-side (see Figure 11). In the high-side application, the TEA1999TK is self-supplying. The capacitor on the CAP pin supplies the TEA1999TK. When the drain voltage is positive, it is charged via the DRAIN pin.

The gate drive voltage for the synchronous rectifier switch is derived from the voltage difference between the corresponding drain sense and source sense pins.

Special attention must be paid to the connection of the drain sense and source sense pins. The voltages measured on these pins are used for the gate drive voltage. Wrong measurement results in a less efficient gate drive because a gate voltage that is either too low or too high. The connections to these pins must not interfere with the power wiring.

The power wiring conducts currents with high dI/dt values. It can easily cause measurement errors resulting from induced voltages due to parasitic inductances. The separate source sense pins make it possible to sense the source voltage of the external MOSFETs directly, without having to use the current carrying power ground tracks.

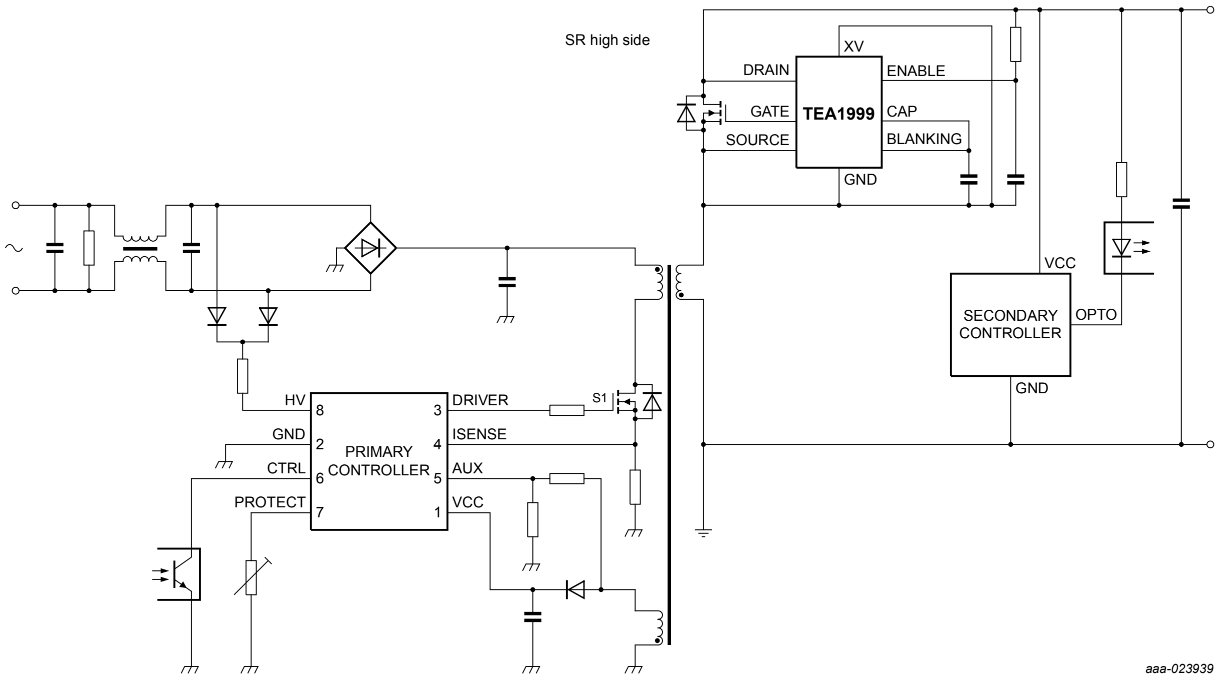


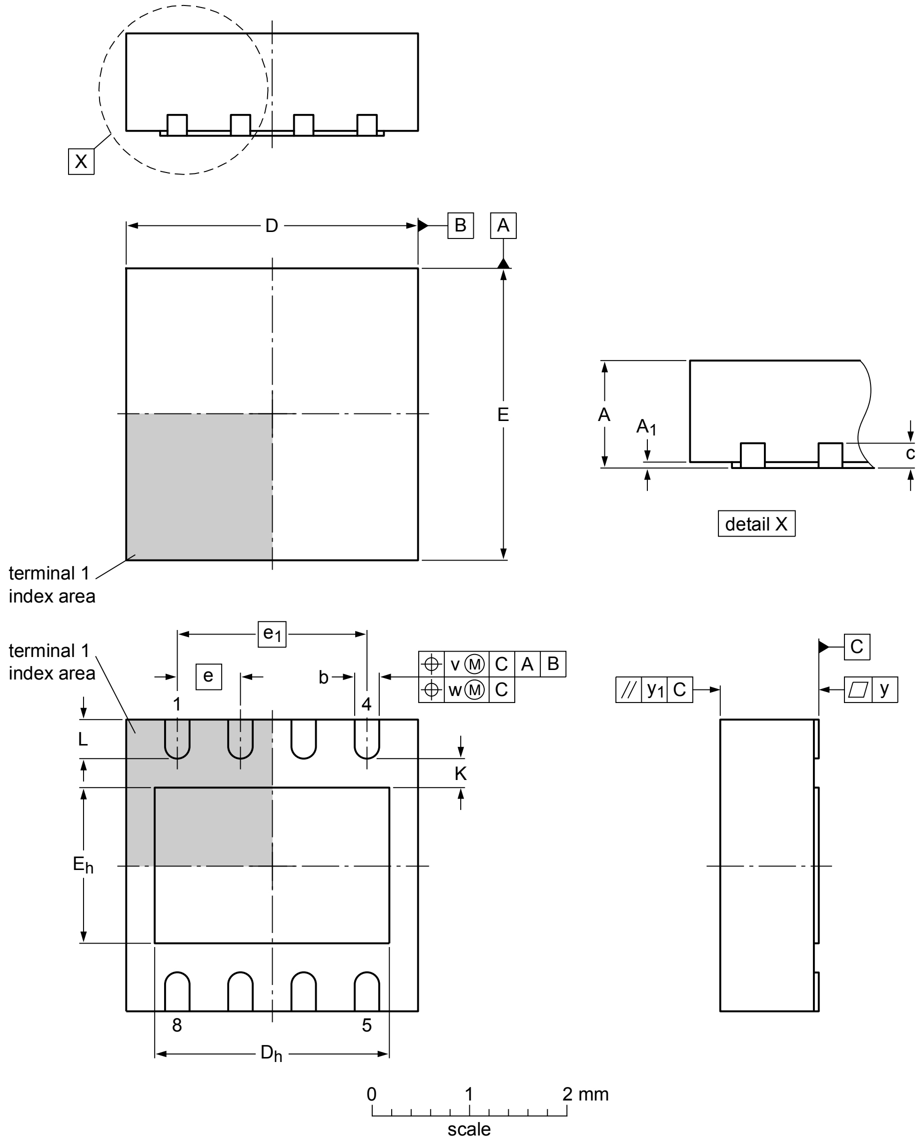
Figure 11. TEA1999TK configuration with high-side rectification

Some important guidelines for a good layout:

- Keep the trace from the DRAIN pin to the MOSFET drain as short as possible.
- Keep the trace from the SOURCE pin to the MOSFET source as short as possible.
- Keep the area of the loop from the DRAIN pin to the MOSFET drain, to the MOSFET source, and to the SOURCE pin as small as possible. Make sure that the overlap of this loop over the power drain track or the power source track is as small as possible.
- Keep the track from the GATE pin to the gate of the MOSFET as short as possible.
- Use separate clean tracks for the XV and GND pins. If possible, use a small ground plane underneath the IC, which improves the heat dispersion.

14 Package outline

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm **SOT782-1**



Dimensions

Unit(1)		A	A_1	b	c	D	D_h	E	E_h	e	e_1	K	L	v	w	y	y_1
	max	1.00	0.05	0.35		3.10	2.45	3.10	1.65			0.35	0.45				
mm	nom	0.85	0.03	0.30	0.2	3.00	2.40	3.00	1.60	0.65	1.95	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.25		2.90	2.35	2.90	1.55			0.25	0.35				

Note
1. Plastic or metal protrusions of 0.075 maximum per side are not included.

sot782-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT782-1	- - -	MO-229	- - -			~~09-08-25~~ 09-08-28

Figure 12. Package outline SOT782-1 (HVSON8)

15 Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1999TK v.3	20180913	Product data sheet	-	TEA1999TK v.2
Modifications:	• Text and graphics have been updated throughout this document.			
TEA1999TK v.2	20171103	Product data sheet	-	TEA1999TK v.1
TEA1999TK v.1	201710818	Product data sheet	-	-

16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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