

# TFA9888

## 9.7 V stereo boosted audio system with adaptive sound maximizer and speaker protection

Rev. 2 — 14 July 2017

Product short data sheet

### 1. General description

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The TFA9888 is a high-efficiency stereo class-D audio amplifier featuring an adaptive sound maximizer and speaker protection (implemented via a speaker-boost and protection algorithm). It can deliver 4.8 W peak output power per channel into an 8  $\Omega$  speaker at a supply voltage of 3.6 V. The internal adaptive DC-to-DC converter raises the supply voltage to 9.7 V, providing ample headroom for major improvements in sound quality.

A safe working environment is provided for the speaker under all operating conditions. The TFA9888 maximizes acoustic output while ensuring diaphragm displacement and voice coil temperature do not exceed their rated limits. This function is based on a speaker box model that operates in all loudspeaker environments (e.g. free air, closed box or vented box). Furthermore, advanced signal processing ensures that the quality of the audio signal is never degraded by unwanted clipping or distortion in the amplifier or speaker. The speaker-boost and protection algorithm uses feedback to calculate both the temperature and the excursion, allowing the TFA9888 to adapt to changes in the acoustic environment.

The device allows a single speaker to support both the handset call and hands-free call use-cases. This feature reduces the number of amplifiers needed in an application without the need for additional external components.

Smart Receiver stereo playback is supported with a hands-free speaker and an earpiece speaker (32  $\Omega$ ) connected to the two channels of the TFA9888. The speaker-boost and protection algorithm allows the TFA9888 to deliver about 1.2 W at the earpiece speaker, making it possible to generate a loud stereo impression using normal mobile phone acoustics.

The TFA9888 is available in a 99-bump WLCSP (Wafer Level Chip-Size Package) with a 400  $\mu\text{m}$  pitch.

### 2. Features and benefits

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- Sophisticated speaker-boost and protection algorithm that maximizes speaker performance while protecting the speaker:
  - ◆ Fully embedded software, no additional license fee or porting required
  - ◆ Total integrated solution that includes Digital Signal Processor (DSP), stereo amplifiers, DC-to-DC converter sensing and more
- Adaptive excursion control - guarantees that the speaker membrane excursion never exceeds its rated limit



**9.7 V stereo boosted audio system with adaptive sound maximizer and speaker protection**

- Real-time temperature protection - direct measurement ensures that voice coil temperature never exceeds its rated limit
- Environmentally aware - automatically adapts speaker parameters to acoustic and thermal changes including compensation for speaker-box leakage
- Support for handset call and hands-free call use cases using the same speaker:
  - ◆ Handset use case,  $V_{n(o)} = 11 \mu\text{V}$  (typical), PSRR = 110 dB (typical),  $P_O = 300 \text{ mW}$  (THD = 1%,  $R_L = 8 \Omega$ ),  $P_O = 120 \text{ mW}$  (THD = 1%,  $R_L = 32 \Omega$ )
  - ◆ Hands-free use case,  $V_{n(o)} = 45 \mu\text{V}$  (typical), PSRR = 80 dB (typical),  $P_O = 2 \times 2.4 \text{ W}$  (THD = 1%,  $R_L = 2 \times 8 \Omega$ )
- Smart Receiver stereo support using the main and earpiece speakers in hands-free use case for stereo playback,  $P_O = 4.1 \text{ W}$  (THD = 1%,  $R_L = 8 \Omega$ , no signal on receiver speaker) and  $P_O = 1.2 \text{ W}$  (THD = 1%,  $R_L = 32 \Omega$ , no signal on main speaker)
- Clip avoidance - DSP algorithm prevents clipping even with sagging supply voltage
- Bandwidth extension option to increase low frequency response
- Compatible with standard Acoustic Echo Cancellers (AECs)
- Adaptive DC-to-DC converter increases the supply voltage smoothly when necessary, preventing large battery supply spikes and limiting quiescent power consumption
- High efficiency and low power dissipation
- Wide supply voltage range (fully operational from 2.7 V to 5.5 V)
- I<sup>2</sup>C-bus control interface (400 kHz)
- Dedicated speech mode with speech activity detector
- Speaker current and voltage monitoring (via the I<sup>2</sup>S-bus) for Acoustic Echo Cancellation (AEC) at the host
- 48 kHz sample frequency supported
- Configurable TDM/I<sup>2</sup>S input interface supporting up to 16 slots
- Bi-directional TDM/I<sup>2</sup>S interface supported (full duplex)
- PDM input interface supporting:
  - ◆ Stereo audio input or
  - ◆ Two digital microphones
- Sidetone mixing supported
- External haptic driver supported via the TFA9881
- Interrupt control via a dedicated interrupt pin
- Four GPIOs
- Volume control
- Low RF susceptibility
- Input clock jitter insensitive interface (jitter caused by thermal noise)
- Thermal foldback and overtemperature protection
- 15 kV system-level ESD protection without external components
- 'Pop and click noise' free at all transitions between use cases

### 3. Applications

- Mobile phones
- Tablets
- Portable Navigation Devices (PND)
- Notebooks/Netbooks

9.7 V stereo boosted audio system with adaptive sound maximizer and speaker protection

- MP3 players and portable media players
- Small audio systems

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>BAT</sub>	battery supply voltage	on pin V <sub>BAT1</sub> /V <sub>BAT2</sub>	2.7	-	5.5	V
V <sub>DDD</sub>	digital supply voltage	on pin V <sub>DDD</sub>	1.65	1.8	1.95	V
V <sub>DD(IO)</sub>	input/output supply voltage	on pin V <sub>DD(IO)</sub>	1.65	1.8	1.95	V
I <sub>BAT</sub>	battery supply current	on pin V <sub>BAT1</sub> /V <sub>BAT2</sub> and in DC-to-DC converter coil; hands-free or multimedia playback use case; DPSAL = DPSAR = 0; silence	-	8	-	mA
		on pin V <sub>BAT1</sub> /V <sub>BAT2</sub> and in DC-to-DC converter coil; handset call use case; DPSAL = DPSAR = 0; silence;	-	6	-	mA
		Power-down state	-	1	-	μA
I <sub>DDD</sub>	digital supply current	on pin V <sub>DDD</sub> ; hands-free or multimedia playback use case; silence	-	47	-	mA
		on pin V <sub>DDD</sub> ; handset call use case; SSPDME = CSRIGHTE = CSLEFTTE = VSRIGHTE = VSLEFTTE = SSRIGHTE = 0	-	6	-	mA
		on pin V <sub>DDD</sub> ; Power-down state; BCK = FS = DIO1 = DIO2 = GAINIO = 0 V; MANAOOSC = 1;	-	30	-	μA
P <sub>o(RMS)</sub>	RMS output power	THD+N = 1 %; stereo application (2 x R <sub>L</sub> = 8 Ω); hands-free call or multimedia playback use case; V <sub>BST</sub> = 9.2 V				
		one output channel active	-	3.5	-	W
		two output channels active	-	2 × 2.4	-	W
		THD+N = 1 %; Smart Receiver application; hands-free call or multimedia playback use case; V <sub>BST</sub> = 9.7 V				
		main speaker; R <sub>L</sub> = 8 Ω; L <sub>L</sub> = 44 μH, no signal on receiver speaker	-	4.1	-	W
		receiver speaker; R <sub>L</sub> = 32 Ω; L <sub>L</sub> = 160 μH, no signal on main speaker	-	1.2	-	W

## 5. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
TFA9888UK	WLCSP99	wafer level chip-scale package; 99 bumps; 4.37 × 3.82 × 0.5 mm	SOT1447-1

6. Block diagram

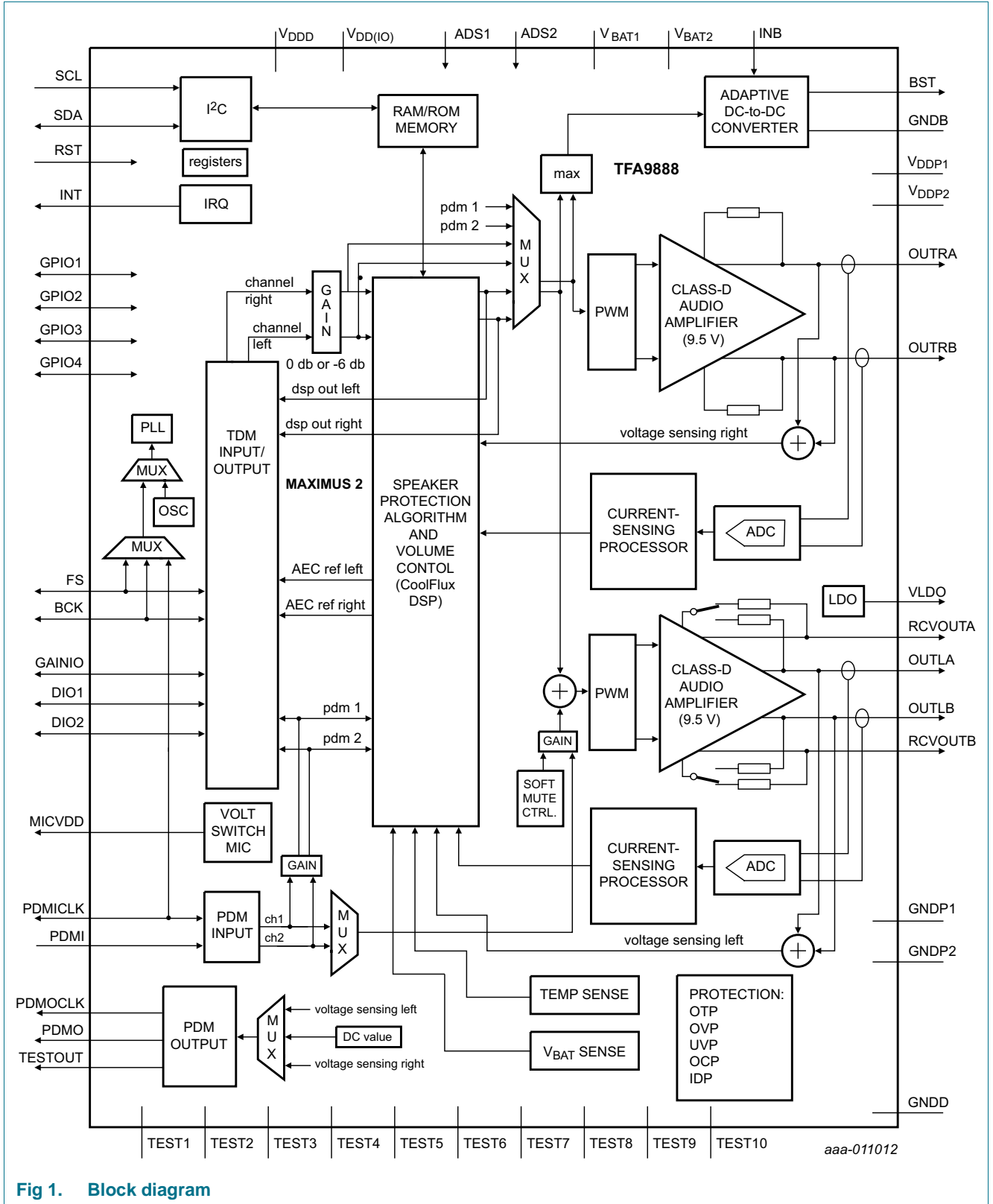
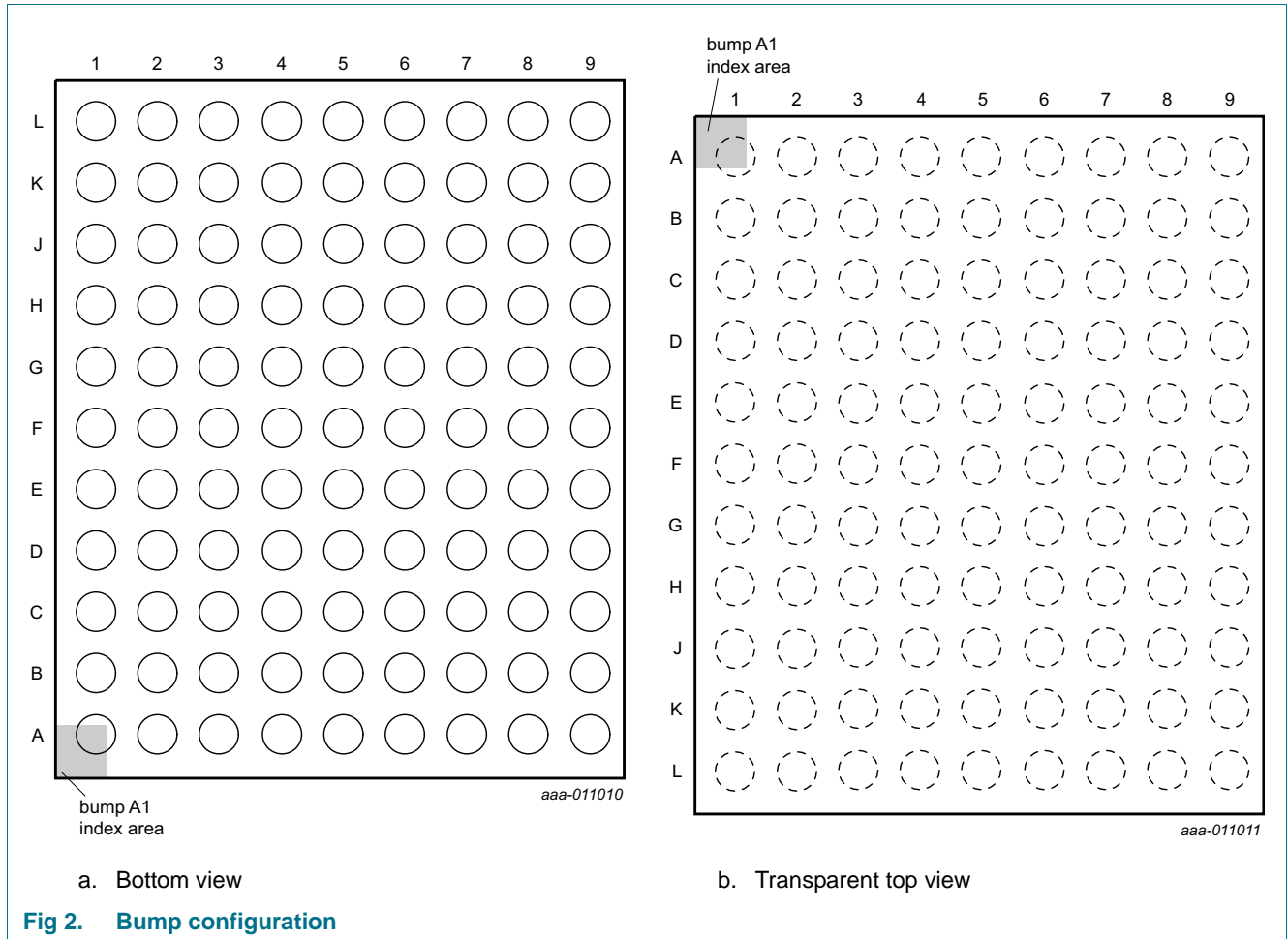


Fig 1. Block diagram

## 7. Pinning information

### 7.1 Pinning



	1	2	3	4	5	6	7	8	9
A	SCL	V <sub>DD(IO)</sub>	V <sub>DDD</sub>	GNDD	V <sub>BAT1</sub>	GNDD	GNDP1	OUTLA	V <sub>DDP1</sub>
B	SDA	V <sub>DD(IO)</sub>	V <sub>DDD</sub>	GNDD	GNDD	GNDD	GNDP1	RCVOUTA	V <sub>DDP1</sub>
C	FS	GPIO1	ADS1	ADS2	TEST5	GNDD	GNDP1	OUTLB	V <sub>DDP1</sub>
D	BCK	GPIO2	INT	RST	TEST1	GNDD	GNDP1	RCVOUTB	V <sub>DDP1</sub>
E	DIO1	GPIO3	GNDD	GNDD	TEST7	GNDD	GNDP1	VLDO	V <sub>DDP1</sub>
F	DIO2	GPIO4	GNDD	GNDD	TEST4	GNDD	GNDB	INB	BST
G	GAINIO	PDMI	GNDD	TEST8	TEST3	GNDD	GNDB	INB	BST
H	PDMICKL	GNDD	MICVDD	TEST9	TEST2	GNDD	GNDB	INB	BST
J	GNDD	PDMO	MICVDD	TEST10	GNDD	GNDD	GNDP2	OUTRB	V <sub>DDP2</sub>
K	PDMOCLK	V <sub>DD(IO)</sub>	V <sub>DDD</sub>	GNDD	TEST6	GNDD	GNDP2	GNDP2	V <sub>DDP2</sub>
L	TESTOUT	V <sub>DD(IO)</sub>	V <sub>DDD</sub>	GNDD	V <sub>BAT2</sub>	GNDD	GNDP2	OUTRA	V <sub>DDP2</sub>

aaa-011009

Transparent top view

**Fig 3. Bump mapping**

## 8. Functional description

The TFA9888 is a highly efficient stereo Bridge Tied Load (BTL) class-D audio amplifier with a sophisticated speaker-boost and protection algorithm. [Figure 1](#) is a block diagram of the TFA9888.

It contains a TDM/I<sup>2</sup>S input/output interface for communicating with the audio host. The TDM/I<sup>2</sup>S data pins (DIO1, DIO2 and GAINIO) can be configured as inputs or outputs. It is possible to configure the interface in full duplex mode with one data pin. Some TDM slots can be configured as data inputs and others as TDM data outputs per TDM frame sync. The maximum number of slots is 16 and the minimum number is 2 (like I<sup>2</sup>S). The interface is therefore compliant with all I<sup>2</sup>S interface configurations and supports a wide range of TDM interface configurations.

A PDM input stream can be applied to the TFA9888 (via pin PDMI). This audio interface can be used for connecting digital microphones or connected to the audio host.

A speaker-boost and protection algorithm, running on a CoolFlux Digital Signal Processor (DSP) core, maximizes the acoustical output of the speaker while limiting membrane excursion and voice coil temperature to a safe level. The mechanical protection implemented guarantees that speaker membrane excursion never exceeds its rated limit, to an accuracy of 10 %. Thermal protection guarantees that the voice coil temperature never exceeds its rated limit, to an accuracy of ±10 °C. Furthermore, advanced signal processing ensures the audio quality is always acceptable.

The speaker-boost and protection algorithm implements an adaptive loudspeaker model that is used to predict the extent of membrane excursion. The model is continuously updated to ensure that the protection scheme remains effective even when speaker parameter values change or the acoustic enclosure is modified.

9.7 V stereo boosted audio system with adaptive sound maximizer and speaker protection

Output sound pressure levels (SPLs) are boosted within given mechanical, thermal and quality limits. An optional bandwidth extension mode extends the low frequency response up to a predefined limit before maximizing the output level. This mode is suitable for listening to high quality music in quiet environments.

The frequency response of the TFA9888 can be modified via  $2 \times 10$  fully programmable cascaded second-order biquad filters. The first two biquads in each channel are processed with 48-bit double precision; biquads 3 to 10 are processed with 24-bit single precision.

The speaker-boost and protection algorithm can also be used for Smart receiver stereo. Stereo imaging can be achieved with this option by using a hands-free speaker in combination with an earpiece speaker (receiver speaker).

The left channel class-D audio amplifier can be configured for hands-free and handset call use cases. The maximum output power, the gain, and the noise levels are lower in handset call use case than in hands-free call use case. The receiver outputs can be connected to the earpiece for a handset call or to the hands-free outputs, so only one speaker is needed for both use cases. Power supply rejection is increased via an internal LDO used to supply the receiver amplifier.

The gain is automatically reduced to limit battery current when the battery voltage is low. The output volume can be controlled by the speaker-boost and protection algorithm or by the host application (external). In the latter case, the boost features of the speaker-boost and protection algorithm must be disabled to avoid neutralizing external volume control.

The speaker-boost and protection algorithm output is converted into two pulse width modulated (PWM) signals that are then injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

The speaker must be calibrated to prevent speaker impedance spread influencing the speaker temperature calculation/measurement. Failure to calibrate the speaker correctly can result in low volumes or damage to the speaker. Speaker binding and/or calibration is generally performed once during the phone manufacturing process.

## 9. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>BAT</sub>	battery supply voltage	on pin V <sub>BAT1</sub> /V <sub>BAT2</sub>	-0.3	+6	V
V <sub>BST</sub>	voltage on pin BST		-0.3	+12	V
V <sub>DDP</sub>	power supply voltage	on pin V <sub>DDP1</sub> /V <sub>DDP2</sub>	-0.3	+12	V
V <sub>DDD</sub>	digital supply voltage	on pin V <sub>DDD</sub>	-0.3	+1.95	V
V <sub>DD(IO)</sub>	input/output supply voltage	on pin V <sub>DD(IO)</sub>	-0.3	+1.95	V
T <sub>j</sub>	junction temperature		-	+150	°C
T <sub>stg</sub>	storage temperature		-55	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+85	°C
V <sub>ESD</sub>	electrostatic discharge voltage	according to Human Body Model (HBM)	-2	+2	kV
		according to Charge Device Model (CDM)	-500	+500	V

## 10. Thermal characteristics

**Table 4. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	4-layer application board	38	-	K/W



11. Package outline

WLCSP99: wafer level chip-scale package; 99 bumps; 4.37 x 3.82 x 0.5 mm

SOT1447-1

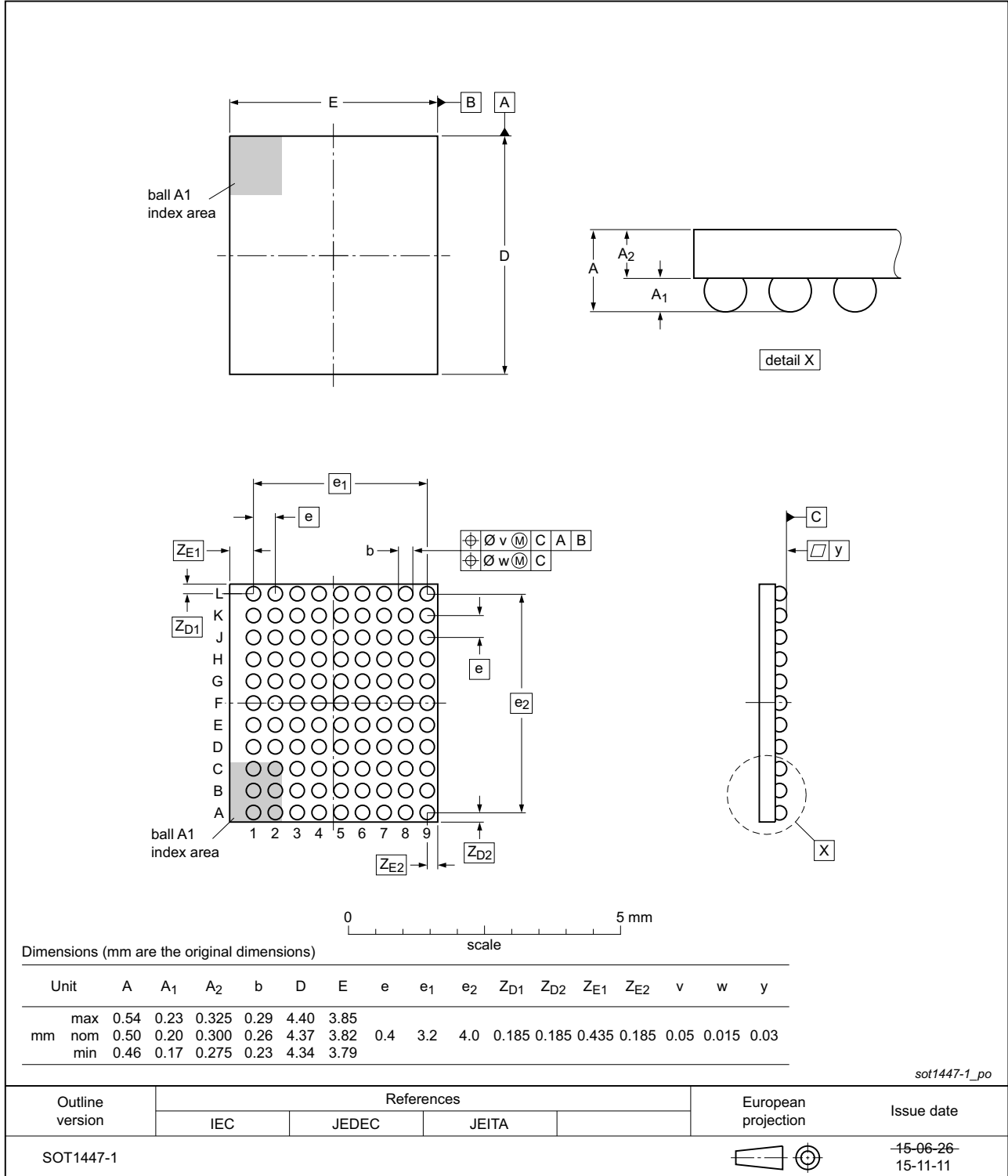


Fig 4. Package outline TFA9888 (WLCSP99)

## 12. Soldering of WLCSP packages

### 12.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note AN10439 “Wafer Level Chip Scale Package” and in application note AN10365 “Surface mount reflow soldering description”.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

### 12.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

### 12.3 Reflow soldering

Key characteristics in reflow soldering are:

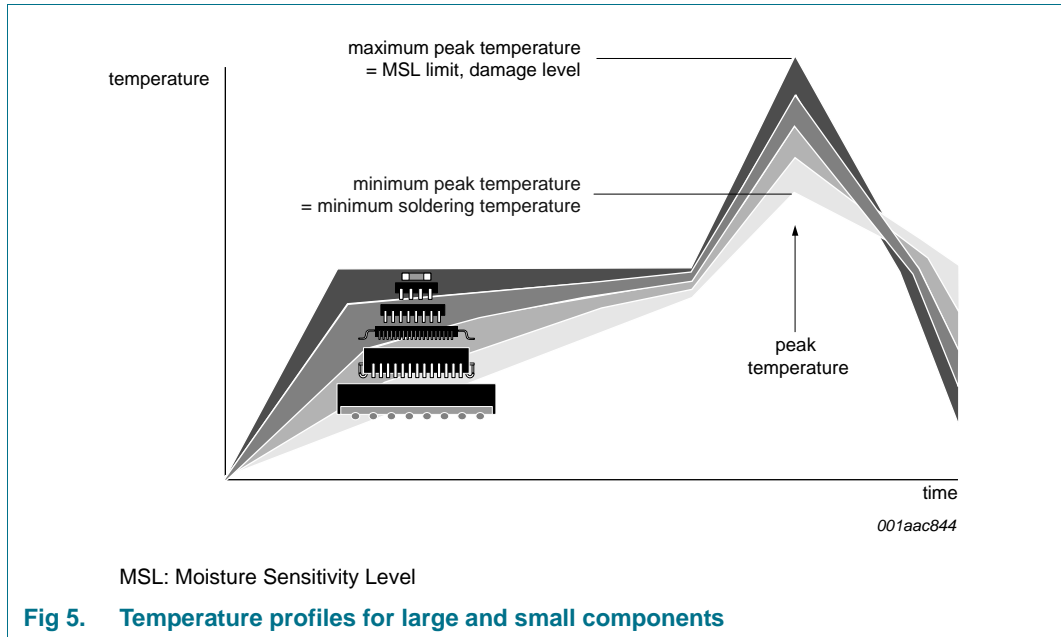
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 5](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 5](#).

**Table 5. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 5](#).



For further information on temperature profiles, refer to application note AN10365 “Surface mount reflow soldering description”.

**12.3.1 Stand off**

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

**12.3.2 Quality of solder joint**

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

**12.3.3 Rework**

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note AN10365 "Surface mount reflow soldering description".

#### 12.3.4 Cleaning

Cleaning can be done after reflow soldering.

## 13. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9888_SDS v.2	20170714	Product short data sheet	-	TFA9888_SDS v.1
Modifications	• <a href="#">Table 1 “Quick reference data”</a> : I <sub>DD</sub> value changed			
TFA9888_SDS v.1	20160229	Product short data sheet	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

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For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 16. Contents

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<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Applications</b> .....	<b>2</b>
<b>4</b>	<b>Quick reference data</b> .....	<b>3</b>
<b>5</b>	<b>Ordering information</b> .....	<b>3</b>
<b>6</b>	<b>Block diagram</b> .....	<b>4</b>
<b>7</b>	<b>Pinning information</b> .....	<b>5</b>
7.1	Pinning .....	5
<b>8</b>	<b>Functional description</b> .....	<b>6</b>
<b>9</b>	<b>Limiting values</b> .....	<b>7</b>
<b>10</b>	<b>Thermal characteristics</b> .....	<b>8</b>
<b>11</b>	<b>Package outline</b> .....	<b>9</b>
<b>12</b>	<b>Soldering of WLCSP packages</b> .....	<b>10</b>
12.1	Introduction to soldering WLCSP packages ..	10
12.2	Board mounting .....	10
12.3	Reflow soldering .....	10
12.3.1	Stand off .....	11
12.3.2	Quality of solder joint .....	11
12.3.3	Rework .....	11
12.3.4	Cleaning .....	12
<b>13</b>	<b>Revision history</b> .....	<b>13</b>
<b>14</b>	<b>Legal information</b> .....	<b>14</b>
14.1	Data sheet status .....	14
14.2	Definitions .....	14
14.3	Disclaimers .....	14
14.4	Trademarks .....	15
<b>15</b>	<b>Contact information</b> .....	<b>15</b>
<b>16</b>	<b>Contents</b> .....	<b>16</b>

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