AR0239AT

Product Preview

AR0239AT 1/2.7-inch 2.3 Mp Digital Image Sensor

The AR0239AT from ON Semiconductor is a 1/2.7-inch CMOS digital image sensor with an active-pixel array of 1936 (H) × 1188 (V). It captures images in either linear or high dynamic range modes, with rolling-shutter readout. It includes sophisticated camera functions such as in-pixel binning, windowing and both video and single frame modes. It is designed for both low light and high dynamic range scene performance. It is programmable through a simple two-wire serial interface. The AR0239AT produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for automotive in−cabin applications such as occupants monitoring camera, object detection, car digital video recorder, etc.

Table 1. KEY PERFORMANCE PARAMETERS

Parameter	Typical Value
Optical Format	1/2.7 inch
Active Pixels	1936 (H) × 1188 (V) (16:9)
Pixel Size	3 μm × 3 μm BSI
Chief Ray Angle	0 Degrees (See Note)
Color Filter Array	RGB Bayer, RGB−IR
Shutter Type	Electronic Rolling Shutter (ERS)
Input Clock Range	6−54 MHz
Output Pixel Clock Maximum	88.28 MHz
Serial Data Rate Maximum	1.236 Gbps/Lane
Output Interfaces and Formats	Parallel, 12-bit MIPI, 10-12-bit; up to 4 lanes
Frame Rate 1080p	MIPI 90 fps / Linear 50 fps / 2-exposure 30 fps / 3-exposure Parallel 30 fps / Linear 15 fps / 2-exposure 10 fps / 3-exposure
Responsivity	28.6 Ke−/lux−sec
SNR_{MAX}	43 dB
Max Dynamic Range	Linear Mode: up to 83 dB Line−Interleaved Mode: up to 128 dB
Supply Voltage	I/O 1.8 V or 2.8 V Digital 1.2 V Analog 2.8 V
Power Consumption (Typical)	210 mW, 1080p30 linear parallel 190 mW, 1080p30 linear MIPI 252 mW, 1080p30 Line−Interleaved MIPI
Operating Temperature	−40°C to +105°C (Ambient), −40°C to +125°C (Junction)
Package	9 × 9 mm 63-pin iBGA

NOTE: Accommodates Lens CRA up to 20°.

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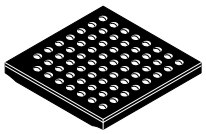


IBGA63 9x9
CASE 503BQ

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Features

- Superior Low-light Performance
- Key Technologies:
  - Backside Illuminated Pixel
  - Up to 3-exposure HDR at 1080p and 30 fps
  - 1080p Up to 90 fps (Linear Mode, Serial Interface)
- Latest 3.0 μm Back Side Illuminated (BSI) Pixel with ON Semiconductor DR−Pix™ Technology
- Full HD Support at Up to 1080p 90 fps for Superior Video Performance
- Linear or High Dynamic Range Capture
- Supports Line Interleaved T1/T2/T3 Readout to Enable HDR Processing in ISP Chip
- AEC−Q100 Grade 2 Qualified Qualified

Features (Continued)

- Support for External Mechanical Shutter
- On-chip Phase-locked Loop (PLL) Oscillator
- Slave Mode for Precise Frame-rate Control
- Statistics Engine
- Data interfaces: Up to 4-lane MIPI CSI-2 or Parallel
- Advanced HDR with Flexible Exposure Ratio Control
- Multi-Camera Synchronization Support
- Auto Black Level Calibration
- High-speed Configurable Context Switching
- Temperature Sensor

Applications

- Car Digital Video Recorder
- Automotive In−cabin Applications
- Object Detection

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
AR0239ATSC00XUEA0−DRBR−E	2.3MP, 1/2.7”, RGB, 0deg, MIPI/Parallel, 9x9 iBGA.	Double Sided BBAR Glass, Drypack without PF, Sample
AR0239ATSC00XUEA0−DPBR−E	2.3MP, 1/2.7”, RGB, 0deg, MIPI/Parallel, 9x9 iBGA.	Double Sided BBAR Glass, Drypack with PF, Sample
AR0239ATSC00XUD20−E	2.3MP, 1/2.7”, RGB, 0deg, MIPI/Parallel.	Die, Sample
AR0239ATSH00XUEA0−DRBR−E	2.3MP, 1/2.7”, RGB−IR, 0deg, MIPI/Parallel, 9x9 iBGA.	Double Sided BBAR Glass, Drypack without PF, Sample
AR0239ATSH00XUEA0−DPBR−E	2.3MP, 1/2.7”, RGB−IR, 0deg, MIPI/Parallel, 9x9 iBGA.	Double Sided BBAR Glass, Drypack with PF, Sample
AR0239ATSH00XUD20−E	2.3MP, 1/2.7”, RGB−IR, 0deg, MIPI/Parallel.	Die, Sample

See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

GENERAL DESCRIPTION

The ON Semiconductor AR0239AT can be programmed and operated for various frame size, frame rate, exposure, gain, and other parameters. In linear mode, it outputs 12-bit uncompressed or 10-bit A-Law compressed raw data, using either the parallel or MIPI output ports. In line-interleaved high dynamic range mode (HDR), it outputs three exposure values that the off-chip ISP could combine into an HDR image. The device may be operated in video (master) mode or in single frame trigger mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock in parallel mode.

The AR0239AT includes additional features to allow application-specific tuning: windowing and offset, auto black level correction, and on-board temperature sensor. Optional register information can be embedded in the first 2 lines of the image frame.

The AR0239AT is designed to operate over a wide temperature range of −40°C to +125°C junction.

FUNCTIONAL OVERVIEW

The AR0239AT is a 1/2.7 inch progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 54 MHz. The PLL can also be bypassed in parallel mode, which allows for the input clock to run between 6 and 88.28 MHz. The maximum output data rate is 1.236 Gb/s per lane in serial modes, and 88.28 Mp/s in parallel modes, corresponding to a pixel clock rate of 88.28 MHz. Figure 1 shows a block diagram of the sensor.

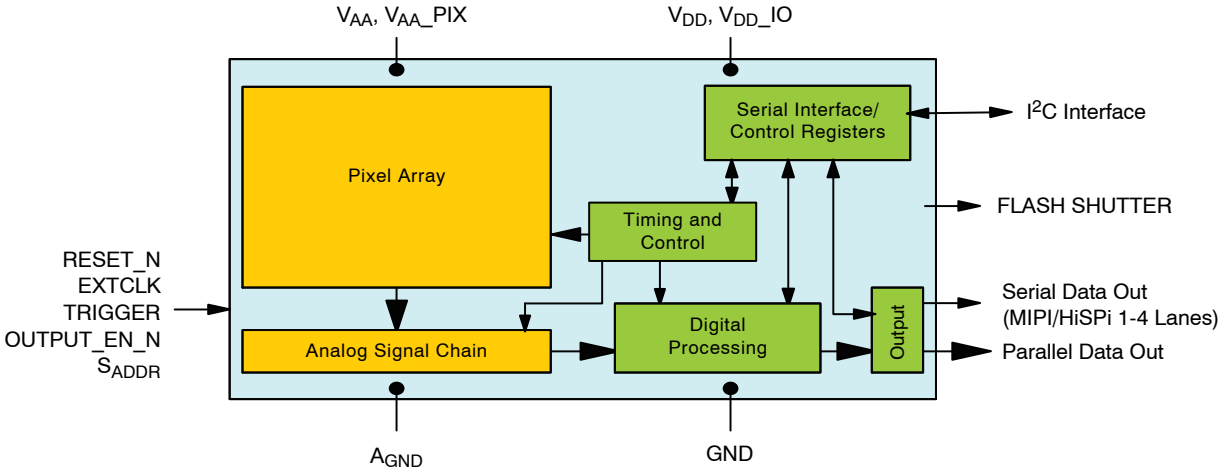
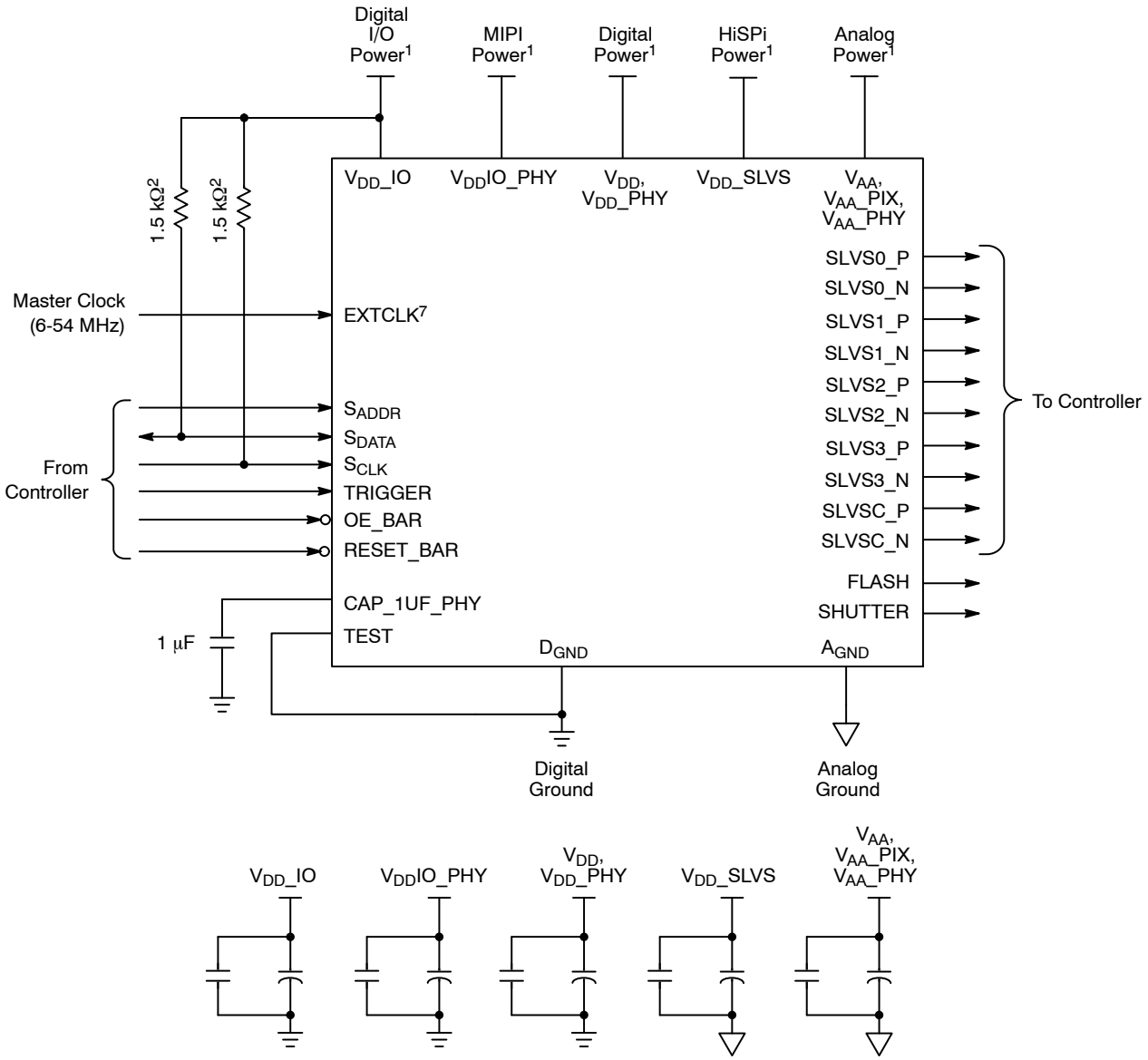


Figure 1. Block Diagram

User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 2.3 Mp BSI Active-Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain).

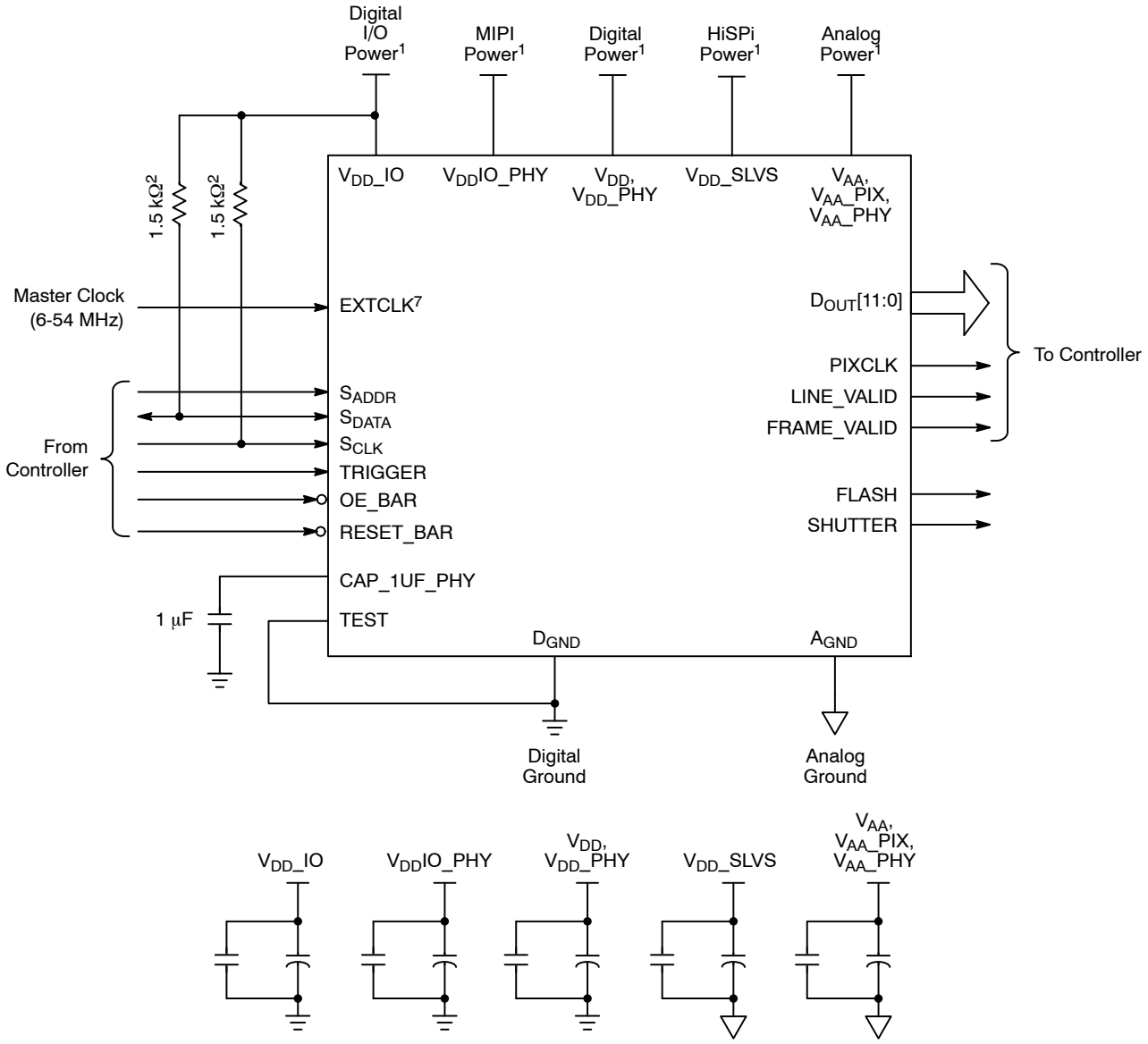
TYPICAL CONFIGURATION



Notes:

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. The parallel interface output pads can be left unconnected if the serial output interface is used.
4. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0239AT demo headboard schematics for circuit recommendations.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.
7. The EXTCLK input is limited to 6-54 MHz.

Figure 2. Serial 4-lane HiSPi/MIPI Interface



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5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.
7. The EXTCLK input is limited to 6-54 MHz.

Figure 3. Parallel Pixel Data Interface

PIN DESCRIPTIONS

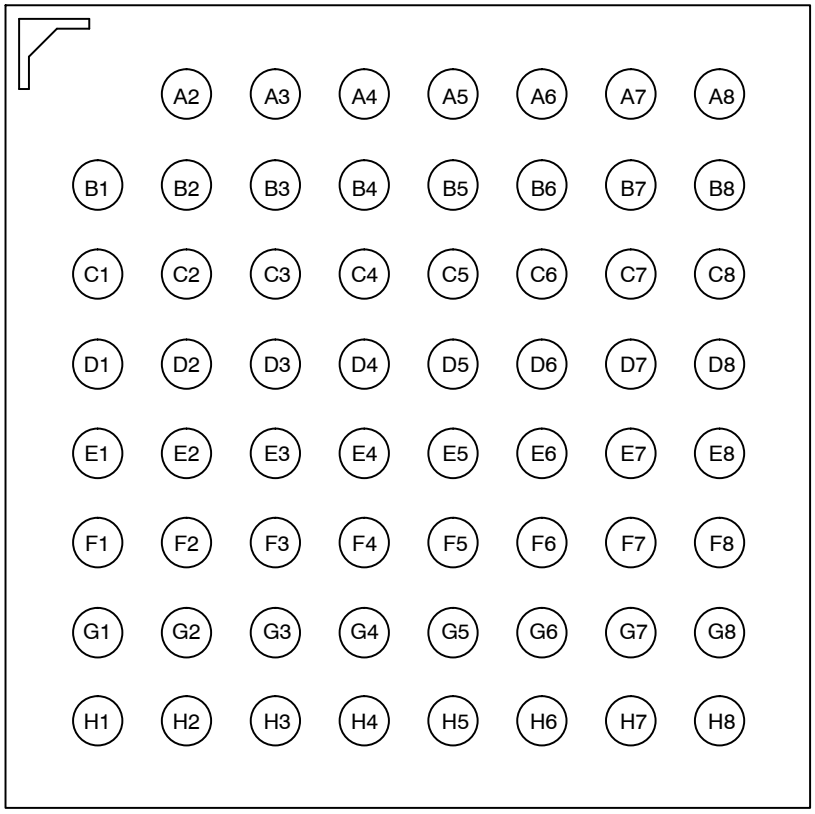


Figure 4. 63-ball iBGA Package (Top View)

Table 3. 63-BALL IBGA BALL MAP

	1	2	3	4	5	6	7	8
A		SLVS0P	SLVS1N	SLVSCN	SLVS2N	SLVS3N	CAP_1UF_PHY	D_{GND}
B	V_{DD}	SLVS0N	SLVS1P	SLVSCP	SLVS2P	SLVS3P	V_{DD}_SLVS	V_{DD}
C	V_{DD}IO	D_{GND}	EXTCLK	V_{DD}IO_PHY	V_{DD}	V_{AA}_PHY	S_{CLK}	V_{DD}IO
D	V_{DD}	FRAME_VALID	PIXCLK	V_{DD}_PHY	TEST	SHUTTER	RESERVED	V_{AA}
E	V_{DD}IO	D_{OUT}1	D_{OUT}0	LINE_VALID	RESET_N	FLASH	TRIGGER	A_{GND}
F	D_{GND}	D_{OUT}5	D_{OUT}4	D_{OUT}3	D_{OUT}2	S_{DATA}	ATEST	V_{AA}_PIX
G	V_{AA}	A_{GND}	D_{OUT}8	D_{OUT}7	D_{OUT}6	S_{ADDR}	A_{GND}	V_{AA}
H	D_{GND}	V_{DD}	D_{OUT}11	D_{OUT}10	D_{OUT}9	OE_BAR	V_{DD}	D_{GND}

Table 4. PIN DESCRIPTION, 63-BALL IBGA

Pin Name, Release	Pin	Type	Description
SLVS0P	A2	Output	Differential MIPI/HiSPi serial data lane 0
SLVS1N	A3	Output	Differential MIPI/HiSPi serial data lane 1
SLVSCN	A4	Output	Differential MIPI/HiSPi serial clock
SLVS2N	A5	Output	Differential MIPI/HiSPi serial data lane 2
SLVS3N	A6	Output	Differential MIPI/HiSPi serial data lane 3
CAP_1UF_PHY	A7	Power	External bypass capacitor for MIPI Regulator
D_{GND}	A8, C2, F1, H1, H8	Power	Digital Ground
V_{DD}	B1, B8, C5, D1, H2, H7	Power	Digital Power, 1.2 V nominal
SLVS0N	B2	Output	Differential MIPI/HiSPi serial lane 0

Table 4. PIN DESCRIPTION, 63-BALL IBGA (continued)

Pin Name, Release	Pin	Type	Description
SLVS1P	B3	Output	Differential MIPI/HiSPi serial lane 1
SLVSCP	B4	Output	Differential MIPI/HiSPi serial clock
SLVS2P	B5	Output	Differential MIPI/HiSPi serial lane 2
SLVS3P	B6	Output	Differential MIPI/HiSPi serial lane 3
V_{DD}_SLVS	B7	Power	SLVS PHY power, 1.2 V nominal
V_{DD}IO	C1, C8, E1	Power	IO Power, 1.8/2.8 V nominal
EXTCLK	C3	Input	Master input clock. PLL input clock
V_{DD}IO_PHY	C4	Power	Power to MIPI. 1.8 V nominal
V_{AA}_PHY	C6	Power	Power to MIPI. 2.8 V nominal
S_{CLK}	C7	Input	Two-wire Serial Clock Input
FRAME_VALID	D2	Output	Parallel data output FRAME_VALID output. Qualified by PIXCLK
PIXCLK	D3	Output	Parallel data output pixel clock. Used to qualify the LINE_VALID, FRAME_VALID, and D_{OUT}11 to D_{OUT}0 outputs
V_{DD}_PHY	D4	Power	Power to MIPI, 1.2 V nominal
TEST	D5	Input	Connect to ground through a 10 kΩ resistor
SHUTTER	D6	Output	Control for external mechanical shutter. Can be left floating if not used
RESERVED	D7	–	RESERVED, NC
V_{AA}	D8, G1, G8	Power	Analog Power, 2.8 V nominal
D_{OUT}1	E2	Output	Parallel data output pixel data bit 1. Qualified by PIXCLK
D_{OUT}0	E3	Output	Parallel data output pixel data bit 0. Qualified by PIXCLK
LINE_VALID	E4	Output	Parallel data output LINE_VALID output. Qualified by PIXCLK
RESET_N	E5	Input	Reset bar
FLASH	E6	Output	Flash output
TRIGGER	E7	Input	Trigger Input
A_{GND}	E8, G2, G7	Power	Analog Ground
D_{OUT}5	F2	Output	Parallel data output pixel data bit 5. Qualified by PIXCLK
D_{OUT}4	F3	Output	Parallel data output pixel data bit 4. Qualified by PIXCLK
D_{OUT}3	F4	Output	Parallel data output pixel data bit 3. Qualified by PIXCLK
D_{OUT}2	F5	Output	Parallel data output pixel data bit 2. Qualified by PIXCLK
S_{DATA}	F6	I/O	Two-wire Serial Data I/O
ATEST	F7	–	RESERVED, NC
V_{AA}_PIX	F8	Power	Analog Pixel Voltage, 2.8 V nominal
D_{OUT}8	G3	Output	Parallel data output pixel data bit 8. Qualified by PIXCLK
D_{OUT}7	G4	Output	Parallel data output pixel data bit 7. Qualified by PIXCLK
D_{OUT}6	G5	Output	Parallel data output pixel data bit 6. Qualified by PIXCLK
S_{ADDR}	G6	Input	Two-wire Serial address select
D_{OUT}11	H3	Output	Parallel data output pixel data bit 11. Qualified by PIXCLK
D_{OUT}10	H4	Output	Parallel data output pixel data bit 10. Qualified by PIXCLK
D_{OUT}9	H5	Output	Parallel data output pixel data bit 9. Qualified by PIXCLK
OE_BAR	H6	Input	Output Enable Bar

1. V_{DD}_PHY must be tied to V_{DD}.

PIXEL DATA FORMAT

Pixel Array Structure

While the typical sensor's format is 1920 × 1080, additional 100 active rows are included for the use when FOV adjustment is required.

Additional 8 rows and 8 columns are added to support demosaicing. The pixel color order is maintained in flip and horizontal mirror mode by shifting the ROI to right and down by 1 pixel. The pixel adjustment is always performed for monochrome or color versions. The maximum size of active window is 1936 × 1188. Additional 4 columns, border pixels, on either side help in taking care of the CRM requirements by making the total column number a multiple of 24. This provides more FOV flexibility in addition to the typical 1080p. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

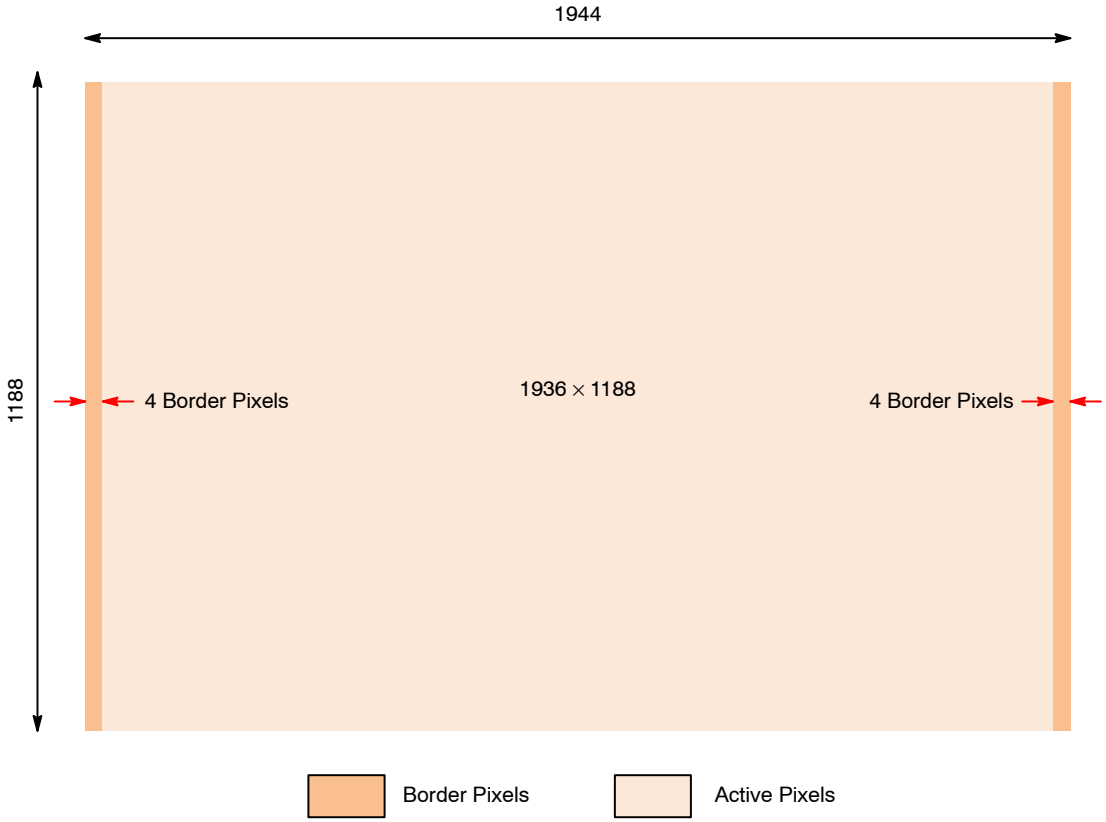


Figure 5. Pixel Array Description

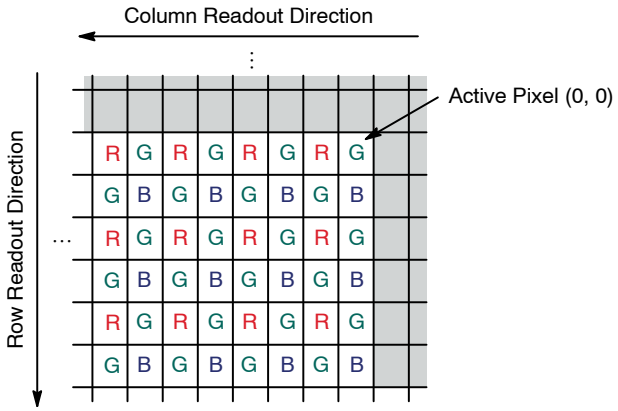


Figure 6. Pixel Color Pattern Detail (Top Right Corner)

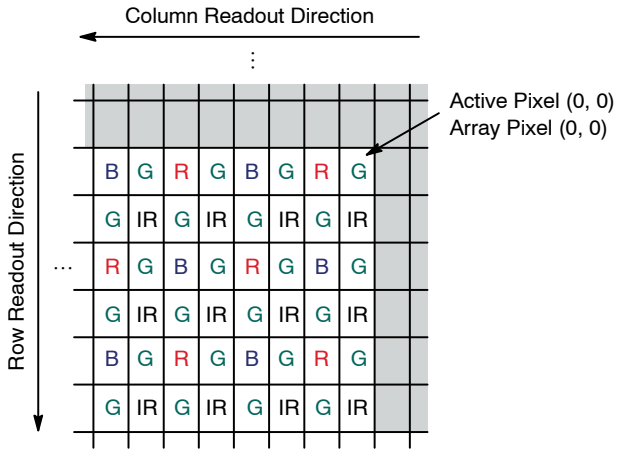


Figure 7. Pixel Color Pattern Detail (RGB–IR) (Top Right Corner)

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 6). This reflects the actual layout of the array on the die. Also, the first readable pixel location of the sensor in default condition is that of physical pixel address (2, 4). This first readable pixel location corresponds to the register X_ADDR_START_ (R0x3004) = 0x0000 and the register Y_ADDR_START_ (R0x3002) = 0x0000.

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 8. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 6.

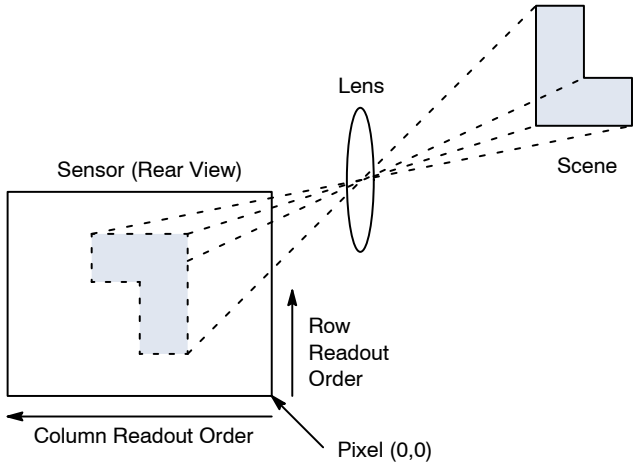


Figure 8. Imaging a Scene

OPERATING MODES AND FEATURES

3.0 μm Dual Conversion Gain Pixel

To improve the low light performance and keep the high dynamic range, a large (3.0 μm) dual conversion gain pixel is implemented for better image optimization. With a dual conversion gain pixel, the conversion gain of the pixel may be dynamically changed to better adapt the pixel response based on dynamic range of the scene. This gain can be switched manually or automatically by an external auto exposure control module.

Dual conversion gain can also be controlled independently for each exposure in HDR mode, allowing a mixture of high conversion gain (HCG) and low conversion gain (LCG) across multiple exposures.

Resolution

The active array supports a maximum of 1936 × 1188 pixels to support 1080p resolution. Utilizing a 3.0 μm pixel will result in an optical format of 1/2.7-inch.

Frame Rate

At full resolution, the AR0239AT is capable of running up to 90 fps 12 bit in linear mode with HiSPi or MIPI interfaces and 30 fps with parallel interface. 3-exposure line-interleaved mode is supported and could run up to 30 fps with HiSPi or MIPI interfaces and 10 fps with parallel interface.

Image Acquisition Mode

The AR0239AT supports two image acquisition modes:

- Electronic Rolling Shutter (ERS) Mode:
  This is the normal mode of operation. When the AR0239AT is streaming, it generates frames at a fixed rate, and each frame is integrated (exposed) using the ERS. When ERS mode is in use, timing and control logic within the sensor sequence through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and subsequently reading that row, the pixels in the row integrate incident light. The integration (exposure) time is controlled by varying the time between row reset and row readout. For each row in a frame, the time between row reset and row readout is the same, leading to a uniform integration time across the frame. When the integration time is changed (by using the two-wire serial interface to change register settings), the timing and control logic controls the transition from old to new integration time in such a way that the stream of output frames from the AR0239AT switches cleanly from the old integration time to the new while only generating frames with uniform integration. See “Changes to Integration Time” in the AR0239AT Register Reference.
- Global Reset Mode:
  This mode can be used to acquire a single image at the current resolution. In this mode, the end point of the pixel integration time is controlled by an external electromechanical shutter, and the AR0239AT provides control signals to interface to that shutter. The benefit of using an external electromechanical shutter is that it eliminates the visual artifacts associated with ERS operation. Visual artifacts arise in ERS operation, particularly at low frame rates, because an ERS image effectively integrates each row of the pixel array at a different point in time.

High Dynamic Range

The AR0239AT can operate in line-interleaved HDR mode to acquire video data using ON Semiconductor’s multi-exposure technology. This allows the sensor to handle > 120 dB of intrascene dynamic range. Line-interleaved HDR outputs the T1, T2, and T3 exposures separately, in a line interleaved format. The sensor also features a linear or standard dynamic range (SDR) mode where a single image is captured. In line-interleaved HDR mode, the sensor sequentially captures multiple exposures by maintaining separate read and reset pointers that are interleaved within the rolling shutter readout. The exposures are output as they are ready. An off-chip HDR ISP must have memory to store the longer exposures while waiting for the shortest exposure.

The exposure ratios may be set to 4×, 8×, 16×, or 32×, or can be individually controlled per exposure to allow a wide range of flexible exposure ratios. The individual exposure ratio control for T1, T2, and T3 is limited by the number of line buffers allocated to each exposure.

The dual conversion gain (LCG and HCG) can be controlled independently for each HDR exposure. For example, it is now possible to have an HDR frame where T1 uses HCG, but T2 and T3 use LCG.

Dual Conversion Gain (DCG)

To improve the low light performance and keep the high dynamic range, the AR0239AT has a dual conversion gain pixel implemented for better image optimization. With a dual conversion gain pixel, the conversion gain of the pixel may be dynamically changed to better adapt the pixel response based on dynamic range of the scene.

Multi-camera Synchronization

AR0239AT supports multi-camera synchronization Slave modes. The Slave modes support synchronization of multiple cameras within 8 pixel clocks from the beginning of FRAME_VALID/LINE_VALID from sensors without reducing the maximum frame rate. This feature saves the line memory buffer at the host system to combine a multiple of video input streams from the sensors.

Slave Mode

The slave mode feature of the AR0239AT supports triggering the start of a frame readout from an input signal that is supplied from an external ASIC. The slave mode signal allows for precise control of frame rate and register change updates.

Context Switching and Register Updates

The user has the option of using the highly configurable context memory, or a simplified implementation in which only a subset of registers is available for switching. The AR0239AT supports a highly configurable context switching RAM of size 256 × 16. Within this Context Memory, changes to registers within the chip may be stored. The register set for each context must be the same, but the number of contexts and registers per context are limited only by the size of the context memory.

Alternatively, the user may switch between two predefined register sets A and B by writing to a context switch change bit. When the context switch is configured to context A the sensor will reference the context A registers. If the context switch is changed from A to B during the readout of frame n, the sensor will then reference the context B coarse_integration_time registers in frame n+1 and all other context B registers at the beginning of reading frame n+2. The sensor will show the same behavior when changing from context B to context A. The registers listed in Table 5 are context switchable.

Table 5. LIST OF CONFIGURABLE REGISTERS FOR CONTEXT A AND CONTEXT B

Context A Register Description	Context B Register Description
coarse_integration_time	coarse_integration_time_cb
line_length_pck	line_length_pck_cb
frame_length_lines	frame_length_lines_cb
row_bin	row_bin_cb
col_bin	col_bin_cb
fine_gain	fine_gain_cb
coarse_gain	coarse_gain_cb
x_addr_start	x_addr_start_cb
y_addr_start	y_addr_start_cb
x_addr_end	x_addr_end_cb
y_addr_end	y_addr_end_cb
y_odd_inc	y_odd_inc_cb
x_odd_inc	x_odd_inc_cb
green1_gain	green1_gain_cb
blue_gain	blue_gain_cb
red_gain	red_gain_cb
green2_gain	green2_gain_cb
global_gain	global_gain_cb
operation_mode_ctrl	operation_mode_ctrl_cb
bypass_pix_comb	bypass_pix_comb_cb

Embedded Data

The AR0239AT has the capability to output image data within the frame timing. Embedded data can be enabled on two rows before the active image pixels are displayed, and show the current settings for the part.

Black Level Control/Correction

Black level correction can optionally be automatically controlled by the AR0239AT; the default setting is for automatic black level calibration to be enabled. The automatic black level correction measures the average value of pixels from a set of optically black lines in the image sensor. The pixels are averaged as if they were light sensitive and passed through the appropriate gain. This line average is then digitally low-pass filtered over many lines to remove temporal noise and random instabilities associated with this measurement.

Column Noise Correction

Row and column noise correction is applied automatically by the image sensor on a frame by frame basis. Re-triggering of correction circuits due to settings or temperature changes are not necessary. No adjustments are provided for these correction circuits but they may be individually enabled / disabled.

Analog/Digital Gains

A programmable analog gain of 1× to 28× applied simultaneously to all color channels will be featured along with a digital gain of 1× to 16× that may be configured on a per color channel basis. There is an option to separate the digital gain for use as an AWB function or as a global gain. Table 6 shows the recommended analog gain settings for linear mode. Table 7 lists the Line−Interleaved HDR gain registers. HDR gains of each exposure use the same gain table with their own designated registers. Note that with the RGB IR sensor digital gain should only be applied to all color channels equally since with the 4 x 4 kernel the gains will not be applied to the proper color channel.

Table 6. LINEAR MODE GAIN TABLE

Conversion Gain	COARSE_GAIN	FINE_GAIN	
R0x3100[2]	R0x3060[6:4]	R0x3060[3:0]	Total Gain (x)
0	0	0	1.000
0	0	1	1.032
0	0	2	1.067
0	0	3	1.103
0	0	4	1.143
0	0	5	1.185
0	0	6	1.231
0	0	7	1.280
0	0	8	1.333
0	0	9	1.391
0	0	10	1.455
0	0	11	1.524
0	0	12	1.600
0	0	13	1.684
0	0	14	1.778
0	0	15	1.882
0	1	0	2.000
0	1	2	2.133
0	1	4	2.286
0	1	6	2.462
0	1	8	2.667
0	1	10	2.909
1	0	0	3.000
1	0	1	3.097
1	0	2	3.200
1	0	3	3.310
1	0	4	3.429
1	0	5	3.556
1	0	6	3.692
1	0	7	3.840
1	0	8	4.000
1	0	9	4.174
1	0	10	4.364
1	0	11	4.571
1	0	12	4.800
1	0	13	5.053
1	0	14	5.333
1	0	15	5.647
1	1	0	6.000
1	1	2	6.400
1	1	4	6.857
1	1	6	7.385
1	1	8	8.000
1	1	10	8.727
1	1	12	9.600
1	1	14	10.667
1	2	0	12.000
1	2	1	12.387
1	2	2	12.800
1	2	3	13.241
1	2	4	13.714

Table 6. LINEAR MODE GAIN TABLE

Conversion Gain	COARSE_GAIN	FINE_GAIN	
R0x3100[2]	R0x3060[6:4]	R0x3060[3:0]	Total Gain (x)
1	2	5	14.222
1	2	6	14.769
1	2	7	15.360
1	2	8	16.000
1	2	9	16.696
1	2	10	17.455
1	2	11	18.286
1	2	12	19.200
1	2	13	20.211
1	2	14	21.333
1	2	15	22.588
1	3	0	24.000
1	3	1	24.774
1	3	2	25.600
1	3	3	26.483
1	3	4	27.429
1	3	5	28.444
1	3	6	29.538
1	3	7	30.720
1	3	8	32.000
1	3	9	33.391
1	3	10	34.909
1	3	11	36.571
1	3	12	38.400
1	3	13	40.421
1	3	14	42.667
1	3	15	45.176
1	4	0	48.000
1	4	2	51.200
1	4	4	54.857
1	4	6	59.077
1	4	8	64.000
1	4	10	69.818
1	4	12	76.800
1	4	14	85.333

Table 7. GAIN REGISTERS FOR ALL MODES

Exposure	DCG	Coarse Gain	Fine Gain	Remark
All	R0x3100[2]	R0x3060[6:4]	R0x3060[3:0]	Linear mode or LI−HDR when all exposure use the same gain (R0x3100[10] = 0)
T1	R0x3100[8]	R0x312C[6:4]	R0x312C[3:0]	3−exposure LI−HDR when T1/T2/T3 use separate gain (R0x3100[10] = 1)
T2	R0x3100[12]	R0x3060[6:4]	R0x3060[3:0]	
T3	R0x3100[2]	R0x32A6[6:4]	R0x32A6[3:0]	
T1	R0x3100[8]	R0x312C[6:4]	R0x312C[3:0]	2−exposure LI−HDR when T1/T2 use separate gain (R0x3100[10] = 1)
T2	R0x3100[2]	R0x3060[6:4]	R0x3060[3:0]	

Skipping/Binning Modes

The AR0239AT supports subsampling. Subsampling allows the sensor to read out a smaller set of active pixels by either skipping, binning, or summing pixels within the readout window. Horizontal binning is achieved in the digital readout. The sensor will sample the combined two adjacent pixels within the same color plane. Vertical row binning is applied in the pixel readout. Row binning can be configured as two rows within the same color plane. Pixel skipping can be configured up to two in both the x-direction and y-direction. Skipping pixels in the x-direction will not reduce the row time. Skipping pixels in the y direction will reduce the number of rows from the sensor effectively reducing the frame time. Skipping will introduce image artifacts from aliasing. The AR0239AT supports row wise vertical binning. Row wise vertical summing is supported in mono mode. Note that RGB−IR CFA variant does not support Skipping/Binning.

CFA Type Identification

CFA type (e.g. RGB, mono, etc.) may be determined by reading an identification register via the 2-wire control interface.

PLL and Clock Control

The sensor contains a phase−locked loop (PLL) that is used for timing generation and control. The max PIXCLK this PLL supports is up to 88.28 MHz. However, to achieve the best image quality, the recommended PIXCLK range is 44 ~ 72 MHz for serial interfaces and 88 MHz for parallel interface. The PLL diagram is shown in Figure 9.

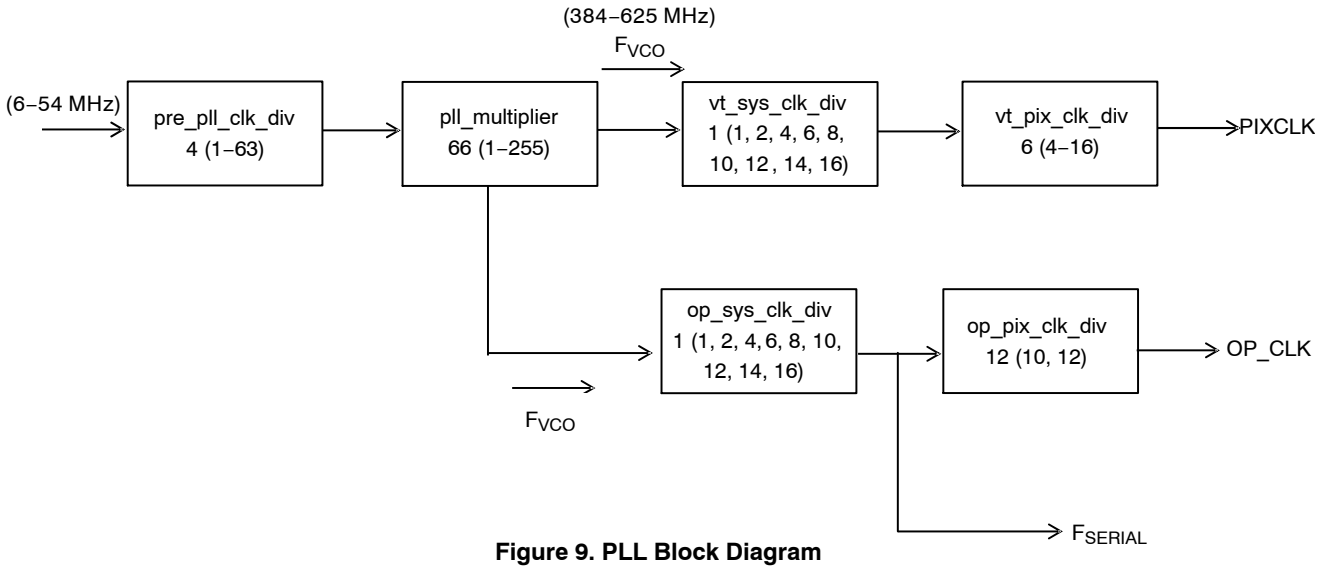


Figure 9. PLL Block Diagram

VCO

The required VCO clock frequency is attained through the use of a pre−PLL clock divider followed by a multiplier. The PLL multiplier should be an even integer. If an odd integer (M) is programmed, the PLL will default to the lower (M − 1) value to maintain an even multiplier value. The multiplier is followed by a set of dividers used to generate the output clocks required for the sensor array, the pixel analog and digital readout paths, and the output parallel and serial interfaces. FVCO can be calculated using the following equations:

$$F_{VCO} = \frac{EXTCLK \times pll\_multiplier}{pre\_pll\_clk\_div} \quad \text{(eq. 1)}$$

$$PIXCLK = \frac{F_{VCO}}{vt\_sys\_clk\_div \times vt\_pix\_clk\_div} \quad \text{(eq. 2)}$$

$$OP\_CLK = \frac{F_{VCO} \times 2}{op\_sys\_clk\_div \times op\_pix\_clk\_div} \quad \text{(eq. 3)}$$

Six Readout Paths

There are six readout paths within the sensor array block. The sensor PLL should be configured such that the total pixel rate across the six readout paths is equal to the output pixel rate.

Parallel PLL Configuration

The optimal output of the parallel interface is 88 MPixel/s with PIXCLK = 88 MHz. To sync up the output pixel rate from the six readout paths and parallel interface clock, the sampling frequency inside the sensor array is PIXCLK / 6. This will limit the sensor array readout clock to 14.67 MHz. The sensor will not use the F_{SERIAL} or OP_CLK when configured to use the parallel interface.

Table 8. PLL PARAMETERS FOR THE PARALLEL INTERFACE

Parameter	Symbol	Min	Max	Unit
External Clock	EXTCLK	6	54	MHz
VCO Clock	F_{VCO}	384	625	MHz
Readout Clock	PIXCLK	–	88.28	MHz

Serial PLL Configuration

For both MIPI and HiSPi, the sampling frequency inside the sensor array is PIXCLK. The max supported PIXCLK frequency is 88.28 MHz, which has a readout pixel rate of 530 MPixels/s. The sensor will use op_sys_clk_div and op_pix_clk_div to configure the output word clock per lane (OP_CLK). The configuration will depend on the number of active lanes (1, 2, or 4) configured.

Table 9. PLL PARAMETERS FOR THE SERIAL INTERFACE

Parameter	Symbol	Min	Max	Unit
External Clock	EXTCLK	6	54	MHz
VCO Clock	FVCO	384	625	MHz
Readout Clock	PIXCLK	–	88.28	MHz
Output Serial Clock	F_{SERIAL}	–	618	MHz
Output Serial Data Rate per Lane		–	1.236	Gbps

The following is PLL example setting for parallel and serial interfaces with input clock (EXTCLK) = 27 MHz.

Table 10. EXAMPLE PLL CONFIGURATIONS

Parameter	Parallel 12−bit	Serial 12−bit, 4 lane	Serial 12−bit, 4 lane	Serial 12−bit, 2 lane	Unit
pll_multiplier	176	144	176	128	
pre_pll_clk_div	9	9	9	9	
vt_sys_clk_div	1	1	2	2	
vt_pix_clk_div	6	6	6	6	
op_sys_clk_div	1	1	2	1	
op_pix_clk_div	12	12	12	12	
F_{VCO}	528	432	528	384	MHz
F_{SERIAL}	–	432	264	384	MHz
Data Bit Rate / Lane	–	864	528	768	Mbit/s
PIXCLK	88	72	44	32	MHz
OP_CLK	–	72	44	64	MHz

Temperature Sensor

The AR0239AT sensor has a built-in PTAT-based temperature sensor, accessible through registers, that is capable of measuring die junction temperature. The value read out from the temperature sensor register is an ADC output value that needs to be converted downstream to a final temperature value in degrees Celsius. Since the PTAT device characteristic response is quite linear in the temperature range of operation required, a simple linear function can be used to convert the ADC output value to the final temperature in degrees Celsius.

A single reference point will be made available via register read as well as a slope for back-calculating the junction temperature value. An error of ±5% or better over the full specified operating range of the sensor is to be expected.

Silicon/Firmware/Sequencer Revision Information

Revision registers are provided to read out (via I^2C) silicon and sequencer/OTPM revision information. This will be helpful to distinguish among different lots of material if there are future OTPM or sequencer revisions.

SYSTEM INTERFACES

This section describes the AR0239AT interfaces. Note that all output port options may not be available on all packaging options.

HiSPi Pixel Output Port

The AR0239AT provides a 4-lane HiSPi pixel output port with support for SLVS mode. 1, 2, or 4 lanes is supported with 12/10 bit Bayer using SP-packetized, SP-streaming or Streaming-S at a maximum data rate of 1.236 Gbps per lane. Additional information is provided in the ON Semiconductor HiSPi Protocol and Physical Layer documents.

MIPI CSI-2 Pixel Output Port

The AR0239AT provides a 4-lane MIPI CSI-2 pixel output port. The data protocol is 1,2, or 4 lanes, 12/10-bit, Bayer, at a maximum data rate of 1.236 Gbps per lane. Please contact ON Semiconductor for additional information.

Parallel Pixel Output Port

The AR0239AT provides a 12-bit data pixel output port with frame and line valid signals.

Two-Wire Sensor Control Interface

The two-wire serial interface bus enables read/write access to control and status registers within the AR0239AT. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (S_{CLK}) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (S_{DATA}). S_{DATA} is pulled up to V_{DD}_IO off-chip by a 1.5 kΩ resistor. Either the slave or master device can drive S_{DATA} LOW-the interface protocol determines which device is allowed to drive S_{DATA} at any given time. The protocols described in the two-wire serial interface specification allow the slave device to drive S_{CLK} LOW; the AR0239AT uses SCLK as an input only and therefore never drives it LOW.

POWER-ON RESET AND STANDBY TIMING

Power-Up Sequence

The recommended power-up sequence for the AR0239AT is shown in Figure 10. The available power supplies (V_{AA}/V_{AA}_PIX/V_{AA}_PHY, V_{DD}IO, V_{DD}IO_PHY, V_{DD}/V_{DD}_PHY, and V_{DD}_SLVS) must have the separation specified below.

1. Turn on V_{AA}/V_{AA}_PIX/V_{AA}_PHY power supply.
2. After 100 µs, turn on V_{DD}IO power supply.
3. After 100 µs, turn on V_{DD}IO_PHY(1.8 V) power supply.
4. After 100 µs, turn on V_{DD}/V_{DD}_PHY power supply
5. After 100 µs, turn on V_{DD}_SLVS power supply.
6. After the last power supply is stable, enable EXTCLK.
7. Assert RESET_N for at least 1 ms. The parallel interface will be tri-stated during this time.
8. Wait for ~150000 EXTCLKs for internal initialization into soft standby where M3ROM and full OTPM upload would be complete.
9. Set streaming mode (mode_select/stream (R0x301A[2]) = 1) and the internal PLL would be enabled (not locked yet).
10. Wait for 1 ms for PLL lock to complete, Part will then go into streaming mode.

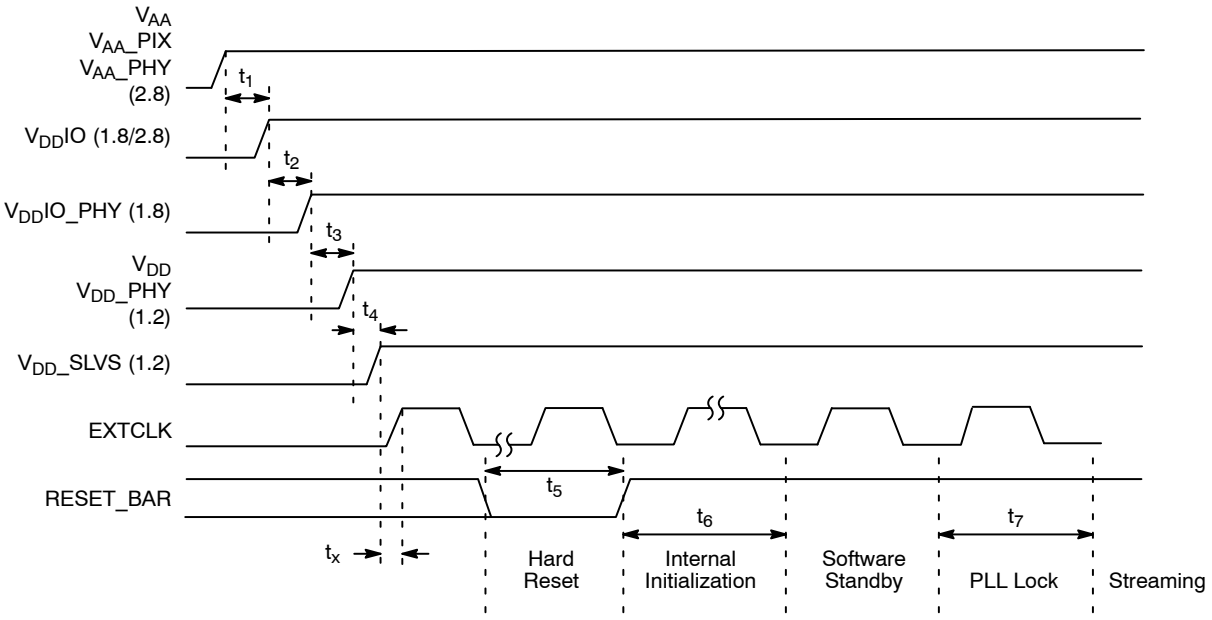


Figure 10. Power-up Sequence

Table 11. POWER-UP SEQUENCE

SN	Definition	Symbol	Min	Typ	Max	Unit
1	V_{AA}/V_{AA}_PIX/V_{AA}_PHY to V_{DD}IO	t_1	0	100	–	µs
2	V_{DD}IO to V_{DD}IO_PHY	t_2	0	100	–	µs
3	V_{DD}IO_PHY to V_{DD}/V_{DD}_PHY	t_3	0	100	–	µs
4	V_{DD}/V_{DD}_PHY to V_{DD}_SLVS	t_4	0	100	–	µs
5	Xtal Settle Time (Component Dependent)	t_x	–	30 ms	–	ms
6	Hard Reset	t_5	1	–	–	ms
7	Internal Initialization	t_6	150000	–	–	Ext CLK Cycles
8	PLL Lock Time	t_7	1	–	–	ms

2. V_{DD} and V_{DD}_SLVS can be tied together (t_4 becomes '0' in this case).
3. V_{DD}IO if 2.8 V can be tied together with V_{AA}/V_{AA}PIX/V_{AA}_PHY (t_1 becomes '0' in this case).

Power Down Sequence

The recommended power-down sequence for the AR0239AT is shown in Figure 11. The available power supplies (V_{AA}/V_{AA}_PIX/V_{AA}_PHY, V_{DD}IO, V_{DD}IO_PHY, V_{DD}/ V_{DD}_PHY, and V_{DD}_SLVS) must have the separation specified below.

1. [Optional] Disable streaming if output is active by setting standby R0x301a[2] = 0.
2. [Optional] The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off V_{DD}_SLVS.
4. Turn off V_{DD}/V_{DD}_PHY.
5. Turn off V_{DD}IO_PHY.
6. Turn off V_{DD}IO.
7. Turn off V_{AA}/V_{AA}_PIX/V_{AA}_PHY.

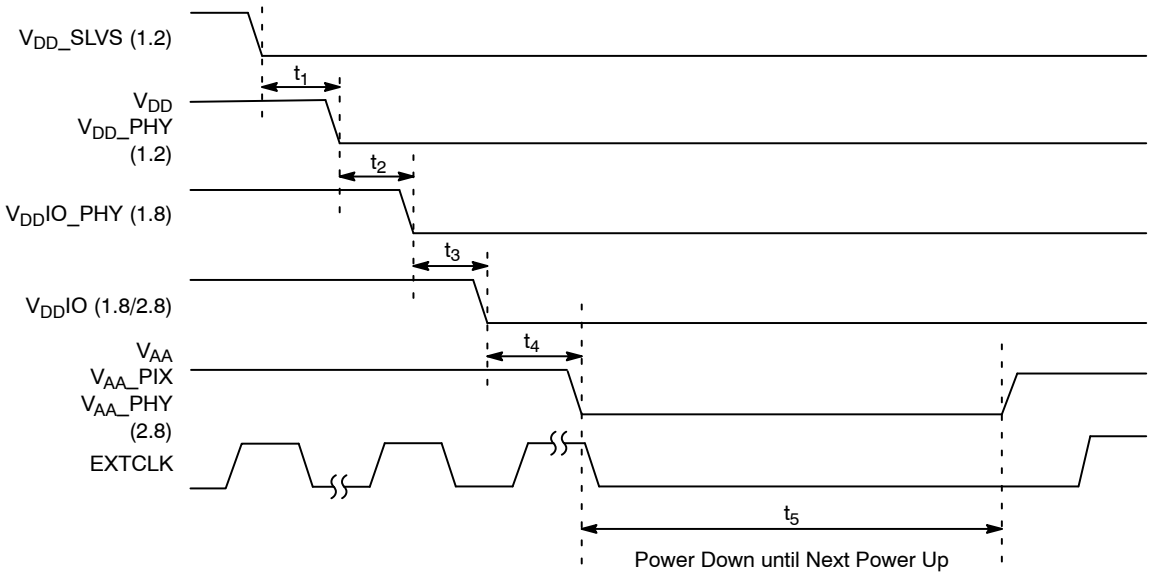


Figure 11. Power-down Sequence

Table 12. POWER-DOWN SEQUENCE

SN	Definition	Symbol	Min	Typ	Max	Unit
1	V_{DD}_SLVS to V_{DD}/V_{DD}_PHY	t_1	0	–	–	
2	V_{DD}/V_{DD}_PHY to V_{DD}IO_PHY	t_2	0	–	–	
3	V_{DD}IO_PHY to V_{DD}IO	t_3	0	–	–	
4	V_{DD}IO to V_{AA}/V_{AA}_PIX/V_{AA}_PHY	t_4	0	–	–	
5	PwrDn until Next Pwrup Time	t_5	100	–	–	ms

4. V_{DD} and V_{DD}_SLVS can be tied together.
5. V_{DD}IO if 2.8 V can be tied together with V_{AA}/V_{AA}PIX/V_{AA}_PHY.

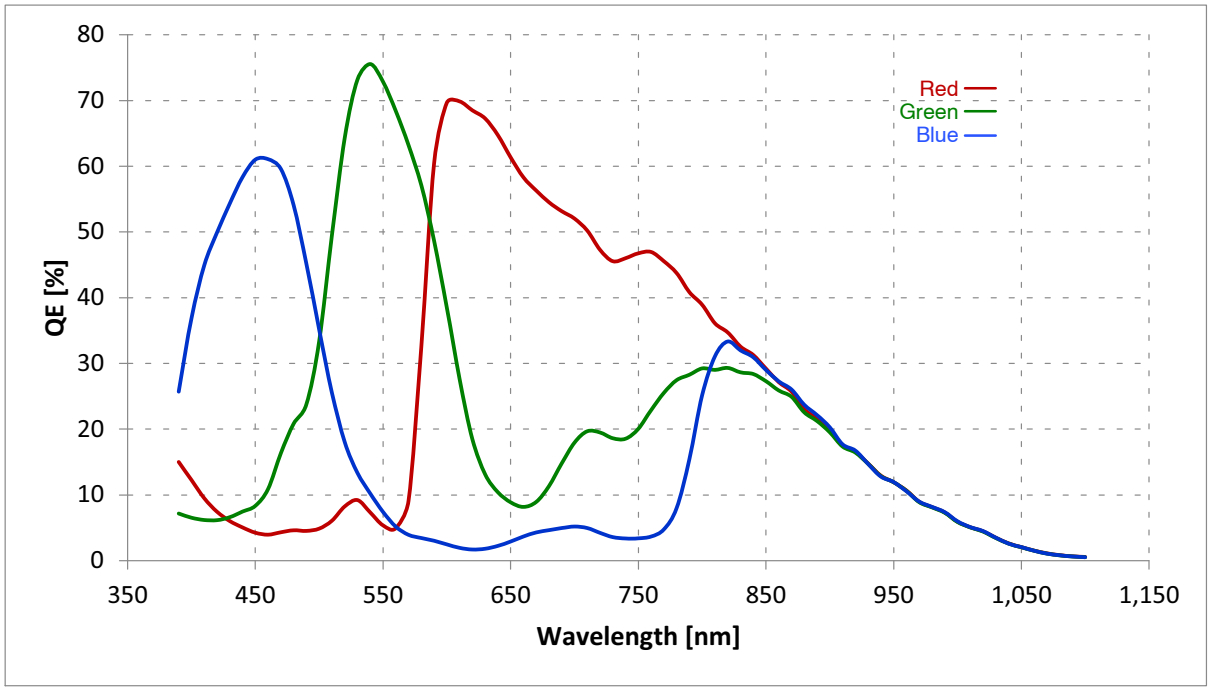


Figure 12. RGB Quantum Efficiency Curve

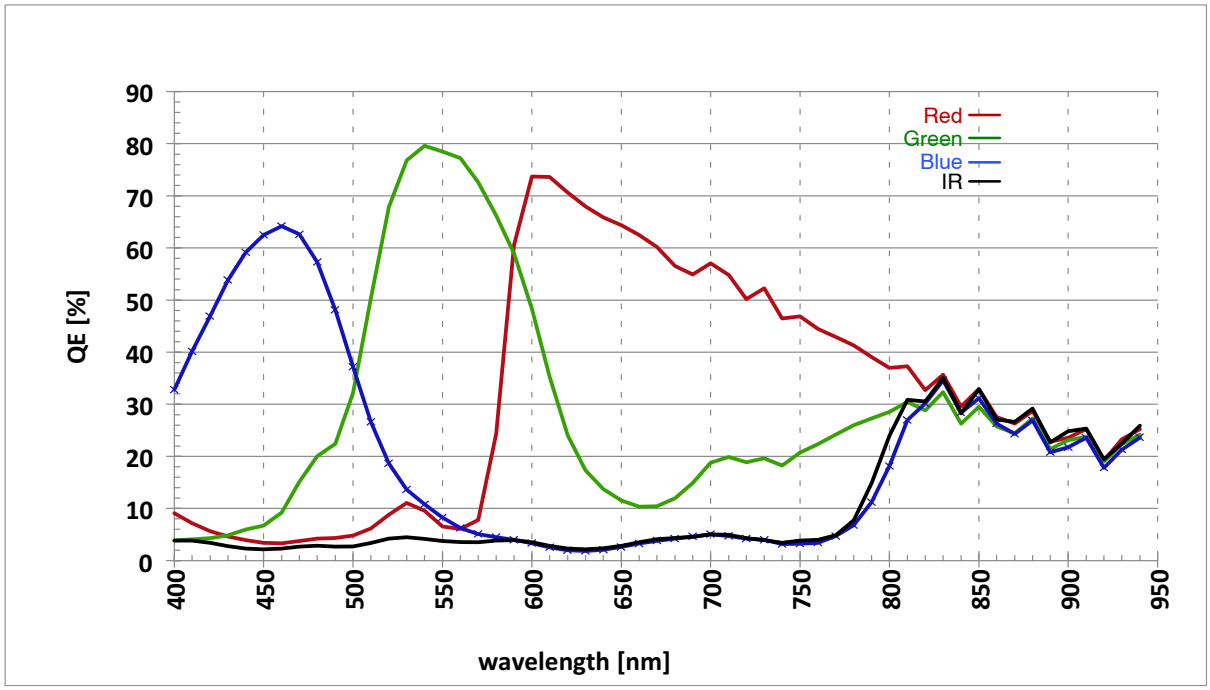


Figure 13. RGB–IR Quantum Efficiency Curve

ELECTRICAL SPECIFICATIONS

Table 13. ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Condition	Min	Max	Unit
V_{AA}_MAX	Analog Voltage		–0.3	4	V
V_{AA}_PIX	Pixel Supply Voltage		–0.3	4	V
V_{DD}_IO_MAX	I/O Digital Voltage		–0.3	4	V
V_{DD}_IO_PHY	Power to MIPI		–0.3	2.4	V
V_{DD}_MAX	Core Digital Voltage		–0.3	2.4	V
V_{DD}_SLVS_MAX	HiSPi I/O Digital Voltage		–0.3	2.4	V
t_{ST}	Storage Temperature		–40	125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 14. OPERATING CONDITIONS

Symbol	Definition	Min	Typ	Max	Unit
V_{AA}	Analog Power	2.66	2.8	2.94	V
V_{AA}_PIX	Analog Pixel Voltage	2.66	2.8	2.94	V
V_{AA}_PHY	Power to MIPI	2.66	2.8	2.94	V
V_{DD}IO	IO Power	1.71/2.66	1.8/2.8	1.89/2.94	V
V_{DD}IO_PHY	Power to MIPI	1.71	1.8	1.89	V
V_{DD}	Digital Power	1.14	1.2	1.26	V
V_{DD}_PHY	Power to MIPI	1.14	1.2	1.26	V
V_{DD}_SLVS	SLVS PHY Power	1.14	1.2	1.26	V

Table 15. DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage		V_{DD}_IO × 0.7	–	–	V
V_{IL}	Input LOW Voltage		–	–	V_{DD}_IO × 0.3	V
I_{IN}	Input leakage Current	No Pull-up Resistor; V_{IN} = V_{DD}_IO or D_{GND}	20	–	–	μA
V_{OH}	Output HIGH Voltage		V_{DD}_IO – 0.3	–	–	V
V_{OL}	Output LOW Voltage		–	–	0.4	V
I_{OH}	Output HIGH Current	At Specified V_{OH}	–22	–	–	mA
I_{OL}	Output LOW Current	At Specified V_{OL}	–	–	22	mA

Table 16. OPERATING CURRENT CONSUMPTION

Conditions	Symbol	Min	Typ	Max	Unit
1080p30 Linear 88 MHz Parallel	$I_{AA}/I_{AA}\_PIX/I_{AA}\_PHY$	20	49	75	mA
	$I_{DD}IO$	6	11	40	
	$I_{DD}IO\_PHY$	0.01	0.2	1	
	$I_{DD}/I_{DD}\_PHY/I_{DD}\_SLVS$	20	35	55	
	Power	97	210	390	mW
1080p30 Linear 88 MHz HiSPi SLVS	$I_{AA}/I_{AA}\_PIX/I_{AA}\_PHY$	12	22	45	mA
	$I_{DD}IO$	0.01	0.2	1	
	$I_{DD}IO\_PHY$	4	8	20	
	$I_{DD}/I_{DD}\_PHY/I_{DD}\_SLVS$	100	118	140	
	Power	161	218	333	mW
1080p60 Linear 88 MHz HiSPi SLVS	$I_{AA}/I_{AA}\_PIX/I_{AA}\_PHY$	15	33.5	60	mA
	$I_{DD}IO$	0.01	0.2	1	
	$I_{DD}IO\_PHY$	4	9	20	
	$I_{DD}/I_{DD}\_PHY/I_{DD}\_SLVS$	100	123	150	
	Power	169	258	387	mW
1080p30 Linear 88 MHz MIPI	$I_{AA}/I_{AA}\_PIX/I_{AA}\_PHY$	10	22	45	mA
	$I_{DD}IO$	0.01	0.2	1	
	$I_{DD}IO\_PHY$	2	7	15	
	$I_{DD}/I_{DD}\_PHY/I_{DD}\_SLVS$	80	96	130	
	Power	128	190	312	mW
1080p60 Linear 88 MHz MIPI	$I_{AA}/I_{AA}\_PIX/I_{AA}\_PHY$	10	33.5	60	mA
	$I_{DD}IO$	0.01	0.2	1	
	$I_{DD}IO\_PHY$	3	7.5	15	
	$I_{DD}/I_{DD}\_PHY/I_{DD}\_SLVS$	80	105	140	
	Power	129	234	366	mW
1080p30 Line-interleaved 88 MHz HiSPi SLVS	$I_{AA}/I_{AA}\_PIX/I_{AA}\_PHY$	15	33	60	mA
	$I_{DD}IO$	0.01	0.2	1	
	$I_{DD}IO\_PHY$	4	9.5	20	
	$I_{DD}/I_{DD}\_PHY/I_{DD}\_SLVS$	100	128	160	
	Power	169	264	399	mW
1080p30 Line-interleaved 88 MHz MIPI	$I_{AA}/I_{AA}\_PIX/I_{AA}\_PHY$	15	33	60	mA
	$I_{DD}IO$	0.01	0.2	1	
	$I_{DD}IO\_PHY$	4	9.5	20	
	$I_{DD}/I_{DD}\_PHY/I_{DD}\_SLVS$	90	118	150	
	Power	157	252	387	mW

NOTE: (Operating currents are measured in mA at the following conditions:
6. VAA= VAA_PIX = VDD_IO = 2.8 V; VDDIO_PHY = 1.8V; VDD = VDD_SLVS = 1.2 V
7. PLL Enabled and PIXCLK = 88 MHz
8. T_A=25°C
9. Parallel uses Low Power mode

Table 17. STANDBY CURRENT

Conditions	Symbol	Typ	Max	Unit
Hard Standby Clock On	IAA/IAA_PIX/IAA_PHY	0.025	0.075	mA
	IDDIO	0.005	0.03	
	IDDIO_PHY	0.005	0.03	
	IDD/IDD_PHY/IDD_SLVS	1.2	3.3	
	Total current	1.235	3.435	
	Power	1.533	4.308	mW
Hard Standby Clock Off	IAA/IAA_PIX/IAA_PHY	0.025	0.075	mA
	IDDIO	0.005	0.03	
	IDDIO_PHY	0.005	0.03	
	IDD/IDD_PHY/IDD_SLVS	1.2	3.3	
	Total current	1.235	3.435	
	Power	1.533	4.308	mW
Soft Standby Clock On	IAA/IAA_PIX/IAA_PHY	0.025	0.075	mA
	IDDIO	0.03	0.06	
	IDDIO_PHY	0.005	0.03	
	IDD/IDD_PHY/IDD_SLVS	18	24	
	Total current	18.06	24.165	
	Power	21.763	29.232	mW
Soft Standby Clock Off	IAA/IAA_PIX/IAA_PHY	0.025	0.075	mA
	IDDIO	0.006	0.03	
	IDDIO_PHY	0.005	0.03	
	IDD/IDD_PHY/IDD_SLVS	1.2	3.3	
	Total current	1.236	3.435	
	Power	1.536	4.308	mW

I/O Timing

By default, the AR0239AT launches pixel data, FV, and LV with the falling edge of PIXCLK. The expectation is that the user captures D_{OUT}[11:0], FV, and LV using the rising edge of PIXCLK.

See Figure 14 below and Table 18 for I/O timing (AC) characteristics.

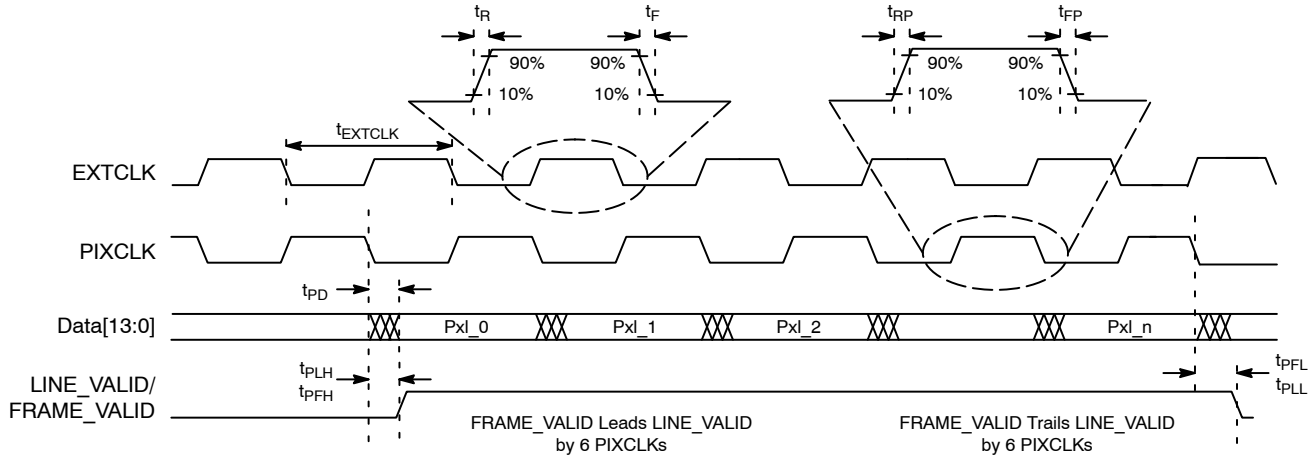


Figure 14. I/O Timing Diagram

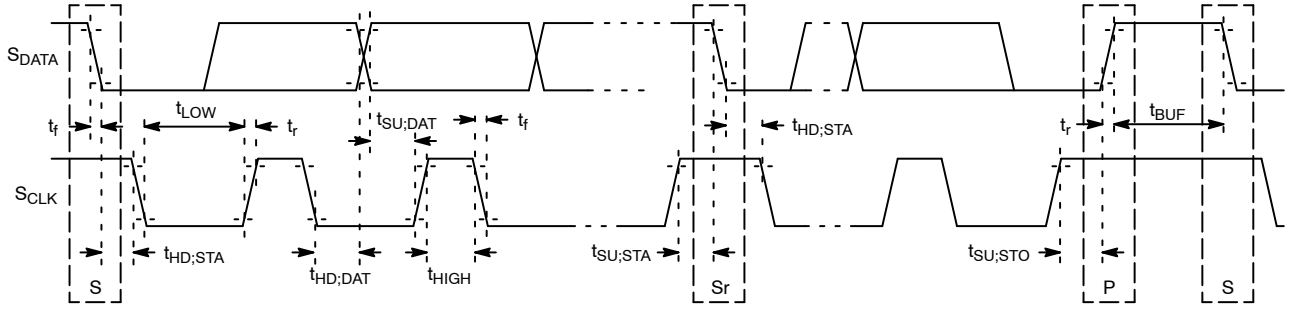
Table 18. I/O TIMING CHARACTERISTICS (Note 10)

Symbol	Definition	Condition	Min	Nom	Max	Unit
f_{EXTCLK}	Input Clock Frequency		6 (Note 11)	27	54	MHz
t_{EXTCLK}	Input Clock Period		18.5	37.04	166	ns
t_R	Input Clock Rise Time		–	3	–	ns
t_F	Input Clock Fall Time		–	3	–	ns
t_{RP}	Pixclk Rise Time		2	3.5	5	ns
t_{FP}	Pixclk Fall Time		2	3.5	5	ns
	Clock Duty Cycle		42	50	58	%
t_{CP}	EXTCLK to PIXCLK Propagation Delay	Nominal Voltages, PLL Disabled, without half clock cycle delay	10	16.5	20	ns
$t_{PIX\ JITTER}$	Jitter on PIXCLK		–	1	–	ns
f_{PIXCLK}	PIXCLK Frequency	Default, Nominal Voltages	6	–	88	MHz
t_{PD}	PIXCLK to Data Valid	Default, Nominal Voltages	0	3.5	6.5	ns
t_{PFH}	PIXCLK to FV HIGH	Default, Nominal Voltages	–2	4.5	7.5	ns
t_{PLH}	PIXCLK to LV HIGH	Default, Nominal Voltages	–2	4.2	7.5	ns
t_{PFL}	PIXCLK to FV LOW	Default, Nominal Voltages	–2	4.5	7.5	ns
t_{PLL}	PIXCLK to LV LOW	Default, Nominal Voltages	–2	4.5	7.5	ns
C_{LOAD}	Output Load Capacitance		–	< 10	–	pF
C_{IN}	Input Pin Capacitance		–	2.5	–	pF

10. I/O timing characteristics are measured under the following conditions:
    a. Temperature is 25°C ambient
    b. 10 pF load
    c. 1.8 V I/O supply voltage
11. When using a 1 MHz two-wire interface clock, the minimum clock frequency is 16 MHz.

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (S_{CLK}, S_{DATA}) are shown in Figure 15 and Table 19.



NOTE: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Figure 15. Two-wire Serial Bus Timing Parameters

Table 19. TWO-WIRE SERIAL BUS CHARACTERISTICS

(f_{EXTCLK} = 27 MHz; V_{AA} = V_{AA_PIX} = V_{DD_IO} = 2.8 V; V_{DDIO_PHY} = 1.8 V; V_{DD} = V_{DD_SLVS} = 1.2 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
S_{CLK} Clock Frequency	f_{SCL}	0	100	0	400	0	1000	kHz
S_{CLK} High		8*EXTCLK +SCLK rise time		8*EXTCLK +SCLK rise time		8*EXTCLK +SCLK rise time		µs
S_{CLK} Low	f_{SCL}	6*EXTCLK +SCLK rise time		6*EXTCLK +SCLK rise time		6*EXTCLK +SCLK rise time		µs
Hold Time (repeated) START Condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4	–	0.6	–	0.26	–	µs
LOW Period of the S_{CLK} Clock	t_{LOW}	4.7	–	1.2	–	0.5	–	µs
HIGH Period of the S_{CLK} Clock	t_{HIGH}	4	–	0.6	–	0.26	–	µs
Set-up Time for a Repeated START Condition	$t_{SU;STA}$	4.7	–	0.6	–	0.26	–	µs
Data Hold Time	$t_{HD;DAT}$	0 (Note 15)	3.45 (Note 16)	0 (Note 15)	0.9 (Note 16)	0	–	µs
Data Set-up Time	$t_{SU;DAT}$	250	–	100 (Note 17)	–	50	–	ns
Rise Time of both S_{DATA} and S_{CLK} Signals	t_r	–	1000	20 + 0.1 C_b (Note 18)	300	–	120	ns
Fall Time of both S_{DATA} and S_{CLK} Signals	t_f	–	300	20 + 0.1 C_b (Note 18)	300	–	120	ns
Set-up Time for STOP Condition	$t_{SU;STO}$	4	–	0.6	–	0.26	–	µs
Bus Free Time between a STOP and START Condition	t_{BUF}	4.7	–	1.3	–	0.5	–	µs
Capacitive Load for each Bus Line	C_b	–	400	–	400	–	500	pF
Serial Interface Input Pin Capacitance	C_{IN_SI}	–	3.3	–	3.3	–	3.3	pF

Table 19. TWO-WIRE SERIAL BUS CHARACTERISTICS (continued)
(f_{EXTCLK} = 27 MHz; V_{AA} = V_{AA}_PIX = V_{DD}_IO = 2.8 V; V_{DDIO}_PHY = 1.8 V; V_{DD} = V_{DD}_SLVS = 1.2 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
S_{DATA} Max Load Capacitance	C_{LOAD_SD}	–	30	–	30	–	30	pF
S_{DATA} Pull-up Resistor	R_{SD}	1.5	4.7	1.5	4.7	1.5	4.7	kΩ

12. This table is based on I^2C bus specification.
13. Two-wire control is I^2C-compatible.
14. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1 V_{DD} levels. Sensor EXCLK = 27 MHz.
15. A device must internally provide a hold time of at least 300 ns for the S_{DATA} signal to bridge the undefined region of the falling edge of S_{CLK}.
16. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the S_{CLK} signal.
17. A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the S_{CLK} signal. If such a device does stretch the LOW period of the S_{CLK} signal, it must output the next data bit to the S_{DATA} line t_r max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the S_{CLK} line is released.
18. C_b = total capacitance of one bus line in pF.
19. I^2C Signal voltage range for SDA/SCL should be either 1.8 V or 2.8 V with a margin of ±5%.

HiSPi Electrical Specifications

The ON Semiconductor AR0239AT sensor supports HiSPi SLVS mode. Please refer to the High-Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing information. The V_{DD}_SLVS supply in this datasheet corresponds to V_{DD}_TX in the HiSPi Physical Layer Specification. Similarly, V_{DD} is equivalent to V_{DD}_HiSPi as referenced in the specification. The DLL as implemented on AR0239AT is limited in the number of available delay steps and differs from the HiSPi specification as described in this section.

Table 20. CHANNEL SKEW
(Measurement Conditions: V_{DD}_HiSPi = 1.2 V; V_{DD}_HiSPi_TX = 0.4 V; Data Rate = 480 Mbps; DLL set to 0)

Parameter	Symbol	Value	Unit
Data Lane Skew in Reference to Clock	$t_{CHSKEW1PHY}$	−150	ps

MIPI Electrical Specifications

The ON Semiconductor AR0221 sensor supports four lanes of MIPI data. Compliant to MIPI standards:

- MIPI Alliance Standard for CSI−2 version 1.0
- MIPI Alliance Standard for D−PHY version 1.1

MIPI AC AND DC ELECTRICAL CHARACTERISTICS

Table 21. MIPI HIGH−SPEED TRANSMITTER DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{OD}	HS transmit differential voltage	140	–	270	mV
V_{CMTX}	HS transmit static common mode voltage	150	–	250	mV
ΔV_{OD}	V_{OD} mismatch when output is Differential−1 or Differential−0	–	–	14	mV
$\Delta V_{CMTX}(1,0)$	V_{CMTX} mismatch when output is Differential−1 or Differential−0	–	–	5	mV
V_{OHHS}	HS output HIGH voltage	–	–	360	mV
Z_{OS}	Single−ended output impedance	40	–	62.5	Ω
ΔZ_{OS}	Single−ended output impedance mismatch	–	–	10	%

Table 22. MIPI HIGH−SPEED TRANSMITTER AC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
	Data bit rate	–	–	600	Mb/s
Data Lane t_{rise}	20–80% rise time	100	–	500	ps
Data Lane t_{fall}	20–80% fall time	100	–	500	ps
Clock Lane t_{rise}	20–80% rise time	150	–	500	ps
Clock Lane t_{fall}	20–80% fall time	150	–	500	ps

Table 23. MIPI LOW−POWER TRANSMITTER DC CHARACTERISTICS

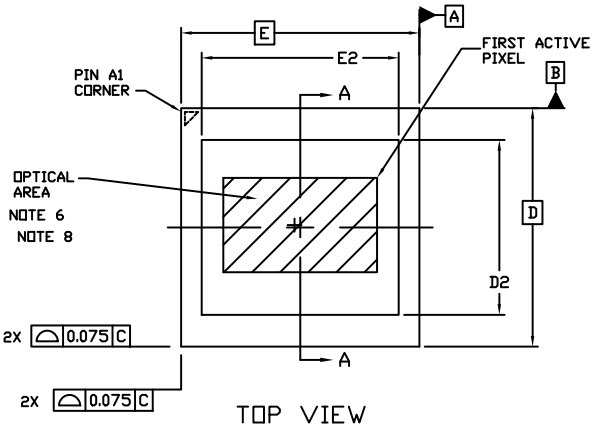
Symbol	Parameter	Min	Typ	Max	Unit
V_{OL}	Thevenin output low level	–	–	50	mV
V_{OH}	Thevenin output high level	1.1	1.15	1.3	V
Z_{OLP}	Output impedance of LP transmitter	110	–	–	

Table 24. MIPI LOW−POWER TRANSMITTER AC CHARACTERISTICS

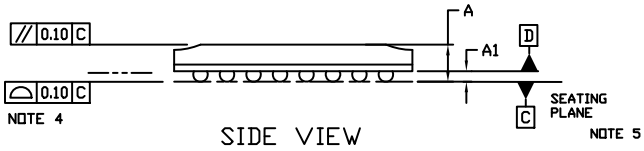
Symbol	Parameter	Min	Typ	Max	Unit
t_{rise}	15–85% rise time	–	–	25	ns
t_{fall}	15–85% fall time	–	–	25	ns
Slew	Slew rate (C_{LOAD} 5–20 pF)	–	–	250	mV/ns
Slew	Slew rate (C_{LOAD} 20–70 pF)	–	–	150	mV/ns

PACKAGE DIMENSIONS

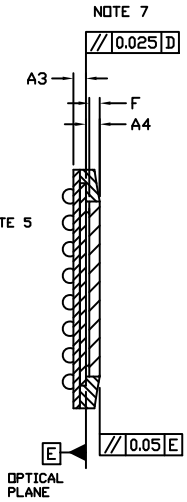
IBGA63 9x9
CASE 503BQ
ISSUE A



TOP VIEW



SIDE VIEW

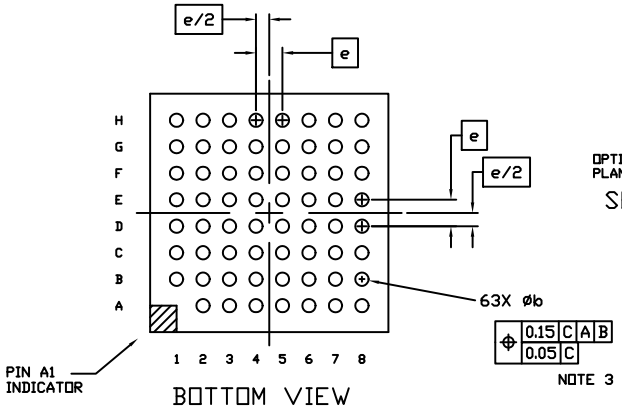


SECTION A-A

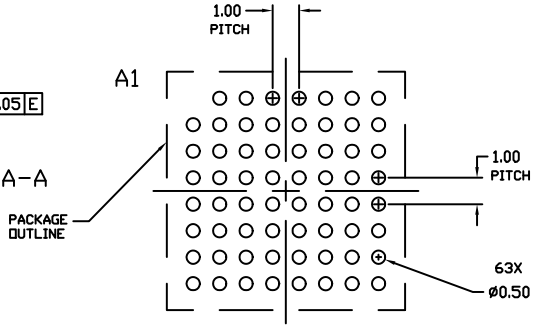
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. MAXIMUM ROTATION OF THE OPTICAL AREA RELATIVE TO D AND E WILL BE 1°. OPTICAL AREA IS DEFINED BY THE ACTIVE PIXEL ARRAY. REFER TO THE DEVICE DATASHEET FOR TOTAL ARRAY AND FIRST PIXEL DEFINITIONS.
7. PARALLELISM APPLIES ONLY TO THE OPTICAL AREA.
8. OPTICAL CENTER OFFSET WITH RESPECT TO THE PACKAGE CENTER IS X=−214.68 MICRONS, Y=86.83 MICRONS ±75 MICRONS.

	MILLIMETERS	
DIM	MIN.	MAX.
A	---	1.55
A1	0.35	0.45
A3	0.425	0.525
A4	0.475	0.575
b	0.45	0.55
D	9.00 BSC	
D2	6.50	6.70
E	9.00 BSC	
E2	7.30	7.50
e	1.00 BSC	
F	3.98	4.02



BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

9.. ENCAPSULANT: EPOXY
10.. SUBSTRATE MATERIAL: EPOXY LAMINANTE 0.25 THICKNESS
11.. LID MATERIAL: BOROSILICATE GLASS 0.4 THICKNESS
12.. SOLDER BALL MATERIAL: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu)
13.. SOLDER BALL PAD: ø0.4 SMD

PUBLICATION ORDERING INFORMATION

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