1/2-Inch CMOS Digital Image Sensor

Product Preview

AR0323AT

ON Semiconductor®

www.onsemi.com

General Description

ON Semiconductor AR0323AT is a 1/2−inch CMOS digital image sensor with a 2880 H x 1080 V active−pixel array. This advanced automotive sensor captures images in either linear, or high dynamic range, with rolling−shutter readout. AR0323AT is optimized for both low light and challenging high dynamic range scene performance, with a 3 μm Super−Exposure BSI pixel and more than 140 dB HDR capture capability on−chip. The sensor includes flexible functions such as in−pixel binning, windowing, and operates at up to 45 frames per second in full−resolution. The sophisticated sensor real time safety mechanism and fault detection features on AR0323AT enable ASIL−B compliance. The device is programmable through a simple two−wire serial interface, and supports MIPI CSI−2 output interfaces.

Table 1. KEY PARAMETERS

Parameter		Typical Value
Optical Format		1/2 inch (9.23 mm)
Active Pixels		2880 x 1080 = 3.1M
Pixel Size		3 μm
Color Filter Array		RCCB
CRA		17°
Shutter Type		Electronic rolling shutter
Input Clock Range		6 − 64 MHz
Output Pixel Rate Maximum		190 Mpixel/sec
Output	Serial	MIPI CSI−2 12−, 14−, 16−, 20−, or 24−bit
Frame Rate	Full Resolution	2880 x 1080 at up to 45 fps
Responsivity*	RCCB (Clear)	67 ke−/lux*sec
SNR_{MAX}		40 dB in Single Super Exposure mode
Maximum Dynamic Range		> 95 dB from single Super−Exposure > 120 dB in Dual−Exposure HDR+LFM Mode
Supply Voltage	I/O	1.8 or 2.8 V
	Digital	1.2 V
	Analog	2.8 V
	MIPI	1.2 V
Power Consumption (Typical)		480 mW (Full−Resolution, 45 fps, Dual−Exposure HDR+LFM Mode, 55°C junction temperature)
Operating Temperature		−40°C to +105°C (ambient) −40°C to +125°C (junction)
Package Options		13 × 11 mm iBGA

*D65, 670 nm IRCF

Features

- On−chip Combined HDR RAW Output, up to 24−bit (>140 dB) with companding down to 20, 16, 14, or 12−bit
- Support for Full−resolution 120 dB to 140 dB HDR+LFM
- New High−Performance 3 μm BSI Pixel with Super−Exposure HDR+LFM Mode
- Advanced HDR Image Combination with Flexible Exposure Ratio Control
- 2880 x 1080 at up to 45 fps
- Real−time Functional Safety Mechanisms and Fault Detection
- ASIL−B Safety Element Out of Context
- Data Interfaces: 4−lane MIPI CSI−2, Parallel
- Selectable Automatic or User Controlled Black Level Control
- Frame to Frame Switching to Enable Multi−function Systems
- Multi−Camera Synchronization Support
- This is a Pb−Free Device

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Applications

- Automotive Front Camera (ADAS)
- Mirror Replacement (CMS)
- ADAS + Viewing Fusion
- High Dynamic Range Imaging

ORDERING INFORMATION

Part number	Description	Orderable Product Attribute Description	Package
AR0323ATSB17XUEA0−DRBR−E	RCCB iBGA	Dry Pack without Protective Film Engineering Samples	iBGA 107 (Pb−Free)
AR0323ATSB17XUEA0−DPBR−E	RCCB iBGA	Dry Pack with Protective Film Engineering Samples	

NOTE: Contact the ON Semiconductor sales or marketing representative to discuss your specific requirements.

General Description

The ON Semiconductor AR0323AT can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 2880 x 1080 resolution image at 45 frames per second (fps) dual−exposure HDR+LFM using the Super−Exposure pixel. In high dynamic range mode, it outputs 12−bit, 14−bit, 16−bit, or 20−bit companded or up to 24−bit linearized data using the MIPI port. The device may be operated in video (master) mode or in single frame trigger mode.

FRAME_VALID, LINE_VALID and pixel clock can be programmed to output by GPIO pins in serial mode.

The AR0323AT includes additional features to allow application−specific tuning: windowing and offset, auto black level correction, and on−board temperature sensor. Optional register information and histogram statistic information can be embedded in first and last two lines of the image frame.

The sensor is designed to operate in a wide temperature range (−40°C to +125°C junction).

Functional Overview

The AR0323AT is a progressive−scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on−chip, phase−locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 64 MHz. The maximum output pixel rate is 190 Mp/s. Figure 1 shows a block diagram of the sensor.

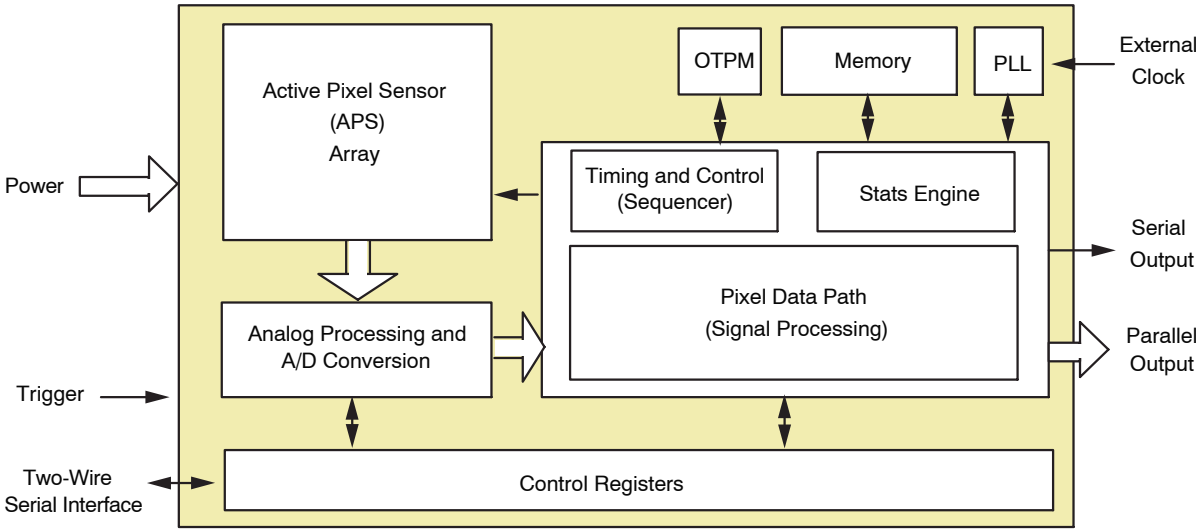


Figure 1. Block Diagram

User interaction with the sensor is through the two−wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 3.1 Mp BSI Active−Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog−to−digital converter (ADC). The output from the ADC is a 12−bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor also offers a high dynamic range mode of operation where multiple images are combined onchip to produce a single image at 24−bit per pixel value. A compressing mode is further offered to allow this 24−bit pixel value to be transmitted to the host system as a 12−, 14−, 16−, or 20−bit value with close to zero loss in image quality. The pixel data are output at a rate of up to 190 Mp/s.

Features Overview

The AR0323AT has a wide array of features to enhance functionality and to increase versatility. A summary of features follows. Please refer to the AR0323AT Developer Guide for detailed feature descriptions, register settings, and tuning guidelines and recommendations.

- Operating Modes
  The AR0323AT works in master (video), trigger (single frame), or Auto Trigger modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two−wire serial interface for both modes.
- Window Control
  Configurable window size and blanking times allow a wide range of resolutions and frame rates. Digital

binning and skipping modes are supported, as are vertical and horizontal mirror operations.

- Context Switching
  Context switching may be used to rapidly switch between two sets of register values. Refer to the AR0323AT Developer Guide for a complete set of context switchable registers.
- Gain
  The AR0323AT can be configured for digital gain of up to 2x.
- MIPI
  The AR0323 image sensor supports 4−lane MIPI CSI−2 D−PHY
- PLL
  An on chip PLL provides reference clock flexibility
- Reset
  The AR0323AT may be reset by a register write, or by a dedicated input pin.
- Output Enable
  The AR0323AT output pins may be tri−stated using dedicated register bits.
- Temperature Sensor
- Black Level Correction
- Row Noise Correction
- Digital Correlated Double Sampling (CDS)
- Test Patterns
  Several test patterns may be enabled for debug purposes. These include a solid color, color bar, fade to gray, and a walking 1s test pattern.

ASIL / ISO26262 Support Features

The AR0323AT incorporates many features assisting the achievement of ASIL−B system compliance by a system that integrates it. Please refer to the AR0323AT Safety Manual for more information.

PIXEL DATA FORMAT

Pixel Array Structure

The AR0323AT pixel array is configured as 2896 columns by 1088 rows (see Figure 2). The dark pixels are optically black and are used internally to monitor black level. There are 2896 columns by 1088 rows of optically active pixels. While the sensor's format is 2880 x 1080, the additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for RCCB or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out. The optical center of the readable active pixels can be found between X_ADDR 1439 and 1440, and between Y_ADDR 543 and 544.

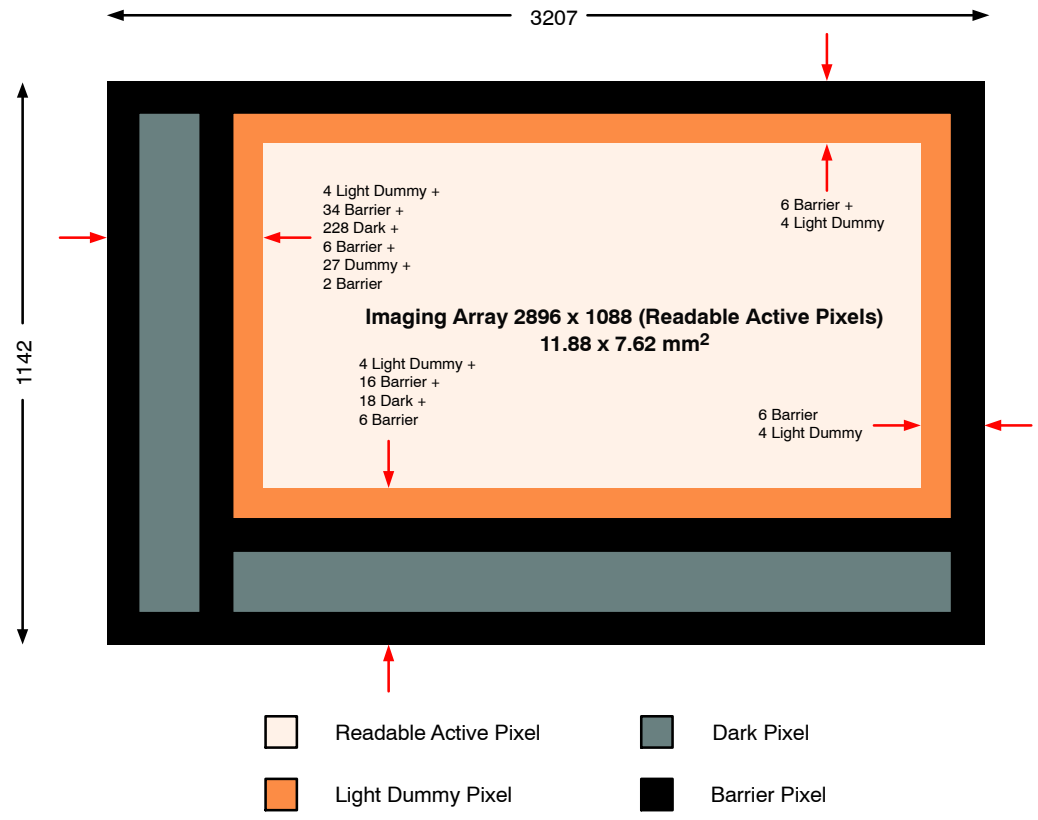


Figure 2. Pixel Array Description

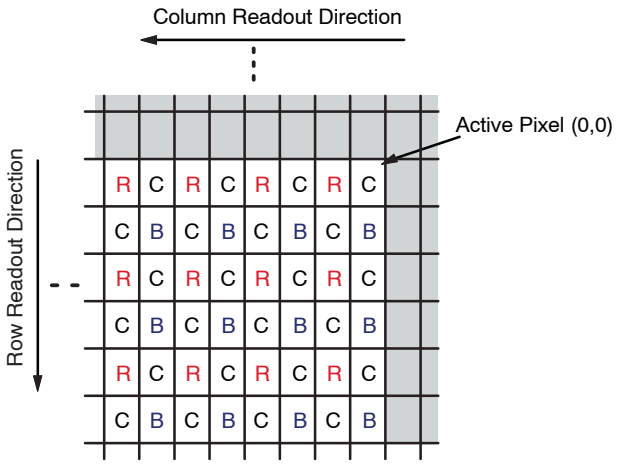


Figure 3. Pixel Color Pattern Detail (Top Right Corner) RCCB

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 3). This reflects the actual layout of the array on the die.

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 4. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 4.

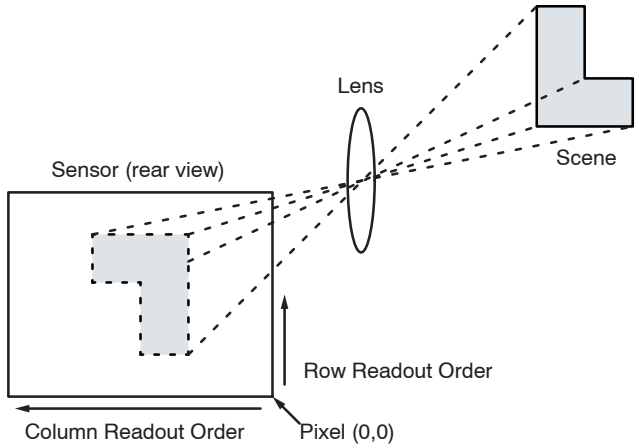
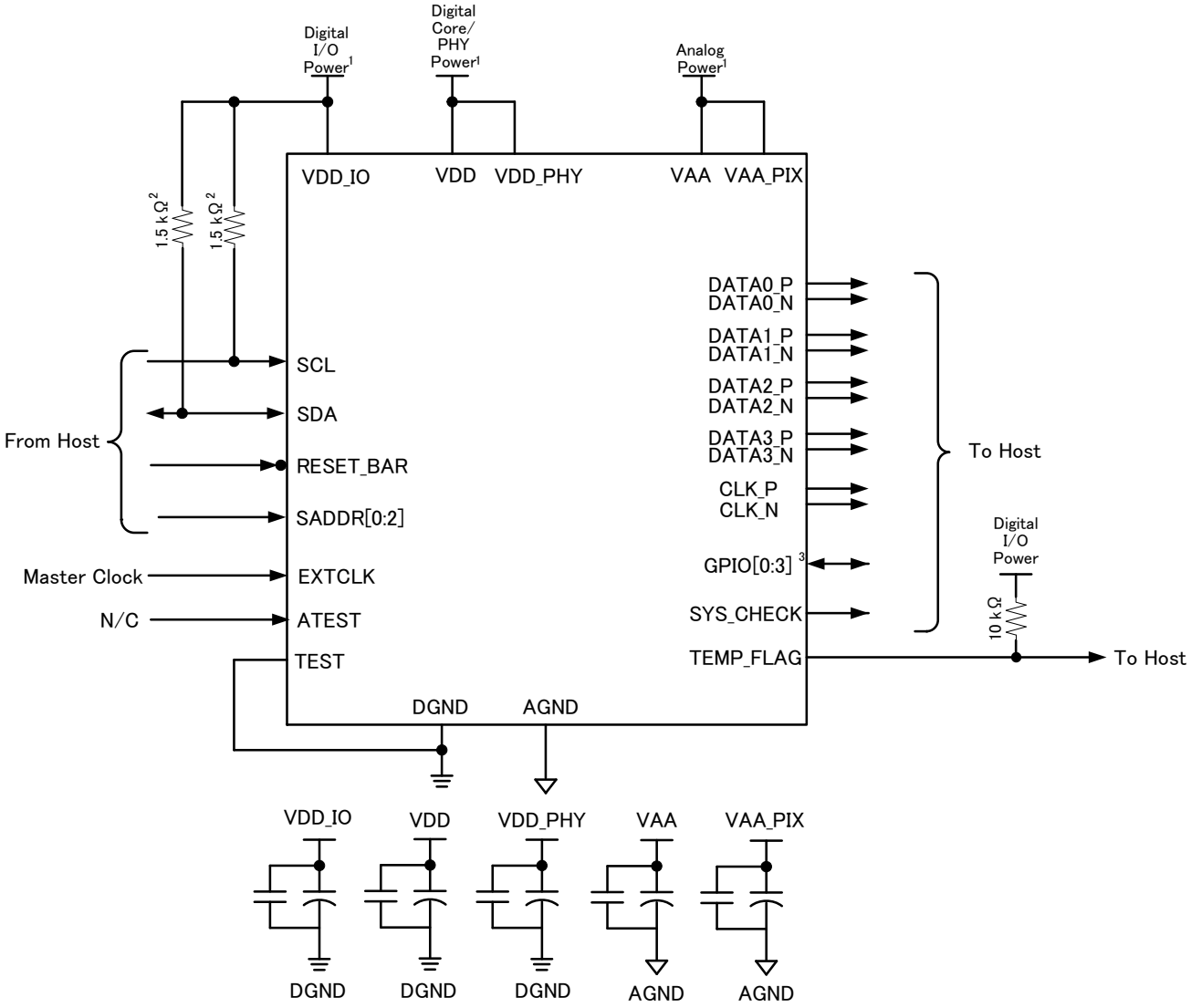


Figure 4. Imaging a Scene

CONFIGURATION AND PINOUT

The figures and tables below show a typical configuration for the AR0323 image sensor and show the package pinout.



NOTES:

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
3. With default GPIO configuration setting, GPIO[2:0] can be left unconnected if not used. It is recommended to tie GPIO3 to DGND if not used.
4. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0323AT demo headboard schematics for circuit recommendations.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match VDD_IO voltage to minimize any leakage currents.
7. V_{AA} and V_{AA}_PIX are independent on chip but should be tied together externally.

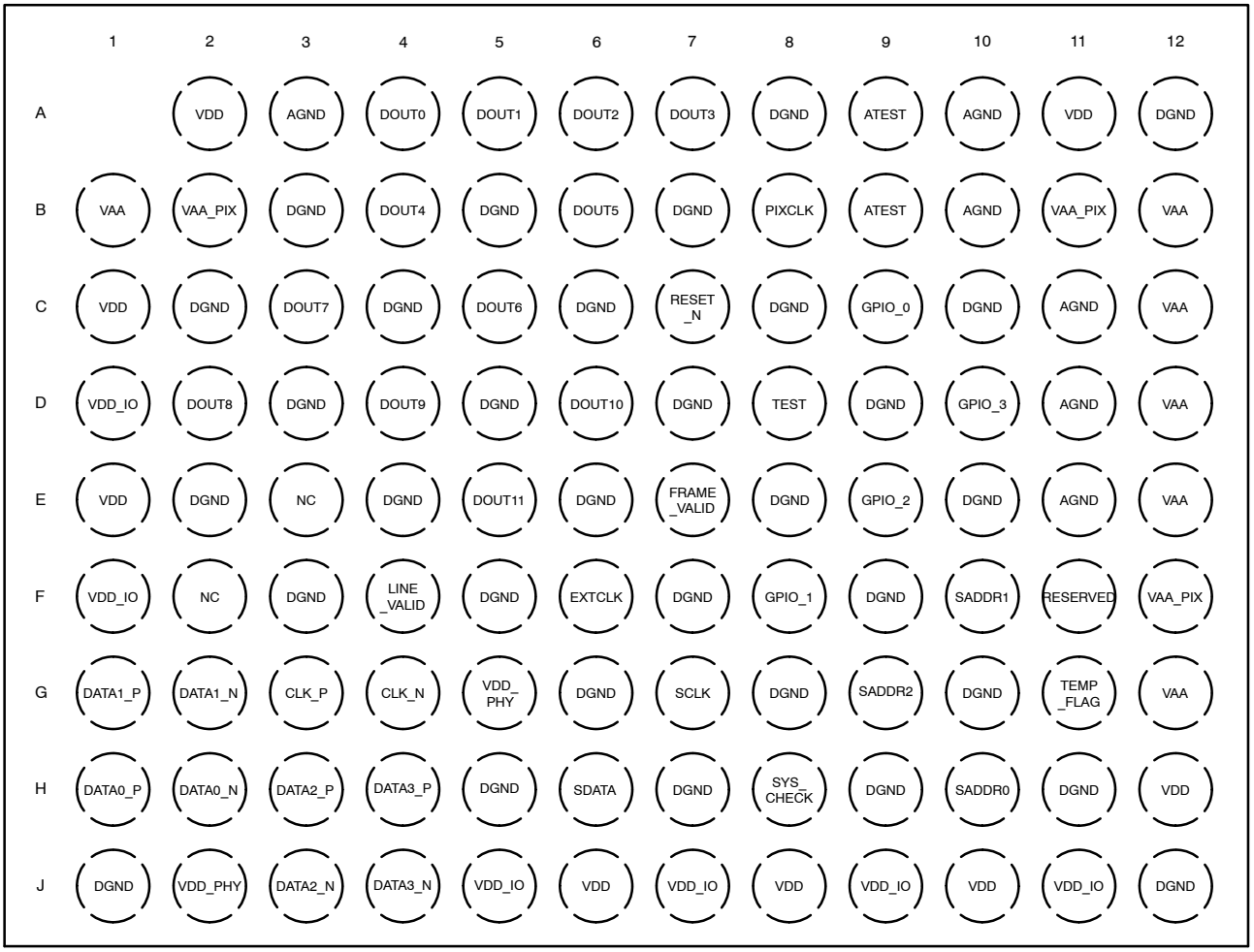
Figure 5. Typical Configuration, Four−Lane MIPI

Table 2. PIN DESCRIPTIONS, 11 x 13 mm, 107−BALL iBGA

Name	iBGA Pin	Type	Description
CLK_N	G4	Output	MIPI serial clock differential N
CLK_P	G3	Output	MIPI serial clock differential P
DATA0_N	H2	Output	MIPI serial data, lane 0, differential N
DATA0_P	H1	Output	MIPI serial data, lane 0, differential P
DATA1_N	G2	Output	MIPI serial data, lane 1, differential N
DATA1_P	G1	Output	MIPI serial data, lane 1, differential P
DATA2_N	J3	Output	MIPI serial data, lane 2, differential N
DATA2_P	H3	Output	MIPI serial data, lane 2, differential P
DATA3_N	J4	Output	MIPI serial data, lane 3, differential N
DATA3_P	H4	Output	MIPI serial data, lane 3, differential P
DOUT0	A4	Output	Parallel pixel data output (LSB)
DOUT1	A5	Output	Parallel pixel data output
DOUT2	A6	Output	Parallel pixel data output
DOUT3	A7	Output	Parallel pixel data output
DOUT4	B4	Output	Parallel pixel data output
DOUT5	B6	Output	Parallel pixel data output
DOUT6	C5	Output	Parallel pixel data output
DOUT7	C3	Output	Parallel pixel data output
DOUT8	D2	Output	Parallel pixel data output
DOUT9	D4	Output	Parallel pixel data output
DOUT10	D6	Output	Parallel pixel data output
DOUT11	E5	Output	Parallel pixel data output (MSB)
PIXCLK	B8	Output	Pixel clock out, DOUT is valid on rising edge of this clock
LINE_VALID	F4	Output	Asserted when DOUT line data is valid
FRAME_VALID	E7	Output	Asserted when DOUT frame data is valid
TEMP_FLAG	G11	Output	Temperature monitoring flag
SYS_CHECK	H8	Output	Active low error indicating signal
EXTCLK	F6	Input	External Input clock
RESET_BAR	C7	Input	Asynchronous reset (active LOW) all settings are restored to factory default
TEST	D8	Input	Manufacturing test enable pin (Tied to GND for normal operation)
SCLK	G7	Input	Two−Wire Serial clock input
SDATA	H6	I/O	Two−Wire Serial data I/O
SADDR0	H10	Input	Two−Wire Serial address select (LSB)
SADDR1	F10	Input	Two−Wire Serial address select
SADDR2	G9	Input	Two−Wire Serial address select (MSB)
GPIO_0	C9	I/O	General Purpose I/O
GPIO_1	F8	I/O	General Purpose I/O
GPIO_2	E9	I/O	General Purpose I/O
GPIO_3	D10	I/O	General Purpose I/O
VAA	B1, B12, C12, D12, E12, G12	Power	Analog power, 2.8 V nominal
VAA_PIX	B2, B11, F12	Power	Analog pixel array power, 2.8 V nominal
VDD_IO	D1, F1, J5, J7, J9, J11	Power	Digital I/O power, 1.8 V or 2.8 V nominal
VDD	A2, A11, C1, E1, H12, J6, J8, J10	Power	Core digital power, 1.2 V nominal

Table 2. PIN DESCRIPTIONS, 11 x 13 mm, 107−BALL iBGA (continued)

Name	iBGA Pin	Type	Description
VDD_PHY	J2, G5	Power	MIPI PHY I/O power, 1.2 V nominal
AGND	A3, A10, B10, C11, D11, E11	Power	Analog ground
DGND	A8, A12, B3, B5, B7, C2, C4, C6, C8, C10, D3, D5, D7, D9, E2, E4, E6, E8, E10, F3, F5, F7, F9, G6, G8, G10, H5, H7, H9, H11, J1, J12	Power	Digital ground
ATEST	A9, B9		Analog manufacturing test access, must be left floating for normal operation
RESERVED	F11, F2, E3		Left floating for normal operation



Top View
(Ball Down)

Figure 6. 13 x 11 mm 107−Ball iBGA Package

TWO−WIRE SERIAL REGISTER INTERFACE

The two−wire serial interface bus enables read/write access to control and status registers within the AR0323AT. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off−chip by a 1.5 kΩ resistor. Either the slave or master device can drive SDATA LOW − the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two−wire serial interface specification allow the slave device to drive SCLK LOW; the AR0323AT uses SCLK as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two−wire serial interface bus are performed by a sequence of low−level protocol elements:

8. A (repeated) start condition
9. A slave address/data direction byte
10. An (a no) acknowledge bit
11. A message byte
12. A stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH−to−LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a "repeated start" or "restart" condition.

Stop Condition

A stop condition is defined as a LOW−to−HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A "0" in bit [0] indicates a WRITE, and a "1" indicates a READ. The default slave addresses used by the AR0323AT are 0x20 (write address) and 0x21 (read address) in accordance with the specification. An additional 7 alternate slave address can be selected by enabling and asserting the SADDR [2:0] inputs.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No Acknowledge Bit

The no−acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a "0" indicates a write and a "1" indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which the WRITE should take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8−bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8−bit transfer. The slave's internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

Single READ from Random Location

This sequence (Figure 7) starts with a dummy WRITE to the 16−bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8−bit read slave

address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. Figure 7 shows how the internal register address maintained by the AR0323AT is loaded and incremented as the sequence proceeds.

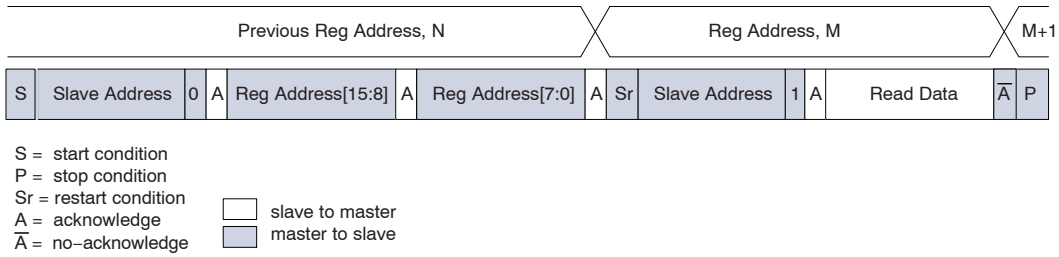


Figure 7. Single READ from Random Location

Single READ from Current Location

This sequence (Figure 8) performs a read using the current value of the AR0323AT internal register address. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

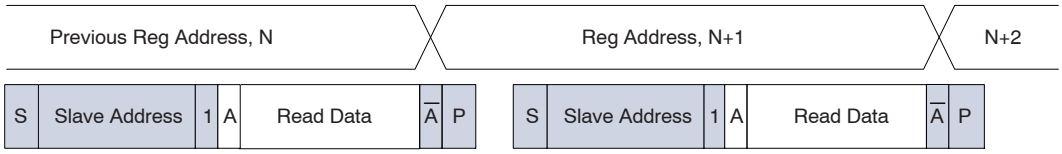


Figure 8. Single READ from Current Location

Sequential READ, Start from Random Location

This sequence (Figure 9) starts in the same way as the single READ from random location (Figure 7). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

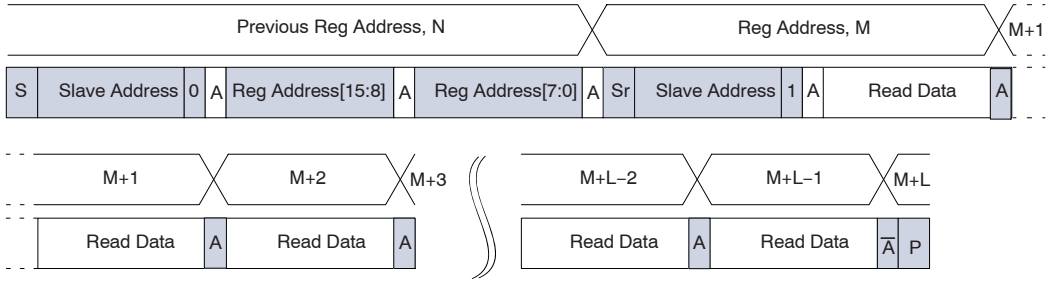


Figure 9. Sequential READ, Start from Random Location

Sequential READ, Start from Current Location

This sequence (Figure 10) starts in the same way as the single READ from current location (Figure 8). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

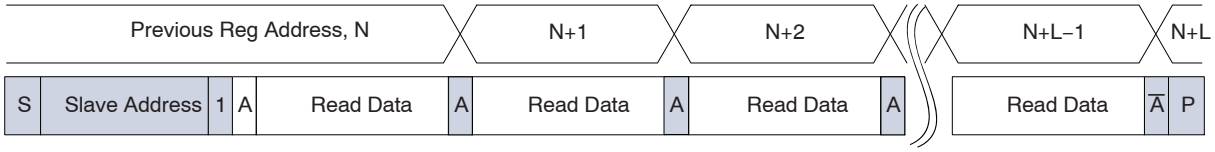


Figure 10. Sequential READ, Start from Current Location

Single WRITE to Random Location

This sequence (Figure 11) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

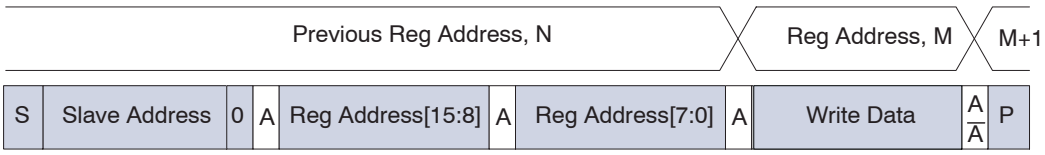


Figure 11. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 12) starts in the same way as the single WRITE to random location (Figure 11). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

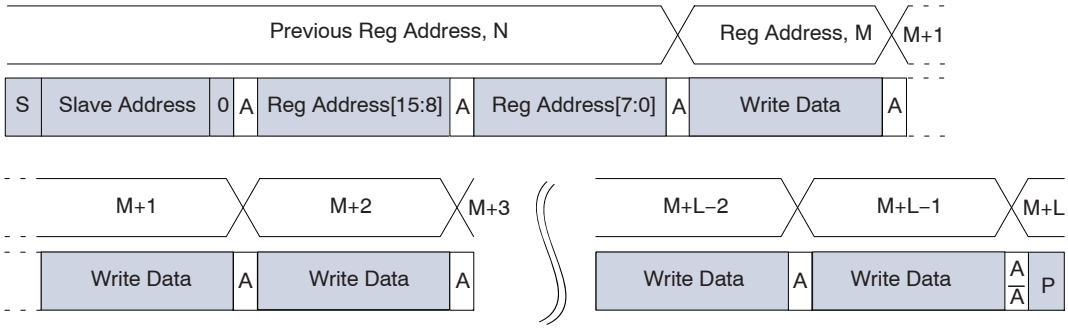
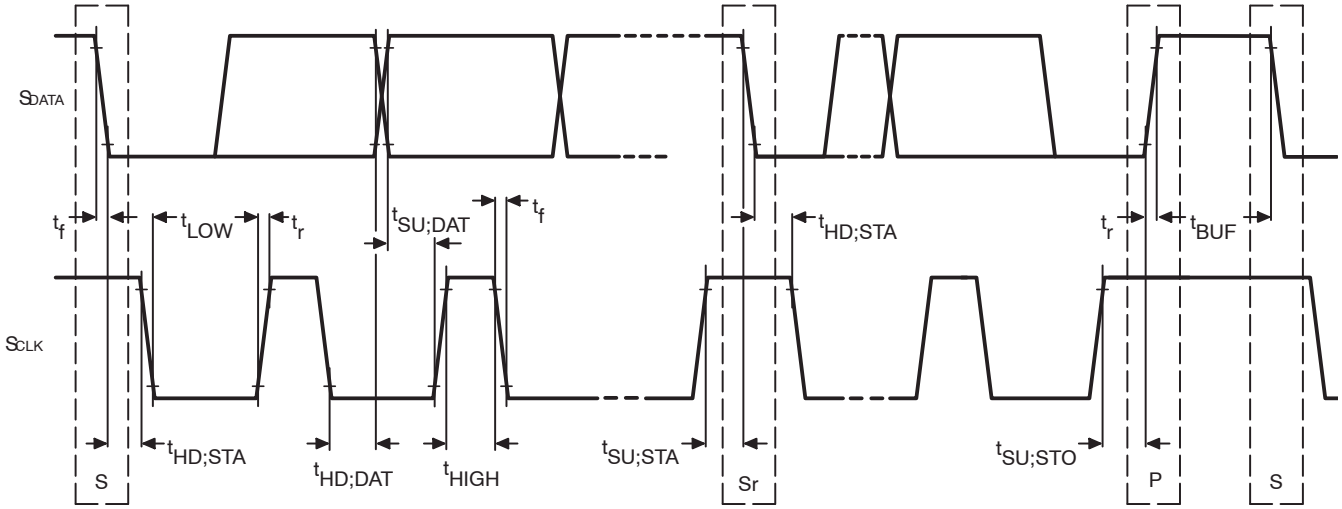


Figure 12. Sequential WRITE, Start at Random Location

ELECTRICAL SPECIFICATIONS

Two−Wire Serial Register Interface

The electrical characteristics of the two−wire serial register interface (SCLK, SDATA) are shown in Figure 13 and Table 3.



Note: Read sequence: For an 8−bit READ, read waveforms start after WRITE command and register address are issued.

Figure 13. Two−Wire Serial Bus Timing Parameters

Table 3. TWO−WIRE SERIAL BUS CHARACTERISTICS

(f_{EXTCLK} = 27 MHz; V_{DD} = V_{DD}_PHY = 1.2 V; V_{DD}_IO = V_{AA} = V_{AA}_PIX = 2.8 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
M_S_{CLK} Clock Frequency	f_{SCL}	0	100	0	400	0	1000	kHz
S_{CLK} High		8*EXTCLK + S_{CLK} rise time		8*EXTCLK + EXTCLK rise time				µs
S_{CLK} Low		6*EXTCLK + S_{CLK} rise time		6*EXTCLK + S_{CLK} rise time				µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4	–	0.6	–	0.26	–	µs
LOW period of the M_S_{CLK} clock	t_{LOW}	4.7	–	1.2	–	0.5	–	µs
HIGH period of the M_S_{CLK} clock	t_{HIGH}	4	–	0.6	–	0.26	–	µs
Set−up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	0.26	–	µs
Data hold time	$t_{HD;DAT}$	0	3.453	0	0.93	0	–	µs
Data set−up time	$t_{SU;DAT}$	250	–	100	–	50	–	ns
Rise time of both M_S_{DATA} and M_S_{CLK} time (10−90%)	t_r	–	1000	20 + 0.1 Cb (Note 4)	300	20 + 0.1 Cb (Note 4)	120	ns
Fall time of both M_S_{DATA} and M_S_{CLK} time (10−90%)	t_f	–	300	20 + 0.1 Cb (Note 4)	300	20 + 0.1 Cb (Note 4)	120	ns
Set−up time for STOP condition	$t_{SU;STO}$	4	–	0.6	–	0.26	–	µs

Table 3. TWO−WIRE SERIAL BUS CHARACTERISTICS

(f_{EXTCLK} = 27 MHz; V_{DD} = V_{DD}_PHY = 1.2 V; V_{DD}_IO = V_{AA} = V_{AA}_PIX = 2.8 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	0.5	–	μs
Capacitive load for each bus line	Cb	–	400	–	400	–	500	pF
Serial interface input pin capacitance	C_{IN_SI}	–	3.3	–	3.3	–	3.3	pF
M_S_{DATA} max load capacitance	C_{LOAD_SD}	–	30	–	30	–	30	pF
M_S_{DATA} pull−up resistor	R_{SD}	1.5	4.7	1.5	4.7	1.5	4.7	kΩ

1. This table is based on I^2C standard (v2.1 January 2000). Philips Semiconductor.
2. Two−wire control is I^2C compatible.
3. All values referred to V_{IHmin} = 0.9 V_{DD_IO} and V_{ILmax} = 0.1 V_{DD_IO} levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of S_{CLK}. The two−wire standard specifies a minimum rise and fall time for Fast−Mode and Fast−Mode Plus modes of operation. This specification is not a timing requirement that is enforced on ON Semiconductor sensor's as a receiver, because our receivers are designed to work in mixed systems with std−mode where no such minimum rise and fall times are required/specified. However, it's the host's responsibility when using fast edge rates, especially when two−wire slew−rate driver control isn't available, to manage the generated EMI, and the potential voltage undershoot on the sensor receiver circuitry, to avoid activating sensor ESD diodes and current−clamping circuits. This is typically not an issue in most applications, but should be checked if below minimum fall times and rise times are required.
5. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the S_{CLK} signal.
6. A Fast−mode I^2C−bus device can be used in a Standard−mode I^2C−bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the S_{CLK} signal. If such a device does stretch the LOW period of the S_{CLK} signal, it must output the next data bit to the S_{DATA} line t_r max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard−mode I^2C−bus specification) before the S_{CLK} line is released.
7. Cb = total capacitance of one bus line in pF.
8. Fast Mode Plus operation is not supported with an EXTCLK frequency less than 16 MHz.

Table 4. TWO−WIRE SERIAL REGISTER INTERFACE ELECTRICAL CHARACTERISTICS

(f_{EXTCLK} = 27 MHz; V_{DD} = V_{DD}_PHY = 1.2 V; V_{DD}_IO = V_{AA} = V_{AA}_PIX = 2.8 V; T_A = 25°C)

Parameter	Symbol	Condition	Standard Mode		Fast Mode		Fast Mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
Input HIGH Voltage	V_{IH}		0.7 * V_{DDIO}	–	0.7 * V_{DDIO}	–	0.7 * V_{DDIO}	–	V
Input LOW Voltage	V_{IL}		–	0.3 * V_{DDIO}	–	0.3 * V_{DDIO}	–	0.3 * V_{DDIO}	V
Output LOW Voltage	V_{OL}	V_{DDIO} = (1.7 V – 1.9 V) I_{OL} = 3 mA	–	0.4	–	0.4	–	0.4	V
Output LOW Voltage	V_{OL}	V_{DDIO} = (2.66 V – 2.94 V) I_{OL} = 3 mA	–	0.2 * V_{DDIO}	–	0.2 * V_{DDIO}	–	0.2 * V_{DDIO}	V

I/O Timing

By default, the AR0323AT launches pixel data, FV, and LV with the falling edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV, and LV using the rising edge of PIXCLK. This can be changed using register R0x3028.

See Figure 14 and Table 15 for I/O timing (AC) characteristics.

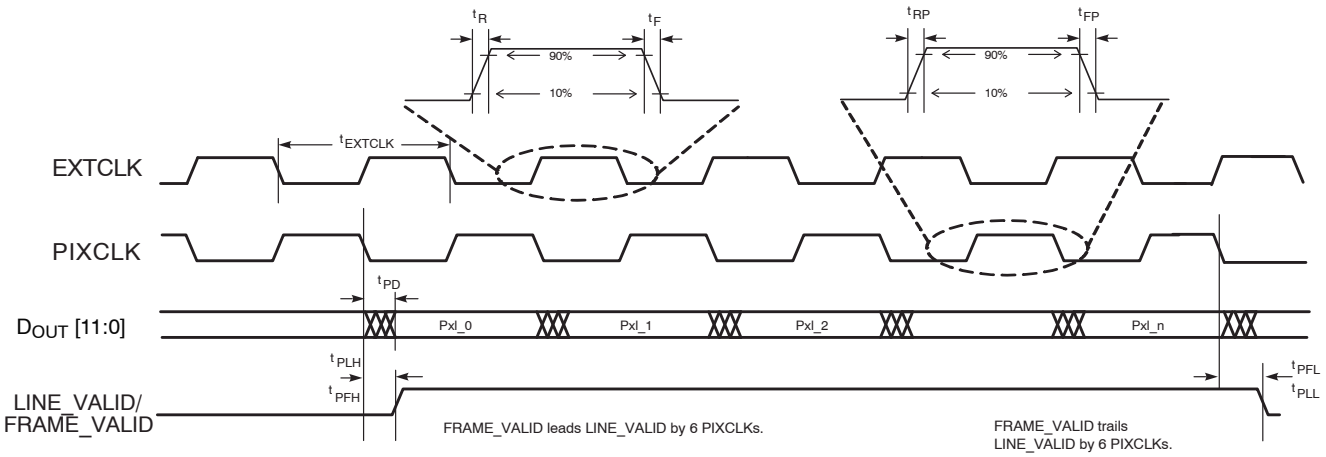


Figure 14. I/O Timing Diagram

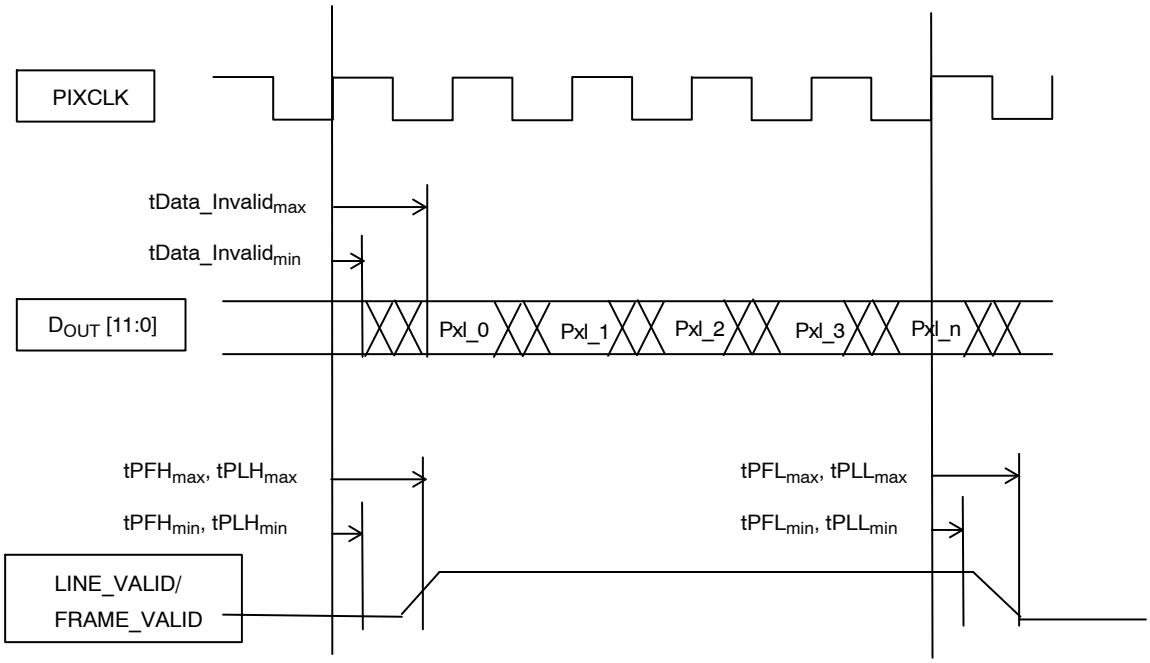


Figure 15. I/O Timing Diagram Detail

Table 5. I/O TIMING CHARACTERISTICS (2.8 V V_{DD}_IO) (Note 9)

Symol	Definition	Condition	VDD_IO = 2.8 V [1]			Units
			Min	Typ	Max	
f_{EXTCLK}1	Input clock frequency	PLL Enabled	6	–	64	MHz
t_{EXTCLK}1	Input clock period	PLL Enabled	15.63	–	166	ns
t_R	Input clock rise time		–	3	–	ns
t_F	Input clock fall time		–	3	–	ns
t_{JITTER}	Input clock jitter		–	1	–	ns
t_{RP}	Pixclk rise time	PIXCLK slew rate = 7		2.0		ns
t_{FP}	Pixclk fall time	PIXCLK slew rate = 7		2.0		ns
f_{PIXCLK}	PIXCLK frequency	PIXCLK slew rate = 7 Data slew rate = 7	6	–	140	MHz
t_{PD}	PIXCLK to data valid	PIXCLK slew rate = 7 Data slew rate = 7	2.0	–	7.8	ns
t_{PFH}	PIXCLK to FV HIGH Transition	PIXCLK slew rate = 7 Data slew rate = 7	2.0	–	7.8	ns
t_{PLH}	PIXCLK to LV HIGH Transition	PIXCLK slew rate = 7 Data slew rate = 7	2.0	–	7.8	ns
t_{PFL}	PIXCLK to FV LOW Transition	PIXCLK slew rate = 7 Data slew rate = 7	2.0	–	7.8	ns
t_{PLL}	PIXCLK to LV LOW Transition	PIXCLK slew rate = 7 Data slew rate = 7	2.0	–	7.8	ns
CIN	Input pin capacitance		–	2.5 pf	–	pf

9. Minimum and maximum values are taken at 105°C, 2.5 V, and −40°C, 3.1 V. All values are taken at the 50% transition point. The loading used is 20 pF.

Table 6. I/O TIMING CHARACTERISTICS (1.8 V V_{DD}_IO) (Note 10)

Symol	Definition	Condition	VDD_IO = 1.8 V [1]			Units
			Min	Typ	Max	
f_{EXTCLK}1	Input clock frequency	PLL Enabled	6	–	64	MHz
t_{EXTCLK}1	Input clock period	PLL Enabled	15.6	–	166	ns
t_R	Input clock rise time		–	3	–	ns
t_F	Input clock fall time		–	3	–	ns
t_{JITTER}	Input clock jitter		–	1	–	ns
t_{RP}	Pixclk rise time	PIXCLK slew rate = 7		1.3		ns
t_{FP}	Pixclk fall time	PIXCLK slew rate = 7		1.3		ns
f_{PIXCLK}	PIXCLK frequency	PIXCLK slew rate = 7 Data slew rate = 7	6	–	140	MHz
t_{PD}	PIXCLK to data valid	PIXCLK slew rate = 7 Data slew rate = 7	2.0	–	7.8	ns
t_{PFH}	PIXCLK to FV HIGH Transition	PIXCLK slew rate = 7 Data slew rate = 7	2.0	–	7.8	ns
t_{PLH}	PIXCLK to LV HIGH Transition	PIXCLK slew rate = 7 Data slew rate = 7	2.0	–	7.8	ns
t_{PFL}	PIXCLK to FV LOW Transition	PIXCLK slew rate = 7 Data slew rate = 7	2.0	–	7.8	ns
t_{PLL}	PIXCLK to LV LOW Transition	PIXCLK slew rate = 7 Data slew rate = 7	2.0	–	7.8	ns
CIN	Input pin capacitance		–	2.5 pf	–	pf

10. Minimum and maximum values are taken at 105°C, 1.7 V, and −40°C, 1.95 V. All values are taken at the 50% transition point. The loading used is 20 pF.

Table 7. I/O RISE SLEW RATE (2.8 V V_{DD}_IO) (Note 11)

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	–	2.00	–	V/ns
6	Default	–	1.80	–	V/ns
5	Default	–	1.50	–	V/ns
4	Default	–	1.30	–	V/ns
3	Default	–	1.10	–	V/ns
2	Default	–	0.90	–	V/ns
1	Default	–	0.70	–	V/ns
0	Default	–	0.50	–	V/ns

11. Minimum and maximum values are taken at 105°C, 2.5 V, and −40°C, 3.1 V. The loading used is 20 pF.

Table 8. I/O FALL SLEW RATE (2.8 V V_{DD}_IO) (Note 12)

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	–	2.00	–	V/ns
6	Default	–	1.80	–	V/ns
5	Default	–	1.50	–	V/ns
4	Default	–	1.30	–	V/ns
3	Default	–	1.10	–	V/ns
2	Default	–	0.90	–	V/ns
1	Default	–	0.70	–	V/ns
0	Default	–	0.50	–	V/ns

12. Minimum and maximum values are taken at 105°C, 2.5 V, and −40°C, 3.1 V. The loading used is 20 pF.

Table 9. I/O RISE SLEW RATE (1.8 V V_{DD}_IO) (Note 13)

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	–	1.32	–	V/ns
6	Default	–	1.23	–	V/ns
5	Default	–	1.13	–	V/ns
4	Default	–	1.02	–	V/ns
3	Default	–	0.89	–	V/ns
2	Default	–	0.75	–	V/ns
1	Default	–	0.58	–	V/ns
0	Default	–	0.38	–	V/ns

13. Minimum and maximum values are taken at 105°C, 1.7 V, and −40°C, 1.95 V. The loading used is 20 pF.

Table 10. I/O FALL SLEW RATE (1.8 V V_{DD}_IO) (Note 14)

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	–	1.32	–	V/ns
6	Default	–	1.23	–	V/ns
5	Default	–	1.13	–	V/ns
4	Default	–	1.02	–	V/ns
3	Default	–	0.89	–	V/ns
2	Default	–	0.75	–	V/ns
1	Default	–	0.58	–	V/ns
0	Default	–	0.38	–	V/ns

14. Minimum and maximum values are taken at 105°C, 1.7 V, and −40°C, 1.95 V. The loading used is 20 pF.

Table 11. DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Units
V_{DD}	Core digital voltage		1.14	1.2	1.26	V
V_{DD}_IO	I/O digital voltage		1.7/2.66	1.8/2.8	1.9/2.94	V
V_{AA}	Analog voltage		2.66	2.8	2.94	V
V_{AA}_PIX	Pixel supply voltage		2.66	2.8	2.94	V
V_{DD}_PHY	PHY digital voltage		1.14	1.2	1.26	V
V_{IH}	Input HIGH voltage		V_{DD}_IO * 0.7	–	–	V
V_{IL}	Input LOW voltage		–	–	V_{DD}_IO * 0.3	V
I_{IN}	Input leakage current	No pull−up resistor; V_{IN} = V_{DD}_IO or D_{GND}	–	–	40	μA
V_{OH}	Output HIGH voltage		V_{DD}_IO − 0.4	–	–	V
V_{OL}	Output LOW voltage		–	–	0.4	V
I_{OH}	Output HIGH current	At specified V_{OH}	21	–	–	mA
I_{OL}	Output LOW current	At specified V_{OL}	–	–	24	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 12. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Minimum	Maximum	Units
V_{SUPPLY_2V8}	Power supply voltage 2V8	−0.3	3.5	V
V_{SUPPLY_1V8}	Power supply voltage 1V8	−0.3	2.6	V
V_{SUPPLY_1V2}	Power supply voltage 1V2	−0.3	1.7	V
I_{SUPPLY_2V8}	Power supply current 2V8	–	274	mA
I_{SUPPLY_1V8}	Power supply current 1V8	–	2	mA
I_{SUPPLY_1V2}	Power supply current 1V2	–	546	mA
I_{GND}	Total ground current	–	822	mA
V_{IN}	DC input voltage	−0.3	V_{DD}_IO + 0.3	V
V_{OUT}	DC output voltage	−0.3	V_{DD}_IO + 0.3	V
T_{STG} (Note 1)	Storage temperature	−40	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

15. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
16. To keep dark current and shot noise artifacts from impacting image quality, keep operating temperature at a minimum.

Table 13. OPERATING CURRENTS IN 4−LANE MIPI OUTPUT AND DUAL−EXPOSURE HDR+LFM MODE

Definition	Condition	Symbol	Min	Typ	Max	Unit
Digital operating current	Streaming, 2880 x 1080, 45 fps	I_{DD}	−	170	250	mA
I/O digital operating current	Streaming, 2880 x 1080, 45 fps	I_{DD_IO}	−	1.5	3	mA
Analog operating current	Streaming, 2880 x 1080, 45 fps	I_{AA}	−	80	130	mA
Pixel supply current	Streaming, 2880 x 1080, 45 fps	I_{AA_PIX}	−	13	30	mA

1. V_{AA} = V_{AA_PIX} = V_{DD_IO} = 2.8 V
   V_{DD} = V_{DD_PHY} = 1.2 V
   PLL Enabled and PIXCLK = 140 MHz
   T_A = 55°C

Table 14. STANDBY CURRENT CONSUMPTION

Definition	Condition	Symbol	Min	Typ	Max	Unit
Hard standby (clock off)	Analog, 2.8 V		−	0.34	0.6	mA
	Digital, 1.2 V		−	2.8	8	mA
	I/O, 1.8 V		−	0.13	0.3	mA
Hard standby (clock on)	Analog, 2.8 V		−	0.34	0.6	mA
	Digital, 1.2 V		−	3.2	8	mA
	I/O, 1.8 V		−	19.09	23.1	mA
Soft standby (clock off)	Analog, 2.8 V		−	0.32	0.6	mA
	Digital, 1.2 V		−	2.8	8	mA
	I/O, 1.8 V		−	0.47	0.72	mA
Soft standby (clock on)	Analog, 2.8 V		−	0.32	0.62	mA
	Digital, 1.2 V		−	27.8	36	mA
	I/O, 1.8 V		−	0.57	0.77	mA

2. Analog is V_{AA} + V_{AA_PIX}
   Digital is V_{DD} + V_{DD_PHY}
   I/O is V_{DD_IO}
   T_A = 55°C

MIPI Electrical Specifications

The ON Semiconductor AR0323AT sensor supports four lanes of MIPI data.

Compliant to MIPI standards:

- MIPI Alliance Standard for CSI−2 version 1.2
- MIPI Alliance Standard for D−PHY version 1.2

MIPI AC and DC Electrical Characteristics

Table 15. MIPI HIGH−SPEED TRANSMITTER DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{OD}	HS transmit differential voltage	140	–	270	mV
V_{CMTX}	HS transmit static common mode voltage	150	–	250	mV
ΔV_{OD}	V_{OD} mismatch when output is Differential−1 or Differential−0	–	–	14	mV
$\Delta V_{CMTX}(1,0)$	V_{CMTX} mismatch when output is Differential−1 or Differential−0	–	–	5	mV
V_{OHHS}	HS output HIGH voltage	–	–	360	mV
Z_{OS}	Single−ended output impedance	40	–	62.5	Ω
ΔZ_{OS}	Single−ended output impedance mismatch	–	–	10	%

Table 16. MIPI HIGH−SPEED TRANSMITTER AC CHARACTERISTICS 4 LANE

Symbol	Parameter	Min	Typ	Max	Unit
	Data bit rate (4 lane configuration)	–	–	1500	Mbps/lane
Data Lane t_{rise}	20–80% rise time	93.5	–	103	ps
Data Lane t_{fall}	20–80% fall time	107.5	–	117	ps
Clock Lane t_{rise}	20–80% rise time	93.5	–	103	ps
Clock Lane t_{fall}	20–80% fall time	107.5	–	117	ps

3. Simulation result run with 2.75 nH, 2.75 pF, 100 Ω termination.

Table 17. MIPI LOW−POWER TRANSMITTER AC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
t_{rise}	15–85% rise time	–	–	25	ns
t_{fall}	15–85% fall time	–	–	25	ns
Slew	Slew rate (C_{LOAD} 5–20 pF)	–	–	250	mV/ns
Slew	Slew rate (C_{LOAD} 20–70 pF)	–	–	150	mV/ns

Power Up/Down Timing

Power Up

There is no limitation to the order in which the power supplies are applied. However, the following sequence of events is recommended.

1. Turn on VAA, and VAA_PIX power supply.
2. After 100 μs, turn on VDD_IO power supply.
3. After 100 μs, turn on VDD and VDD_PHY power supply.
4. After the last power supply is stable, enable EXTCLK.
5. Assert RESET_BAR for at least 1 ms. The parallel interface will be tri−stated during this time.
6. Wait for 250000 clock cycles for power on self test finished.
7. Set streaming mode (mode_select/stream (R0x301A[2]) = 1) and the internal PLL would be enabled (not locked yet).
8. Wait for 1 ms for PLL lock to complete. Part will then go into streaming mode.

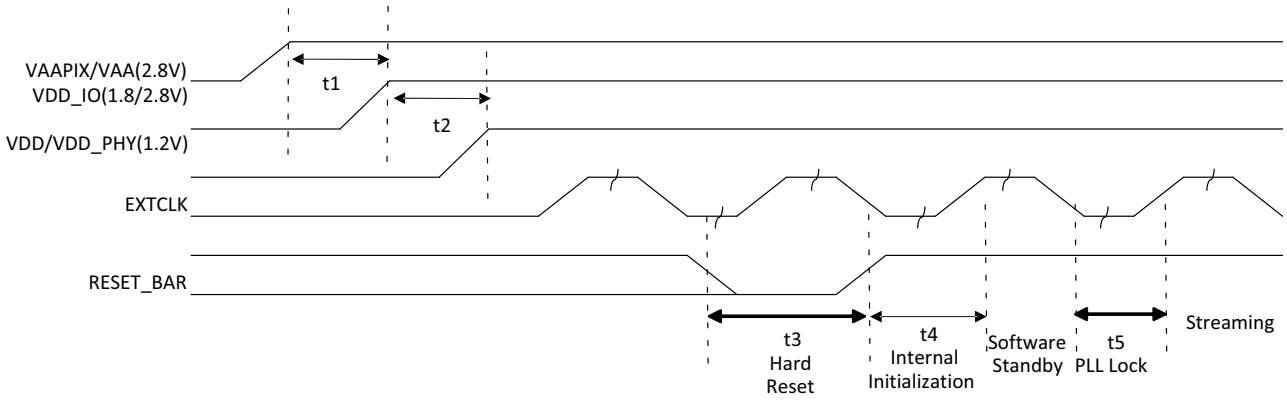


Figure 16. Initial Power Up Sequence

Table 18. POWER UP SEQUENCE

Definition	Symbol	Min	Typ	Max	Unit
VAA/VAA_pix to VDD_IO	t1	0	100	–	μs
VDD_IO to VDD	t2	0	100	–	μs
Hard Reset	t3	30	–	–	EXTCLK cycles
Internal Initialization	t4	–	–	250000	EXTCLK cycles
PLL Lock Time	t5	–	–	1	ms

Power Down

The following sequence of events is recommended.

1. [Optional] Disable streaming if output is active by setting standby R0x301A[2] = 0.
2. [Optional] Wait for soft standby state to be reached, occurs after the current row or frame, depending on configuration, has ended.
3. Turn off VDD/VDD_PHY
4. Turn off VDD_IO
5. Turn off VAA, VAA_PIX

By following the “OPTIONAL” steps, data output will end on a row or frame boundary.

The AR0323 will require at least 100 ms before it can be powered on again.

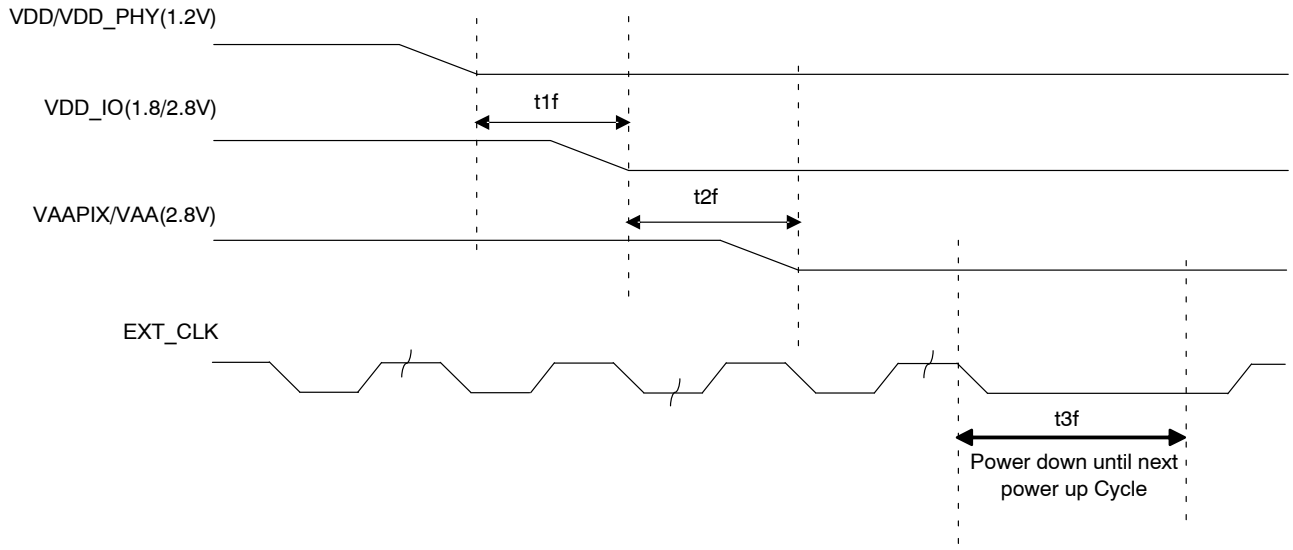


Figure 17. Power Down Sequence

Table 19. POWER DOWN SEQUENCE

Definition	Symbol	Min	Typ	Max	Unit
VDD/VDD_PHY to VDD_IO	t1f	0	–	–	
VDD_IO to VAA/VAA_PIX	t2f	0	–	–	
PwrDn until Next PwrUp Time	t3f	100	–	–	ms

CRA vs. Image Height Plot

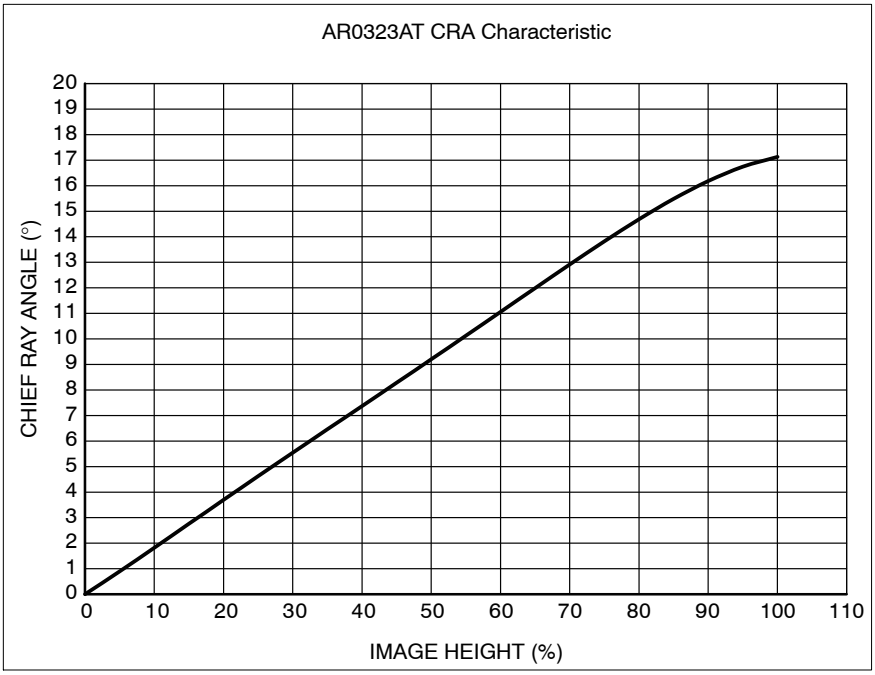
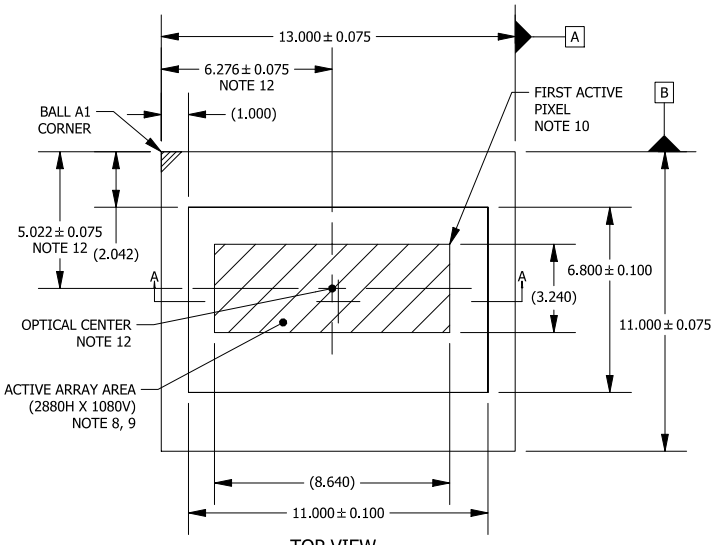


Figure 18. Chief Ray Angle – 17°

Image Height		CRA
(%)	(mm)	(deg)
0	0	0
5	0.231	0.89
10	0.461	1.82
15	0.692	2.76
20	0.923	3.69
25	1.153	4.62
30	1.384	5.54
35	1.615	6.46
40	1.846	7.37
45	2.076	8.28
50	2.307	9.20
55	2.538	10.12
60	2.768	11.05
65	2.999	11.99
70	3.230	12.91
75	3.460	13.82
80	3.691	14.68
85	3.922	15.48
90	4.152	16.18
95	4.383	16.74
100	4.614	17.13

IBGA107, 13x11
CASE 503CG
ISSUE A

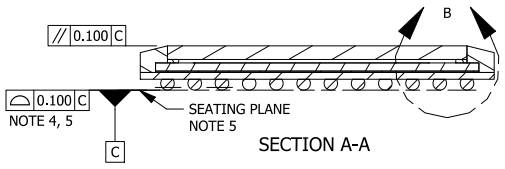
DATE 13 SEP 2019



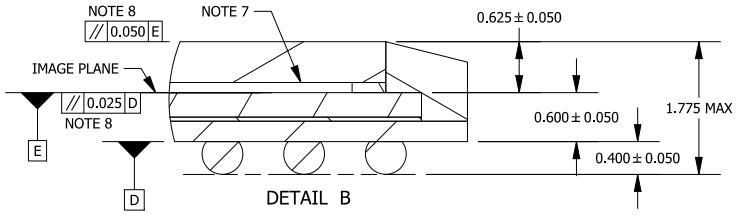
TOP VIEW

NOTES:

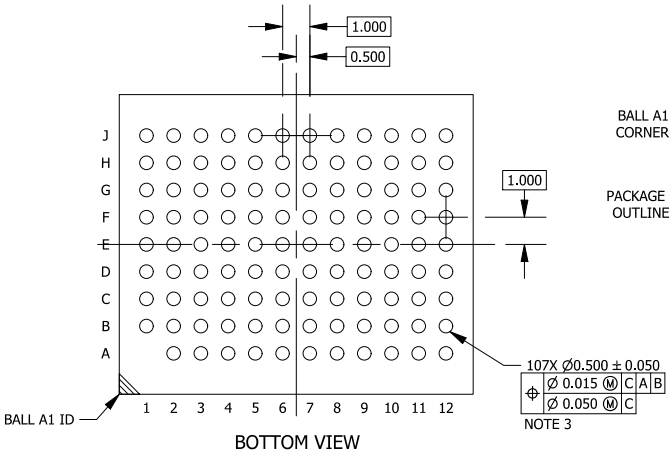
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS [mm].
3. SOLDER BALL DIAMETER IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. GLASS: 0.500 THICKNESS; REFRACTIVE INDEX = 1.52; AR COATING R<1% 420-850nm (EACH SIDE).
7. AIR GAP BETWEEN GLASS AND PIXEL ARRAY: 0.125 THICKNESS.
8. PARALLELISM APPLIES ONLY TO THE ACTIVE ARRAY.
9. MAXIMUM ROTATION OF ACTIVE ARRAY RELATIVE TO DATUMS A AND B IS ± 0.7°.
10. REFER TO THE DEVICE DATA SHEET FOR TOTAL PIXEL ARRAY DEFINITIONS.
11. PACKAGE CENTER (X, Y) = (0.000, 0.000).
12. OPTICAL CENTER RELATIVE TO PACKAGE CENTER (X, Y) = (-0.224, 0.478).



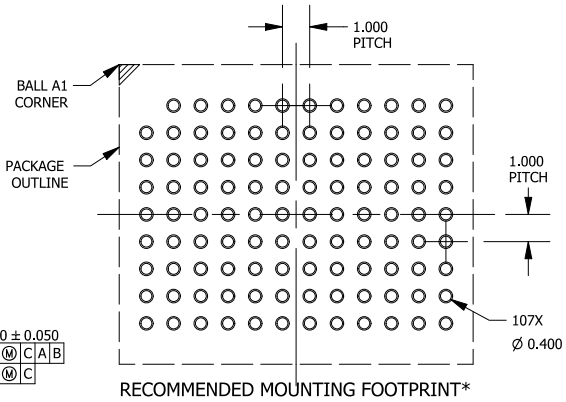
SECTION A-A



DETAIL B



BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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