# AR0833-DIE

# 1/3.2-Inch 8 Mp CMOS Digital Image Sensor Die

The AR0833 from ON Semiconductor is a 1/3.2-inch BSI (back side illuminated) CMOS active-pixel digital image sensor with a pixel array of 3,264 (H) × 2,448 (V) (3,280 (H) × 2,464 (V) including border pixels). It incorporates sophisticated on-chip camera functions such as mirroring, column and row skip modes, and context switching for zero shutter lag snapshot mode. It is programmable through a simple two-wire serial interface and has very low power consumption.

The AR0833 digital image sensor features ON Semiconductor's breakthrough low-noise 1.4 μm pixel CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The AR0833 sensor can generate full resolution image at up to 30 frames per second (fps). An on-chip analog-to-digital converter (ADC) generates a 10-bit value for each pixel.

### Features

- High-Speed Sensor Supporting 8 Mp (4:3) 30 fps Still Images and Full HD 1080p 30 fps Video
- 1.4 μm Pixel with A-PixHS™ Technology Providing Best-in-Class Low-Light Performance
- Optional On-Chip High-Quality Bayer Scaler to Resize Image to Desired Size
- Data Interfaces: 2-, 3-, and 4-Lane Serial Mobile Industry Processor Interface (MIPI)
- Bit-Depth Compression Available for MIPI Interface: 10−8 and 10−6 to Enable Lower Bandwidth Receivers for Full Frame Rate Applications
- On-Chip Temperature Sensor
- On-Die Phase-Locked Loop (PLL) Oscillator
- 4 Kb One-Time Programmable Memory (OTPM) for Storing Module Information
- On-Chip 8-Bit VCM Driver
- 3D Synchronization Controls to Enable Stereo Video Capture
- Interlaced Multi-Exposure Readout Enabling High Dynamic Range (HDR) Still and Video Applications
- Programmable Controls: Gain, Horizontal and Vertical Blanking, Auto Black Level Offset Correction, Frame Size/Rate, Exposure, Left-Right and Top-Bottom Image Reversal, Window Size, and Panning
- Support for External Mechanical Shutter
- Support for External LED or Xenon Flash

### General Physical Specifications

- Die Thickness: 200 μm ±12 μm *(Consult Factory for other Die Thickness)*
- Back Side Wafer Surface of Bare Silicon
- Bond Pad Metallization Composition: 10,000 Å Al over Cu
- Typical Top Side Passivation: 2.2 kÅ Nitride over 6.0 kÅ of Undoped Oxide
- Passivation Openings (MIN): 75 × 81 μm

**ON Semiconductor®**

www.onsemi.com

| Options | Designator |
|---|---|
| Form − Die | D |
| Testing − Standard (Level 1) Probe | C1 |

### ORDERING INFORMATION

| Die |
|---|
| AR0833CS3C29SMD20 |

Consult die distributor or factory before ordering to verify long-term availability of these die products.

### Die Database

- Die Outline (see Figure 2)
- Singulated Die Size: 6,860 μm ± 25 μm × 6,440 μm ± 25 μm
- Bond Pad Location and Identification Tables (See Table 1 and Table 2)

### Key Performance Parameters

- Optical Format: 1/3.2-Inch (4:3)
- Active Imager Size: 5.74 mm Diagonal: 4.59 mm (H) × 3.45 mm (V)
- Active Pixels: 3,264 (H) × 2,448 (V)
- Pixel Size: 1.4 μm Back Side Illumination (BSI)
- Color Filter Array: RGB Bayer Pattern
- CRA: 29°
- Shutter Type:
  - Electronic Rolling Shutter (ERS) with Global Reset Release (GRR)
- MIPI CSI−2 (2-, 3-, 4-Lane Modes Supported) with 800 MHz max MIPI Clock Speed per Lane
- Frame Rate:
  - Full Resolution at 30 fps
- ADC Resolution: 10-Bit, On-Die
- Responsivity: 0.6 V/lux−seconds
- Dynamic Range: 64 dB
- $SNR_{MAX}$: 36 dB
- Supply Voltage
  - Digital I/O: 1.7−1.9 V (1.8 V Nominal) or 2.5−3.1 V (2.8 V Nominal)
  - DVDD_1V8: 1.7−1.9 V (1.8 V Nominal) can be Combined with Digital I/O if that is 1.8 V

**Key Performance Parameters** (Continued)

- Digital Core: 1.14−1.3 V (1.2 V Nominal)
- Analog: 2.5–3.1 V (2.8 V Nominal)
- Digital PHY: 1.14−1.3 V (1.2 V Nominal)

- Power Consumption:
  - Full Resolution (MIPI):
    350 mW at 25°C and Nominal Voltages
  - Hardware Standby/Shutdown:
    10/30 μA Typical/Max
    30 μA at 55°C (by XSHUTDOWN pin).
    No State Retention.
- Operating Temperature: −30°C to +70°C (at Junction)

### Die Testing Procedures

ON Semiconductor imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to ensure product functionality in ON Semiconductor's standard package. Because the package environment is not within ON Semiconductor's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

ON Semiconductor retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. ON Semiconductor reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to ON Semiconductor's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

### Functional Specifications

The specifications provided in this document are for reference only. For target functional and parametric specifications, refer to the product data sheet found on our web site (www.onsemi.com).

### Bonding Instructions

The AR0833 imager die has 67 bond pads. Refer to Table 1 and Table 2 for a complete list of bond pads and coordinates.

The AR0833 imager die does not require the user to determine bond option features.

The die also has several pads defined as "do not use." These pads are used for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

Figure 1 shows the AR0833 typical die connections. For low-noise operation, the AR0833 die requires separate supplies for analog and digital power. Power supply rails should be decoupled to ground using capacitors. The use of inductance filters is not recommended.

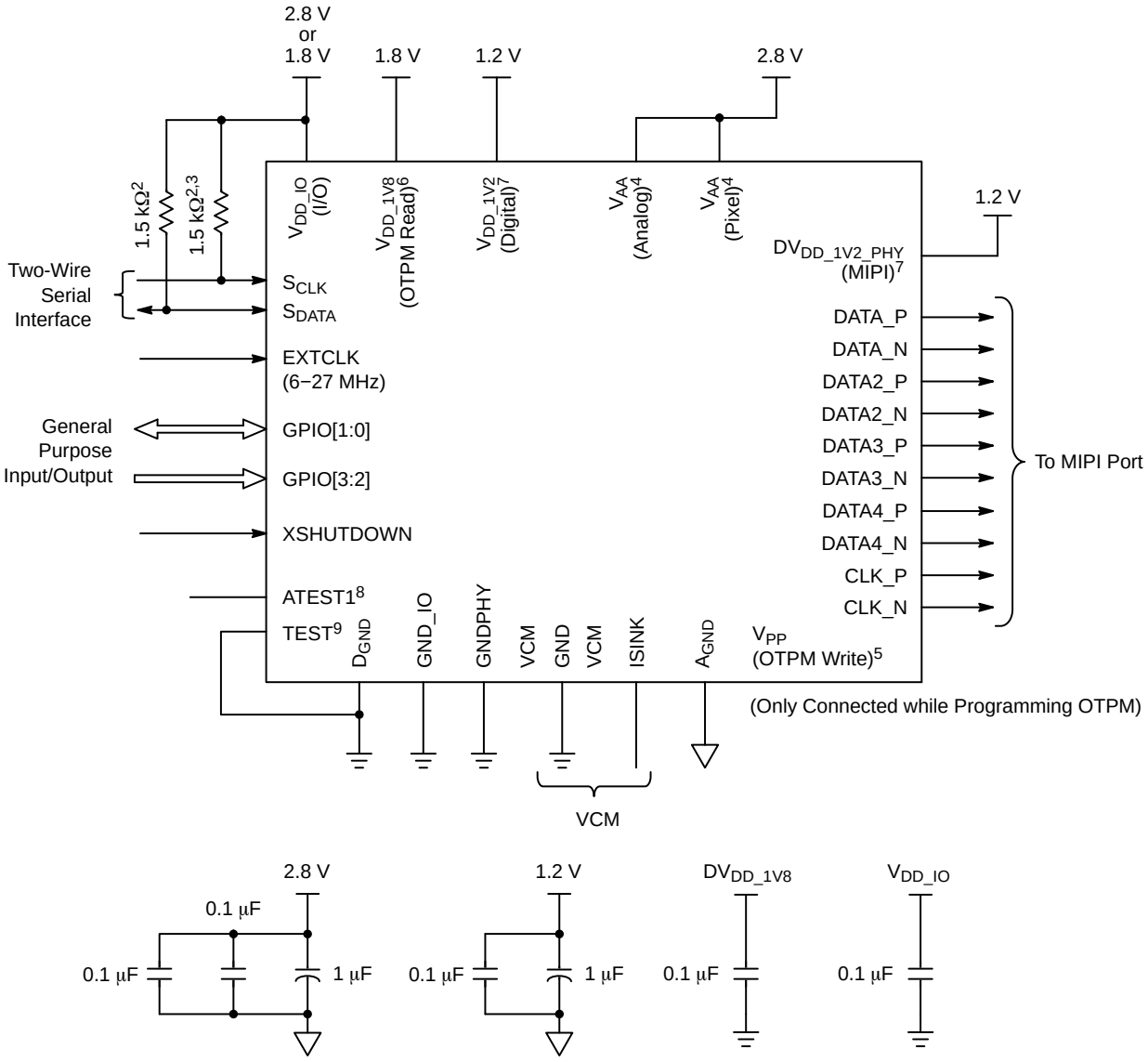
All $D_{GND}$ pads must be tied together, as must all $A_{GND}$ pads, all $V_{DD\_IO}$ pads, and all $V_{DD}$ pads. Doing so will minimize risk of damage to the sensor in an ESD event. Pin 37 is an optional pin that connects to the $DV_{DD\_1V2}$ power rail. If not connected it should be left floating

### Storage Requirements

ON Semiconductor die products are packaged in a clean room environment for shipping. Upon receipt, the customer should transfer the die to a similar environment for storage. ON Semiconductor recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% relative humidity ±10%. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

### Typical Connections

Figure 1 shows the typical AR0833 connections.




Notes:

1. All power supplies must be adequately decoupled. The order of preference is as follows:
   2.8 V supply − 1.0 μF, 0.1 μF and then 0.01 μF
   1.2 V supply − 1.0 μF and 0.1 μF
   1.8V supply − 0.1 μF
2. ON Semiconductor recommends using a resistor value of 1.5 kΩ, but a greater value can be used for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on $S_{CLK}$ at all times.
4. $V_{AA}$ and $V_{AA\_PIX}$ can be tied together. However, for noise immunity it is recommended to have them separate (i.e. two sets of 2.8 V decoupling caps).
5. $V_{PP}$, 6−7 V, is used for programming OTPM. This pad is left unconnected if OTPM is not being programmed.
6. $DV_{DD\_1V8}$ can be combined with $V_{DD\_IO}$, if $V_{DD\_IO}$ = 1.8 V.
7. $DV_{DD\_1V2}$ and $DV_{DD\_1V2\_PHY}$ can be tied together.
8. ATEST1 must be floating.
9. TEST pin must be tied to $D_{GND}$.
10. $DV_{DD\_1V8}$ is the OTPM read voltage.

**Figure 1. Typical Application Circuit − MIPI Connection**

## Bond Pad Location and Identification Tables

**Table 1. BOND PAD LOCATION AND IDENTIFICATION FROM CENTER OF PAD 1**

| Pad Number | Pad Name | “X” Microns (Note 1) | “Y” Microns (Note 1) |
|---|---|---|---|
| 1 | DGND_ANA | 0 | 0 |
| 2 | DGND_ANA | 0 | 130 |
| 3 | VDD_ANA | 0 | 260 |
| 4 | VDD_ANA | 0 | 390 |
| 5 | AGND | 0 | 544.08 |
| 6 | VAA | 0 | 677.215 |
| 7 | VAA | 0 | 1039.725 |
| 8 | AGND | 0 | 1169.725 |
| 9 | AGND | 0 | 1299.725 |
| 10 | VAA | 0 | 1429.725 |
| 11 | AGND | 0 | 1559.725 |
| 12 | AGND | 0 | 1689.725 |
| 13 | VAA | 0 | 1819.725 |
| 14 | AGND | 0 | 1949.725 |
| 15 | VAA | 0 | 2079.725 |
| 16 | ATEST1 | 0 | 2825.455 |
| 17 | AGND | 0 | 2955.455 |
| 18 | VAA | 0 | 3085.455 |
| 19 | VAA_PIX | 0 | 3215.455 |
| 20 | VAA_PIX | 0 | 3345.455 |
| 21 | PIX_GND | 0 | 3475.455 |
| 22 | AGND | 0 | 3605.455 |
| 23 | VAA | 0 | 3735.455 |
| 24 | VCM_ISINK | 0 | 3891.315 |
| 25 | VCM_GND | 0 | 4259.01 |
| 26 | DGND | 0 | 4426.495 |
| 27 | VDD_IO | 0 | 4556.495 |
| 28 | XSHUSTDOWN | 0 | 4697.76 |
| 29 | GPIO1 | 0 | 4867.92 |
| 30 | GPIO0 | 0 | 5041.68 |
| 31 | VDD_SW | 0 | 5188.08 |
| 32 | VDD_IO | 0 | 5485.8 |
| 33 | GPI3 | 0 | 5641.72 |
| 34 | GPI2 | 0 | 5775.88 |
| 35 | DGND | 0 | 5905.88 |
| 36 | VDD_SW | 0 | 6189.92 |
| 37 | VDD_SW | 5255.3 | 6250.1 |
| 38 | VDD_PLL | 6720.2 | 5995.88 |
| 39 | DGND | 6720.2 | 5711.84 |
| 40 | SDATA | 6720.2 | 5581.52 |

**Table 1. BOND PAD LOCATION AND IDENTIFICATION FROM CENTER OF PAD 1** (continued)

| Pad Number | Pad Name | "X" Microns (Note 1) | "Y" Microns (Note 1) |
|---|---|---|---|
| 41 | SCLK | 6720.2 | 5435.72 |
| 42 | DGND | 6720.2 | 5301.08 |
| 43 | EXTCLK | 6720.2 | 5159.88 |
| 44 | VDD_IO | 6720.2 | 5009.76 |
| 45 | TEST | 6720.2 | 4895.6 |
| 46 | VDD_SW | 6720.2 | 4745.24 |
| 47 | DGND | 6720.2 | 4445.72 |
| 48 | DATA_P | 6720.2 | 4270.94 |
| 49 | DATA_N | 6720.2 | 3971.06 |
| 50 | VDD_SLVS_PHY | 6720.2 | 3796.28 |
| 51 | DATA2_N | 6720.2 | 3621.5 |
| 52 | DATA2_P | 6720.2 | 3321.62 |
| 53 | VDD_PHY | 6720.2 | 3146.84 |
| 54 | CLK_P | 6720.2 | 2887.82 |
| 55 | CLK_N | 6720.2 | 2587.94 |
| 56 | DATA3_P | 6720.2 | 2209.94 |
| 57 | DATA3_N | 6720.2 | 1910.06 |
| 58 | VDDIO_1V8_P | 6720.2 | 1735.28 |
| 59 | DATA4_N | 6720.2 | 1560.5 |
| 60 | DATA4_P | 6720.2 | 1260.62 |
| 61 | DGND | 6720.2 | 1085.84 |
| 62 | VDD_SW | 6720.2 | 796.4 |
| 63 | VDD_1V8 | 6720.2 | 585.44 |
| 64 | VPP | 6720.2 | 420.92 |
| 65 | VDD_ANA | 6720.2 | 260 |
| 66 | VDD_ANA | 6720.2 | 130 |
| 67 | DGND_ANA | 6720.2 | 0 |

1. Reference to center of each bond pad from center of bond pad 1.
2. ATEST1 must be floating.
3. Pin 37 is an optional pin that connects to the $DV_{DD\_1V2}$ power rail. If not connected it should be left floating.

**Table 2. BOND PAD LOCATION AND IDENTIFICATION FROM CENTER OF DIE**

| Pad Number | Pad Name | "X" Microns (Note 1) | "Y" Microns (Note 1) |
|---|---|---|---|
| 1 | DGND_ANA | −3360.1 | −3100 |
| 2 | DGND_ANA | −3360.1 | −2970 |
| 3 | VDD_ANA | −3360.1 | −2840 |
| 4 | VDD_ANA | −3360.1 | −2710 |
| 5 | AGND | −3360.1 | −2555.92 |
| 6 | VAA | −3360.1 | −2422.785 |
| 7 | VAA | −3360.1 | −2060.275 |
| 8 | AGND | −3360.1 | −1930.275 |
| 9 | AGND | −3360.1 | −1800.275 |
| 10 | VAA | −3360.1 | −1670.275 |
| 11 | AGND | −3360.1 | −1540.275 |
| 12 | AGND | −3360.1 | −1410.275 |
| 13 | VAA | −3360.1 | −1280.275 |
| 14 | AGND | −3360.1 | −1150.275 |
| 15 | VAA | −3360.1 | −1020.275 |
| 16 | ATEST1 | −3360.1 | −274.545 |
| 17 | AGND | −3360.1 | −144.545 |
| 18 | VAA | −3360.1 | −14.545 |
| 19 | VAA_PIX | −3360.1 | 115.455 |
| 20 | VAA_PIX | −3360.1 | 245.455 |
| 21 | PIX_GND | −3360.1 | 375.455 |
| 22 | AGND | −3360.1 | 505.455 |
| 23 | VAA | −3360.1 | 635.455 |
| 24 | VCM_ISINK | −3360.1 | 791.315 |
| 25 | VCM_GND | −3360.1 | 1159.01 |
| 26 | DGND | −3360.1 | 1326.495 |
| 27 | VDD_IO | −3360.1 | 1456.495 |
| 28 | XSHUSTDOWN | −3360.1 | 1597.76 |
| 29 | GPIO1 | −3360.1 | 1767.92 |
| 30 | GPIO0 | −3360.1 | 1941.68 |
| 31 | VDD_SW | −3360.1 | 2088.08 |
| 32 | VDD_IO | −3360.1 | 2385.8 |
| 33 | GPI3 | −3360.1 | 2541.72 |
| 34 | GPI2 | −3360.1 | 2675.88 |
| 35 | DGND | −3360.1 | 2805.88 |
| 36 | VDD_SW | −3360.1 | 3089.92 |
| 37 | VDD_SW | 1895.2 | 3150.1 |
| 38 | VDD_PLL | 3360.1 | 2895.88 |
| 39 | DGND | 3360.1 | 2611.84 |
| 40 | SDATA | 3360.1 | 2481.52 |
| 41 | SCLK | 3360.1 | 2335.72 |

**Table 2. BOND PAD LOCATION AND IDENTIFICATION FROM CENTER OF DIE** (continued)

| Pad Number | Pad Name | "X" Microns (Note 1) | "Y" Microns (Note 1) |
|---|---|---|---|
| 42 | DGND | 3360.1 | 2201.08 |
| 43 | EXTCLK | 3360.1 | 2059.88 |
| 44 | VDD_IO | 3360.1 | 1909.76 |
| 45 | TEST | 3360.1 | 1795.6 |
| 46 | VDD_SW | 3360.1 | 1645.24 |
| 47 | DGND | 3360.1 | 1345.72 |
| 48 | DATA_P | 3360.1 | 1170.94 |
| 49 | DATA_N | 3360.1 | 871.06 |
| 50 | VDD_SLVS_PHY | 3360.1 | 696.28 |
| 51 | DATA2_N | 3360.1 | 521.5 |
| 52 | DATA2_P | 3360.1 | 221.62 |
| 53 | VDD_PHY | 3360.1 | 46.84 |
| 54 | CLK_P | 3360.1 | −212.18 |
| 55 | CLK_N | 3360.1 | −512.06 |
| 56 | DATA3_P | 3360.1 | −890.06 |
| 57 | DATA3_N | 3360.1 | −1189.94 |
| 58 | VDDIO_1V8_P | 3360.1 | −1364.72 |
| 59 | DATA4_N | 3360.1 | −1539.5 |
| 60 | DATA4_P | 3360.1 | −1839.38 |
| 61 | DGND | 3360.1 | −2014.16 |
| 62 | VDD_SW | 3360.1 | −2303.6 |
| 63 | VDD_1V8 | 3360.1 | −2514.56 |
| 64 | VPP | 3360.1 | −2679.08 |
| 65 | VDD_ANA | 3360.1 | −2840 |
| 66 | VDD_ANA | 3360.1 | −2970 |
| 67 | DGND_ANA | 3360.1 | −3100 |

1. Reference to center of each bond pad from center of die (0,0).
2. ATEST1 must be floating.
3. Pin 37 is an optional pin that connects to the $DV_{DD\_1V2}$ power rail. If not connected it should be left floating.

## Die Features

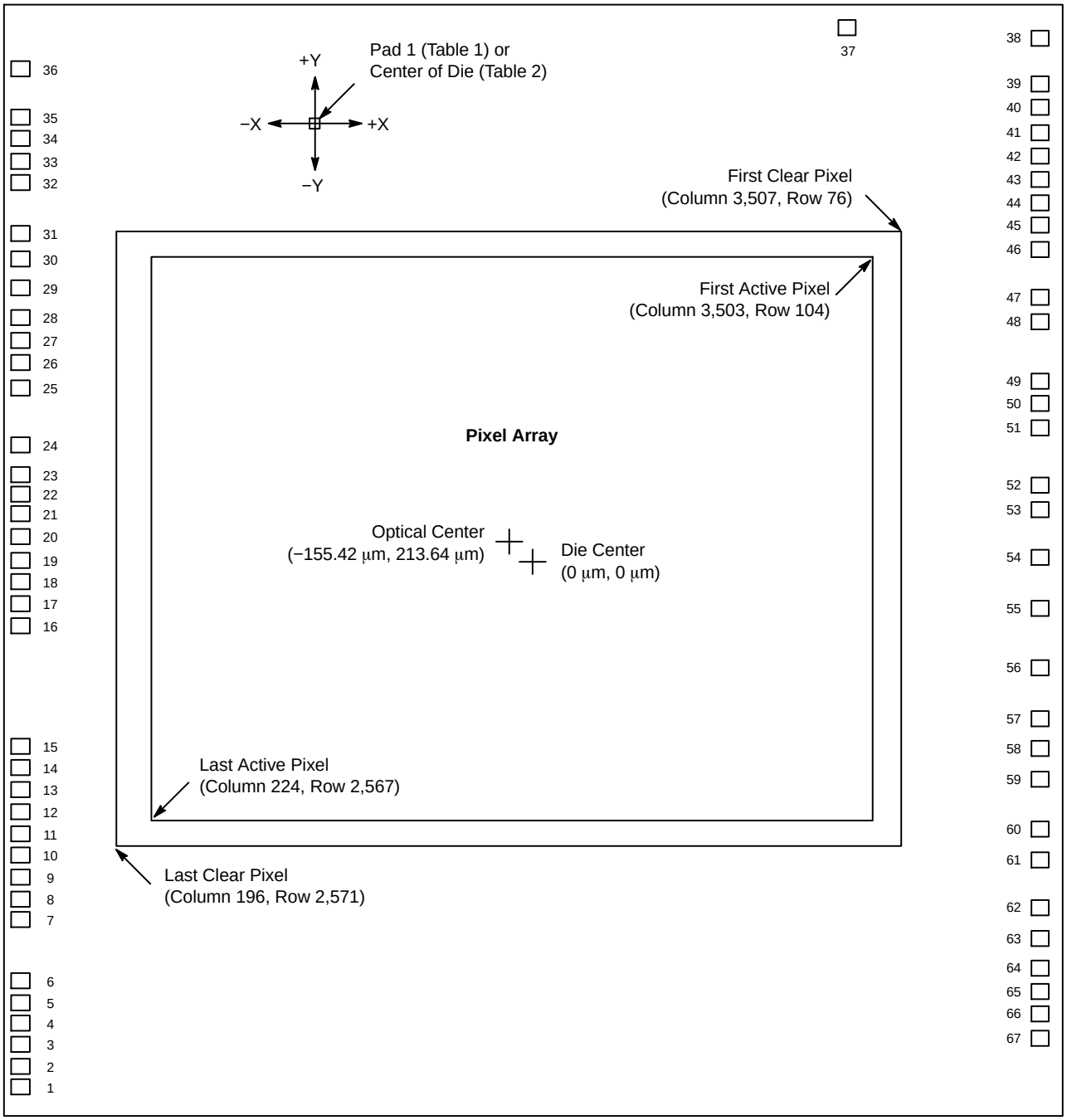



**Figure 2. Die Outline (Top View)**

## Physical Specifications

**Table 3. PHYSICAL DIMENSIONS**

| Feature | Dimensions |
|---|---|
| Wafer Diameter | 200 mm (8″) |
| Die Thickness | 200 μm ±12 μm or 620 μm ±12 μm |
| Singulated Die Size (after Wafer Saw)<br>Width (X Dimension)<br>Length (Y Dimension) | <br>6,864 μm ±25 μm<br>6,444 μm ±25 μm |
| Bond Pad Size (MIN) | 104 μm × 85 μm |
| Passivation Openings (MIN) | 75 μm × 81 μm |
| Minimum Bond Pad Pitch | 114 μm |
| Optical Array<br>Optical Center from Die Center<br>Optical Center from Center of Pad 1 | <br>X = −155.42 μm, Y = 213.64 μm<br>X = 3,190.18 μm, Y = 3,313.64 μm |
| First Clear Pixel (Column 3,507, Row 76)<br>From Die Center<br>From Center of Pad 1 | <br>X = 2,146.18 μm, Y = 1,977.64 μm<br>X = 5,491.78 μm, Y = 5,077.64 μm |
| First Active Pixel (Column 3,503, Row 104)<br>From Die Center<br>From Center of Pad 1 | <br>X = 2,140.58 μm, Y = 1,938.44 μm<br>X = 5,486.18 μm, Y = 5,038.44 μm |
| Last Clear Pixel (Column 196, Row 2,571)<br>From Die Center<br>From Center of Pad 1 | <br>X = −2,490.62 μm, Y = –1,516.76 μm<br>X = 854.98 μm, Y = 1,583.24 μm |
| Last Active Pixel (Column 224, Row 2,567)<br>From Die Center<br>From Center of Pad 1 | <br>X = −2,451.42 μm, Y = –1,511.16 μm<br>X = 894.18 μm, Y = 1,588.84 μm |

## Die Orientation in Reconstructed Wafer

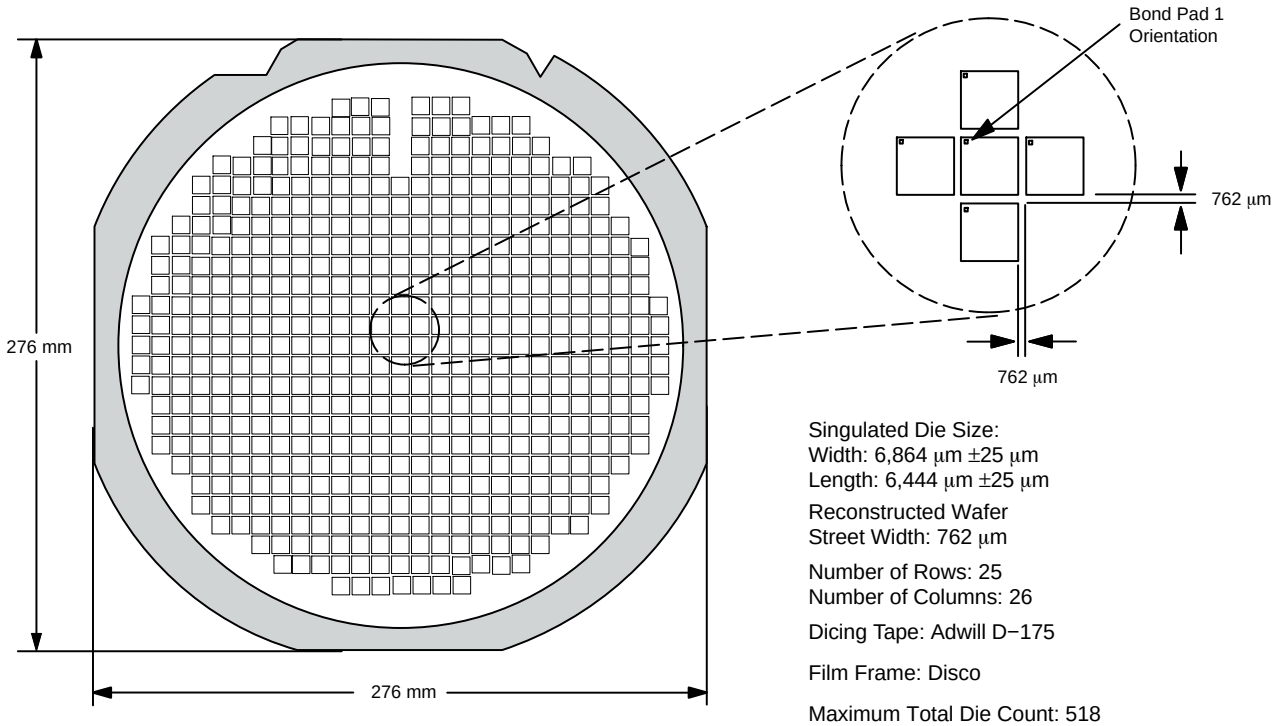



**Figure 3. Die Orientation in Reconstructed Wafer − Maximum Total Die Count (Thickness = 200 μm)**

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## PUBLICATION ORDERING INFORMATION

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**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
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**ON Semiconductor Website**: **www.onsemi.com**

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