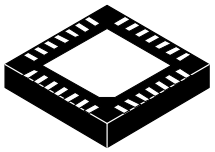
AX5044

Product Preview

High Performance Narrow-band Software Defined RF Transceiver for Frequencies from 60 MHz to 1050 MHz

ON Semiconductor®

www.onsemi.com



QFN28
CASE 485EH

OVERVIEW

Features

Advanced Multi−channel Narrow−band Single Chip UHF Transceiver (FSK/MSK/4−FSK/GFSK/GMSK/ASK/AFSK/FM/PSK).

Low−Power

- RX
  ~14 mA @ 868 MHz and 433 MHz
- TX @ 868 MHz
  48 mA @ 16 dBm
- 50 nA Deep Sleep Current
- 500 nA Power−down Current with Low Frequency Duty Cycle Clock Running

Supply Voltage Range

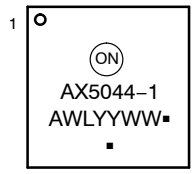
- 1.8 V to 3.6 V Single Supply

High Sensitivity/High Selectivity Receiver

- Data Rates from 0.1 kbps to 200 kbps
- Optional Forward Error Correction (FEC)
- Sensitivity without FEC
  - −135 dBm @ 0.1 kbps, 868 MHz, FSK
  - −126 dBm @ 1 kbps, 868 MHz, FSK
  - −117 dBm @ 10 kbps, 868 MHz, FSK
  - −107 dBm @ 100 kbps, 868 MHz, FSK
  - −105 dBm @ 125 kbps, 868 MHz, FSK
  - −138 dBm @ 0.1 kbps, 868 MHz, PSK
  - −130 dBm @ 1 kbps, 868 MHz, PSK
  - −120 dBm @ 10 kbps, 868 MHz, PSK
  - −109 dBm @ 100 kbps, 868 MHz, PSK
  - −108 dBm @ 125 kbps, 868 MHz, PSK
- Sensitivity with FEC
  - −137 dBm @ 0.1 kbps, 868 MHz, FSK
  - −122 dBm @ 5 kbps, 868 MHz, FSK
  - −111 dBm @ 50 kbps, 868 MHz, FSK
- High Selectivity Receiver with up to 55 dB Adjacent Channel Rejection
- 0 dBm Maximum Input Power
- > ±10% Data−rate Error Tolerance
- Support for Antenna Diversity with External Antenna Switch

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

MARKING DIAGRAM



AX5044−1	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
AX5044−1−TW30	QFN	3000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Features (continued)

- Short Preamble Modes allow the Receiver to work with as little as 16 Preamble Bits
- Fast State Switching Times
  - 200 µs TX → RX Switching Time
  - 62 µs RX → TX Switching Time

Transmitter

- Data−rates from 0.1 kbps to 200 kbps
- High Efficiency, High Linearity Integrated Power Amplifier
- Maximum Output Power
  - 15 dBm @ 915 MHz
  - 15 dBm @ 433 MHz
  - 15 dBm @ 169 MHz
- Power Level programmable in 0.5 dB Steps
- GFSK Shaping with BT = 0.3 or BT = 0.5
- Unrestricted Power Ramp Shaping

Frequency Generation

- Configurable for Usage in 60 − 1050 MHz Bands
- RF Carrier Frequency and FSK Deviation Programmable in 1 Hz Steps
- Ultra−Fast Settling RF Frequency Synthesizer for Low−power Consumption
- Fully Integrated RF Frequency Synthesizer with VCO Auto−ranging and Bandwidth Boost Modes for Fast Locking
- Fully Integrated VCO
- Configurable for either Fully Integrated or External Synthesizer Loop Filter for a Large Range of Bandwidths
- Channel Hopping up to 2000 hops/s
- Automatic Frequency Control (AFC)

Wakeup−on−Radio

- 640 Hz or 10 kHz Lowest Power Wake−up Timer
- Wake−up Time Interval programmable between 98 µs and 102 s

Sophisticated Radio Controller

- Antenna Diversity and Optional External RX/TX Switch Control
- Fully Automatic Packet Reception and Transmission without Micro−controller Intervention
- Supports HDLC, Raw, Wireless M−Bus Frames and Arbitrary Defined Frames
- Automatic Channel Noise Level Tracking
- µs Resolution Timestamps for Exact Timing (eg. for Frequency Hopping Systems)
- 256 Byte Micro−programmable FIFO, optionally supports Packet Sizes > 256 Bytes
- Three Matching Units for Preamble Byte, Sync−word and Address
- Ability to store RSSI, Frequency Offset and Data−rate Offset with the Packet Data
- Multiple Receiver Parameter Sets allow the use of more aggressive Receiver Parameters during Preamble, dramatically shortening the Required Preamble Length at no Sensitivity Degradation

Advanced Crystal Oscillator (RF Reference Oscillator)

- Fast Start−up and Lowest Power Steady−state XTAL Oscillator for a Wide Range of Crystals
- Integrated Crystal Tuning Capacitors
- Possibility of Applying an External Clock Reference (TCXO)

Miscellaneous Features

- Few External Components
- SPI Microcontroller Interface
- Extended Radio Register Set
- Fully Integrated Current/Voltage References
- QFN28 5 mm x 5 mm Package
- Internal Power−on−Reset
- Brown−out Detection
- 12 Bit 0.5 MS/s General Purpose ADC (GPADC)

Applications

60 − 1050 MHz Licensed and Unlicensed Radio Systems

- Internet of Things
- Automatic Meter Reading (AMR)
- Security Applications
- Building Automation
- Wireless Networks
- Remote Controls
- Messaging Paging
- Compatible with: Wireless M−Bus, POCSAG, FLEX, KNX, Sigfox, Z−Wave, EnOcean
- Regulatory Regimes: EN 300 220 including the Narrow−band 12.5 kHz, 20 kHz and 25 kHz Definitions; EN 300 422; FCC Part 15.247; FCC Part 15.249; FCC Part 90 6.25 kHz, 12.5 kHz and 25 kHz

BLOCK DIAGRAM

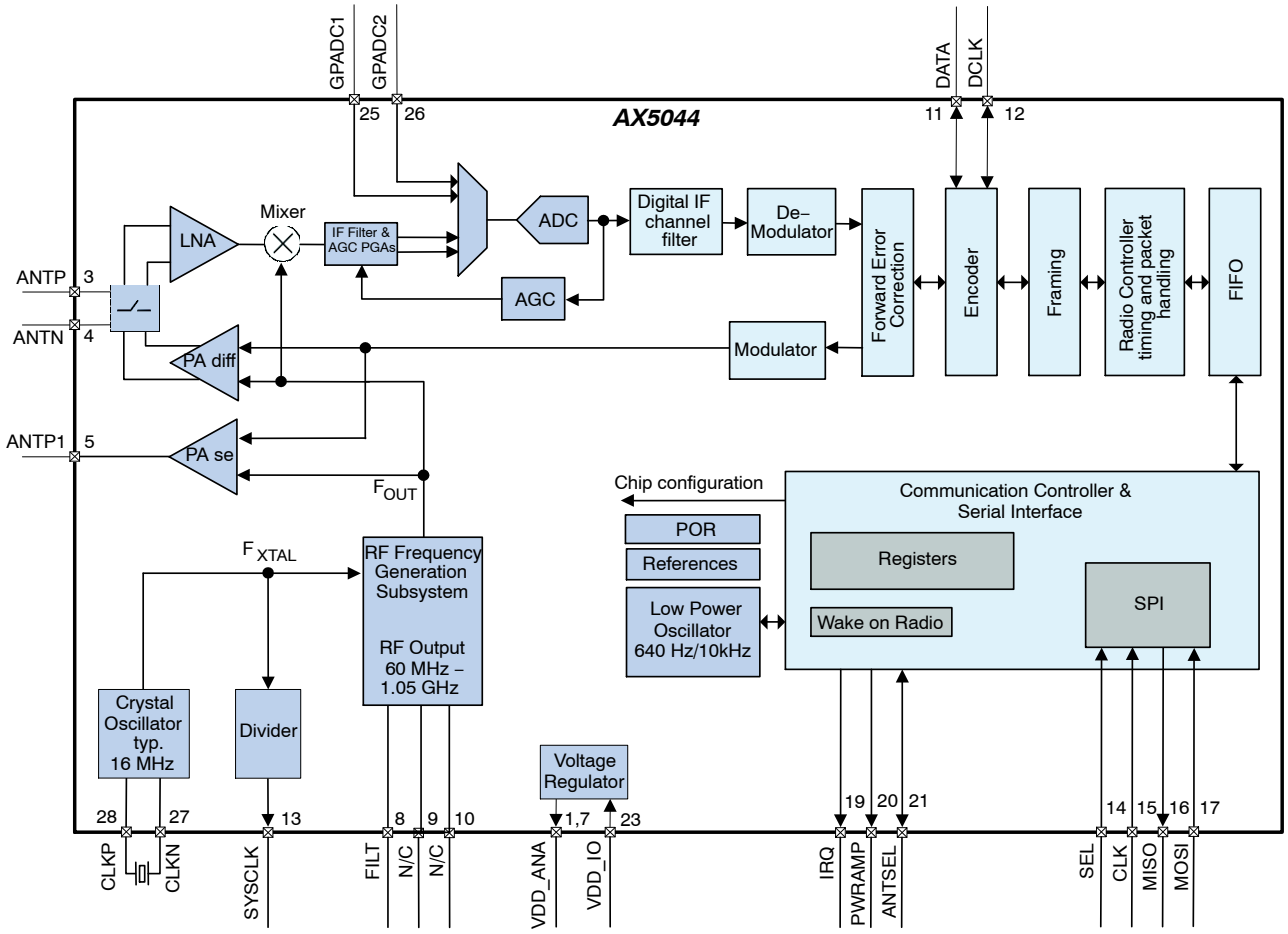


Figure 1. Functional Block Diagram of the AX5044

Table 1. PIN FUNCTION DESCRIPTION

Symbol	Pin(s)	Type	Description
VDD_ANA	1	P	Analog power output, decoupling
VSSA	2	P	Ground
ANTP	3	A	Differential RX/TX antenna connection
ANTN	4	A	Differential RX/TX antenna connection
ANTP1	5	A	Single−ended TX antenna output
VSSA	6	P	Ground
VDD_ANA	7	P	Analog power output, decoupling
FILT	8	A	Optional synthesizer filter
NC	9	A	not used
NC	10	A	not used
DATA	11	I/O	In wire mode: Data input/output Can be programmed to be used as a general purpose I/O pin Selectable internal 65 kΩ pull−up resistor
DCLK	12	I/O	In wire mode: Clock output Can be programmed to be used as a general purpose I/O pin Selectable internal 65 kΩ pull−up resistor

Table 1. PIN FUNCTION DESCRIPTION (continued)

Symbol	Pin(s)	Type	Description
SYSCLK	13	I/O	Default functionality: Crystal oscillator (or divided) clock output Can be programmed to be used as a general purpose I/O pin Selectable internal 65 kΩ pull−up resistor
SEL	14	I	Serial peripheral interface select
CLK	15	I	Serial peripheral interface clock
MISO	16	O	Serial peripheral interface data output
MOSI	17	I	Serial peripheral interface data input
NC	18	N	Must be left unconnected
IRQ	19	I/O	Default functionality: Transmit and receive interrupt Can be programmed to be used as a general purpose I/O pin Selectable internal 65 kΩ pull−up resistor
PWRAMP	20	I/O	Default functionality: Power amplifier control output Can be programmed to be used as a general purpose I/O pin Selectable internal 65 kΩ pull−up resistor
ANTSEL	21	I/O	Default functionality: Diversity antenna selection output Can be programmed to be used as a general purpose I/O pin Selectable internal 65 kΩ pull−up resistor
NC	22	N	Must be left unconnected
VDD_IO	23	P	Power supply 3.0 V − 3.3 V
NC	24	N	Must be left unconnected
GPADC1	25	A	GPADC input, must be connected to GND if not used
GPADC2	26	A	GPADC input, must be connected to GND if not used
CLKN	27	A	Crystal oscillator input/output. Leave unconnected when using TCXO
CLKP	28	A	Crystal oscillator input/output. TCXO input.
GND	Center pad	P	Ground on center pad of QFN, must be connected

NOTE: All digital inputs are Schmitt trigger inputs, digital input and output levels are LVCMOS/LVTTL compatible and 5 V tolerant.
A = analog input
I = digital input signal
O = digital output signal
I/O = digital input/output signal
N = not to be connected
P = power or ground

PINOUT DRAWING

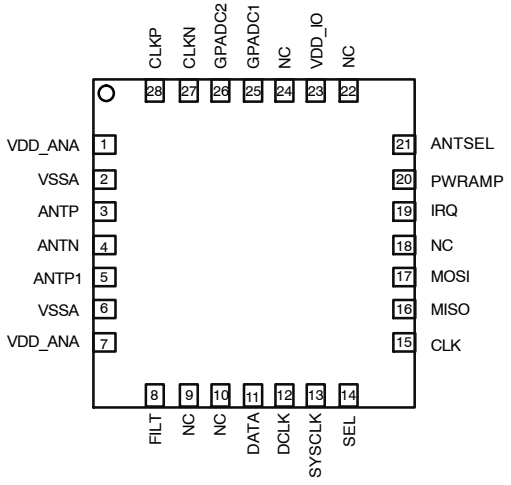


Figure 2. Pinout Drawing (Top View)

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Condition	Min	Max	Unit
VDD_IO	Supply voltage		−0.5	5.5	V
IDD	Supply current			200	mA
P_{tot}	Total power consumption			800	mW
P_i	Absolute maximum input power at receiver input	ANTP and ANTN pins in RX mode		10	dBm
I_{I1}	DC current into any pin except ANTP, ANTN, ANTP1		−10	10	mA
I_{I2}	DC current into pins ANTP, ANTN, ANTP1		−100	100	mA
I_O	Output Current			40	mA
V_{ia}	Input voltage ANTP, ANTN, ANTP1 pins		−0.5	5.5	V
	Input voltage digital pins		−0.5	5.5	V
V_{es}	Electrostatic handling	HBM	−2000	2000	V
T_{amb}	Operating temperature		−40	85	°C
T_{stg}	Storage temperature		−65	150	°C
T_j	Junction Temperature			150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Exposure to absolute maximum rating conditions for extended periods may affect device reliabiloty.

DC CHARACTERISTICS

Table 3. SUPPLIES

Symbol	Description	Condition	Min	Typ	Max	Unit
T_{AMB}	Operational ambient temperature		−40	27	85	°C
VDD_IO	I/O and voltage regulator supply voltage		1.8	3.0	3.6	V
V_{BOUT}	Brown−out threshold	(Note 2)		1.3		V
I_{DSLLEP}	Deep Sleep current: All analog and digital functions are powered down	PWRMODE = 0x01		50		nA
I_{PDOWN}	Power−down current: Register file contents preserved	PWRMODE = 0x00		400		nA
I_{WOR}	Wakeup−on−radio mode: Low power timer and WOR state−machine are running at 640 Hz	PWRMODE = 0x0B		500		nA
I_{STANBY}	Standby−current: All power domains are powered up, crystal oscillator and references are running	PWRMODE = 0x06		230		μA
I_{RX}	Current consumption RX PWRMODE = 0x09 RF Frequency Subsystem: Internal loop−filter	868 MHz, datarate 6 kbps		14		mA
		169 MHz, datarate 6 kbps		TBD		mA
		868 MHz, datarate 100 kbps		TBD		mA
		169 MHz, datarate 100 kbps		TBD		mA
$I_{TX−SE}$	Current consumption TX	868 MHz, 15 dBm, FSK, RF Frequency Subsystem: Internal loop−filter		48		mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Digital circuity is functional down to typically 1 V.
3. Measured with optimized matching networks.

Table 4. LOGIC

Symbol	Description	Condition	Min	Typ	Max	Unit
DIGITAL INPUTS						
VT_+	Schmitt trigger low to high threshold point			1.9		V
VT_-	Schmitt trigger high to low threshold point			1.2		V
V_{IL}	Input voltage, low				0.8	V
V_{IH}	Input voltage, high		2.0			V
I_L	Input leakage current		−10		10	μA
R_{pullup}	Pull−up resistors Pins DATA, DCLK, SYSCLK, IRQ, PWRAMP, ANTSEL	Pull−ups enabled in the relevant pin configuration registers		65		kΩ
DIGITAL INPUTS						
I_{OH}	Output Current, high	VDD_IO = 3 V, V_{OH} = 2.4 V	4			mA
I_{OL}	Output Current, low	VDD_IO = 3 V, V_{OL} = 0.4 V	4			mA
I_{OZ}	Tri−state output leakage current		−10		10	μA

AC CHARACTERISTICS

Table 5. CRYSTAL OSCILLATOR

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{XTAL}	Crystal frequency	(Notes 4, 5, 6)	16	48	50	MHz
gm_{osc}	Oscillator transconductance control range	Self−regulated (Note 7)	0.2		20	mS
C_{osc}	Programmable tuning capacitors at pins CLK16N and CLK16P	XTALCAP = 0x00 default		3		pF
		XTALCAP = 0x01		8.5		pF
		XTALCAP = 0xFF		40		pF
$C_{osc−lsb}$	Programmable tuning capacitors, increment per LSB of XTALCAP	XTALCAP = 0x01 − 0xFF		0.5		pF
f_{ext}	External clock input (TCXO)	(Notes 5, 6, 8)	10	16	50	MHz
RIN_{osc}	Input DC impedance		10			kΩ
$NDIV_{SYSCLK}$	Divider ratio $f_{SYSCLK} = f_{XTAL}/NDIV_{SYSCLK}$		2^0	2^4	2^{10}	

4. Tolerances and start−up times depend on the crystal used. Depending on the RF frequency and channel spacing the IC must be calibrated to the exact crystal frequency using the readings of the register TRKFREQ.
5. The choice of crystal oscillator or TCXO frequency depends on the targeted regulatory regime for TX, see separate documentation on meeting regulatory requirements.
6. To avoid spurious emission, the crystal or TCXO reference frequency should be chosen so that the RF carrier frequency is not an integer multiple of the crystal or TCXO frequency.
7. The oscillator transconductance is regulated for fastest start−up time during start−up and for lowest power curing steady state oscillation. This means that values depend on the crystal used.
8. Register XTALOSCMODE is used to select either a quartz crystal or TCXO as reference clock. TCXO mode is the default.

Table 6. LOW−POWER OSCILLATOR

Symbol	Description	Condition	Min	Typ	Max	Unit
$f_{osc−slow}$	Oscillator frequency slow mode LPOSC FAST = 0	No calibration	480	640	800	Hz
		Internal calibration vs. crystal clock has been performed	630	640	650	
$f_{osc−fast}$	Oscillator frequency fast mode LPOSC FAST = 1	No calibration	7.6	10.2	12.8	kHz
		Internal calibration vs. crystal clock has been performed	9.8	10.2	10.8	

Table 7. RF FREQUENCY GENERATION SUBSYSTEM (SYNTHESIZER)

Symbol	Description	Condition	Min	Typ	Max	Unit
f_{REF}	Reference frequency	The reference frequency must be chosen so that the RF carrier frequency is not an integer multiple of the reference frequency	16	48	50	MHz
DIVIDERS						
$NDIV_{ref}$	Reference divider ratio range	Controlled directly with register REFDIV	2^0		2^2	
$NDIV_m$	Main divider ratio range	Controlled indirectly with register FREQ	4.5		66.5	
$NDIV_{RF}$	RF divider range	Controlled directly with register RFDIV	1		12	
CHARGE PUMP						
I_{CP}	Charge pump current	Programmable in increments of 8.5 μA via register PLLCPI	8.5		2168	μA
INTERNAL VCO						
f_{RF}	RF frequency range	Depends on divider settings	60		1050	MHz
f_{step}	RF frequency step	RFDIV = 1, f_{xtal} = 48.000000 MHz		0.98		Hz
BW	Synthesizer loop bandwidth	The synthesizer loop bandwidth and start−up time can be programmed with registers PLLLOOP and PLLCPI. For recommendations see the AX5044 Programming Manual, the ON−RadioLab software and AX5044 Application Notes on compliance with regulatory regimes.	50		500	kHz
T_{start}	Synthesizer start−up time if crystal oscillator and reference are running		5		25	μs
PN868	Synthesizer phase noise 868 MHz f_{REF} = 48 MHz	10 kHz offset from carrier		TBD		dBc/Hz
		1 MHz offset from carrier		−125		
PN433	Synthesizer phase noise 433 MHz f_{REF} = 48 MHz	10 kHz offset from carrier		TBD		dBc/Hz
		1 MHz offset from carrier		−131		
PN169	Synthesizer phase noise 169 MHz f_{REF} = 48 MHz	10 kHz offset from carrier		TBD		dBc/Hz
		1 MHz offset from carrier		TBD		

Table 8. TRANSMITTER

Symbol	Description	Condition	Min	Typ	Max	Unit
SBR	Signal bit rate		0.1		200	kbps
PTX	Transmitter power @ 868 MHz	50 Ω single ended measurement at an SMA connector behind the matching network (Note 10)	−10		15	dBm
	Transmitter power @ 433 MHz		−10		15	
	Transmitter power @ 169 MHz		−10		15	
PTX_{step}	Programming step size output power	(Note 9)			0.5	dB
dTX_{temp}	Transmitter power variation vs. temperature	−40°C to +85°C (Note 10)		+ 0.5		dB
dTX_{Vdd}	Transmitter power variation vs. VDD_IO	1.8 V to 3.6 V (Note 10)		+ 0.5		dB

Table 8. TRANSMITTER (continued)

Symbol	Description	Condition	Min	Typ	Max	Unit
Padj	Adjacent channel power GFSK BT = 0.5, 500 Hz deviation, 1.2 kbps, 25 kHz channel spacing, 10 kHz channel BW	868 MHz		TBD		dBc
		433 MHz		TBD		
$PTX_{868-harm2}$	Emission @ 2nd harmonic	868 MHz (Note 10)		−40		dBc
$PTX_{868-harm3}$	Emission @ 3rd harmonic			−60		
$PTX_{433-harm2}$	Emission @ 2nd harmonic	433 MHz (Note 10)		−40		dBc
$PTX_{433-harm3}$	Emission @ 3rd harmonic			−40		

9. $P_{OUT} = (TXPWRCOEFFB / 2^{12}-1) \times P_{max}$
10. 50 Ω single ended measurements at an SMA connector behind the matching network. For recommended matching networks see section: Application Information.

Table 9. RECEIVER SENSITIVITIES

The table lists typical input sensitivities (without FEC) in dBm at the SMA connector with the complete matching network for BER=10^{-3} at 433 or 868 MHz

Data rate [kbps]		FSK h = 0.66	FSK h = 1	FSK h = 2	FSK h = 4	FSK h = 5	FSK h = 8	FSK h = 16	PSK
0.1	Sensitivity [dBm]	−135	−134.5	−132.5	−133	−133.5	−133	−132.5	−138
	RX Bandwidth [kHz]	0.2	0.2	0.3	0.5	0.6	0.9	2.1	0.2
	Deviation [kHz]	0.033	0.05	0.1	0.2	0.25	0.4	0.8	
1	Sensitivity [dBm]	−126	−125	−123	−123.5	−124	−123.5	−122.5	−130
	RX Bandwidth [kHz]	1.5	2	3	6	7	11	21	1
	Deviation [kHz]	0.33	0.5	1	2	2.5	4	8	
10	Sensitivity [dBm]	−117	−116	−113	−114	−113.5	−113		−120
	RX Bandwidth [kHz]	15	20	30	50	60	110		10
	Deviation [kHz]	3.3	5	10	20	25	40		
100	Sensitivity [dBm]	−107	−105.5						−109
	RX Bandwidth [kHz]	150	200						100
	Deviation [kHz]	33	50						
125	Sensitivity [dBm]	−105	−104						−108
	RX Bandwidth [kHz]	187.5	200						125
	Deviation [kHz]	42.3	62.5						

11. Sensitivities are equivalent for 1010 data streams and PN9 whitened data streams.

Table 10. RECEIVER

Symbol	Description	Condition	Min	Typ	Max	Unit
SBR	Signal bit rate		0.1		200	kbps
IS_{BER868}	Input sensitivity at BER = 10^{-3} for 868 MHz operation, continuous data, without FEC	FSK, h = 0.5, 100 kbps		−106		dBm
		FSK, h = 0.5, 10 kbps		−116		
		FSK, 500 Hz deviation, 1.2 kbps		−126		
		PSK, 100 kbps		−109		
		PSK, 10 kbps		−120		
		PSK, 1 kbps		−130		

Table 10. RECEIVER (continued)

Symbol	Description	Condition	Min	Typ	Max	Unit
$IS_{BER868FEC}$	Input sensitivity at BER = 10^{-3}, for 868 MHz operation, continuous data, with FEC	FSK, h = 0.5, 50 kbps		−111		dBm
		FSK, h = 0.5, 5 kbps		−122		
		FSK, 500 Hz deviation, 0.1 kbps		−137		
IS_{PER868}	Input sensitivity at PER = 1%, for 868 MHz operation, 144 bit packet data, without FEC	FSK, h = 0.5, 100 kbps		−103		dBm
		FSK, h = 0.5, 10 kbps		−115		
		FSK, 1.2 kbps		−125		
IS_{WOR868}	Input sensitivity at PER = 1% for 868 MHz operation, 144 bit packet data, WOR−mode, without FEC	FSK, h = 0.5, 100 kpbs		−102		dBm
IL	Maximum input level	Full selectivity		0		dBm
IL_{max}	Maximum input level	FSK, reduced selectivity		10		
CP_{1dB}	Input referred compression point	2 tones separated by 100 kHz		−35		dBm
RSSIR	RSSI control range	FSK, 500 Hz deviation, 1.2 kbps	−126		−46	dB
$RSSIS_1$	RSSI step size	Before digital channel filter; calculated from register AGCCOUNTER		0.625		dB
$RSSIS_2$	RSSI step size	Behind digital channel filter; calculated from registers AGCCOUNTER, TRKAMPL		0.1		dB
$RSSIS_3$	RSSI step size	Behind digital channel filter; reading register RSSI		1		dB
SEL_{868}	Adjacent channel suppression	25 kHz channels (Note 12)		TBD		dB
		100 kHz channels (Note 12)		TBD		
BLK_{868}	Blocking at + 10 MHz offset	(Note 13)		78		dB
R_{AFC}	AFC pull−in range	The AFC pull−in range can be programmed with the MAXRFOFFSET registers. The AFC response time can be programmed with the FREQGAIND register.	+ 15			%
R_{DROFF}	Bitrate offset pull−in range	The bitrate pull−in range can be programmed with the MAXDROFFSET registers.	+ 10			%

12. Interferer/Channel @ BER = 10^{-3}, channel level is +3 dB above the typical sensitivity, the interfering signal is CW; channel signal is modulated with shaping.
13. Channel/Blocker @ BER = 10^{-3}, channel level is +3 dB above the typical sensitivity, the blocker signal is CW; channel signal is modulated with shaping.

Table 11. RECEIVER AND TRANSMITTER SETTLING PHASES

Symbol	Description	Condition	Min	Typ	Max	Unit
T_{xtal}	XTAL settling time	Powermodes: POWERDOWN to STANDBY Note that T_{xtal} depends on the specific crystal used.		0.5		ms
T_{synth}	Synthesizer settling time	Powermodes: STANDBY to SYNTHTX or SYNTHRX		40		μs

Table 11. RECEIVER AND TRANSMITTER SETTLING PHASES (continued)

Symbol	Description	Condition	Min	Typ	Max	Unit
T_{tx}	TX settling time	Powermodes: SYNTHTX to FULLTX T_{tx} is the time used for power ramping, this can be programmed to be 1 x t_{bit}, 2 x t_{bit}, 4 x t_{bit} or 8 x t_{bit}. (Notes 14, 15)	0	1 x t_{bit}	8 x t_{bit}	μs
T_{rx_init}	RX initialization time			150		μs
T_{rx_rssi}	RX RSSI acquisition time (after T_{rx_init})	Powermodes: SYNTHRX to FULL-RX		80 + 3 x t_{bit}		μs
$T_{rx\_preamble}$	RX RSSI acquisition time to valid data RX at full sensitivity/ selectivity (after T_{rx_init})	Modulation (G)FSK (Notes 14, 15)		80 + 3 x t_{bit}		μs

14. t_{bit} depends on the datarate, e.g. fr 10 kbps t_{bit} = 100 μs
15. In wire mode there is a processing delay of typically 6 x t_{bit} between antenna and DCLK/DATA pins.

Table 12. OVERALL STATE TRANSITION TIMES

Symbol	Description	Condition	Min	Typ	Max	Unit
T_{tx_on}	TX startup time	Powermodes: STANDBY to FULLTX (Notes 16, 17)	40	40 + 1 x t_{bit}		μs
T_{rx_on}	RX startup time	Powermodes: STANDBY to FULL-RX		190		μs
T_{rx_rssi}	RX startup time to valid RSSI	Powermodes: STANDBY to FULL-RX		270 + 3 x t_{bit}		μs
T_{rx_data}	RX startup time to valid data at full sensitivity/selectivity	Modulation (G)FSK (Notes 16, 17)		190 + 9 x t_{bit}		μs
T_{rxtx}	RX to TX switching	Powermodes: FULLRX to FULLTX		62		μs
T_{txrx}	TX to RX switching (to preamble start)	Powermodes: FULLTX to FULLRX		200		
T_{hop}	Frequency hop	Switch between frequency defined in register FREQA and FREQB		30		μs

16. t_{bit} depends on the datarate, e.g. fr 10 kbps t_{bit} = 100 μs
17. In wire mode there is a processing delay of typically 6 x t_{bit} between antenna and DCLK/DATA pins.

Table 13. SPI TIMING

Symbol	Description	Condition	Min	Typ	Max	Unit
Tss	SEL falling edge to CLK rising edge		10			ns
Tsh	CLK falling edge to SEL rising edge		10			ns
Tssd	SEL falling edge to MISO driving		0		10	ns
Tssz	SEL rising edge to MISO high−Z		0		10	ns
Ts	MOSI setup time		10			ns
Th	MOSI hold time		10			ns
Tco	CLK falling edge to MISO output				10	ns
Tck	CLK period	(Note 18)	50			ns
Tcl	CLK low duration		40			ns
Tch	CLK high duration		40			ns

18. For SPI access during power−down mode the period should be relaxed to 100 ns
19. For a figure showing the SPI timing parameters see section: Serial Peripheral Interface (SPI).

Table 14. WIRE MODE INTERFACE TIMING

Symbol	Description	Condition	Min	Typ	Max	Unit
Tdck	SEL falling edge to CLK rising edge	Depends on bit rate programming	1.6		10.000	ms
Tdcl	DCLK low duration		25		75	%
Tdch	DCLK high duration		25		75	%
Tds	DATA setup time relative to active DCLK edge		10			ns
Tdh	DATA hold time relative to active DCLK edge		10			ns
Tdco	DATA output change relative to active DCLK edge				10	ns

20. For a figure showing the wire mode interface timing parameters see section: Wire Mode Interface.

Table 15. GENERAL PURPOSE ADC (GPADC)

Symbol	Description	Condition	Min	Typ	Max	Unit
Res	Nominal ADC resolution			12		bit
F_{conv}	Conversion rate		0.03		1	MS/s
DR	Dynamic range			72		dB
INL	Integral nonlinearity			±1.5		LSB
DNL	Differential nonlinearity			±1.5		LSB
Z_{in}	Input impedance			50		kΩ
V_{DC-IN}	Input DC level			0.8		V
$V_{IN-DIFF}$	Input signal range (differential)		−500		500	mV
V_{IN-SE}	Input signal range (single−ended, signal input at pin GPADC1, pin GPADC2 open)		300		1300	mV

CIRCUIT DESCRIPTION

The AX5044 is a true single chip ultra−low power narrow−band CMOS RF transceiver for use in licensed and unlicensed bands from 60 to 1050 MHz. The on−chip transceiver consists of a fully integrated RF front−end with modulator, and demodulator. Base band data processing is implemented in an advanced and flexible communication controller that enables user friendly communication via the SPI interface.

AX5044 can be operated from a 1.8 V to 3.6 V power supply over a temperature range of −40°C to 85°C. It consumes 48 mA for transmitting at 868 MHz carrier frequency at 14 dBm, TBD mA for transmitting at 169 MHz. In receive operation RX 5045 consumes TBD mA at 868 MHz carrier frequency and TBD mA at 169 MHz. The AX5044 features make it an ideal interface for integration into various battery powered solutions such as ticketing or as transceiver for telemetric applications e.g. in sensors. As primary application, the transceiver is intended for UHF radio equipment in accordance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220−1 and the US Federal Communications Commission (FCC) standard Title 47 CFR Part 15 as well as Part 90. AX5044 is compliant with respective narrow−band regulations. Additionally AX5044 is suited for systems targeting compliance with Wireless M−Bus standard EN 13757−4:2005. Wireless M−Bus frame support (S, T, R) is built−in.

AX5044 supports any data rate from 0.1 kbps to 200 kbps for FSK, 4−FSK, GFSK, GMSK, MSK, ASK and PSK. To achieve optimum performance for specific data rates and modulation schemes several register settings to configure the AX5044 are necessary, for details see the RadioLab Software which calculates the necessary register settings and the AX5044 Programming Manual.

The AX5044 can be operated in two fundamentally different modes.

In **frame mode** data is sent and received via the SPI port in frames. Pre−and post−ambles as well as checksums can be generated automatically. Interrupts control the data flow between a micro−controller and the AX5044.

In **wire mode** the IC behaves as an extension of any wire. The internal communication controller is disabled and the modem data is directly available on a dedicated pin (DATA). The bit clock is also output on a dedicated pin (DCLK). In this mode the user can connect the data pin to any port of a micro−controller or to a UART, but has to control coding, checksums, pre and post ambles. The user can choose between synchronous and asynchronous wire mode, asynchronous wire mode performs RS232 start bit recognition and re−synchronization for transmit.

Both modes can be used both for transmit and receive. In both cases the AX5044 behaves as a SPI slave interface. Configuration of the AX5044 is always done via the SPI interface.

The receiver and the transmitter support multi−channel operation for all data rates and modulation schemes.

Voltage Regulators

The AX5044 uses an on−chip voltage regulator system to create stable supply voltages for the internal circuitry from the primary supply VDD_IO. The I/O level of the digital pins is VDD_IO.

Pins VDD_ANA are supplied for external decoupling of the power supply used for the on−chip PA.

The voltage regulator system must be set into the appropriate state before receive or transmit operations can be initiated. This is handled automatically when programming the device modes via the PWRMODE register.

Register POWSTAT contains status bits that can be read to check if the regulated voltages are ready (bit SVIO) or if VDD_IO has dropped below the brown−out level of 1.3 V (bit SSUM).

In power−down mode the core supply voltages for digital and analog functions are switched off to minimize leakage power. Most register contents are preserved but access to the FIFO is not possible and FIFO contents are lost. SPI access to registers is possible, but at lower speed.

In deep−sleep mode all supply voltages are switched off. All digital and analog functions are disabled. All register contents are lost. To leave deep−sleep mode the pin SEL has to be pulled low. This will initiate startup and reset of the AX5044. Then the MISO line should be polled, as it will be held low during initialization and will rise to high at the end of the initialization, when the chip becomes ready for operation.

Crystal Oscillator nd TCXO Interface

The AX5044 is normally operated with an external TCXO, which is required by most narrow−band regulations with a tolerance of 0.5 ppm to 1.5 ppm depending on the regulatory requirements. The on−chip crystal oscillator allows the use of an inexpensive quartz crystal as the RF generation subsystem's timing reference when possible from a regulatory point of view.

A wide range of crystal frequencies can be handled by the crystal oscillator circuit. As the reference frequency impacts both the spectral performance of the transmitter as well as the current consumption of the receiver, the choice of reference frequency should be made according to the regulatory regime targeted by the application.

The crystal or TCXO reference frequency should be chosen so that the RF carrier frequency is not an integer multiple of the crystal or TCXO frequency.

The oscillator circuit is enabled by programming the PWRMODE register. At power−up it is disabled. By default the oscillator circuit expects a TCXO to be connected to the

CLK16P pin, while CLK16N has to be left unconnected. No special register settings are required.

Alternatively a quartz crystal can be connected. To adjust the circuit's characteristics to the crystal being used, without using additional external components, the tuning capacitance of the crystal oscillator can be programmed. The transconductance of the oscillator is automatically regulated, to allow for fastest start−up times together with lowest power operation during steady−state oscillation.

The integrated programmable tuning capacitor bank makes it possible to connect the oscillator directly to pins CLK16N and CLK16P without the need for external capacitors. It is programmed using bits XTALCAP[5:0] in register XTALCAP.

To synchronize the receiver frequency to a carrier signal, the oscillator frequency could be tuned using the capacitor bank however, the recommended method to implement frequency synchronization is to make use of the high resolution RF frequency generation sub−system together with the Automatic Frequency Control, both are described further down.

Low Power Oscillator and Wake−on−Radio (WOR) Mode

The AX5044 features an internal lowest power fully integrated oscillator. In default mode the frequency of oscillation is 640 Hz +/− 1.5%, in fast mode it is 10.2 kHz +_/− 1.5%. These accuracies are reached after the internal hardware has been used to calibrate the low power oscillator versus the RF reference clock. This procedure can be run in the background during transmit or receive operations.

The low power oscillator makes a WOR mode with a power consumption of 500 nA possible.

If Wake on Radio Mode is enabled, the receiver wakes up periodically at a user selectable interval, and checks for a radio signal on the selected channel. If no signal is detected, the receiver shuts down again. If a radio signal is detected, and a valid packet is received, the microcontroller is alerted by asserting an interrupt.

The AX5044 can thus autonomously poll for radio signals, while the micro−controller can stay powered down, and only wakes up once a valid packet is received. This allows for very low average receiver power, at the expense of longer preambles at the transmitter.

GPIO Pins

Pins DATA, DCLK,SYSCLK, IRQ, ANTSEL, PWRAMP can be used as general purpose I/O pins by programming pin configuration registers PINFUNCSYSCLK, PINFUNCDCLK, PINFUNCDATA, PINFUNCIRQ, PINFUNCNANTSEL, PINFUNCPWRAMP. Pin input values can be read via register PINSTATE. Pull−ups are disabled if output data is programmed to the GPIO pin.

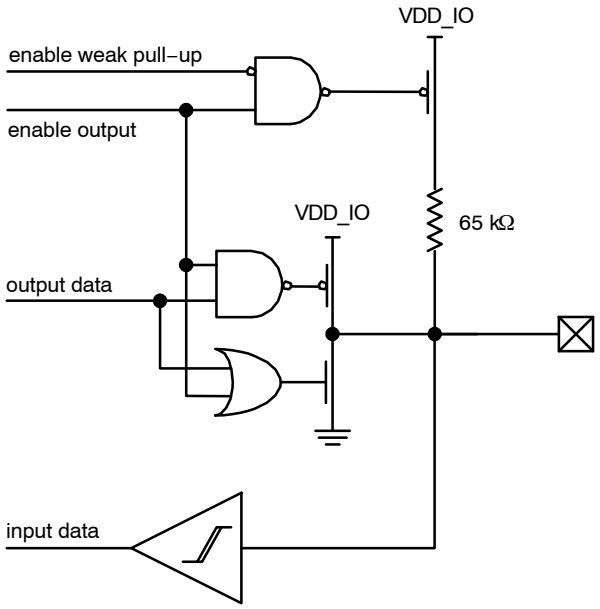


Figure 3. GPIO Pin

SYSCLK Output

The SYSCLK pin outputs either the reference clock signal divided by a programmable power of two or the low power oscillator clock. Division ratios from 1 to 1024 are possible. For divider ratios > 1 the duty cycle is 50%. Bits SYSCLK[4:0] in the PINFUNCSYSCLK register set the divider ratio. By default the SYSCLK output is disabled.

Power−on−Reset (POR)

AX5044 has an integrated power−on−reset block. No external POR circuit is required.

After POR the AX5044 can be reset by first setting the SPI SEL pin to high for at least 100 ns, then setting followed by resetting the bit RST in the PWRMODE register.

After POR or reset all registers are set to their default values.

RF Frequency Generation Subsystem

The RF frequency generation subsystem consists of a fully integrated synthesizer, which multiplies the reference frequency from the crystal oscillator to get the desired RF frequency. The advanced architecture of the synthesizer enables frequency resolutions of 1 Hz, as well as fast settling times of 5 – 50 μs depending on the settings (see section AC Characteristics). Fast settling times mean fast start−up and fast RX/TX switching, which enables low−power system design.

For receive operation the RF frequency is fed to the mixer, for transmit operation to the power−amplifier.

The frequency must be programmed to the desired carrier frequency.

The synthesizer loop bandwidth can be programmed, this serves three purposes:

1. Start−up time optimization, start−up is faster for higher synthesizer loop bandwidths.
2. TX spectrum optimization, phase−noise at 300 kHz to 1 MHz distance from the carrier improves with lower synthesizer loop bandwidths.
3. Adaptation of the bandwidth to the data−rate. For transmission of FSK and MSK it is required that the synthesizer bandwidth must be in the order of the data−rate.

VCO

An on−chip VCO converts the control voltage generated by the charge pump and loop filter into an output frequency. This frequency is used for transmit as well as for receive operation. The frequency can be programmed in 1 Hz steps in the FREQ registers. The RFDIV bits in the PLLVCODIV register must be programmed to the desired frequency band.

The fully integrated VCO allows to operate the device in the frequency range 60 – 1050 MHz.

VCO Auto−Ranging

The AX5044 has an integrated auto−ranging function, which allows to set the correct VCO range for specific frequency generation subsystem settings automatically. Typically it has to be executed after power−up. The function is initiated by setting the RNG_START bit in the PLLRANGINGA or PLLRANGINGB register. The bit is readable and a 0 indicates the end of the ranging process. Setting RNG_START in the PLLRANGINGA register ranges the frequency in FREQA, while setting RNG_START in the PLLRANGINGB register ranges the frequency in FREQB. The RNGERR bit indicates the correct execution of the auto−ranging.

Loop Filter and Charge Pump

The AX5044 internal loop filter configuration together with the charge pump current sets the synthesizer loop band width. The internal loop−filter has three configurations that can be programmed via the register bits FLT[1:0] in registers PLLLOOP or PLLLOOPBOOST the charge pump current can be programmed using register bits PLLCPI[7:0] in registers PLLCPI or PLLCPIBOOST. Synthesizer bandwidths are typically 50 – 500 kHz depending on the PLLLOOP or PLLLOOPBOOST settings, for details see the section: AC Characteristics.

The AX5044 can be setup in such a way that when the synthesizer is started, the settings in the registers PLLLOOPBOOST and PLLCPIBOOST are applied first for a programmable duration before reverting to the settings in PLLLOOP and PLLCPI. This feature enables automated fastest start−up.

Setting bits FLT[1:0] = 00 bypasses the internal loop filter and the VCO control voltage is output to an external loop filter at pin FILT. This mode of operation is recommended for achieving lower bandwidths than with the internal loop filter.

Registers

See Table 16.

Table 16. RF FREQUENCY GENERATION REGISTERS

Register	Bits	Purpose
PLLLOOP PLLLOOPBOOST	FLT[1:0]	Synthesizer loop filter bandwidth and selection of external loop filter, recommended usage is to increase the bandwidth for faster settling time, bandwidth increases of factor 2 and 5 are possible.
PLLCPI PLLCPIBOOST		Synthesizer charge pump current, recommended usage is to decrease the bandwidth (and improve the phase−noise) for low data−rate transmissions.
PLLVCODIV	REFDIV	Sets the synthesizer reference divider ratio.
	RFDIV	Sets the synthesizer output divider ratio.
FREQA, FREQB		Programming of the carrier frequency.
PLLRANGINGA, PLLRANGINGB		Initiate VCO auto−ranging and check results.

RF Input and Output Stage (ANTP/ANTN/ANTP1)

RX uses differential pins ANTP and ANTN. TX uses the single ended antenna pin ANTP1. RX/TX switching can be done either with an external RX/TX switch or with a direct tie configuration.

Pin PWRAMP can be used to control an external RX/TX switch. Pin ANTSEL can be used to control an external antenna switch when receiving with two antennas.

When antenna diversity is enabled, the radio controller will, when not in the middle of receiving a packet, periodically probe both antennas and select the antenna with the highest signal strength. The radio controller can be instructed to periodically write both RSSI values into the FIFO. Antenna diversity mode is fully automatic.

LNA

The LNA amplifies the differential RF signal from the antenna and buffers it to drive the I/Q mixer. An external matching network is used to adapt the antenna impedance to the IC impedance. A DC feed to GND must be provided at the antenna pins (ANTP & ANTN). For recommendations see section: Application Information.

PA

In TX mode the PA is configurable to drive the signal out onto either the single−ended antenna pin ANTP1, or the differential antenna pin pair, ANTP/ANTN. This is controlled in register MODCFGA by appropriately setting TXDIFF and TXSE bits.

The output power of the PA is programmed via the register TXPWRCOEFFB.

The PA can be digitally pre−distorted for high linearity.

The output amplitude can be shaped (raised cosine), this mode is selected with bit AMPLSHAPE in register MODCFGA. PA ramping is programmable in increments of the bit time and can be set to 1 – 8 bit times via bits SLOWRAMP in register MODCFGA.

Output power as well as harmonic content will depend on the external impedance seen by the PA, recommendations are given in the section: Application Information.

Digital IF Channel Filter and Demodulator

The digital IF channel filter and the demodulator extract the data bit−stream from the incoming IF signal. They must be programmed to match the modulation scheme as well as the data−rate. Inaccurate programming will lead to loss of sensitivity.

The channel filter offers bandwidths of 119 Hz up to 221 kHz (with reference frequencies above 16 MHz higher bandwidths may be possible).

The RadioLab Software calculates the necessary register settings for optimal performance and details can be found in the AX5044 Programming Manual. An overview of the registers involved is given in the following Table 17 as reference. The register setups typically must be done once at power−up of the device.

Registers

See Table 17.

Table 17. CHANNEL FILTER AND DEMODULATOR REGISTERS

Register	Remarks
DECIMATION	This register programs the bandwidth of the digital channel filter.
RXDATARATE2… RXDATARATE0	These registers specify the receiver bit rate, relative to the channel filter bandwidth.
MAXDROFFSET2… MAXDROFFSET0	These registers specify the maximum possible data rate offset.
MAXRFOFFSET2… MAXRFOFFSET0	These registers specify the maximum possible RF frequency offset
TIMEGAIN, DRGAIN	These registers specify the aggressiveness of the receiver bit timing recovery. More aggressive settings allow the receiver to synchronize with shorter preambles, at the expense of more timing jitter and thus a higher bit error rate at a given signal−to−noise ratio.
MODULATION	This register selects the modulation to be used by the transmitter and the receiver, i.e. whether ASK, FSK, PSK should be used.
PHASEGAIN, FREQGAINA, FREQGAINB, FREQGAINC, FREQGAIND, AMPLGAIN	These registers control the bandwidth of the phase, frequency offset and amplitude tracking loops.
AGCINCREASE, AGCREDUCE	These register controls the AGC (automatic gain control) loop slopes, and thus the speed of gain adjustments. The faster the bit−rate, the faster the AGC loop should be.
TXRATE	These registers control the bit rate of the transmitter.
FSKDEV	These registers control the frequency deviation of the transmitter in FSK mode. The receiver does not explicitly need to know the frequency deviation, only the channel filter bandwidth has to be set wide enough for the complete modulation to pass.

Encoder

The encoder is located between the Framing Unit, the Demodulator and the Modulator. It can optionally transform the bit−stream in the following ways:

- It can invert the bit stream. In 4−FSK mode, inversion for the LSB and MSB of a DiBit symbol can be set independently.
- It can perform differential encoding. This means that a zero is transmitted as no change in the level, and a one is transmitted as a change in the level.
- It can perform Manchester encoding. Manchester encoding ensures that the modulation has no DC content and enough transitions (changes from 0 to 1 and from 1 to 0) for the demodulator bit timing recovery to function correctly, but does so at a doubling of the data rate.
- It can perform spectral shaping (also known as whitening). Spectral shaping removes DC content of the bit stream, ensures transitions for the demodulator bit timing recovery, and makes sure that the transmitted spectrum does not have discrete lines even if the transmitted data is cyclic. It does so without adding additional bits, i.e. without changing the data rate. Spectral Shaping uses a feedback shift register which can selectively implement the polynomials PN9, PN15 and PN17. Available options are both additive (synchronous) or multiplicative (self−synchronizing) scrambling.

The encoder is programmed using the register ENCODING, details and recommendations on usage are given in the AX5044 Programming Manual.

Framing and FIFO

Most radio systems today group data into packets. The framing unit is responsible for converting these packets into a bit−stream suitable for the modulator, and to extract packets from the continuous bit−stream arriving from the demodulator.

The Framing unit supports two different modes:

- Packet modes
- Raw modes

The micro−controller communicates with the framing unit through a 256 byte FIFO. Data in the FIFO is organized in Chunks. The chunk header encodes the length and what data is contained in the payload. Chunks may contain packet data, but also RSSI, Frequency offset, Timestamps, etc.

The AX5044 contains one FIFO. Its direction is switched depending on whether transmit or receive mode is selected.

The FIFO can be operated in polled or interrupt driven modes. In polled mode, the microcontroller must periodically read the FIFO status register or the FIFO count register to determine whether the FIFO needs servicing.

In interrupt mode EMPTY, NOT EMPTY, FULL, NOT FULL and programmable level interrupts are provided. The AX5044 signals interrupts by asserting (driving high) its IRQ line. The interrupt line is level triggered, active high. Interrupts are acknowledged by removing the cause for the interrupt, i.e. by emptying or filling the FIFO.

Basic FIFO status (EMPTY, FULL, Overrun, Underrun, FIFO fill level above threshold, FIFO free space above threshold) are also provided during each SPI access on MISO while the micro−controller shifts out the register address on MOSI. See the SPI interface section for details. This feature significantly reduces the number of SPI accesses necessary during transmit and receive.

Packet Modes

The AX5044 offers different packet modes. For arbitrary packet sizes HDLC is recommended due to its automated flag and bit−stuffing mechanism. The AX5044 also offers packet modes with fixed packet length with up to 12 bits indicating the length of the packet.

In packet modes a cyclic redundancy check (CRC) can be computed automatically.

HDLC Mode is the main framing mode of the AX5044. In this mode, the AX5044 performs automatic packet delimiting, and optional packet correctness check by inserting and checking a CRC field.

NOTE: HDLC mode follows High−Level Data Link Control (HDLC, ISO 13239) protocol.

The packet structure is given in the following Table 18.

Table 18. HDLC PACKET STRUCTURE

Flag	Address	Control	Information	FCS	Flag
8 bit	8 bit	8 or 16 bit	Variable length, 0 or more bits in multiples of 8	16/32 bit	8 bit

21. The end flag of one frame can be used as the start flag of the next frame.

HDLC packets are delimited with flag sequences of content 0x7E.

In AX5044 the meaning of address and control is user defined. The Frame Check Sequence (FCS) can be programmed to be CRC−CCITT, CRC−16 or CRC−32.

The receiver checks the CRC, the result can be retrieved from the FIFO. In HDLC mode the CRC is always appended to the received data.

Another standardized mode supported by AX5044 is Wireless M−Bus, the packet structure is given in the following Table 19.

NOTE: Wireless M−Bus mode follows EN13757−4.

Table 19. WIRELESS M−BUS PACKET STRUCTURE

Preamble	L	C	M	A	FCS	Optional Data Block (optionally repeated with FCS)	FCS
variable	8 bit	8 bit	16 bit	48 bit	16 bit	8 – 96 bit	16 bit

For details on implementing an HDLC communication as well as Wireless M−Bus please use the RadioLab software and see the AX5044 Programming Manual.

Raw Modes

In Raw mode, the AX5044 does not perform any packet delimiting or byte synchronization. It simply serializes transmit bytes and de−serializes the received bit−stream and groups it into bytes. This mode is ideal for implementing legacy protocols in software.

Raw mode with preamble match is similar to raw mode. In this mode, however, the receiver does not receive anything until it detects a user programmable bit pattern (called the preamble) in the receive bit−stream. When it detects the preamble, it aligns the de−serialization to it.

AX5044 can search for up to two different preambles. Each preamble can be between 4 and 32 bits long.

RX AGC and RSSI

AX5044 features three receiver signal strength indicators (RSSI):

1. RSSI before the digital IF channel filter.
   The gain of the receiver is adjusted in order to keep the analog IF filter output level inside the working range of the ADC and demodulator. The register AGCCOUNTER contains the current value of the AGC and can be used as an RSSI. The step size of this RSSI is 0.75 dB. The value can be used as soon as the RF frequency generation sub−system has been programmed.
2. RSSI behind the digital IF channel filter.
   The register RSSI contains the current value of the RSSI behind the digital IF channel filter. The step size of this RSSI is 1 dB. It is possible to set an interrupt getting asserted when the RSSI exceeds or falls below a defined threshold value.
3. RSSI behind the digital IF channel filter – high accuracy.
   The demodulator also provides amplitude information in the TRK_AMPLITUDE register. By combining both the AGCCOUNTER and the TRK_AMPLITUDE registers, a high resolution (better than 0.1 dB) RSSI value can be computed at the expense of a few arithmetic operations on the micro−controller. The RadioLab Software calculates the necessary register settings for best performance. More details can be found in the AX5044 Programming Manual.

Modulator

Depending on the transmitter settings the modulator generates various inputs for the PA (see Table 20):

Table 20. MODULATIONS

Modulation	Bit = 0	Bit = 1	Main Lobe Bandwidth	Max. Bitrate
ASK	PA off	PA on	BW = BITRATE	200 kBit/s
FSK/MSK/GFSK/GMSK	$\Delta f = -f_{deviation}$	$\Delta f = +f_{deviation}$	BW = (1+h) × BITRATE	200 kBit/s
PSK	$\Delta\phi = 0°$	$\Delta\phi = 180°$	BW = BITRATE	200 kBit/s

NOTE: h = modulation index. It is the ratio of the deviation compared to the bit−rate; $f_{deviation}$ = 0.5VhVBITRATE, AX5044 can demodulate signals with h < 32
ASK = amplitude shift keying
FSK = frequency shift keying
MSK = minimum shift keying; MSK is a special case of FSK, where h = 0.5, and therefore $f_{deviation}$ = 0.25 BITRATE; the advantage of MSK over FSK is that it can be demodulated more robustly
PSK = phase shift keying

All modulation schemes, except 4−FSK, are binary.

Amplitude can be shaped using a raised cosine waveform. Amplitude shaping will also be performed for constant amplitude modulation ((G)FSK, (G)MSK) when ramping up and down the PA. Amplitude shaping should always be enabled.

Frequency shaping can either be hard (FSK, MSK), or Gaussian (GMSK, GFSK), with selectable BT = 0.3 or BT = 0.5.

Table 21. 4−FSK MODULATION

Modulation	DiBit = 00	DiBit = 01	DiBit = 11	DiBit = 10	Main Lobe Bandwidth	Max. Bitrate
4−FSK	$\Delta f = -3f_{deviation}$	$\Delta f = -f_{deviation}$	$\Delta f = +f_{deviation}$	$\Delta f = +3f_{deviation}$	BW = (1 + 3 h) × BITRATE	200 kBit/s

4−FSK Frequency shaping is always hard.

Automatic Frequency Control (AFC)

The AX5044 features an automatic frequency tracking loop which is capable of tracking the transmitter frequency within the RX filter band width. On top of that the AX5044 has a frequency tracking register TRKRFFREQ to synchronize the receiver frequency to a carrier signal. For AFC adjustment, the frequency offset can be computed with the following formula:

$$\Delta f = \frac{TRKRFFREQ}{2^{24}} \times f_{XTAL} \qquad \text{(eq. 1)}$$

The pull−in range of the AFC can be programmed with the MAXRFOFFSET Registers.

PWRMODE Register

The PWRMODE register controls, which parts of the chip are operating.

Table 22. PWRMODE REGISTER

PWRMODE Register	Name	Description
0000	POWERDOWN	All digital and analog functions, except the register file, are disabled. The core supply voltages are switched off to conserve leakage power. Register contents are preserved and accessible registers via SPI, but at a slower speed. Access to the FIFO is not possible and the contents are not preserved. POWERDOWN mode is only entered once the FIFO is empty.
0001	DEEPSLEEP	AX5044 is fully turned off. All digital and analog functions are disabled. All register contents are lost. To leave DEEPSLEEP mode the pin SEL has to be pulled low. This will initiate startup and reset of the AX5044. Then the MISO line should be polled, as it will be held low during initialization and will rise to high at the end of the initialization, when the chip becomes ready for operation.
0101	STANDBY	The crystal oscillator and the reference are powered on; receiver and transmitter are off. Register contents are preserved and accessible registers via SPI. Access to the FIFO is not possible and the contents are not preserved. STANDBY is only entered once the FIFO is empty
0111	FIFO	The reference is powered on. Register contents are preserved and accessible registers via SPI. Access to the FIFO is possible and the contents are preserved.
1000	SYNTHRX	The synthesizer is running on the receive frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for receive.
1001	FULLRX	Synthesizer and receiver are running.
1011	WOR	Receiver wakeup−on−radio mode. The mode the same as POWERDOWN, but the 640 Hz internal low power oscillator is running.
1100	SYNTHTX	The synthesizer is running on the transmit frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for transmit.
1101	FULLTX	Synthesizer and transmitter are running. Do not switch into this mode before the synthesizer has completely settled on the transmit frequency (in SYNTHTX mode), otherwise spurious spectral transmissions will occur.

For the corresponding currents see Table 3.

Table 23. A TYPICAL PWRMODE SEQUENCE FOR A TRANSMIT SESSION

Step	PWRMODE	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3ms.
3	FULLTX	Data transmission.
4	POWERDOWN	

Table 24. A TYPICAL PWRMODE SEQUENCE FOR A RECEIVE SESSION

Step	PWRMODE [3:0]	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3ms.
3	FULLTX	Data reception.
4	POWERDOWN	

Serial Peripheral Interface

The AX5044 can be programmed via a four wire serial interface according SPI using the pins CLK, MOSI, MISO and SEL. Registers for setting up the AX5044 are programmed via the serial peripheral interface in all device modes.

When the interface signal SEL is pulled low, a configuration data stream is expected on the input signal pin MOSI, which is interpreted as D0...Dx, A0...Ax, R_N/W. Data read from the interface appears on MISO.

Figure 4 shows a write/read access to the interface. The data stream is built of an address byte including read/write information and a data byte. Depending on the R_N/W bit and address bits A[6..0], data D[7..0] can be written via MOSI or read at the pin MISO. R_N/W = 0 means read mode, R_N/W = 1 means write mode.

Most registers are 8 bits wide and accessed using the waveforms as detailed in Figure 5. The most important registers are at the beginning of the address space, i.e. at addresses less than 0x70. These registers can be accessed more efficiently using the short address form, which is detailed in Figure 4.

Some registers are longer than 8 bits. These registers can be accessed more quickly than by reading and writing individual 8 bit parts. This is illustrated in Figure 6. Accesses are not limited by 16 bits either, reading and writing data bytes can be continued as long as desired. After each byte, the address counter is incremented by one. This access form works with both, short and long addresses.

During the address phase of the access, the AX5044 outputs the most important status bits. This feature is designed to speed up the software decision on what to do in an interrupt handler.

The status bits contain the following information:

Table 25. SPI STATUS BITS

SPI Bit Cell	Status	Meaning/Register Bit
0	–	1 (when transitioning out of deep sleep mode, this bit transitions from 0 → 1 when the power becomes ready)
1	S14	PLL LOCK
2	S13	FIFO OVER
3	S12	FIFO OVER
4	S11	THRESHOLD FREE (FIFOFREE > FIFOTHRESH)
5	S10	THRESHOLD COUNT (FIFOCOUNT > FIFOTHRESH)
6	S9	FIFO FULL
7	S8	FIFO EMPTY
8	S7	PWRGOOD (not BROWNOUT)
9	S6	PWR INTERRUPT PENDING
10	S5	RADIO EVENT PENDING
11	S4	XTAL OSCILLATOR RUNNING
12	S3	WAKEUP INTERRUPT PENDING
13	S2	LPOSC INTERRUPT PENDING
14	S1	GPADC INTERRUPT PENDING
15	S0	internal

22. Bit cells 8 –15 (S7…S0) are only available in two address byte SPI access formats.

SPI Timing

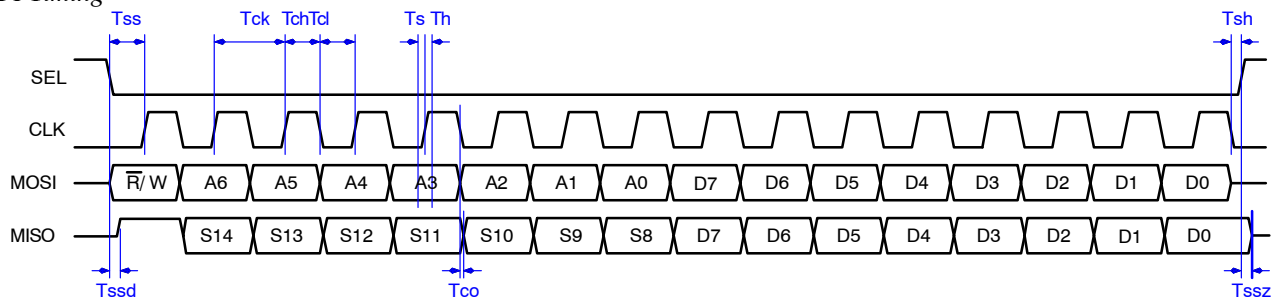


Figure 4. SPI 8 Bit Read/Write Access with Timing

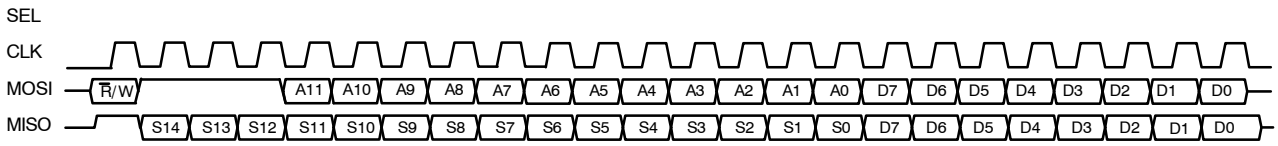


Figure 5. SPI 8 Bit Long Address Read/Write Access

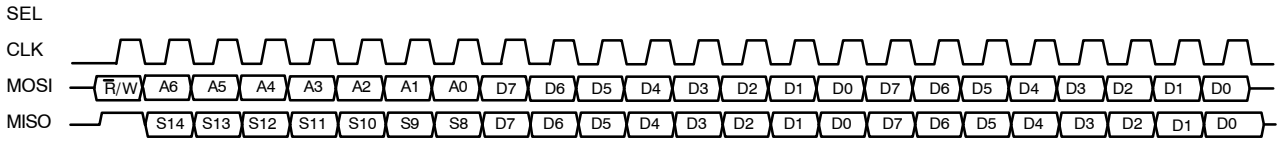


Figure 6. SPI 16 Bit Long Read/Write Access

Wire Mode Interface

In wire mode the transmitted or received data are transferred from and to the AX5044 using the pins DATA and DCLK. DATA is an input when transmitting and an output when receiving.

The direction (i.e. transmit or receive) can be chosen by programming the PWRMODE register.

Wire mode offers two variants: synchronous or asynchronous.

In synchronous wire mode the, the AX5044 always drives DCLK. Transmit data must be applied to DATA synchronously to DCLK, and receive data must be sampled synchronously to DCLK. Timing is given in Figure 7. In asynchronous wire mode, a low voltage RS232 type UART can be connected to DATA. DCLK is optional in this mode. The UART must be programmed to send two stop bits, but must be able to accept only one stop bit. Both the UART data rate and the AX5044 transmit and receive bit rate must match. The AX5044 synchronizes the RS232 signal to its internal transmission clock, by inserting or deleting a stop bit.

Wiremode is also available in 4−FSK mode. The two bits that encode one symbol are serialized on the DATA pin. The PWRAMP pin can be used as a synchronization pin to allow symbol (dibit) boundaries to be reconstructed. Gray coding is used to reduce the number of bit errors in case of a wrong decision. The RadioLab software calculates the necessary register settings for best performance and details can be found in the AX5044 Programming Manual.

Registers for setting up the AX5044 are programmed via the serial peripheral interface (SPI).

Wire Mode Timing

See Figure 7.

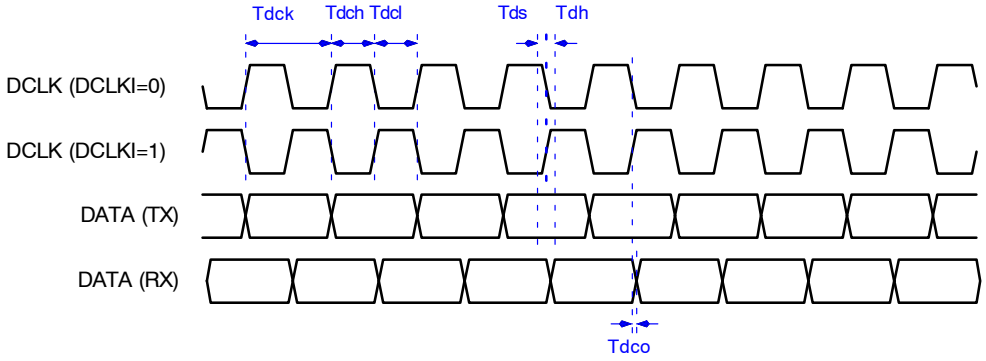


Figure 7. SPI 8 Bit Long Address Read/Write Access

General Purpose ADC (GPADC)

The AX5044 features a general purpose ADC. The ADC input pins are GPADC1 and GPADC2. The ADC converts the voltage difference applied between pins GPADC1 and GPADC2. If pin GPADC2 is left open, the ADC converts the difference between an internally generated value of 800 mV and the voltage applied at pin GPADC1.

The GPADC can only be used if the receiver is disabled. To enable the GPADC write 1 to the ENA bit in the GPADCCTRL register. To start a single conversion, write 1 to the BUSY bit in the GPADCCTRL register. Then wait for the BUSY bit to clear, or the GPADC Interrupt to be asserted.

The GPADC Interrupt is cleared by reading the result register GPADCVALUE.

If continuous sampling is desired, set the CONT bit in register GPADCCTRL. The desired sampling rate can be specified in the GPADCPERIOD register.

ΣΔDAC

One digital Pin (ANTSEL or PWRAMP) may be used as a ΣΔ Digital−to−Analog Converter (DAC). A simple RC lowpass filter is needed to smooth the output. The DAC may be used to output RSSI, many demodulator variables, or a constant value under software control.

REGISTER BANK DESCRIPTION

This section describes the bits of the register bank as reference. The registers are grouped by functional block to facilitate programming. The RadioLab software calculates the necessary register settings for best performance and details can be found in the AX5044 Programming Manual.

An R in the retention column means that this register's contents are not lost during power−down mode.

No checks are made whether the programmed combination of bits makes sense! Bit 0 is always the LSB.

NOTES: Whole registers or register bits marked as reserved should be kept at their default values.

All addresses not documented here must not be accessed, neither in reading nor in writing.

Table 26. CONTROL REGISTER MAP

Add	Name	Dir	Ret	Reset	Bit 7	6	5	4	3	2	1	0	Description
REVISION & INTERFACE PROBING													
000	REVISION	R	R	01010001	SILICONREV(7:0)								Silicon Revision
001	SCRATCH	RW	R	11000101	SCRATCH(7:0)								Scratch Register
OPERATING MODE													
002	PWRMODE	RW	R	011−0000	RST	XOEN	REFEN	WDS	PWRMODE(3:0)				Power Mode
VOLTAGE REGULATOR													
003	POWSTAT	R	R	————	SSUM	SREF	SVREF	SVANA	SVMODEM	SBEVANA	SBEVMODEM	SVIO	Power Management Status
004	POWSTICKYSTAT	R	R	————	SSSUM	SREF	SSVREF	SSVANA	SSVMODEM	SSBE-VANA	SSBEVMODEM	SSVIO	Power Management Sticky Status
005	POWIRQMASK	RW	R	00000000	MPWR GOOD	MSREF	MSVREF	MS VANA	MS VMO-DEM	MSBEVAN-A	MSBE VMODEM	MSVIO	Power Management Interrupt Mask
INTERRUPT CONTROL													
006	IRQMASK1	RW	R	—000000	–	IRQMASK(14:8)							IRQ Mask
007	IRQMASK0	RW	R	00000000	IRQMASK(7:0)								IRQ Mask
008	RADIO-EVENTM ASK1	RW	R	————0	–	–	–	–	–	–	–	RADIO EVENT MASK(8)	Radio Event Mask
009	RADIO-EVENTM ASK0	RW	R	00000000	RADIO EVENT MASK(7:0)								Radio Event Mask
00A	IRQINVERSION 1	RW	R	—000000	–	IRQINVERSION(14:8)							IRQ Inversion
00B	IRQINVERSION 0	RW	R	00000000	IRQINVERSION(7:0)								IRQ Inversion
00C	IRQREQUEST1	R	R	————	–	IRQREQUEST(14:8)							IRQ Request
00D	IRQREQUEST0	R	R	————	IRQREQUEST(7:0)								IRQ Request
00E	RADIOEVENTREQ1	R		————	–	–	–	–	–	–	–	RADIO EVENT REQ(8)	Radio Event Request
00F	RADIOEVENTREQ0	R		————	RADIO EVENT REQ(7:0)								Radio Event Request
MODULATION & FRAMING													
010	MODULATION	RW	R	——01000	–	–	–	RX HALF SPEED	MODULATION (3:0)				Modulation
011	ENCODING1	RW	R	———————0	–	–	–	–	–	–	–	ENC NOSYNC	Encoder/Decoder Settings
012	ENCODING0	RW	R	00000100	TI WHITEN-ING	ENC SCR-MODE	ENC SCRPOLY(1:0>		ENC MAN-CH	ENC SCRAM	ENC INV(1:0)		Encoder/Decoder Settings
013	FRAMING	RW	R	——−0000	FRMRX	–	–	–	FRMMODE (2:0)			FABORT	Framing settings
014	CRCCFG	RW	R	——−0000	–	–	–	–	CRCMODE (2:0)			CRCNOIN	CRC settings
015	CRCINIT3	RW	R	11111111	CRCINIT (31:24)								CRC Initialisation Data
016	CRCINIT2	RW	R	11111111	CRCINIT (23:16)								CRC Initialisation Data

Table 26. CONTROL REGISTER MAP (continued)

Add	Name	Dir	Ret	Reset	Bit 7	6	5	4	3	2	1	0	Description
MODULATION & FRAMING													
017	CRCINIT1	RW	R	11111111	CRCINIT (15:3)								CRC Initialisation Data
018	CRCINIT0	RW	R	11111111	CRCINIT (7:0)								CRC Initialisation Data
FORWARD ERROR CORRECTION													
019	FEC	RW	R	00000000	SHORT MEM	RSTVI TERBI	FEC NEG	FEC POS	FECINPSHIFT (2:0)			FEC ENA	FEC (Viterbi) Configuration
01A	FECSYNC	RW	R	01100010	FECSYNC (7:0)								Interleaver Synchronisation Threshold
01B	FECSTATUS	R	R	————	FEC INV	MAXMETRIC (6:0)							FEC Status
STATUS													
01C	RADIOSTATE	R	–	——0000	–	–	–	–	RADIOSTATE (3:0)				Radio Controller State
01D	XTALSTATUS	R	R	————	–	–	–	–	–	–	–	XTAL RUN	Crystal Oscillator Status
PIN CONFIGURATION													
020	PINSTATE	R	R	————	–	–	PS PWR AMP	PS ANT SEL	PS IRQ	PS DATA	PS DCLK	PS SYS CLK	Pinstate
021	PINFUNCSYSCLK	RW	R	0—01000	PU SYSCLK	–	–	PFSYSCLK(4:0)					SYSCLK Pin Function
022	PINFUNCDCLK	RW	R	00——100	PU DCLK	PI DCLK	–	–	–	PFDCLK(2:0)			DCLK Pin Function
023	PINFUNCDATA	RW	R	10——111	PU DATA	PI DATA	–	–	–	PFDATA(2:0)			DATA Pin Function
024	PINFUNCIRQ	RW	R	00——011	PU IRQ	PI IRQ	–	–	–	PFIRQ(2:0)			IRQ Pin Function
025	PINFUNCANTSEL	RW	R	00——110	PU ANTSEL	PI ANTSEL	–	–	–	PFANTSEL(2:0)			ANTSEL Pin Function
026	PINFUNCPWRAMP	RW	R	00—0110	PU PWRAMP	PI PWRAMP	–	–	PFPWRAMP(3:0)				PWRAMP Pin Function
027	PWRAMP	RW	R	————0	–	–	–	–	–	–	–	PWRAMP	PWRAMP Control
FIFO													
028	FIFOSTAT	R	R	0———	FIFO AUTO COMMIT	–	FIFO FREE THR	FIFO CNT THR	FIFO OVER	FIFO UNDER	FIFO FULL	FIFO EMPTY	FIFO Control
		W	R				FIFOCMD(5:0)						
029	FIFODATA	RW		————	FIFODATA(7:0)								FIFO Data
02A	FIFOCOUNT1	R	R	————0	–	–	–	–	–	–	–	FIFO COUNT(8)	Number of Words currently in FIFO
02B	FIFOCOUNT0	R	R	00000000	FIFOCOUNT(7:0)								Number of Words currently in FIFO
02C	FIFOFREE1	R	R	————1	–	–	–	–	–	–	–	FIFO FREE(8)	Number of Words that can be written to FIFO
02D	FIFOFREE0	R	R	00000000	FIFOFREE(7:0)								Number of Words that can be written to FIFO
02E	FIFOTHRESH1	RW	R	————0	–	–	–	–	–	–	–	FIFO THRESH (8)	FIFO Threshold
02F	FIFOTHRESH0	RW	R	00000000	FIFOTHRESH(7:0)								FIFO Threshold
SYNTHESIZER													
030	PLLLOOP	RW	R	0——1001	FREQB	–	–	–	DIRECT	FILT EN	FLT(1:0)		PLL Loop Filter Settings
031	PLLCPI	RW	R	00001000	PLLCPI								PLL Charge Pump Current (Boosted)
032	PLLRANGINGA1	RW	R	00000001	STICKY LOCK	PLL LOCK	RNGERR	RNG START	–	–	–	VCORA(8)	PLL Autoranging

Table 26. CONTROL REGISTER MAP (continued)

Add	Name	Dir	Ret	Reset	Bit 7	6	5	4	3	2	1	0	Description
SYNTHESIZER													
033	PLLRANGINGA0	RW	R	00000000	VCORA(7:0)								PLL Autoranging
034	FREQA3	RW	R	00111001	FREQA(31:24)								Synthesizer Frequency
035	FREQA2	RW	R	00110100	FREQA(23:16)								Synthesizer Frequency
036	FREQA1	RW	R	11001100	FREQA(15:8)								Synthesizer Frequency
037	FREQA0	RW	R	11001101	FREQA(7:0)								Synthesizer Frequency
038	PLLLOOPBOOS T	RW	R	0——1011	FREQB	–	–	–	DIRECT	FILT EN	FLT(1:0)		PLL Loop Filter Settings (Boosted)
039	PLLCPIBOOST	RW	R	11001000	PLLCPI								PLL Charge Pump Current
03A	PLLRANGINGB1	RW	R	00000001	STICKY LOCK	PLL LOCK	RNGERR	RNG START	–	–	–	VCORB(8)	PLL Autoranging
03B	PLLRANGINGB0	RW	R	00000000	VCORB(7:0)								PLL Autoranging
03C	FREQB3	RW	R	00111001	FREQB(31:24)								Synthesizer Frequency
03D	FREQB2	RW	R	00110100	FREQB(23:16)								Synthesizer Frequency
03E	FREQB1	RW	R	11001100	FREQB(15:8)								Synthesizer Frequency
03F	FREQB0	RW	R	11001101	FREQB(7:0)								Synthesizer Frequency
040	PLLVCODIV	RW	R	——0000	–	–	–	RFDIV			REFDIV(1:0)		PLL Divider Settings
SIGNAL STRENGTH													
041	RSSI	R	R	————	RSSI(7:0)								Received Signal Strength Indicator
042	BGNDRSSI	RW	R	00000000	BGNDRSSI(7:0)								Background RSSI
043	DIVERSITY	RW	R	———00	–	–	–	–	–	–	ANT SEL	DIV ENA	Antenna Diversity Configuration
043	AGCCOUNTER	RW	R	--------	AGCCOUNTER (7:0)								AGC Current Value
RECEIVER TRACKING													
045	TRKDATARATE2	R	R	————	TRKDATARATE(23:16)								Datarate Tracking
046	TRKDATARATE1	R	R	————	TRKDATARATE(15:8)								Datarate Tracking
047	TRKDATARATE0	R	R	————	TRKDATARATE(7:0)								Datarate Tracking
048	TRKAMPL1	R	R	————	TRKAMPL (15:8)								Amplitude Tracking
049	TRKAMPL0	R	R	————	TRKAMPL (7:0)								Amplitude Tracking
04A	TRKPHASE1	R	R	————	–	–	–	–	TRKPHASE(11:8)				Phase Tracking
04B	TRKPHASE0	R	R	————	TRKPHASE (7:0)								Phase Tracking
04D	TRKRFFREQ2	RW	R	————	–	–	–	–	TRRFKFREQ(19:16)				RF Frequency Tracking
04E	TRKRFFREQ1	RW	R	————	TRRFKFREQ(15:8)								RF Frequency Tracking
04F	TRKRFFREQ0	RW	R	————	TRRFKFREQ(7:0)								RF Frequency Tracking
050	TRKFREQ1	RW	R	————	TRKFREQ(15:8)								Frequency Tracking
051	TRKFREQ0	RW	R	————	TRKFREQ(7:0)								Frequency Tracking
052	TRKFSKDEMOD1	R	R	————	–	–	TRKFSKDEMOD(13:8)						FSK Demodulator Tracking

Table 26. CONTROL REGISTER MAP (continued)

Add	Name	Dir	Ret	Reset	Bit 7	6	5	4	3	2	1	0	Description
RECEIVER TRACKING													
053	TRKFSKDEMOD0	R	R	————	TRKFSKDEMOD(7:0)								FSK Demodulator Tracking
054	TRKAFSKDEMOD1	R	R	————	TRKAFSKDEMOD(15:8)								AFSK Demodulator Tracking
055	TRKAFSKDEMOD0	R	R	————	TRKAFSKDEMOD(7:0)								AFSK Demodulator Tracking
TIMER													
059	TIMER2	R	–	————	TIMER(23:16)								1MHz Timer
05A	TIMER1	R	–	————	TIMER(15:8)								1MHz Timer
05B	TIMER0	R	–	————	TIMER(7:0)								1MHz Timer
WAKEUP TIMER													
068	WAKEUPTIMER 1	R	R	————	WAKEUPTIMER(15:8)								Wakeup Timer
069	WAKEUPTIMER 0	R	R	————	WAKEUPTIMER(7:0)								Wakeup Timer
06A	WAKEUP1	RW	R	00000000	WAKEUP(15:8)								Wakeup Time
06B	WAKEUP0	RW	R	00000000	WAKEUP(7:0)								Wakeup Time
06C	WAKEUPFREQ 1	RW	R	00000000	WAKEUPFREQ(15:8)								Wakeup Frequency
06D	WAKEUPFREQ 0	RW	R	00000000	WAKEUPFREQ(7:0)								Wakeup Frequency
06E	WAKEUPXOEARLY	RW	R	00000000	WAKEUPXOEARLY								Wakeup Crystal Oscillator Early
DSPmode2													
06F	DSPMODESHREG	RW		————	DSPMODESHREG								DSPmode SPI Shift Register Access
PHYSICAL LAYER PARAMETERS													
RECEIVER PARAMETERS													
100	IFFREQ1	RW	R	00010001	IFFREQ(15:8)								2nd LO / IF Frequency
101	IFFREQ0	RW	R	00100111	IFFREQ(7:0)								2nd LO / IF Frequency
102	DECIMATION1	RW	R	———00	–	–	–	–	–	–	DECIMATION(9:8)		Decimation Factor
103	DECIMATION0	RW	R	00001101	DECIMATION(7:0)								Decimation Factor
104	RXDATARATE2	RW	R	00000000	RXDATARATE(23:16)								Receiver Datarate
105	RXDATARATE1	RW	R	00111101	RXDATARATE(15:8)								Receiver Datarate
106	RXDATARATE0	RW	R	10001010	RXDATARATE(7:0)								Receiver Datarate
107	MAXDROFFSET2	RW	R	00000000	MAXDROFFSET(23:16)								Maximum Receiver Datarate Offset
108	MAXDROFFSET1	RW	R	00000000	MAXDROFFSET(15:8)								Maximum Receiver Datarate Offset
109	MAXDROFFSET0	RW	R	10011110	MAXDROFFSET(7:0)								Maximum Receiver Datarate Offset
10A	MAXRFOFFSET 2	RW	R	0——0000	FREQOESS	–	–	–	MAXRFOFFSET(19:16)				Maximum Receiver RF Offset
10B	MAXRFOFFSET 1	RW	R	00010110	MAXRFOFFSET(15:8)								Maximum Receiver RF Offset
10C	MAXRFOFFSET 0	RW	R	10000111	MAXRFOFFSET(7:0)								Maximum Receiver RF Offset
10D	FSKDMAX1	RW	R	00000000	FSKDEVMAX(15:8)								Four FSK Rx Deviation
10E	FSKDMAX0	RW	R	10000000	FSKDEVMAX(7:0)								Four FSK Rx Deviation
10F	FSKDMIN1	RW	R	11111111	FSKDEVMIN(15:8)								Four FSK Rx Deviation

Table 26. CONTROL REGISTER MAP (continued)

Add	Name	Dir	Ret	Reset	Bit 7	6	5	4	3	2	1	0	Description
RECEIVER PARAMETERS													
110	FSKDMIN0	RW	R	10000000	FSKDEVMIN(7:0)								Four FSK Rx Deviation
111	AFSKSPACE1	RW	R	——0000	–	–	–	–	AFSKSPACE(11:8)				AFSK Space (0) Frequency
112	AFSKSPACE0	RW	R	01000000	AFSKSPACE(7:0)								AFSK Space (0) Frequency
113	AFSKMARK1	RW	R	——0000	–	–	–	–	AFSKMARK(11:8)				AFSK Mark (1) Frequency
114	AFSKMARK0	RW	R	01110101	AFSKMARK(7:0)								AFSK Mark (1) Frequency
115	AFSKCTRL	RW	R	——00100	–	–	–	AFSKSHIFT0(4:0)					AFSK Control
116	AMPLFILTER	RW	R	——0000	–	–	–	–	AMPLFILTER(3:0)				Amplitude Filter
117	RFZIGZAGAMPL	RW	R	0000000	ZIGZAGAMPLEXP(3:0)				ZIGZAGAMPLMANT(3:0)				RF Zigzag Scanner Amplitude Exponent and Mantissa
118	RFZIGZAGFREQ	RW	R	0000000	ZIGZAGFREQ(7:0)								RF Zigzag Scanner Amplitude Exponent and Mantissa
119	RFFREQUENCYLEAK	RW	R	——00000	–	–	–	RFFREQUENCYLEAK[4:0]					RF Frequency Recovery Loop Leakiness
11A	FREQUENCYLEAK	RW	R	0——0000	PH HALF ACC	–	–	–				FREQUENCYLEAK[3:0]	Baseband Frequency Recovery Loop Leakiness
11B	RXPARAMSETS	RW	R	00000000	RXPS3(1:0)		RXPS2(1:0)		RXPS1(1:0)		RXPS0(1:0)		Receiver Parameter Set Indirection
11C	RXPARAMCURSET	R	R	————	–	–	–	RXSI(2)	RXSN(1:0)		RXSI(1:0)		Receiver Parameter Current Set
11D	RSSIIRQTHRESH	RW	R	0000000	RSSIIRQTHRESH(7:0)								RSSI Interrupt Threshold
11E	RSSIIRQDIR	RW	R	———0	–	–	–	–	–	–	–	RSSIIRQDIR	RSSI Interrupt Threshold Direction
RECEIVER PARAMETER SET 0													
120	AGCTARGET0	RW	R	01110110	AGCTARGET0(7:0)								AGC Target
121	AGCINCREASE0	RW	R	10110100	AGCDECAY0(4:0)					AGCMINDA0(2:0)			AGC Gain Increase Settings
122	AGCREDUCE0	RW	R	00100000	AGCATTACK0(4:0)					AGCMAXDA0(2:0)			AGC Gain Reduce Settings
123	AGCAHYST0	RW	R	———000	–	–	–	–	–	AGCAHYST0(2:0)			AGC Digital Threshold Range
124	TIMEGAIN0	RW	R	11111000	TIMEGAIN0M				TIMEGAIN0E				Timing Gain
125	DRGAIN0	RW	R	11110010	DRGAIN0M				DRGAIN0E				Data Rate Gain
126	PHASEGAIN0	RW	R	11——0011	FILTERIDX0(1:0)		–	–	PHASEGAIN0(3:0)				Filter Index, Phase Gain
127	FREQGAINA0	RW	R	00001111	FREQ LIM0	FREQ MODULO0	FREQ HALFMOD0	FREQ AMPL GATE0	FREQGAINA0(3:0)				Frequency Gain A
128	FREQGAINB0	RW	R	00–11111	FREQ FREEZE0	FREQ AVG0	–	FREQGAINB0(4:0)					Frequency Gain B
129	FREQGAINC0	RW	R	——01010	–	–	–	FREQGAINC0(4:0)					Frequency Gain C
12A	FREQGAIND0	RW	R	0——01010	RFFREQ FREEZE0	–	–	FREQGAIND0(4:0)					Frequency Gain D
12B	AMPLGAIN0	RW	R	01——0110	AMPL AVG	AMPL AGC	–	–	AMPLGAIN0(3:0)				Amplitude Gain
12C	FREQDEV10	RW	R	——0000	–	–	–	–	FREQDEV0(11:8)				Receiver Frequency Deviation
12D	FREQDEV00	RW	R	00100000	FREQDEV0(7:0)								Receiver Frequency Deviation

Table 26. CONTROL REGISTER MAP (continued)

Add	Name	Dir	Ret	Reset	Bit 7	6	5	4	3	2	1	0	Description
RECEIVER PARAMETER SET 0													
12E	FOURFSK0	RW	R	——10110	–	–	–	DEV UPDATE0	DEVDECAY0(3:0)				Four FSK Control
12F	BBOFFSRES0	RW	R	10001000	RESINTB0(3:0)				RESINTA0(3:0)				Baseband Offset Compensation Resistors
RECEIVER PARAMETER SET 1													
130	AGCTARGET1	RW	R	01110110	AGCTARGET1(7:0)								AGC Target
131	AGCINCREASE1	RW	R	10110100	AGCDECAY1(4:0)					AGCMINDA1(2:0)			AGC Gain Increase Settings
132	AGCREDUCE1	RW	R	00100000	AGCATTACK1(4:0)					AGCMAXDA1(2:0)			AGC Gain Reduce Settings
133	AGCAHYST1	RW	R	———000	–	–	–	–	–	AGCAHYST1(2:0)			AGC Digital Threshold Range
134	TIMEGAIN1	RW	R	11110110	TIMEGAIN1M				TIMEGAIN1E				Timing Gain
135	DRGAIN1	RW	R	11110001	DRGAIN1M				DRGAIN1E				Data Rate Gain
136	PHASEGAIN1	RW	R	11—0011	FILTERIDX1(1:0)		–	–	PHASEGAIN1(3:0)				Filter Index, Phase Gain
137	FREQGAINA1	RW	R	00001111	FREQ LIM1	FREQ MODULO1	FREQ HALFMOD1	FREQ AMPL GATE1	FREQGAINA1(3:0)				Frequency Gain A
138	FREQGAINB1	RW	R	00–11111	FREQ FREEZE1	FREQ AVG1	–	FREQGAINB1(4:0)					Frequency Gain B
139	FREQGAINC1	RW	R	——01011	–	–	–	FREQGAINC1(4:0)					Frequency Gain C
13A	FREQGAIND1	RW	R	0—01011	RFFREQ FREEZE1	–	–	FREQGAIND1(4:0)					Frequency Gain D
13B	AMPLGAIN1	RW	R	01—0110	AMPL AVG1	AMPL1 AGC1	–	–	AMPLGAIN1(3:0)				Amplitude Gain
13C	FREQDEV11	RW	R	———0000	–	–	–	–	FREQDEV1(11:8)				Receiver Frequency Deviation
13D	FREQDEV01	RW	R	00100000	FREQDEV1(7:0)								Receiver Frequency Deviation
13E	FOURFSK1	RW	R	——11000	–	–	–	DEV UPDATE1	DEVDECAY1(3:0)				Four FSK Control
13F	BBOFFSRES1	RW	R	10001000	RESINTB1(3:0)				RESINTA1(3:0)				Baseband Offset Compensation Resistors
RECEIVER PARAMETER SET 2													
140	AGCTARGET2	RW	R	01110110	AGCTARGET2(7:0)								AGC Target
141	AGCINCREASE2	RW	R	10110100	AGCDECAY2(4:0)					AGCMINDA2(2:0)			AGC Gain Increase Settings
142	AGCREDUCE2	RW	R	00100000	AGCATTACK2(4:0)					AGCMAXDA2(2:0)			AGC Gain Reduce Settings
143	AGCAHYST2	RW	R	———000	–	–	–	–	–	AGCAHYST2(2:0)			AGC Digital Threshold Range
144	TIMEGAIN2	RW	R	11110101	TIMEGAIN2M				TIMEGAIN2E				Timing Gain
145	DRGAIN2	RW	R	11110000	DRGAIN2M				DRGAIN2E				Data Rate Gain
146	PHASEGAIN2	RW	R	11—0011	FILTERIDX2(1:0)		–	–	PHASEGAIN2(3:0)				Filter Index, Phase Gain
147	FREQGAINA2	RW	R	00001111	FREQ LIM2	FREQ MODULO2	FREQ HALFMOD2	FREQ AMPL GATE 2	FREQGAINA2(3:0)				Frequency Gain A
148	FREQGAINB2	RW	R	00–11111	FREQ FREEZE2	FREQ AVG2	–	FREQGAINB2(4:0)					Frequency Gain B
149	FREQGAINC2	RW	R	——01101	–	–	–	FREQGAINC2(4:0)					Frequency Gain C
14A	FREQGAIND2	RW	R	0—01101	RFFREQ FREEZE2	–	–	FREQGAIND2(4:0)					Frequency Gain D

Table 26. CONTROL REGISTER MAP (continued)

Add	Name	Dir	Ret	Reset	Bit 7	6	5	4	3	2	1	0	Description
RECEIVER PARAMETER SET 2													
14B	AMPLGAIN2	RW	R	01—0110	AMPLAVG2	AMPLAGC2	–	–	AMPLGAIN2(3:0)				Amplitude Gain
14C	FREQDEV12	RW	R	——0000	–	–	–	–	FREQDEV2(11:8)				Receiver Frequency Deviation
14D	FREQDEV02	RW	R	00100000	FREQDEV2(7:0)								Receiver Frequency Deviation
14E	FOURFSK2	RW	R	——11010	–	–	–	DEV UPDATE2	DEVDECAY2(3:0)				Four FSK Control
14F	BBOFFSRES2	RW	R	10001000	RESINTB2(3:0)				RESINTA2(3:0)				Baseband Offset Compensation Resistors
RECEIVER PARAMETER SET 3													
160	MODCFGF	RW	R	———000	–	–	–	–	–	FREQ SHAPE(2:0)			Modulator Configuration F
161	FSKDEV2	RW	R	00000000	FSKDEV(23:16)								FSK Frequency Deviation
162	FSKDEV1	RW	R	00001010	FSKDEV(15:8)								FSK Frequency Deviation
163	FSKDEV0	RW	R	00111101	FSKDEV(7:0)								FSK Frequency Deviation
164	MODCFGA	RW	R	0000–101	BROWNGATE	PTTLCKGATE	SLOW RAMP		–	AMPLSHAPE	TX SE	TX DIFF	Modulator Configuration A
165	TXRATE2	RW	R	00000000	TXRATE(23:16)								Transmitter Bitrate
166	TXRATE1	RW	R	00101000	TXRATE(15:8)								Transmitter Bitrate
167	TXRATE0	RW	R	11110110	TXRATE(7:0)								Transmitter Bitrate
168	TXPWRCOEFF A1	RW	R	00000000	TXPWRCOEFFA(15:8)								Transmitter Predistortion Coefficient A
169	TXPWRCOEFF A0	RW	R	00000000	TXPWRCOEFFA(7:0)								Transmitter Predistortion Coefficient A
16A	TXPWRCOEFF B1	RW	R	00001111	TXPWRCOEFFB(15:8)								Transmitter Predistortion Coefficient B
16B	TXPWRCOEFF B0	RW	R	11111111	TXPWRCOEFFB(7:0)								Transmitter Predistortion Coefficient B
16C	TXPWRCOEFF C1	RW	R	00000000	TXPWRCOEFFC(15:8)								Transmitter Predistortion Coefficient C
16D	TXPWRCOEFF C0	RW	R	00000000	TXPWRCOEFFC(7:0)								Transmitter Predistortion Coefficient C
16E	TXPWRCOEFF D1	RW	R	00000000	TXPWRCOEFFD(15:8)								Transmitter Predistortion Coefficient D
16F	TXPWRCOEFF D0	RW	R	00000000	TXPWRCOEFFD(7:0)								Transmitter Predistortion Coefficient D
170	TXPWRCOEFF E1	RW	R	00000000	TXPWRCOEFFE(15:8)								Transmitter Predistortion Coefficient E
171	TXPWRCOEFF E0	RW	R	00000000	TXPWRCOEFFE(7:0)								Transmitter Predistortion Coefficient E
172	TXCLKDIV	RW	R	——00000	–	–	–	TXHALFSPEED	TXINTERP		TXCLKDIV		Transmitter Clock Divider
173	TXCLKDIV	RW	R	——00000	–	–	–	–	–	–	MSHAPE		Transmitter Amplitude Shaping
PLL PARAMETERS													

Table 26. CONTROL REGISTER MAP (continued)

Add	Name	Dir	Ret	Reset	Bit 7	6	5	4	3	2	1	0	Description
PLL PARAMETERS													
180	PLLVCOI	RW	R	———011	–	–	–	–	–	VCOI(2:0)			VCO Current
182	PLLLOCKDET	RW	R	———011	LOCKDETDLYR(1:0)		–	–	–	LOCK DET DLYM	LOCKDETDLY(1:0)		PLL Lock Detect Delay
183	PLLRNGCFG	RW	R	—000011	–	–	PLLRNGMODE(2:0)			PLLRNGCLK(2:0)			PLL Ranging Configuration
184	PLLDITHER	RW	R	00–10111	DTX	DRX	–	MAGNITUDE(4:0)					PLL Dither
CRYSTAL OSCILLATOR													
184	XTALCAP	RW	R	00000000	XTALCAP(7:0)								Crystal Oscillator Load Capacitance
BASEBAND													
188	BBTUNE	RW	R	——01001	–	–	–	BB TUNE RUN	BBTUNE(3:0)				Baseband Tuning
189	BBOFFSCAP	RW	R	–111–111	–	CAP INT B(2:0)			–	CAP INT A(2:0)			Baseband Offset Compensation Capacitors
190	ADCCLK	RW	R	–0111100		CLKFREQ(4:0)					CLKMUX(1:0)		SAR ADC Clock Settings
191	ADCMISC	RW	R	————0	–	–	–	–	–	–	–	SKIP CALIB	SAR ADC Miscellaneous Settings
192	ADCSPARE	RW	R	———00	–	–	–	–	–	–	ADCSPARE(1:0)		SAR ADC Spare Bits for Analog Settings
MAC LAYER PARAMETERS													
PACKET FORMAT													
200	PKTADDRCFG	RW	R	001–0000	MSB FIRST	CRC SKIP FIRST	FEC SYNC DIS	–	ADDR POS(3:0)				Packet Address Config
201	PKTLENPOS	RW	R	00000000	LEN MSB POS(3:0)				LEN LSB POS(3:0)				Packet Length Byte Position
202	PKTLENBITS	RW	R	——0000	–	–	–	–	LEN BITS(3:0)				Packet Length Significant Bits
203	PKTLENOFFSET1	RW	R	——00000	–	–	–	LEN OFFSET(12:8)					Packet Length Offset 1
204	PKTLENOFFSET0	RW	R	00000000	LEN OFFSET(7:0)								Packet Length Offset 0
205	PKTMAXLEN	RW	R	——0000	–	–	–	–	MAX LEN(11:8)				Packet Maximum Length 1
206	PKTMAXLEN 0	RW	R	00000000	MAX LEN(7:0)								Packet Maximum Length 0
207	PKTADDR3	RW	R	00000000	ADDR(31:24)								Packet Address 3
208	PKTADDR2	RW	R	00000000	ADDR(23:16)								Packet Address 2
209	PKTADDR1	RW	R	00000000	ADDR(15:8)								Packet Address 1
20A	PKTADDR0	RW	R	00000000	ADDR(7:0)								Packet Address 0
20B	PKTADDRMASK3	RW	R	00000000	ADDRMASK(31:24)								Packet Address Mask 1
20C	PKTADDRMASK2	RW	R	00000000	ADDRMASK(23:16)								Packet Address Mask 0
20D	PKTADDRMASK1	RW	R	00000000	ADDRMASK(15:8)								Packet Address Mask 1
20E	PKTADDRMASK0	RW	R	00000000	ADDRMASK(7:0)								Packet Address Mask 0
PATTERN MATCH													
210	MATCH0APAT3	RW	R	00000000	MATCH0APAT(31:24)								Pattern Match Unit 0a, Pattern

Table 26. CONTROL REGISTER MAP (continued)

Add	Name	Dir	Ret	Reset	Bit 7	6	5	4	3	2	1	0	Description
PATTERN MATCH													
211	MATCH0APAT2	RW	R	00000000	MATCH0APAT(23:16)								Pattern Match Unit 0a, Pattern
212	MATCH0APAT1	RW	R	00000000	MATCH0APAT(15:8)								Pattern Match Unit 0a, Pattern
213	MATCH0APAT0	RW	R	00000000	MATCH0APAT(7:0)								Pattern Match Unit 0a, Pattern
214	MATCH0ALEN	RW	R	0—00000	MATCH0 RAW	–	–					MATCH0A-LEN(4:0)	Pattern Match Unit 0a, Pattern Length
215	MATCH0AMIN	RW	R	——00000	–	–	–					MATCH0A-MIN(4:0)	Pattern Match Unit 0a, Minimum Match
216	MATCH0AMAX	RW	R	——11111	–	–	–					MATCH0A-MAX(4:0)	Pattern Match Unit 0a, Maximum Match
217	MATCH0BPAT3	RW	R	00000000	MATCH0BPAT(31:24)								Pattern Match Unit 0b, Pattern
218	MATCH0BPAT2	RW	R	00000000	MATCH0BPAT(23:16)								Pattern Match Unit 0b, Pattern
219	MATCH0BPAT1	RW	R	00000000	MATCH0BPAT(15:8)								Pattern Match Unit 0b, Pattern
21A	MATCH0BPAT0	RW	R	00000000	MATCH0BPAT(7:0)								Pattern Match Unit 0b, Pattern
21B	MATCH0BLEN	RW	R	——00000	–	–	–					MATCH0B-LEN(4:0)	Pattern Match Unit 0b, Pattern Length
21C	MATCH0BMIN	RW	R	——00000	–	–	–					MATCH0B-MIN(4:0)	Pattern Match Unit 0b, Minimum Match
21D	MATCH0BMAX	RW	R	——11111	–	–	–					MATCH0B-MAX(4:0)	Pattern Match Unit 0b, Maximum Match
220	MATCH1PAT1	RW	R	00000000	MATCH1PAT(15:8)								Pattern Match Unit 1, Pattern
221	MATCH1PAT0	RW	R	00000000	MATCH1PAT(7:0)								Pattern Match Unit 1, Pattern
222	MATCH1LEN	RW	R	0——0000	MATCH1 RAW	–	–	–	MATCH1LEN(3:0)				Pattern Match Unit 1, Pattern Length
223	MATCH1MIN	RW	R	——0000	–	–	–	–	MATCH1MIN(3:0)				Pattern Match Unit 1, Minimum Match
224	MATCH1MAX	RW	R	——1111	–	–	–	–	MATCH1MAX(3:0)				Pattern Match Unit 1, Maximum Match
PACKET CONTROLLER													
230	TMGTX-BOOST	RW	R	00110010	TMGTXBOOSTE(2:0)			TMGTXBOOSTM(4:0)					Transmit PLL Boost Time
231	TMGTXSET-TLE	RW	R	00001010	TMGTXSETTLEE(2:0)			TMGTXSETTLEM(4:0)					Transmit PLL (post Boost) Settling Time
232	TMGRX-BOOST	RW	R	00110010	TMGRXBOOSTE(2:0)			TMGRXBOOSTM(4:0)					Receive PLL Boost Time
233	TMGRXSET-TLE	RW	R	00010100	TMGRXSETTLEE(2:0)			TMGRXSETTLEM(4:0)					Receive PLL (post Boost) Settling Time
234	TMGRXOFF-SA CQ	RW	R	01110011	TMGRXOFFSACQE(2:0)			TMGRXOFFSACQM(4:0)					Receive Baseband DC Offset Acquisition Time
235	TMGRX-COARS EAGC	RW	R	00111001	TMGRXCOARSEAGCE(2:0)			TMGRXCOARSEAGCM(4:0)					Receive Coarse AGC Time
236	TMGRXAGC	RW	R	00000000	TMGRXAGCE(2:0)			TMGRXAGCM(4:0)					Receiver AGC Set-tling Time
237	TMGRXRSSI	RW	R	00000000	TMGRXRSSIE(2:0)			TMGRXRSSIM(4:0)					Receiver RSSI Set-tling Time
238	TMGRXPREA-M BLE1	RW	R	00000000	TMGRXPREAMBLE1E(2:0)			TMGRXPREAMBLE1M(4:0)					Receiver Preamble 1 Timeout
239	TMGRXPREA-M BLE2	RW	R	00000000	TMGRXPREAMBLE2E(2:0)			TMGRXPREAMBLE2M(4:0)					Receiver Preamble 2 Timeout

Table 26. CONTROL REGISTER MAP (continued)

Add	Name	Dir	Ret	Reset	Bit 7	6	5	4	3	2	1	0	Description
PACKET CONTROLLER													
23A	TMGRXPREAM BLE3	RW	R	00000000	TMGRXPREAMBLE3E(2:0)			TMGRXPREAMBLE3M(4:0)					Receiver Preamble 3 Timeout
23B	RSSIREFEREN CE	RW	R	00000000	RSSIREFERENCE								RSSI Offset
23C	RSSIABSTHR	RW	R	00000000	RSSIABSTHR								RSSI Absolute Threshold
23D	BGNDRSSIGAI N	RW	R	——0000	–	–	–	–	BGNDRSSIGAIN(3:0)				Background RSSI Averaging Time Constant
23E	BGNDRSSITHR	RW	R	—000000	–	–	BGNDRSSITHR(5:0)						Background RSSI Relative Threshold
240	PKTCHUNKSIZ E	RW	R	00000000	PKTCHUNKSIZE(7:0)								Packet Chunk Size
241	PKTMISCFLAG S	RW	R	—000000	–	–	ADDL FEC SYNCFLG	WOR MULTI PKT	AGC SETTL DET	BGND RSSI	RXAGC CLK	RXRSSI CLK	Packet Controller Miscellaneous Flags
242	PKTSTOREFLA GS	RW	R	–0000000	–	ST ANT RSSI	ST CRCB	ST RSSI	ST DR	ST RFOFFS	ST FOFFS	ST TIMER	Packet Controller Store Flags
243	PKTACCEPTFL AGS	RW	R	—000000	–	–	ACCPT LRGP	ACCPT SZF	ACCPT ADDRF	ACCPT CRCF	ACCPT ABRT	ACCPT RESIDUE	Packet Controller Accept Flags
SPECIAL FUNCTIONS													
GENERAL PURPOSE ADC													
300	GPADCCTRL	RW	R	—000000	BUSY	–	GPADC3	GPADC2	GPADC1	GPADC13	CONT	CH ISOL	General Purpose ADC Control
301	GPADCPERIOD	RW	R	00111111	GPADCPERIOD(7:0)								GPADC Sampling Period
308	GPADC13VALU E1	R		————	–	–	–	–	–	–	GPADC13VALUE(9:8)		GPADC13 Value
309	GPADC13VALU E0	R		————	GPADC13VALUE(7:0)								GPADC13 Value
30A	GPADC1VALUE1	R		————	–	–	–	–	–	–	GPADC1VALUE(9:8)		GPADC1 Value
30B	GPADC1VALUE0	R		————	GPADC1VALUE(7:0)								GPADC1 Value
30C	GPADC2VALUE1	R		————	–	–	–	–	–	–	GPADC2VALUE(9:8)		GPADC2 Value
30D	GPADC2VALUE0	R		————	GPADC2VALUE(7:0)								GPADC2 Value
30E	GPADC3VALUE1	R		————	–	–	–	–	–	–	GPADC3VALUE(9:8)		GPADC3 Value
30F	GPADC3VALUE0	R		————	GPADC3VALUE(7:0)								GPADC3 Value
LOW POWER OSCILLATOR CALIBRATION													
310	LPOSCCONFIG	RW	R	00000000	LPOCOSCIVERT	–	LPOSCCALIBR	LPOSCCALIBF	LPOSCIRQR	LPOSCIRQF	LPOSCFAST	LPOSCENA	Low Power Oscillator Configuration
311	LPOSCSTATUS	R	R	————	–	–	–	–	–	–	LPOSC IRQ	LPOSC EDGE	Low Power Oscillator Status
312	LPOSCCLKMUX	RW	R	———00	–	–	–	–	–	–	LPOSCCLKMUX(1:0)		LPOSC Reference Frequency Divider
313	LPOSCKFILT1	RW	R	00100000	LPOSCKFILT(15:8)								Low Power Oscillator Calibration Filter Constant
314	LPOSCKFILT0	RW	R	11000100	LPOSCKFILT(7:0)								Low Power Oscillator Calibration Filter Constant
315	LPOSCREF1	RW	R	01100001	LPOSCREF(15:8)								Low Power Oscillator Calibration Reference

Table 26. CONTROL REGISTER MAP (continued)

Add	Name	Dir	Ret	Reset	Bit 7	6	5	4	3	2	1	0	Description
LOW POWER OSCILLATOR CALIBRATION													
316	LPOSCREF0	RW	R	10101000	LPOSCREF(7:0)								Low Power Oscillator Calibration Reference
317	LPOSCFREQ1	RW	R	00000000	LPOSCFREQ(9:2)								Low Power Oscillator Calibration Frequency
318	LPOSCFREQ0	RW	R	0000——	LPOSCFREQ(1:–2)				–	–	–	–	Low Power Oscillator Calibration Frequency
319	LPOSCPER1	RW		————	LPOSCPER(15:8)								Low Power Oscillator Calibration Period
31A	LPOSCPER0	RW		————	LPOSCPER(7:0)								Low Power Oscillator Calibration Period
DSP MODE INTERFACE													
320	DSPMODECFG	RW	R	00——00	FSYNC DLY	DSP SPI	–	–	–	–	SYNC SOURCE(1:0)		DSP Mode Setting
321	DSPMODESKIP1	RW	R	–0000000	–	SKIP AGC	SKIP RSSI	SKIP AFSK DEMOD	SKIP FSK DEMOD	SKIP DATARATE	SKIP PHASE	SKIP FREQ	DSP Mode Skip 1
322	DSPMODESKIP0	RW	R	00000000	SKIP RF FREQ	SKIP AMPL	SKIP SAMP PHASE	SKIP SAMP MAG	SKIP SAMP ROTIQ	SKIP SAMP IQ	SKIP BASE BANDIQ	SKIP SOFT SAMP	DSP Mode Skip 0
DAC													
330	DACVALUE1	RW	R	——0000	–	–	–	–	DACVALUE(11:8)				DAC Value
331	DACVALUE2	RW	R	00000000	DACVALUE(7:0)								DAC Value
332	DACCONFIG	RW	R	00—0000	DAC PWM	DAC CLK X2	–	–	DACINPUT(3:0)				DAC Configuration
TX CONTROL													
F00	SPAREOUT	RW	R	00000000	TXREGSNK	TXSTG2	TXSTG3	DACDISABLE	DACTESTEN	DACTRIM(2:0)			TX Control

APPLICATION INFORMATION

Certification

Customers using AX5044, as with any product containing a radio, have the responsibility to ensure, at a product level, that their usage of this product complies with regulatory requirements where it's operated.

ON Semiconductor makes an effort to create pre−compliant reference designs that customers can use or copy directly, however ON Semiconductor is not liable for customer's failure to comply with regulatory obligations.

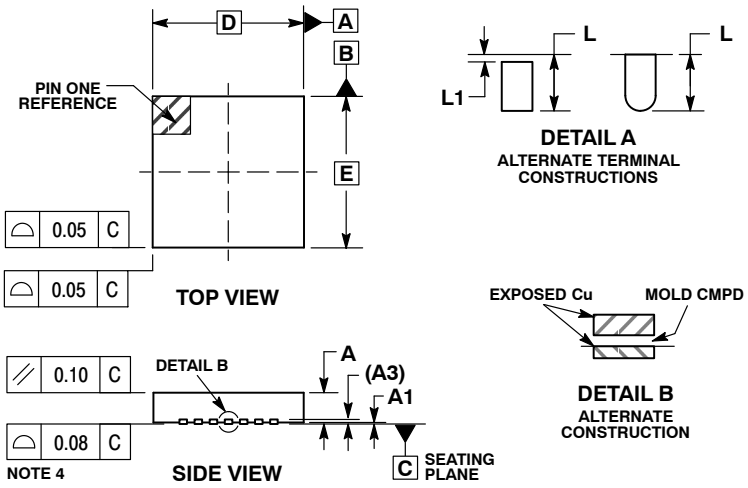
Typical Application Diagrams

The following diagrams and any resulting component values or equations are provided as a starting point. Real components have non−ideal effects, PCBs and soldering introduce additional parasitics, and variations in ground planes, antennas, etc, all influence the RF matching and RF performance and cannot be guaranteed or predicted in advance.

To help lower risk, ON Semiconductor creates reference designs that customers can use as a starting point. However the customer should anticipate some fine tuning of the RF matching network for their system. All RF transceiver products are subject to these fundamental sensitivities.

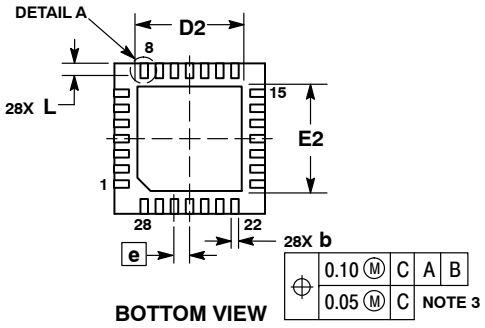
PACKAGE DIMENSIONS

QFN28 5x5, 0.5P
CASE 485EH
ISSUE A

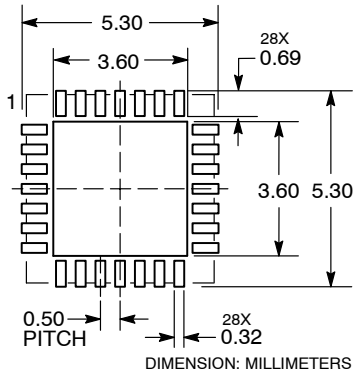


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	5.00 BSC	
D2	3.40	3.50
E	5.00 BSC	
E2	3.40	3.50
e	0.50 BSC	
L	0.44	0.54
L1	---	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative