

BUL42D

High Speed, High Gain Bipolar NPN Transistor Integrating an Antisaturation Network and a Transient Voltage Suppression Capability

The BUL42D is a state-of-the-art bipolar transistor. Tight dynamic characteristics and lot to lot minimum spread make it ideally suitable for light ballast applications.

Main Features:

- Free Wheeling Diode Built In
- Flat DC Current Gain
- Fast Switching Times and Tight Distribution
- “Six Sigma” Process Providing Tight and Reproducible Parameter Spreads

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector-Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector-Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter-Base Voltage	V_{EBO}	9	Vdc
Collector Current – Continuous	I_C	4.0	Adc
– Peak (Note 1)	I_{CM}	8.0	
Base Current – Continuous	I_B	1.0	Adc
– Peak (Note 1)	I_{BM}	2.0	
*Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	75	Watt
*Derate above 25°C		0.6	W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

TYPICAL GAIN

Typical Gain @ $I_C = 1\text{ A}, V_{CE} = 2\text{ V}$	h_{FE}	13	-
Typical Gain @ $I_C = 0.3\text{ A}, V_{CE} = 1\text{ V}$	h_{FE}	16	-

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance – Junction-to-Case	$R_{\theta JC}$	1.66	$^\circ\text{C}/\text{W}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 seconds	T_L	260	$^\circ\text{C}$

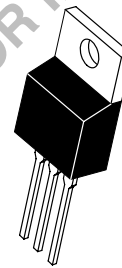
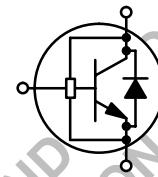
1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%



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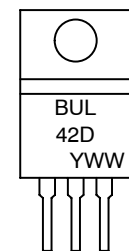
<http://onsemi.com>

4 AMPERES
700 VOLTS, 75 WATTS
POWER TRANSISTOR



TO-220
CASE 221A
STYLE 1

MARKING DIAGRAM



Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
BUL42D	TO-220	50 Units/Rail

BUL42D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I _C = 100 mA, L = 25 mH)	V _{CEO(sus)}	400	430	–	Vdc	
Collector–Base Breakdown Voltage (I _{CBO} = 1 mA)	V _{CBO}	700	780	–	Vdc	
Emitter–Base Breakdown Voltage (I _{EBO} = 1 mA)	V _{EBO}	9.0	12	–	Vdc	
Collector Cutoff Current (V _{CE} = Rated V _{CEO} , I _B = 0)	I _{CEO}	@ T _C = 25°C	–	–	100	μAdc
		@ T _C = 125°C	–	–	200	
Collector Cutoff Current (V _{CE} = Rated V _{CES} , V _{EB} = 0)	I _{CES}	@ T _C = 25°C	–	–	10	μAdc
		@ T _C = 125°C	–	–	200	
Emitter–Cutoff Current (V _{EB} = 9 Vdc, I _C = 0)	I _{EBO}	–	–	100	μAdc	

ON CHARACTERISTICS

Base–Emitter Saturation Voltage (I _C = 1 Adc, I _B = 0.2 Adc)	V _{BE(sat)}	–	0.85	1.2	Vdc
Collector–Emitter Saturation Voltage (I _C = 2 Adc, I _B = 0.5 Adc)	V _{CE(sat)}	–	0.2	1.0	Vdc
DC Current Gain (I _C = 1 Adc, V _{CE} = 2 Vdc) (I _C = 2 Adc, V _{CE} = 5 Vdc)	h _{FE}	8.0	13	–	–
		10	12	–	

DIODE CHARACTERISTICS

Forward Diode Voltage (I _{EC} = 1.0 Adc)	V _{EC}	–	0.9	1.5	V
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SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)

Turn–Off Time (I _C = 1.2 Adc, I _{B1} = 0.4 A, I _{B2} = 0.1 A, V _{CC} = 300 V)	T _{off}	4.6	–	6.55	μs
Fall Time (I _C = 2.5 Adc, I _{B1} = I _{B2} = 0.5 A, V _{CC} = 150 V, V _{BE} = –2 V)	T _f	–	–	0.8	μs

DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I _{B1} reaches 90% of final I _{B1}	I _C = 400 mA I _{B1} = 40 mA V _{CC} = 300 V	@ 1 μs	@ T _C = 25°C @ T _C = 125°C	V _{CE(dsat)}	–	2.8	–	V
		@ 3 μs	@ T _C = 25°C @ T _C = 125°C		–	3.2	–	
	I _C = 1 A I _{B1} = 200 mA V _{CC} = 300 V	@ 1 μs	@ T _C = 25°C @ T _C = 125°C		–	0.75	–	
		@ 3 μs	@ T _C = 25°C @ T _C = 125°C		–	1.3	–	
		@ 1 μs	@ T _C = 25°C @ T _C = 125°C		–	2.1	–	
		@ 3 μs	@ T _C = 25°C @ T _C = 125°C		–	4.7	–	
					–	0.35	–	
					–	0.6	–	

TYPICAL STATIC CHARACTERISTICS

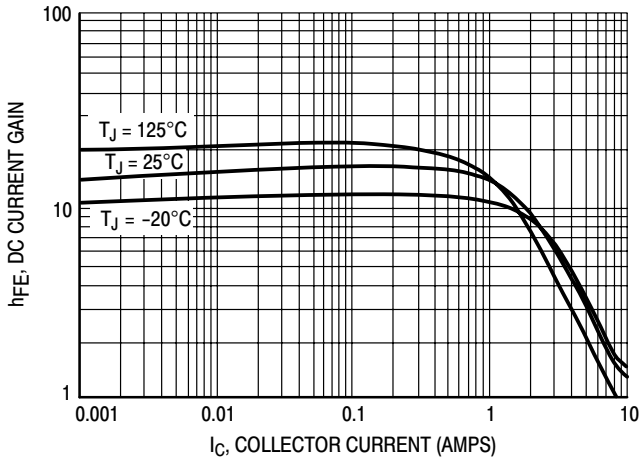


Figure 1. DC Current Gain @ $V_{CE} = 1\text{ V}$

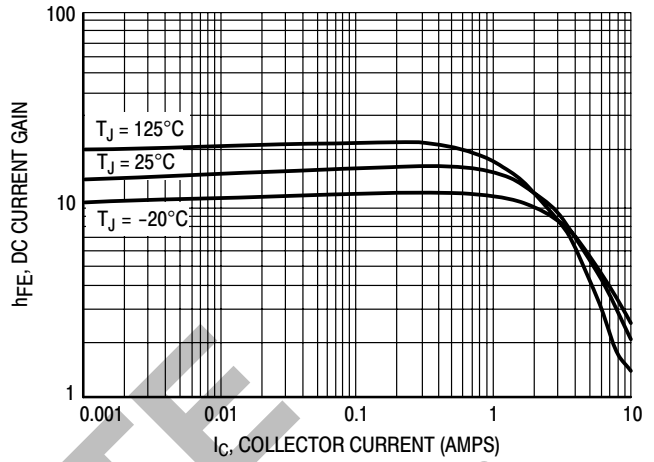


Figure 2. DC Current Gain @ $V_{CE} = 5\text{ V}$

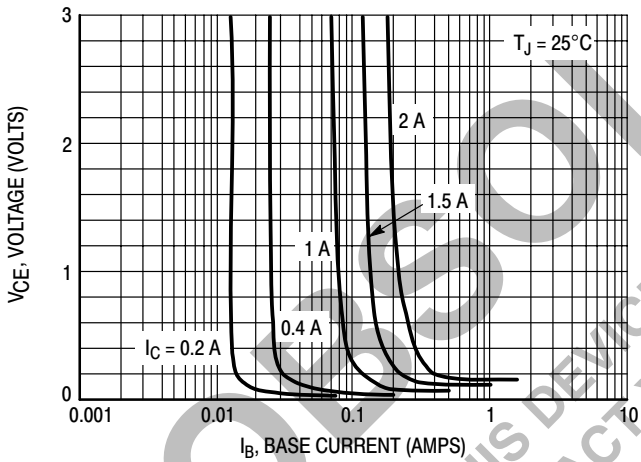


Figure 3. Collector Saturation Region

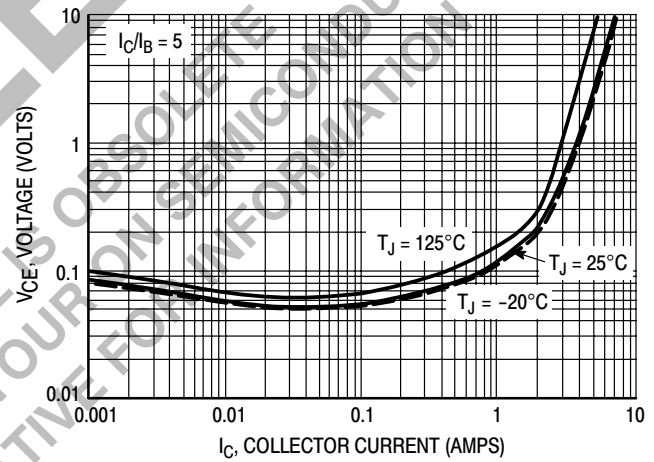


Figure 4. Collector-Emitter Saturation Voltage

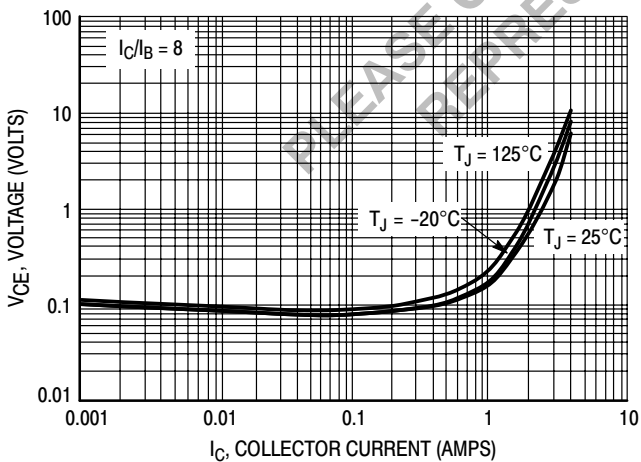


Figure 5. Collector-Emitter Saturation Voltage

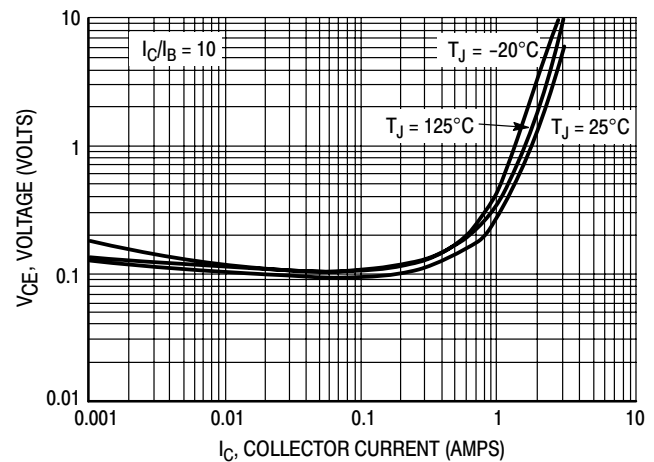


Figure 6. Collector-Emitter Saturation Voltage

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TYPICAL STATIC CHARACTERISTICS

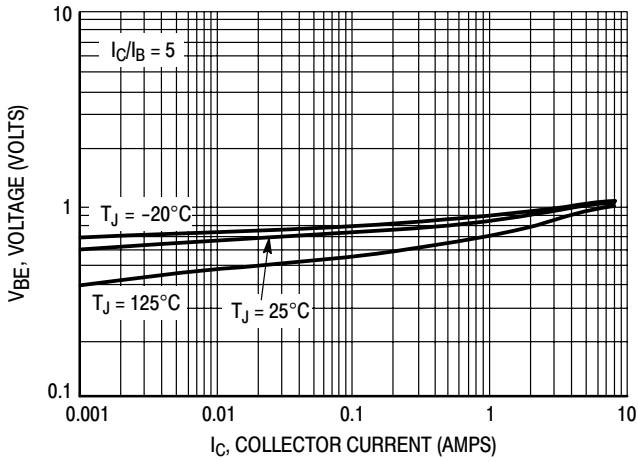


Figure 7. Base-Emitter Saturation Region

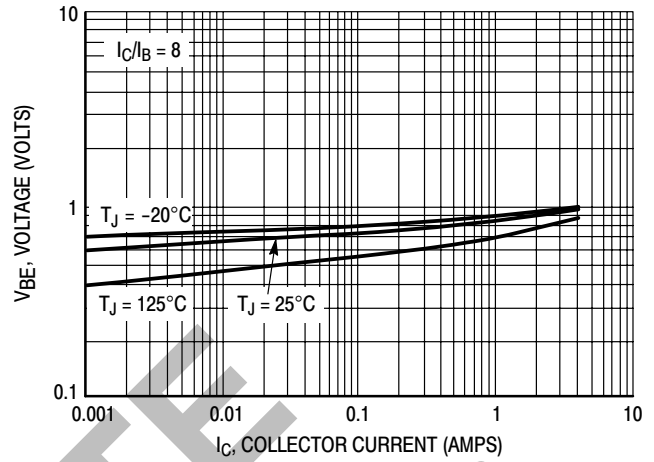


Figure 8. Base-Emitter Saturation Region

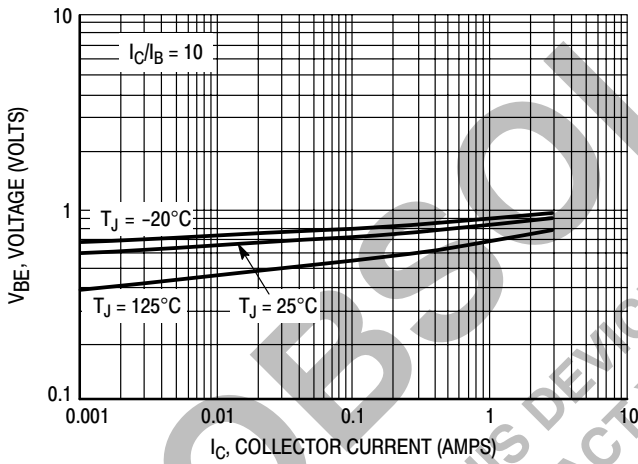


Figure 9. Base-Emitter Saturation Region

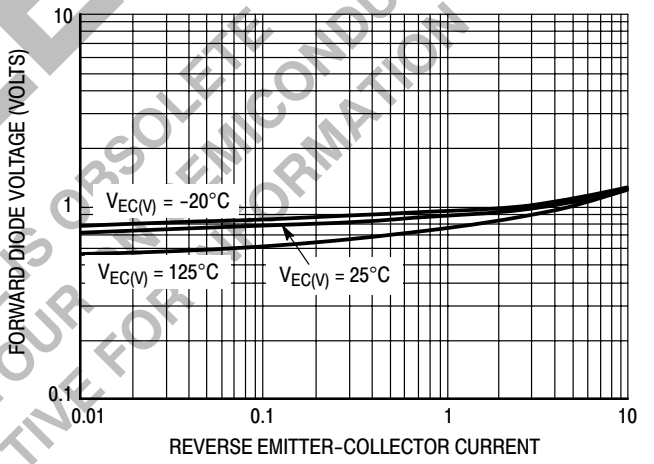


Figure 10. Forward Diode Voltage

TYPICAL SWITCHING CHARACTERISTICS

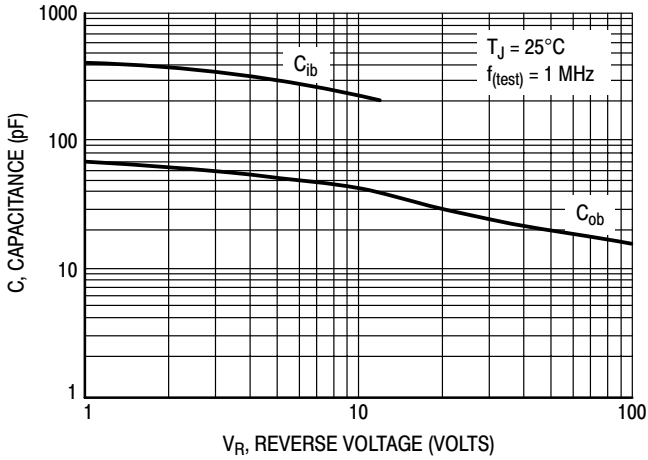


Figure 11. Capacitance

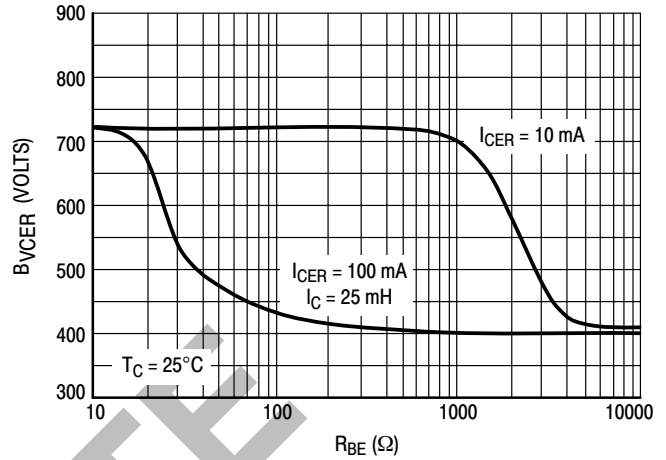


Figure 12. $B_{VCEr} = f(R_{BE})$

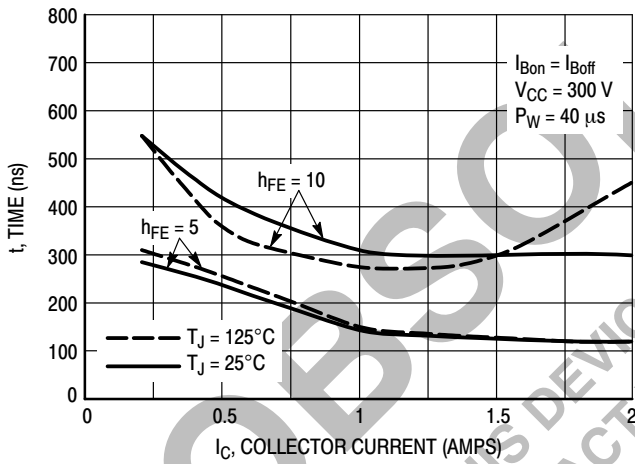


Figure 13. Resistive Switching, t_{on}

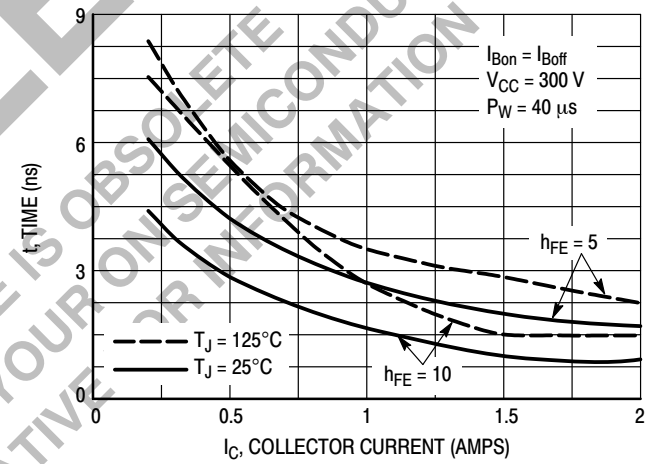


Figure 14. Resistive Switching, t_{off}

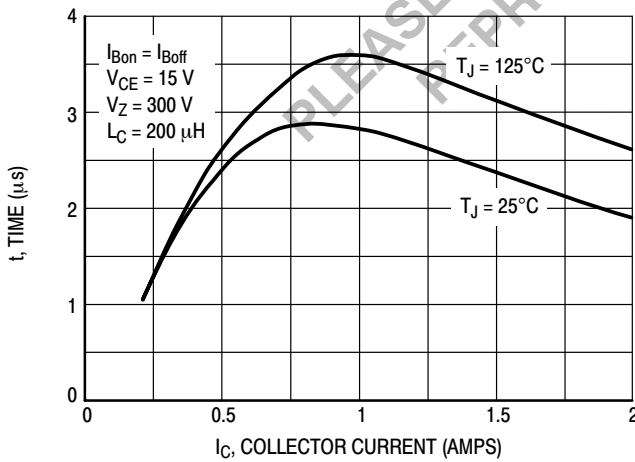


Figure 15. Inductive Storage Time, t_{si} @ $h_{FE} = 5$

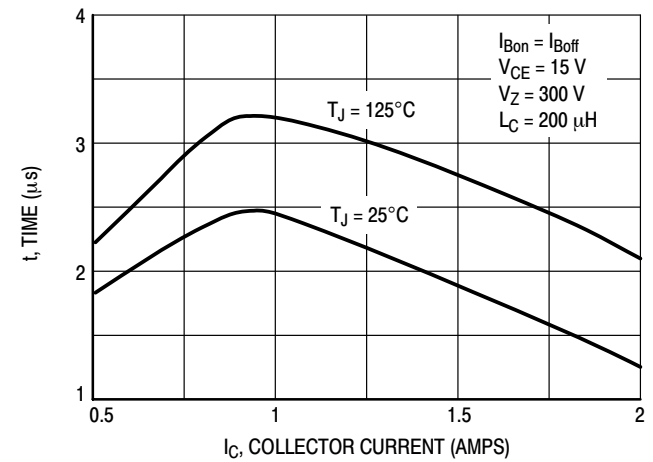


Figure 16. Inductive Storage Time, t_{si} @ $h_{FE} = 10$

TYPICAL SWITCHING CHARACTERISTICS

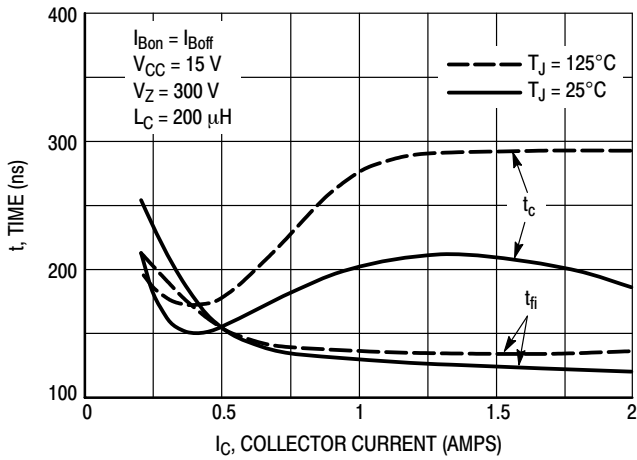


Figure 17. Inductive Fall and Cross Over Time, t_{fi} and t_c @ $h_{FE} = 5$

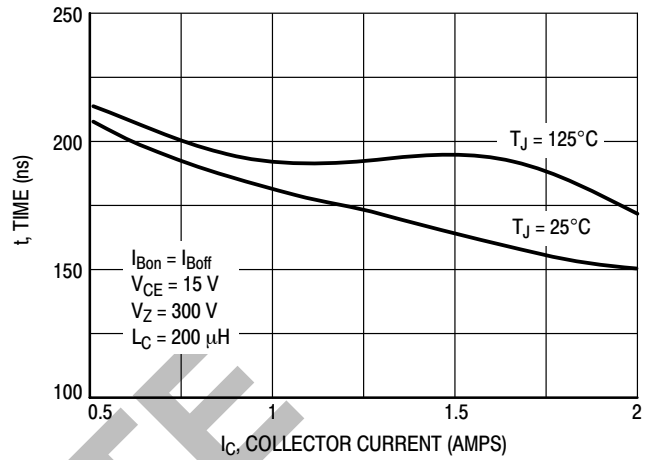


Figure 18. Inductive Fall Time, t_{fi} @ $h_{FE} = 10$

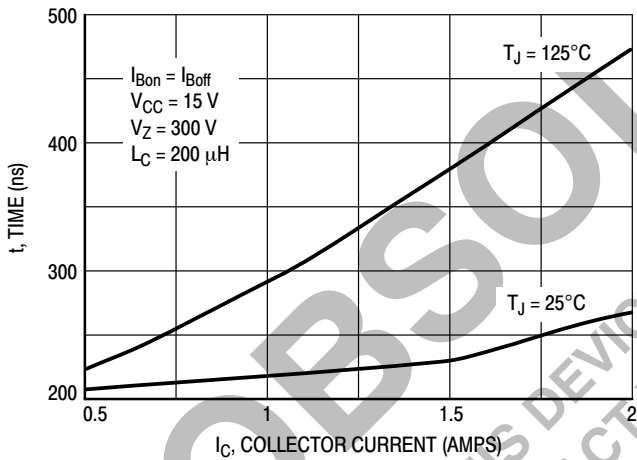


Figure 19. Inductive Cross Over Time, t_c @ $h_{FE} = 10$

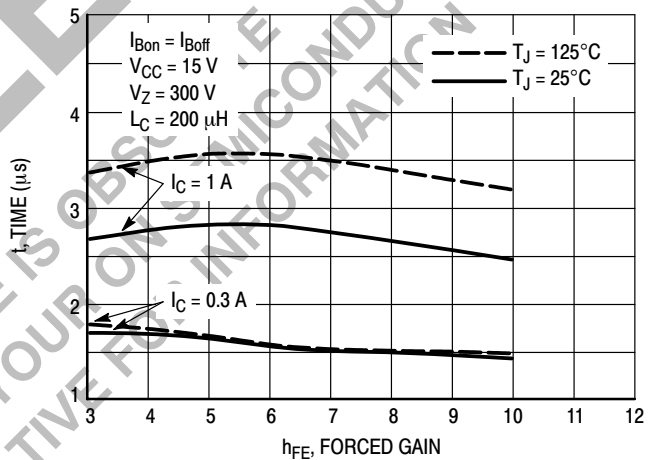


Figure 20. Inductive Storage Time, t_{si}

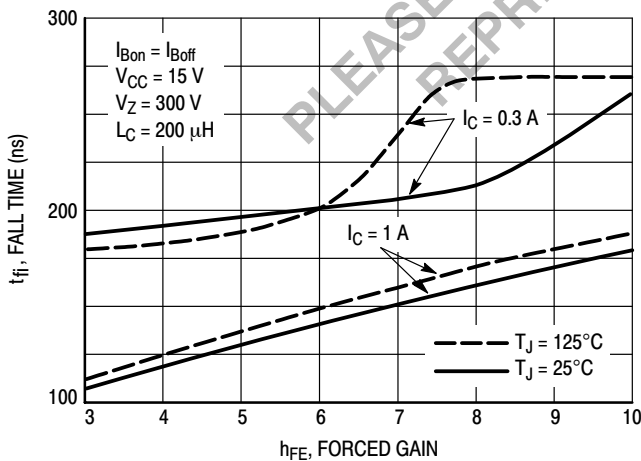


Figure 21. Inductive Fall Time, t_f

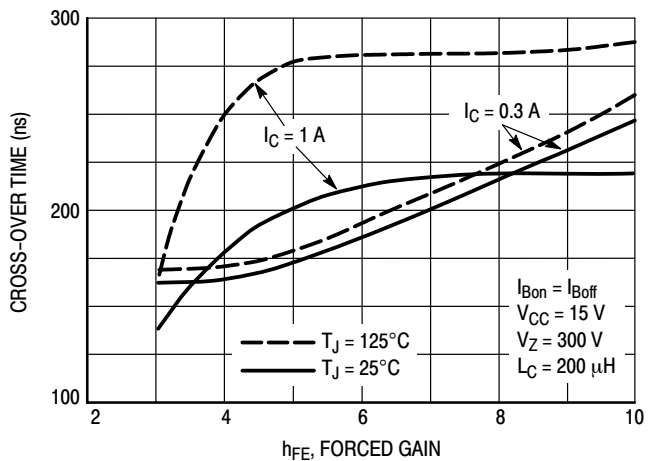


Figure 22. Inductive Cross Over Time, t_c

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TYPICAL SWITCHING CHARACTERISTICS

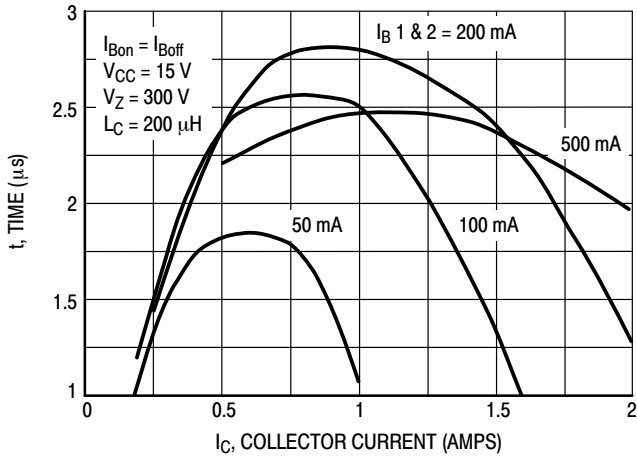


Figure 23. Inductive Storage Time, t_{si}

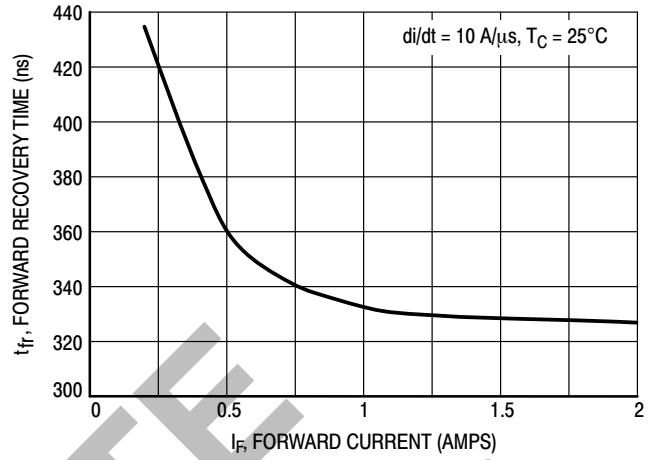


Figure 24. Forward Recovery Time, t_{fr}

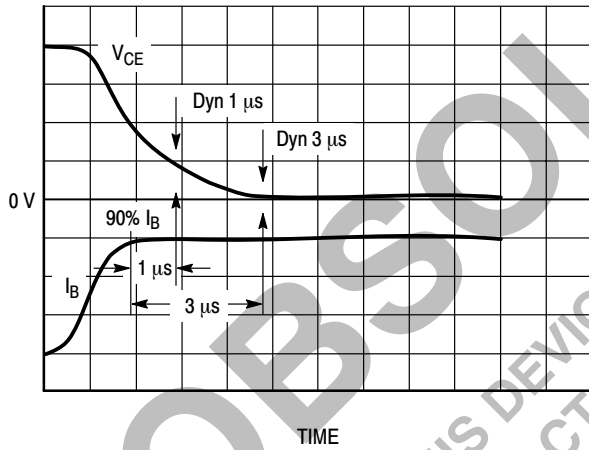


Figure 25. Dynamic Saturation Voltage Measurements

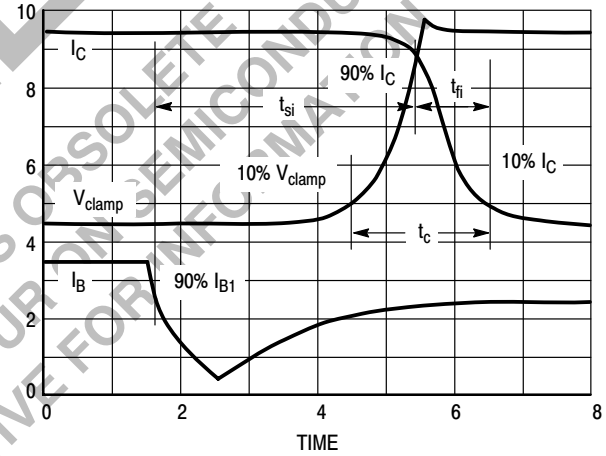
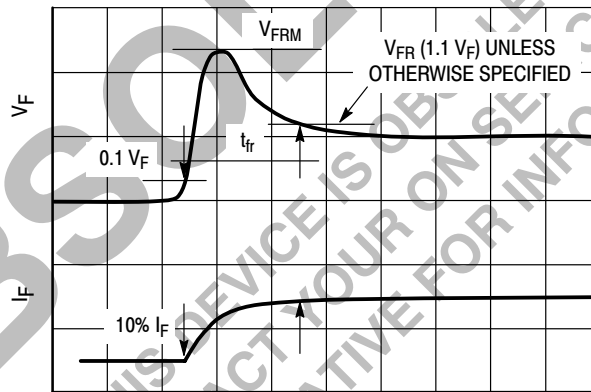
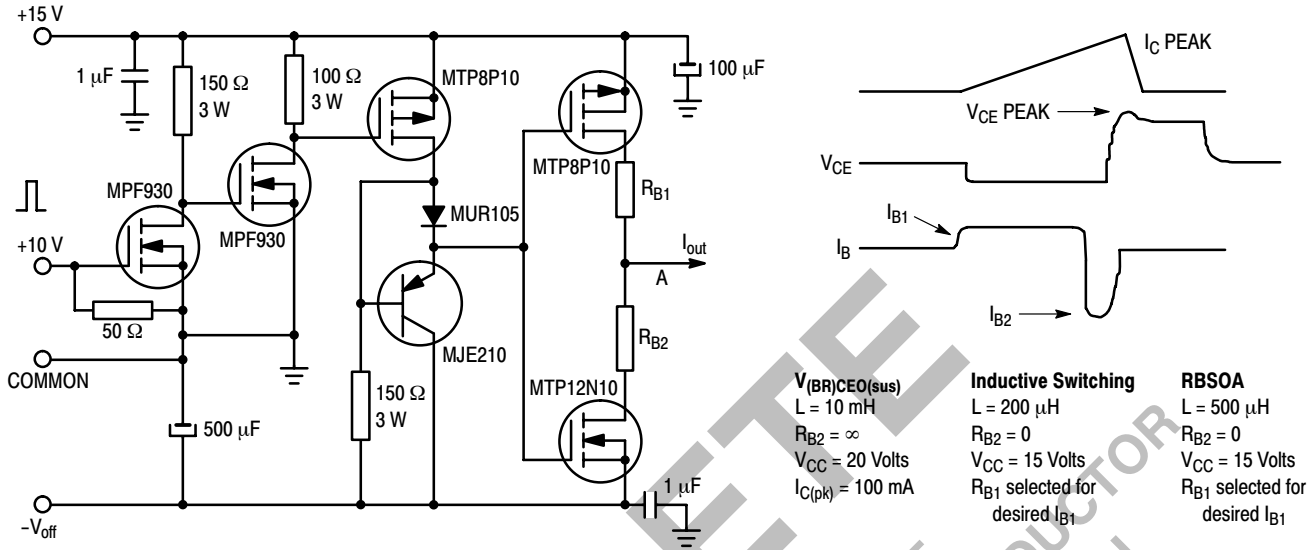


Figure 26. Inductive Switching Measurements

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TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



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MAXIMUM RATINGS

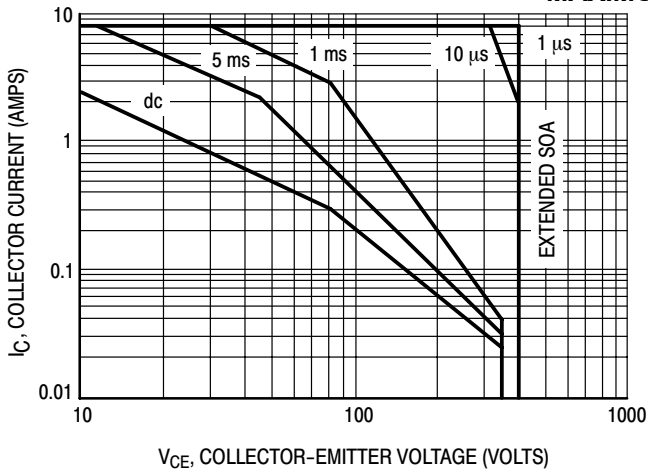


Figure 28. Forward Bias Safe Operating Area

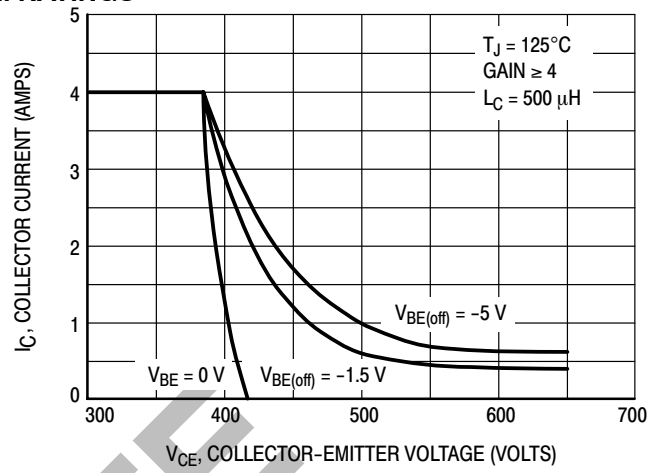


Figure 29. Reverse Bias Safe Operating Area

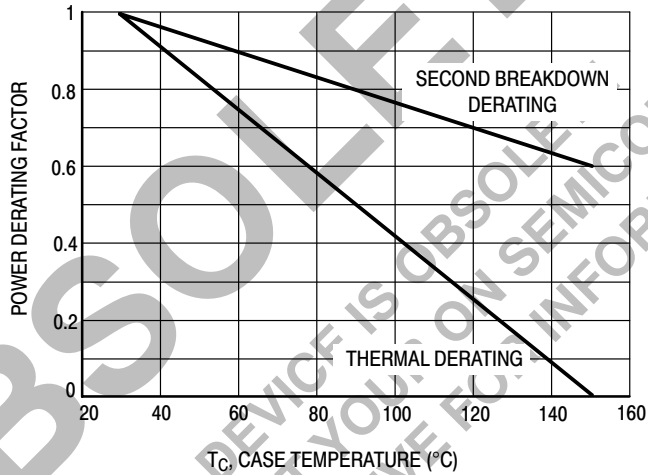


Figure 30. Power Derating

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There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on $T_C = 25^\circ\text{C}$; $T_{j(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25^\circ\text{C}$. Second Breakdown limitations do not derate like thermal limitations. Allowable current at the voltages shown on

Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

$T_{j(pk)}$ may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as reverse biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

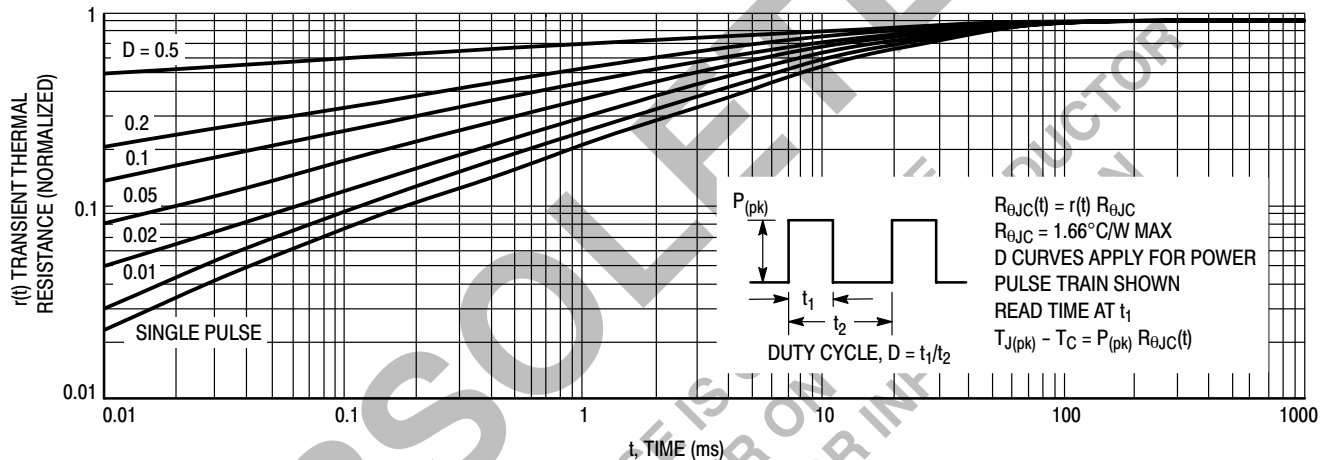
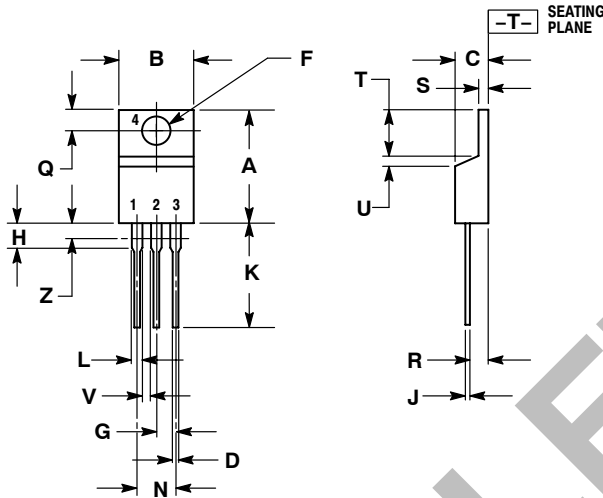


Figure 31. Thermal Response

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PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AA




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.295	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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