CM2009-05CP

Advance Information

VGA or DVI-I Port Companion Circuit

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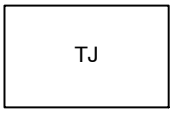
WLCSP14
CP SUFFIX
CASE 567CR

MARKING DIAGRAM



CM2009−05CP
14−Bump CSP Package

TJ = CM2009−05CP

ORDERING INFORMATION

Device	Package	Shipping†
CM2009−05CP	CSP−14 (Pb−Free)	3500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Product Description

The CM2009−05CP connects between the VGA or DVI−I port connector and the internal analog or digital flat panel controller logic. It can also be used for source devices such as a set−top box. The CM2009−05CP incorporates ESD protection for all signals, level shifting for the DDC signals and buffering for the SYNC signals. ESD protection for the video, DDC and SYNC lines is implemented with low−capacitance current steering diodes.

All connector interface pins are designed to safely handle the high current spikes specified by IEC−61000−4−2 Level 4 (±8 kV contact discharge). The ESD protection for the DDC, SYNC and VIDEO signal pins is designed to prevent “back current” when the device is powered down while connected to a video source or a video sink that is powered up. Positive supply rails are provided for the VIDEO / SYNC signals and DDC signals to facilitate interfacing with low voltage video controller ICs and microcontrollers to provide design flexibility in multi−supply−voltage environments.

Two Schmitt−triggered non−inverting buffers redrive and condition the HSYNC and VSYNC signals from the video connector (SYNC1, SYNC2). These buffers accept VESA VSIS compliant TTL input signals and convert them to CMOS output levels that swing between ground and V_{CC}.

Two N−channel MOSFETs provide the level shifting function required when the DDC controller or EDID EEPROM is operated at a lower supply voltage than the monitor. The gate terminals for these MOSFETS should be connected to the supply rail (typically 3.3 V, 2.5 V, etc.) that supplies power to the transceivers of the DDC controller.

Features

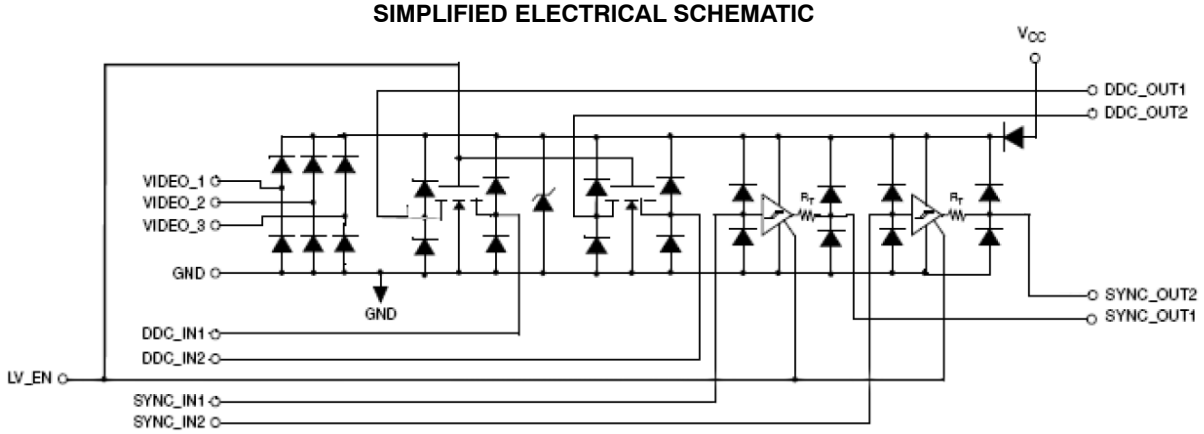
- Includes ESD Protection, Level−Shifting, Buffering and Sync Impedance Matching
- VESA VSIS Version 1 Revision 2 Compatible Interface
- Supports both Source and Sink Devices
- Supports Optional NAVI Signaling Requirements
- Seven Channels of ESD Protection for all VGA Port Connector Pins Meeting IEC−61000−4−2 Level 4 ESD Requirements (±8 kV Contact Discharge)
- Very Low Loading Capacitance from ESD Protection Diodes on VIDEO Lines, 3 pF Maximum
- Schmitt−Triggered Input Buffers for HSYNC and VSYNC Lines
- Bi−directional Level Shifting N−Channel FETs Provided for DDC_CLK & DDC_DATA Channels
- Backdrive Protection on all Lines
- 14−Bump, 5 x 4 x 5, 0.4 mm Chip Scale Package (CSP)
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Monitors
- Video Graphics Controllers Embedded in PCs
- Graphics Adapter Cards
- Set−Top Boxes

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SIMPLIFIED ELECTRICAL SCHEMATIC



PACKAGE / PINOUT DIAGRAM

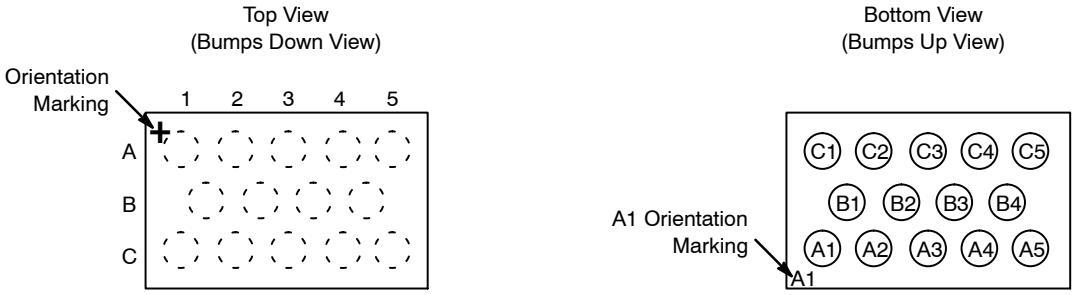


Table 1. PIN DESCRIPTIONS

Lead(s)	Name	Description
A1	GND	Ground reference supply pin.
A2	VIDEO_1	Video signal ESD protection channel. This pin is typically tied one of the video lines between the controller device and the video connector.
A3	VIDEO_2	Video signal ESD protection channel. This pin is typically tied one of the video lines between the controller device and the video connector.
A4	VIDEO_3	Video signal ESD protection channel. This pin is typically tied one of the video lines between the controller device and the video connector.
A5	V_{CC}	This is a supply input for the SYNC_1 and SYNC_2 level shifters, video protection and the DDC circuits.
B1	DDC_OUT1	DDC signal output. Connects to the DDC logic.
B2	DDC_OUT2	DDC signal output. Connects to the DDC logic.
B3	SYNC_OUT1	Sync signal buffer output. Connects to the monitor Sync logic. (Note 1)
B4	SYNC_OUT2	Sync signal buffer output. Connects to the monitor Sync logic. (Note 1)
C1	DDC_IN1	DDC signal input. Connects to the video connector side of one of the DDC lines.
C2	DDC_IN2	DDC signal input. Connects to the video connector side of one of the DDC lines.
C3	LV_EN	Disables the Sync buffer outputs when low.
C4	SYNC_IN1	Sync signal buffer input. Connects to the video connector side of one of the Sync lines. (Note 2)
C5	SYNC_IN2	Sync signal buffer input. Connects to the video connector side of one of the Sync lines. (Note 2)

1. Can also be connected to the VGA connector side if used for a source device.
2. Can also be used to connect to the Video Chip Sync Logic if it is used for a source device.

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
V_{CC} Supply Voltage Inputs	[GND − 0.5] to +6.0	V
DC Voltage at Inputs VIDEO_1, VIDEO_2, VIDEO_3 DDC_IN1, DDC_IN2 DDC_OUT1, DDC_OUT2 SYNC_IN1, SYNC_IN2, LV_EN	 [GND − 0.5] to [V_{CC} + 0.5] [GND − 0.5] to 6.0 [GND − 0.5] to 6.0 [GND − 0.5] to [V_{CC} + 0.5]	V
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−40 to +150	°C
Package Power Rating (T_A = 25°C)	500	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	−40 to +85	°C
V_{CC}	5	V

SPECIFICATIONS

Table 4. ELECTRICAL OPERATING CHARACTERISTIC (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	V_{CC} Supply Current	V_{CC} = 5 V; SYNC inputs at GND or V_{CC}; SYNC outputs unloaded, DDC_In and DDC_OUT floating			1.0	mA
		V_{CC} = 5 V; SYNC inputs at 3.0 V; SYNC outputs unloaded, DDC_In and DDC_OUT floating			2.0	mA
V_F	ESD Diode Forward Voltage	I_F = 10 mA			1.0	V
V_{IH}	Logic High Input Voltage	V_{CC} = 5.0 V; (Note 2)	2.0			V
V_{IL}	Logic Low Input Voltage	V_{CC} = 5.0 V; (Note 2)			0.55	V
V_{HYS}	Hysteresis Voltage	V_{CC} = 5.0 V; (Note 2)		450		mV
V_{OH}	Logic High Output Voltage	I_{OH} = 0 mA, V_{CC} = 5.0 V; (Note 2)	4.0			V
V_{OL}	Logic Low Output Voltage	I_{OL} = 0 mA, V_{CC} = 5.0 V; (Note 2)			0.15	V
R_{OUT}	SYNC Driver Output Resistance	V_{CC} = 5.0 V; SYNC Inputs at GND or 3.0 V		65		Ω
I_{IN}	Input Current VIDEO Inputs	V_{CC} = 5.0 V; V_{IN} = V_{CC} or GND			±10	μA
	SYNC_IN1, SYNC_IN2 Inputs	V_{CC} = 5.0 V; V_{IN} = V_{CC} or GND			±10	μA
I_{OFF}	Level Shifting N−MOSFET “OFF” State Leakage Current	(LV_EN − V_{DDC_IN}) < 0.4 V; V_{DDC_OUT} = LV_EN			10	μA
		(LV_EN − V_{DDC_OUT}) < 0.4 V; V_{DDC_IN} = LV_EN			10	μA
$I_{BACKDRIVE}$	Current conducted from input pins when Vcc is powered down.	V_{CC} < V_{INPUT_PIN}		10		μA
V_{ON}	Voltage Drop Across Level−shifting N−MOSFET when “ON”	LV_EN = 2.5 V; V_S = GND; I_{DS} = 3 mA			0.18	V
C_{IN_VID}	VIDEO Input Capacitance	V_{CC} = 5.0 V; V_{IN} = 2.5 V; f = 1 MHz			3	pF
		V_{CC} = 2.5 V; V_{IN} = 1.25 V; f = 1 MHz			3.5	pF
t_{PLH}	SYNC Driver L => H Propagation Delay	C_L = 50 pF; V_{CC} = 5.0 V; Input t_R and t_F < 5 ns			12	ns
t_{PHL}	SYNC Driver H => L Propagation Delay	C_L = 50 pF; V_{CC} = 5.0 V; Input t_R and t_F < 5 ns			12	ns
$t_{R,}$ t_F	SYNC Driver Output Rise & Fall Times	V_{CC} = 5 V		7		ns
V_{ESD}	ESD Withstand Voltage	V_{CC} = 5 V; (Note 3)	±8			kV

1. All parameters specified over standard operating conditions unless otherwise noted
2. These parameters apply only to the SYNC drivers. Note that R_{OUT} = R_T + R_{BUFFER}.
3. Per the IEC−61000−4−2 International ESD Standard, Level 4 contact discharge method. V_{CC} must be bypassed to GND via a low impedance ground plane with a 0.22 μF, low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between the applicable pins and GND. ESD pulses can be positive or negative with respect to GND.

APPLICATION INFORMATION

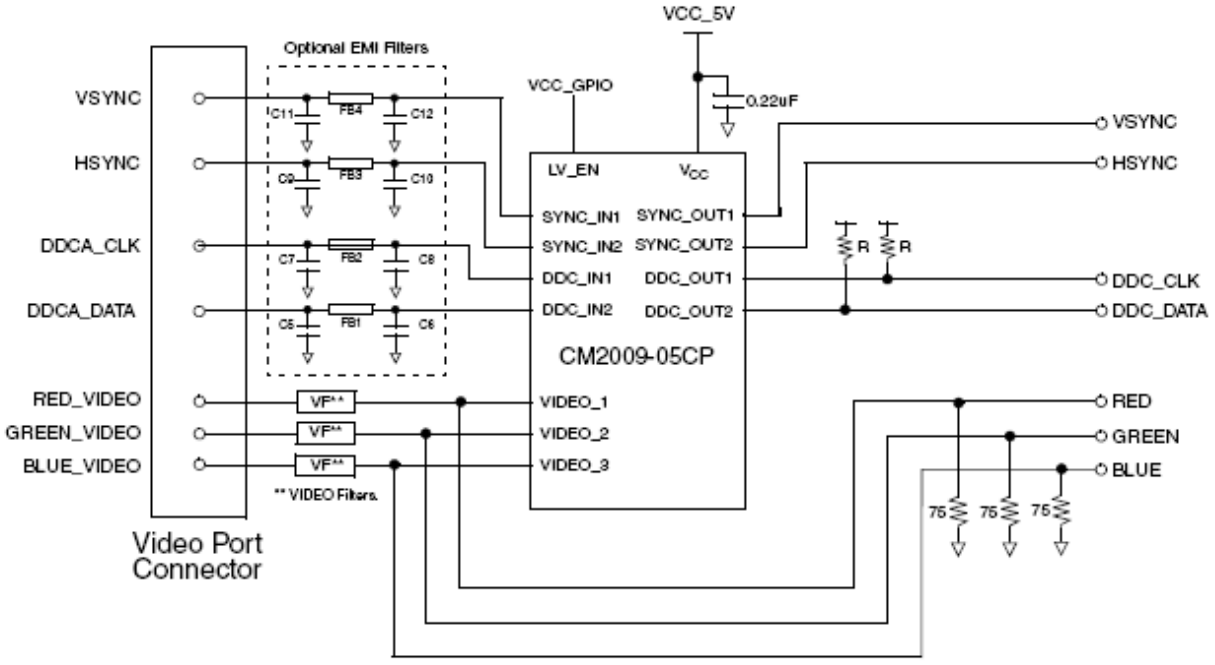


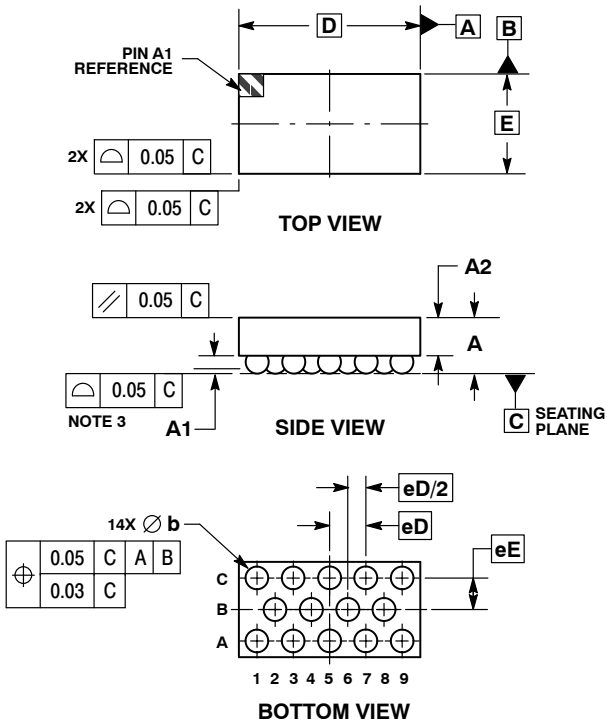
Figure 1. Typical Application Connection Diagram

NOTES:

1. The CM2009−05CP should be placed as close to the VGA or DVI−I connector as possible.
2. The ESD protection channels VIDEO_1, VIDEO_2, VIDEO_3 may be used interchangeably between the R, G, B signals.
3. If differential video signal routing is used, the RED, BLUE, and GREEN signal lines should be terminated with external 37.5 Ω resistors.
4. “VF” are external video filters for the RGB signals.
5. Supply bypass capacitors C1 and C2 must be placed immediately adjacent to the corresponding Vcc pins. Connections to the Vcc pins and ground plane must be made with minimal length copper traces (preferably less than 5 mm) for best ESD protection.
6. The bypass capacitor for the BYP pin has been omitted in this diagram. This results in a reduction in the maximum ESD withstand voltage at the DDC_OUT pins from ±8 kV to ±2 kV. If 8 kV ESD protection is required, a 0.22 μF ceramic bypass capacitor should be connected between BYP and ground.
7. The SYNC buffers may be used interchangeably between HSYNC and VSYNC.
8. The EMI filters at the SYNC_OUT and DDC_OUT pins (C5 to C12, and Ferrite Beads FB1 to FB4) are for reference only. The component values and filter configuration may be changed to suit the application.
9. The DDC level shifters DDC_IN, DDC_OUT, may be used interchangeably between DDCA_CLK and DDCA_DATA.
10. R1, R2 are optional. They may be used, if required, to pull the DDC_CLK and DDC_DATA lines to VCC_5V when no monitor is connected to the VGA connector. If used, it should be noted that “back current” may flow between the DDC pins and VCC_5V via these resistors when VCC_5V is powered down.

PACKAGE DIMENSIONS

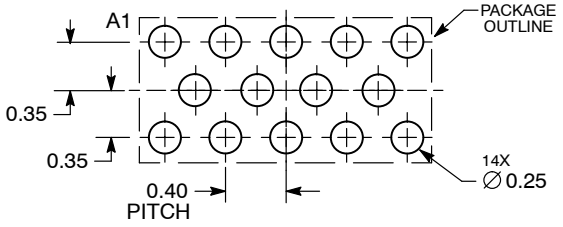
WLCSP14, 2.00x1.10
CASE 567CR−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.53	0.63
A1	0.17	0.24
A2	0.39 REF	
b	0.24	0.29
D	2.00 BSC	
E	1.10 BSC	
eD	0.400 BSC	
eE	0.347 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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