Ordering number : ENA2080A

LC786960E

CMOS LSI

Compact Disc Player IC

ON Semiconductor®

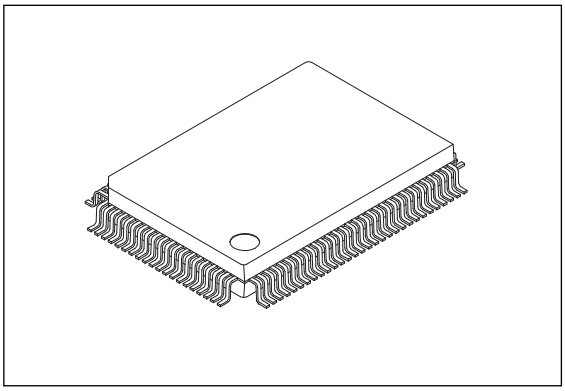
http://onsemi.com

Overview

The LC786960E integrates ARM7TDMI-S™, CD servo control, CD signal processing, compressed audio decode processing, audio signal processing, USB host processing, SD memory card host processing and a flash memory to store the program for ARM7TDMI-S™ and various data in a package. Furthermore, various kinds of interface functions such as SIO, UART etc. reduce the external main controller's processing load and make high performance and much functional CD player system, using with less components.

Features

- RF signal processing for CD-DA/R/RW, servo control, and EFM signal processing
- MP3*, WMA*, AAC* decoder processing
- Sampling rate convertor, High frequency compensation filter and other various audio signal processing
- USB host function (Full speed as 12Mbps), SD memory card host function
- ARM7TDMI-S™ as internal CPU core, flash memory for program and various data storage
- Operating voltage: 3.3V typical
- Operating temperature: -40°C to +85°C
- Packages: QIP100E (14 × 20)



QIP100E(14X20)

ORDERING INFORMATION

See detailed ordering and shipping information on page 24 of this data sheet.

Detail of Functions

[CD DSP functions]

<Playback functions>

- Playback mode: CLV playback/Jitter free playback (VCEC)
- Playback speed: Normal speed, double speed

<RF Processing block>

- RF system: AGC, CD-R and CD-R/W playback support, peak hold, bottom hold
- Error system: TE signal generation, FE signal generation
- Detection: Track count signal, Jitter, Defect (black, mirror)
- LASER power controller (APC)
- DC offset voltage cancellation

<Servo control block>

- All servo systems as tracking, focus, sled and spindle are implemented with digital processing.
- Automatic adjustment functions: focus gain, focus bias, focus offset, tracking gain, tracking offset and tracking balance
- Shock detection / Interruption detection

<CD signal processing block>

- EFM signal synchronization detection, protection and interpolation
- Error detection, correction (C1=double, C2=quadruple/double)
- Jitter margin ±19 frames

<CD TEXT processing block>

- Buffers CD-TEXT data
- Starts buffering desired ID3/ID4 of CD-TEXT data.

<CD-ROM processing block>

- CD-ROM decoding (Mode1, Mode2 <form1, form2>)
- Outputs CD-ROM decoded data

[Compressed audio decode functions]

- MP3 decode (ISO/IEC 11172-3, ISO/IEC 13818-3)
  - Sampling rate support: MPEG1-Layer1/2/3 (32kHz, 44.1kHz, 48kHz)
    MPEG2-Layer1/2/3 (16kHz, 22.05kHz, 24kHz)
    MPEG2.5-Layer3 (8kHz, 11.025kHz, 12kHz)
  - Bit rate support: All Bit Rate (Variable Bit Rate support)
  - MPEG header read support
- WMA decode (Version 9 standard)
  - Sampling rate support: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz, 44.1kHz, 48kHz
  - Bit rate support: 5kbps to 384kbps (Variable Bit Rate support)
- AAC decode (ISO/IEC 14496-3, ISO/IEC 13818-7)
  - Profile: MPEG4-AAC-LowComplexity
  - Sampling rate support: 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
  - Bit rate support: Monaural 8kbps to 160kbps (Variable bit rate support)
    Stereo 16kbps to 320kbps (Variable bit rate support)
- Decodes both the compressed data read from the disc and input from outside through the interface pins

[Audio processing functions]

<Audio processing block>

- Sampling rate converter (SRC) for compressed audio data playback
- High frequency compensation filter for compressed audio data playback
- Interpolation (CD-DA only)
- Digital attenuator
- Bilingual function
- Mute function (-12dB, -∞)
- De-emphasis filter
- Bass / Treble filter

<Digital filter and D/A convertor processing block>

- Eight-fold over-sampling digital filter (24bit)
- One bit DAC (tertiary ΔΣ noise shaper type)
- Secondary LPF for audio output

<Interface block>

- Allows external audio data supply to the digital filter and D/A converter (Uses four signals)
- Various external audio data output format
  IIS (48fs/64fs), MSB first right justified (32fs/48fs/64fs), 16 bit data length

[External interface functions]

<USB host control block>

- Open Host Controller Interface 1.0a
- Universal Serial Bus Specification 1.1
  Supports up to Full speed (12MHz)for USB2.0
- Supports four kinds of transfer type (Control/Bulk/Interrupt/Isochronous)

<SD memory card host control block>

- Multimedia Card Specification v2.11
- Secure Digital Memory Card Physical Layer Specification v0.96

* Individual contract is necessary to use SD memory card controller. For detail, please contact to us.

[Internal Microcontroller functions]

<Sequencer control>

- CD, USB, SD memory card playback control
  Servo control, CD-ROM/USB/SD file analysis, etc.

<Communication control between main controller>

- Communication format: SIO

<Peripheral interface block>

- GPIO port 27ports maximum (Shared with other functions. Several pins are 5V tolerant.)
- External interrupt pins 4pins maximum (Shared with other functions.)
- Serial interface

SIO	clock synchronized full duplex (3 lines)	2 channel
UART	full duplex	2 channel
IIC	master function	1 channel

<Program memory block>

- Flash memory
  Program version up from the external media (CD-ROM/USB)or main controller is available.

<Others>

- Watch Dog Timer
  Notify to outside from the pin or reset internally.
- Power management
  2 kinds of sleep mode
  (1) Only CPU core operates at slow clock and clocks for other blocks are stopping.
  (2) All clocks are stopping.

[Others]

<Internal power supply>

- 1.5V regulator for internal blocks

Specifications

Absolute Maximum Ratings at Ta = 25°C, DV_{SS} = AV_{SS} = LRV_{SS} = $XV_{SS}1$ = $XV_{SS}2$ = $VV_{SS}1$ = $VV_{SS}2$ = 0V

Parameter	Symbol	Pin names	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	DV_{DD}, AV_{DD}, LRV_{DD}, $XV_{DD}1$, $XV_{DD}2$, UV_{DD}, $VV_{DD}1$, $VV_{DD}2$, $VV_{DD}3$		-0.3 to +3.95	V
Input voltage 1	$V_{IN}1$	Input pins other than $V_{IN}2$		-0.3 to DV_{DD}+0.3	V
Input voltage 2	$V_{IN}2$	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, JTRSTB, JTCK, JTDI, JTMS		-0.3 to +5.6	V
Output voltage	V_{OUT}			-0.3 to DV_{DD}+0.3	V
Allowable power dissipation	Pd max		Ta ≤ 85°C Mounted reference PCB (*)	519	mW
Operating temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-40 to +125	°C

(*)Reference PCB: 114.3mm×76.1mm×1.6mm, glass epoxy resin

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ranges at Ta = -40 to +85°C,

DV_{SS} = AV_{SS} = LRV_{SS} = $XV_{SS}1$ = $XV_{SS}2$ = $VV_{SS}1$ = $VV_{SS}2$ = 0V

Parameter	Symbol	Pin names	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}1$	DV_{DD}, AV_{DD}, LRV_{DD}, $XV_{DD}1$, $XV_{DD}2$, UV_{DD}, $VV_{DD}1$, $VV_{DD}2$, $VV_{DD}3$		3.00		3.60	V
High-level input voltage	V_{IH}(1)	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, JTMS, JTRSTB, JTCK, JTDI	Schmitt	2.00		5.50	V
	V_{IH}(2)	GP13, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP43, GP44, GP45, GP50, GP51, GP52, GP53	Schmitt	2.00		$V_{DD}1$	V
Low-level input voltage	V_{IL}(1)	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, JTMS, JTRSTB, JTCK, JTDI	Schmitt	0		0.80	V
	V_{IL}(2)	GP13, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP43, GP44, GP45, GP50, GP51, GP52, GP53, MODE0, MODE1, MODE2	Schmitt	0		0.80	V
Crystal oscillator frequency	FX1	XIN XOUT	Oscillator circuit		12.0		MHz
	FX2	X16IN X16OUT	Oscillator circuit		16.9344		MHz

Electrical Characteristics at Ta = -40 to +85°C, $V_{DD}1$ = 3.0V to 3.6V,
DV_{SS} = AV_{SS} = LRV_{SS} = $XV_{SS}1$ = $XV_{SS}2$ = $VV_{SS}1$ = $VV_{SS}2$ = 0V

Parameter	Symbol	Pin names	Conditions	min	typ	max	Unit
Current drain	$I_{DD}1$	DV_{DD}, AV_{DD}, LRV_{DD}, $XV_{DD}1$, $XV_{DD}2$, UV_{DD}, $VV_{DD}1$, $VV_{DD}2$, $VV_{DD}3$			125	144	mA
High-level input current	I_{IH}(1)	RESB, SIFCK, SIFDI, JTMS, JTRSTB, JTCK, JTDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12	Schmitt, V_{IN} = 5.50V Built-in Pull-down resistor OFF			10.00	μA
	I_{IH}(2)	GP13, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP43, GP44, GP45, GP50, GP51, GP52, GP53	Schmitt, V_{IN} = $V_{DD}1$ Built-in Pull-down resistor OFF			10.00	μA
Low-level input current	I_{IL}(1)	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP43, GP44, GP45, GP50, GP51, GP52, GP53, JTMS, JTRSTB, JTCK, JTDI, MODE0, MODE1, MODE2	Schmitt, V_{IN} = 0V	-10.00			μA
High-level output voltage	V_{OH}(1)	GP04, GP05, GP06, GP07, GP12, GP13, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP43, GP44, GP50, GP51, GP52, GP53	CMOS, I_{OH} = -2mA	$V_{DD}1$-0.6			V
	V_{OH}(2)	SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP10, GP11, GP45, JTDO, JTRTCK	CMOS, I_{OH} = -4mA	$V_{DD}1$-0.6			V
Low-level output voltage	V_{OL}(1)	GP04, GP05, GP06, GP07, GP12, GP13, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP43, GP44, GP50, GP51, GP52, GP53	CMOS, I_{OL} = 2mA			0.40	V
	V_{OL}(2)	SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP10, GP11, GP45, JTDO, JTRTCK	CMOS, I_{OL} = 4mA			0.40	V
Output off-leakage current	IOFF(1)	PDOUT0, PDOUT1, AFILT	Hi-Z Out	-10.00		10.00	μA
	IOFF(2)	SIFDO	Hi-Z Out	-10.00		10.00	μA
Built-in pull down resistor	RPD	SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP43, GP44, GP45, GP50, GP51, GP52, GP53		50	100	200	kΩ
Charge pump output current	IPDOH	PDOUT1, PDOUT0	PCKIST = 100kΩ Current value setting: 1x	42.50	50.00	57.50	μA
	IPDOL	PDOUT1, PDOUT0		-57.50	-50.00	-42.50	μA
	IAFILH	AFILT			15.0		μA
	IAFILL	AFILT			15.0		μA

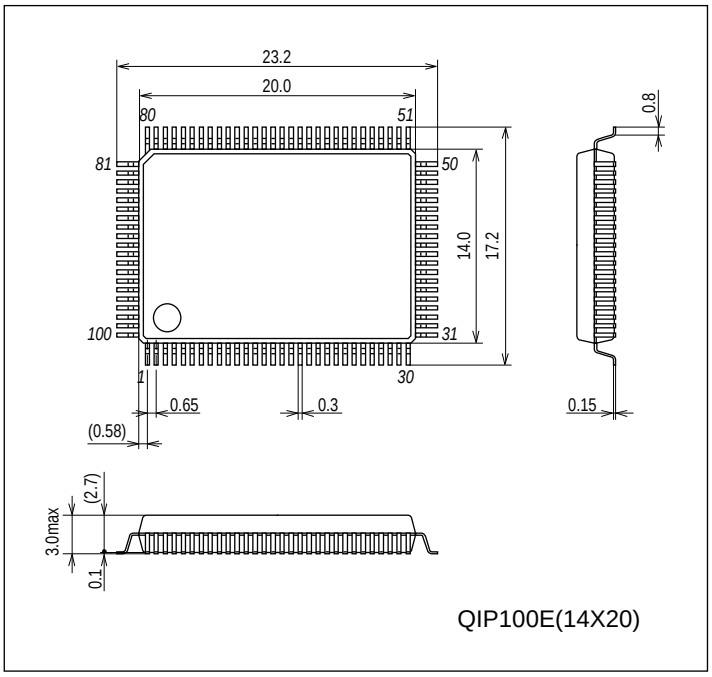
<Note>

- Put a internal pull down resistor or external pull down resistor or external pull up resistor to the SIFDO pin if its output condition is set to 3-State mode.

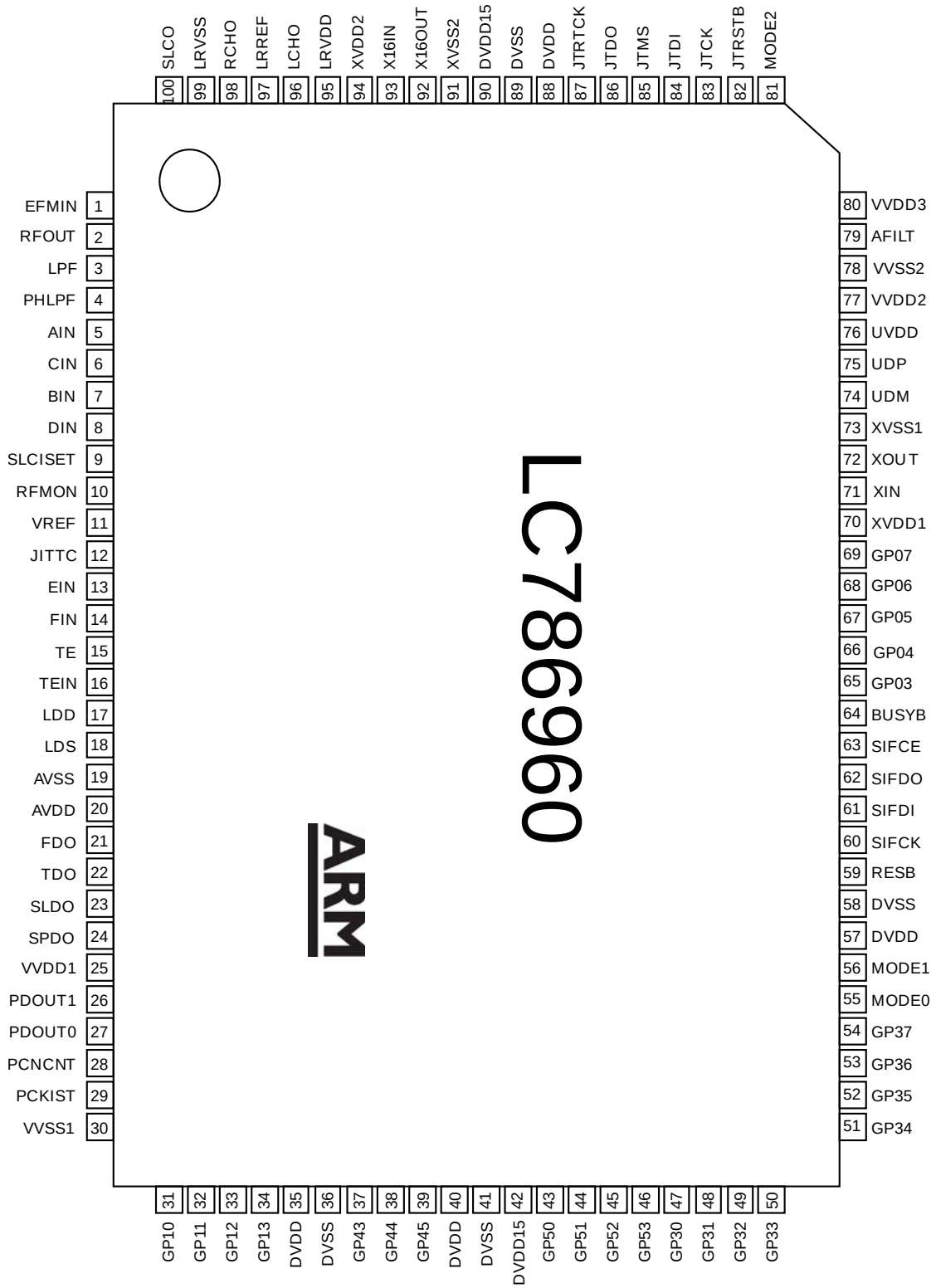
Package Dimensions

unit : mm (typ)

3151A



Pin Assignment



Top view

Pin Description

Pin No.	Pin name	I/O	State when "Reset"	Function
1	EFMIN	AI	Input	RF signal input
2	RFOUT	AO	Undefined	RF signal output
3	LPF	AO	Undefined	RF signal DC level detection low-pass filter capacitor connection
4	PHLPF	AO	Undefined	Defect detection low-pass filter capacitor connection
5	AIN	AI	Input	A signal input
6	CIN	AI	Input	C signal input
7	BIN	AI	Input	B signal input
8	DIN	AI	Input	D signal input
9	SLCISET	AI	Input	SLCO output current setting resistor connection
10	RFMON	AO	Undefined	IC internal analog signal monitor
11	VREF	AO	$AV_{DD}/2$	VREF voltage output
12	JITTC	AO	Undefined	Jitter detection capacitor connection
13	EIN	AI	Input	E signal input
14	FIN	AI	Input	F signal input
15	TE	AO	Undefined	TE signal output
16	TEIN	AI	Input	TE signal input used for TES signal generation
17	LDD	AO	Undefined	Laser power control signal output
18	LDS	AI	Input	Laser power detection signal input
19	AV_{SS}	-	-	Analog system ground. This pin must be connected to the 0V level.
20	AV_{DD}	-	-	Analog system power supply
21	FDO	AO	$AV_{DD}/2$	Focus control signal output
22	TDO	AO	$AV_{DD}/2$	Tracking control signal output
23	SLDO	AO	$AV_{DD}/2$	Sled control signal output
24	SPDO	AO	$AV_{DD}/2$	Spindle control signal output
25	$VV_{DD}1$	-	-	EFMPLL power supply
26	PDOUT1	AO	Undefined	EFMPLL charge pump output 1
27	PDOUT0	AO	Undefined	EFMPLL charge pump output 0
28	PCNCNT	AI	Input	EFMPLL charge pump control voltage input
29	PCKIST	AI	Input	EFMPLL charge pump current setting resistor connection pin
30	$VV_{SS}1$	-	-	EFMPLL ground. This pin must be connected to the 0V level.
31	GP10	I/O	Input (L)	General purpose I/O port with pull down resistor UART1 data transmit
32	GP11	I/O	Input (L)	General purpose I/O port with pull down resistor UART1 data receive
33	GP12	I/O	Input (L)	General purpose I/O port with pull down resistor Clock control input 1
34	GP13	I/O	Input (L)	General purpose I/O port with pull down resistor Clock control input 2
35	DV_{DD}	-	-	Digital system power supply
36	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
37	GP43	I/O	Input (L)	General purpose I/O port with pull down resistor
38	GP44	I/O	Input (L)	General purpose I/O port with pull down resistor
39	GP45	I/O	Input (L)	General purpose I/O port with pull down resistor
40	DV_{DD}	-	-	Digital system power supply
41	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
42	$DV_{DD}15$	AO	High	Capacitor connection pin for internal regulator
43	GP50	I/O	Input (L)	General purpose I/O port with pull down resistor
44	GP51	I/O	Input (L)	General purpose I/O port with pull down resistor
45	GP52	I/O	Input (L)	General purpose I/O port with pull down resistor
46	GP53	I/O	Input (L)	General purpose I/O port with pull down resistor

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Pin No.	Pin name	I/O	State when "Reset"	Function
47	GP30	I/O	Input (L)	General purpose I/O port with pull down resistor
48	GP31	I/O	Input (L)	General purpose I/O port with pull down resistor
49	GP32	I/O	Input (L)	General purpose I/O port with pull down resistor Data 1 input/output for SD memory card
50	GP33	I/O	Input (L)	General purpose I/O port with pull down resistor Data 0 input/output for SD memory card
51	GP34	I/O	Input (L)	General purpose I/O port with pull down resistor Clock output for SD memory card
52	GP35	I/O	Input (L)	General purpose I/O port with pull down resistor Command input/output for SD memory card
53	GP36	I/O	Input (L)	General purpose I/O port with pull down resistor Data 3 input/output for SD memory card
54	GP37	I/O	Input (L)	General purpose I/O port with pull down resistor Data 2 input/output for SD memory card
55	MODE0	I	Input	LSI mode set pin 0 This pin must be connected to the 0V level.
56	MODE1	I	Input	LSI mode set pin 1 This pin must be connected to the 0V level.
57	DV_{DD}	-	-	Digital system power supply
58	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
59	RESB	I	-	IC reset input ("L"-active) This pin must be set low once after power is first applied.
60	SIFCK	I	Input	Host-I/F Data transmit clock input for serial communication 1
61	SIFDI	I/O	Input	Host-I/F Data input for serial communication 1
62	SIFDO	I/O	Input	Host-I/F Data output for serial communication 1 (CMOS or 3-State output)
63	SIFCE	I/O	Input	Host -I/F Enable signal input for serial communication 1 ("H"-active)
64	BUSYB	I/O	Input (L)	Host -I/F System busy signal output ("L"-active)
65	GP03	I/O	Input (L)	General purpose I/O port with pull down resistor USB device detection flag output
66	GP04	I/O	Input (L)	General purpose I/O port with pull down resistor IIC (master) clock output
67	GP05	I/O	Input (L)	General purpose I/O port with pull down resistor IIC (master) data input/output
68	GP06	I/O	Input (L)	General purpose I/O port with pull down resistor
69	GP07	I/O	Input (L)	General purpose I/O port with pull down resistor
70	$XV_{DD}1$	-	-	Oscillator power supply
71	XIN	I	Oscillation	12MHz oscillator connection
72	XOUT	O	Oscillation	12MHz oscillator connection
73	$XV_{SS}1$	-	-	Oscillator ground. This pin must be connected to the 0V level.
74	UDM	I/O	-	USB data input/output D- signal connection
75	UDP	I/O	-	USB data input/output D+ signal connection
76	UV_{DD}	-	-	USB power supply
77	$VV_{DD}2$	-	-	System PLL power supply
78	$VV_{SS}2$	-	-	System PLL ground. This pin must be connected to the 0V level.
79	AFILT	AO	Undefined	Audio PLL charge pump output
80	$VV_{DD}3$	-	-	Audio PLL power supply
81	MODE2	I	Input	LSI mode set pin 2 This pin must be connected to the 0V level.

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Pin No.	Pin name	I/O	State when "Reset"	Function
82	JTRSTB	I	Input	JTAG reset input (Connect to pll-down resister or 0V level in normal mode.)
83	JTCK	I	Input	JTAG clock input (Connect to pll-down resister or 0V level in normal mode.)
84	JTDI	I	Input	JTAG data input (Connect to pll-down resister or 0V level in normal mode.)
85	JTMS	I	Input	JTAG mode input (Connect to pll-up resister or DV_{DD} level in normal mode.)
86	JTDO	O	Low	JTAG data output (Leave open in normal mode.)
87	JTRTCK	O	Low	JTAG return clock output (Leave open in normal mode.)
88	DV_{DD}	-	-	Digital system power supply
89	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
90	$DV_{DD}15$	AO	High	Capacitor connection pin for internal regulator
91	$XV_{SS}2$	-	-	Oscillator ground. This pin must be connected to the 0V level.
92	X16OUT	O	Oscillation	16.9344MHz oscillator connection
93	X16IN	I	Oscillation	16.9344MHz oscillator connection
94	$XV_{DD}2$	-	-	Oscillator power supply
95	LRV_{DD}	-	-	Audio LPF power supply
96	LCHO	AO	$LRV_{DD}/2$	Audio Lch data output
97	LRREF	AO	$LRV_{DD}/2$	Reference voltage for audio LPF
98	RCHO	AO	$LRV_{DD}/2$	Audio Rch data output
99	LRV_{SS}	-	-	Audio LPF ground. This pin must be connected to the 0V level.
100	SLCO	AO	Undefined	Slice Level Control output

<Note>

(1) For unused pins:

- The unused input pins must be connected to the GND (0V) level if there is no individual note in the above table.
- The unused output pins must be left open (No connection) if there is no individual note in the above table.
- The unused input/output pins must be connected to the GND (0V) or power supply pin for I/O block with internal pull down resistor OFF or be left open with internal pull down resistor ON when input pin mode or must be left open (No connection) when output pin mode if there is no individual note in the above table.
  When you connect an I/O pin which is an input pin without internal pull-down resistor at reset mode to the GND or power supply level, we recommend you to use pull-down resistor or pull-up resistor individually as fail-safe.

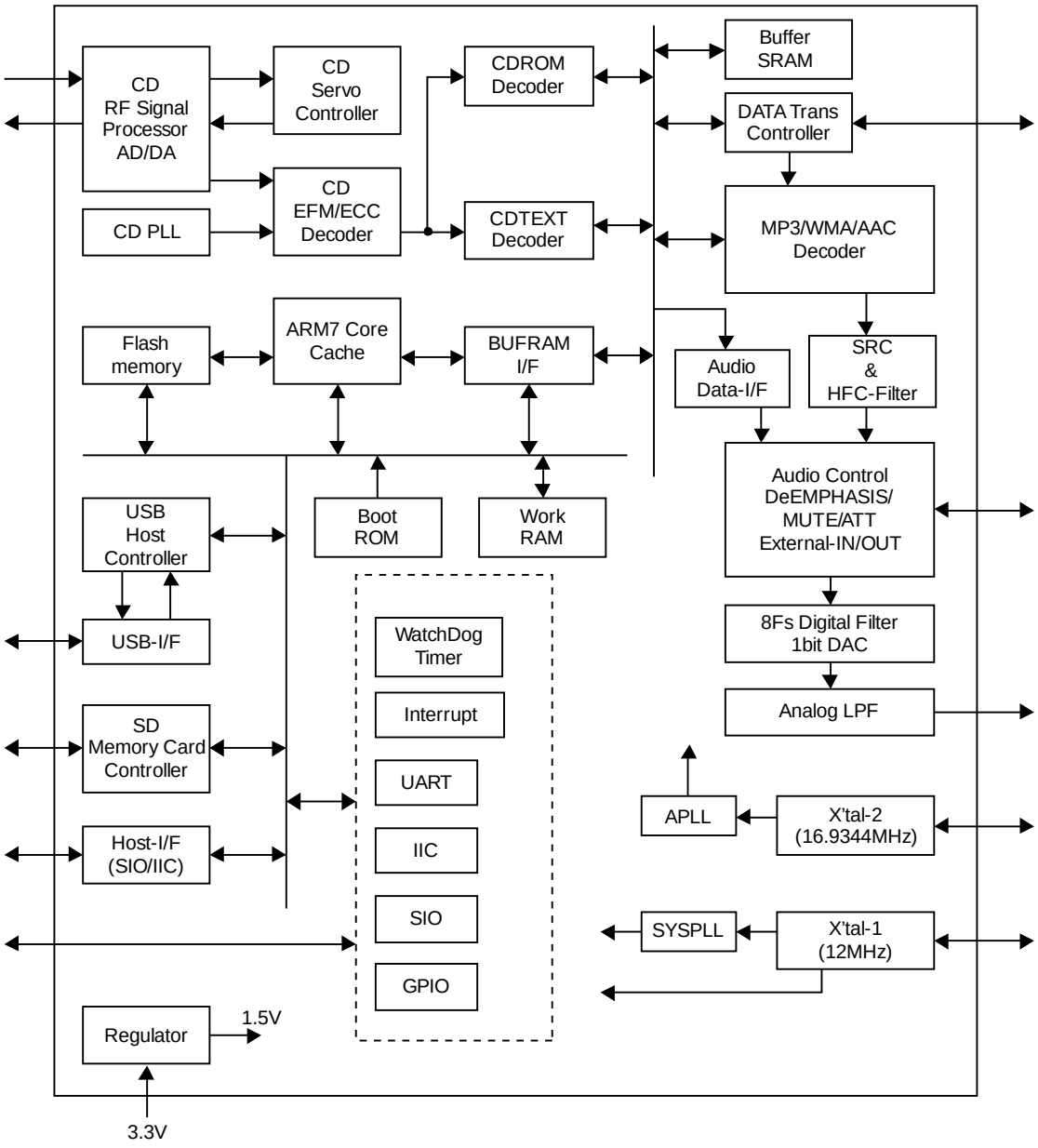
(2) For power supply pins:

- Same voltage level must be supplied to DV_{DD}, AV_{DD}, $XV_{DD}1$, $XV_{DD}2$, $VV_{DD}1$, $VV_{DD}2$, $VV_{DD}3$, UV_{DD} and LRV_{DD} power supply pins.
  (Refer to“Allowable operating ranges”.)

(3) For “Reset” condition:

- This LSI is not reset only by making the RESB pin “Low”.
  Refer to “Power on and Reset control” for detail of “Reset” condition.

Block Diagram

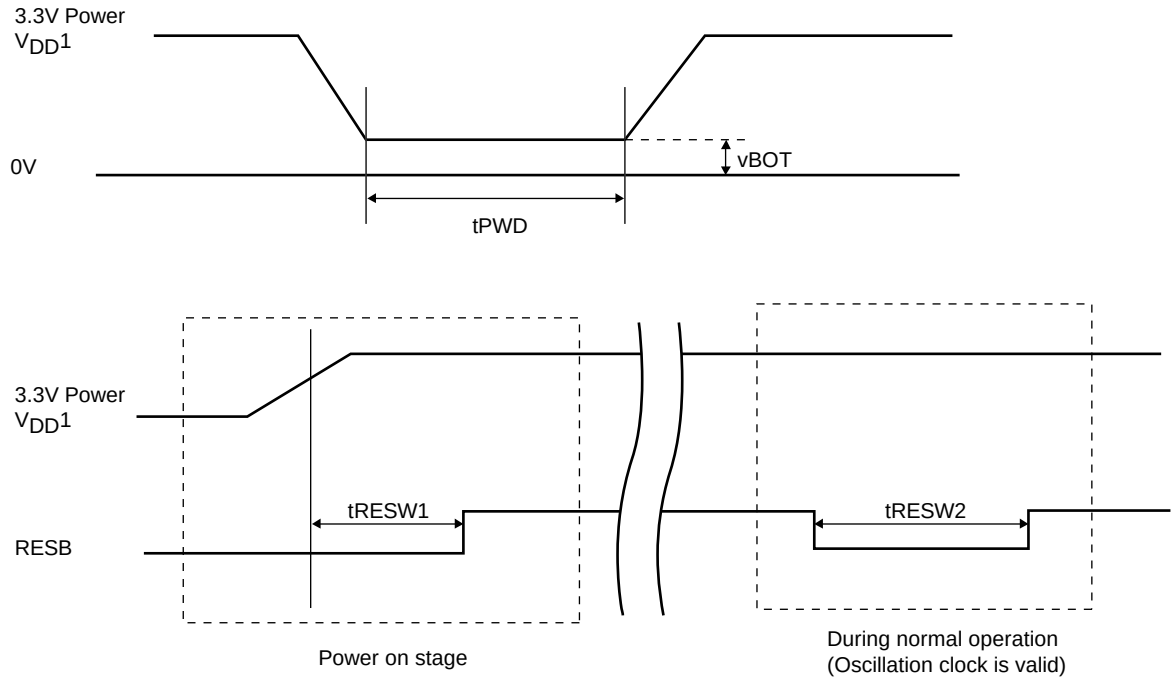


Power on and Reset control

- Attention when power on

  The RESB pin must be set to “Low” level to initialize the operating state of internal flash memory.
  If the power is on during the RESB pin is “High” level, this LSI may operate incorrectly because the internal flash memory is not initialized. In this case, this LSI is not initialized even if a low level supplied to RESB pin.
  Therefore, the RESB pin must be set to “Low” level when power is first supplied.
  You may input the voltage of 3.6V or less to each input pin when the power supply is off. However, it is necessary to supply a regulated voltage to the power supply pin beforehand when more than 3.6V voltage is input to the 5V tolerant input pins.

Power ON/Power Down/Reset timing



Parameter	Symbol	min	typ	max	unit
Power down time	tPWD	10			ms
Power down voltage	vBOT	0		0.2	V
Reset time (Power on)	tRESW1	20			ms
Reset time (Normal) (*1)	tRESW2	1			ms

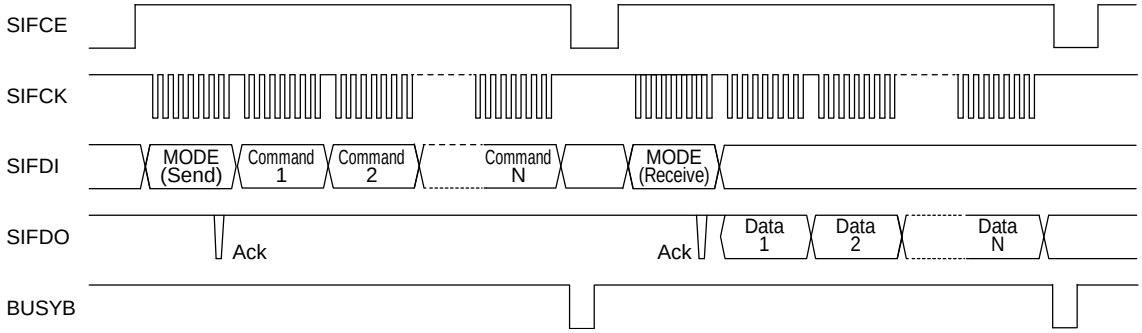
*1: The specification of tRESW2 above is the time defined while steady the X16 clock and having oscillated.
When the X16 clock has been stopped by the command etc. , the specification of tRESW2 could be larger than the value shown above, because it takes time that the X16 oscillator becomes stable.

Host interface

The data transmission between this LSI and Host controller is performed with SPI type synchronous SIO protocol. The transmission procedure is as follows.

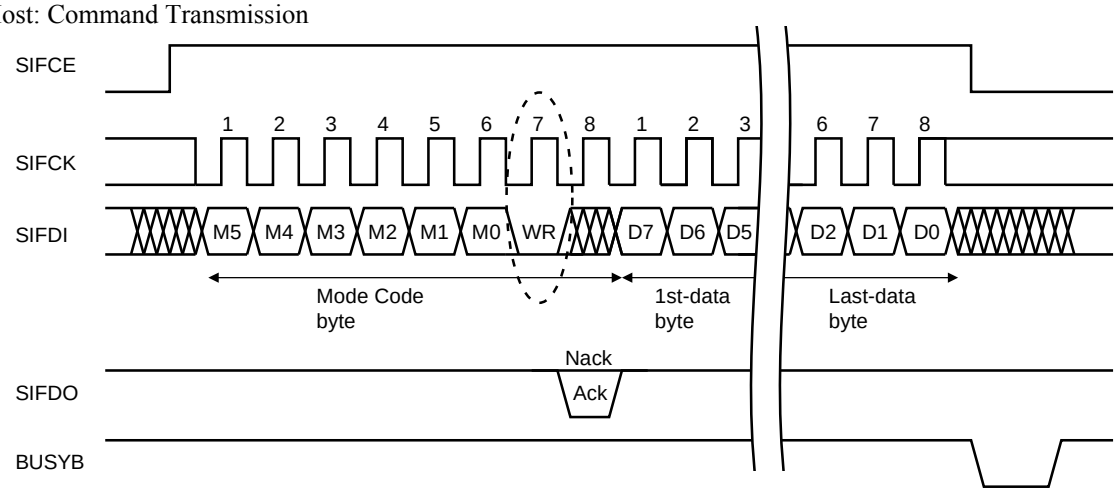
- Refer to the internal software specification of this LSI about M5 to M0 code in Mode code transmission. When the input data of M5 to M0 coincide to the data in the internal register, the SIFDO pin becomes to "Low" level (Ack) then the transmission is enabled.
  When not coincide, the SIFDO pin keeps "High" level (Nack) then the transmission is not enabled.
- The seventh data in Mode code transmission shows whether the following procedure is the Command transmission or the Data reception. When the seventh data is "Low", the following procedure is Command transmission. When the seventh data is "High", the following procedure is Data reception.
- Attention because the specifications of transmission timings are different depending on the internal CPU's operating speed modes (Low speed or Normal speed). Refer to the table in next page.

Communication Interface format between Host controller

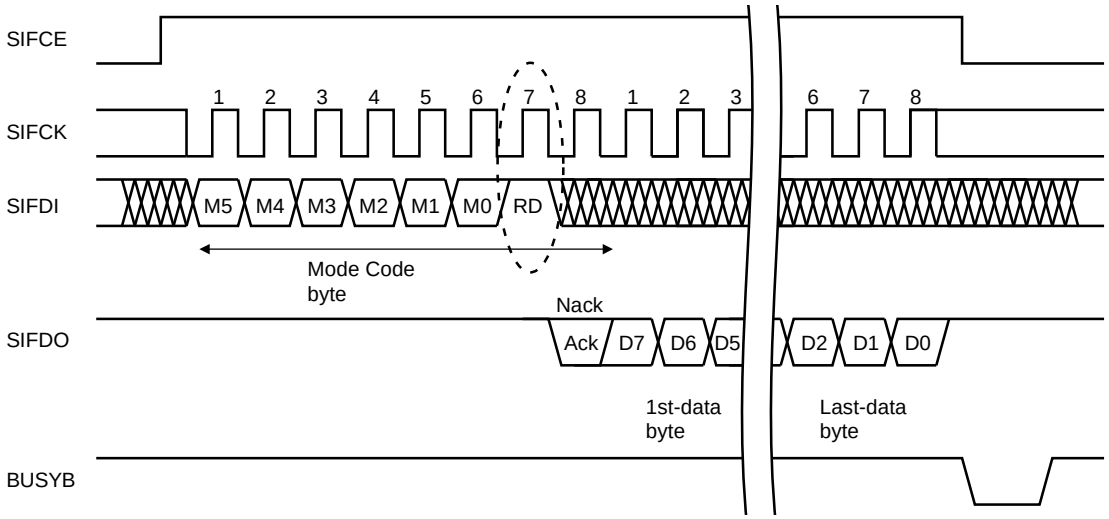


Transmission/Reception format between Host controller

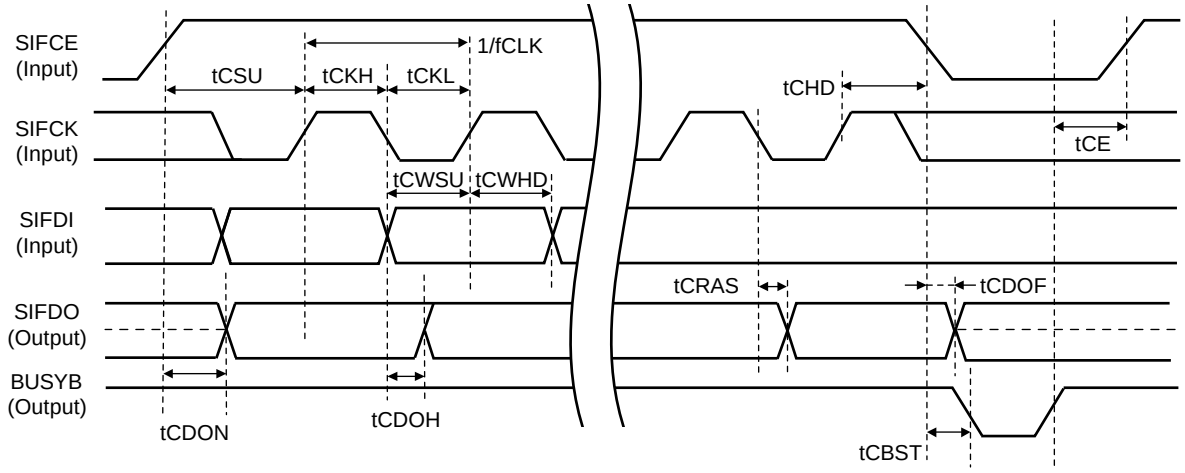
(1) Host: Command Transmission



(2) Host: Data Reception



Communication Timing specification between Host controller



Parameter	Symbol	Pin names	min	typ	max	unit
SIFCK clock frequency	fCLK	SIFCK			3.3 0.725	MHz
SIFCK clock "H" level width	tCKH	SIFCK	150 690			ns
SIFCK clock "L" level width	tCKL	SIFCK	150 690			ns
Transfer start enable time	tCE	BUSYB, SIFCE	0 0			ns
Setup time for transfer start	tCSU	SIFCE, SIFCK	100 200			ns
Hold time for transfer end	tCHD	SIFCE, SIFCK	100 200			ns
Setup time for SIFDI	tCWSU	SIFDI, SIFCK	75 75			ns
Hold time for SIFDI	tCWHD	SIFDI, SIFCK	75 200			ns
Output delay time for SIFDO “H”	tCDOH	SIFDO, SIFCK			100 350	ns
Output delay time for SIFDO	tCRAS	SIFDO, SIFCK			100 350	ns
Turn on time for SIFDO *1	tCDON	SIFDO, SIFCE			100 100	ns
Turn off time for SIFDO *1	tCDOF	SIFDO, SIFCE			150 150	ns
BUSYB "L" level output delay time	tCBST	BUSYB			150 350	ns

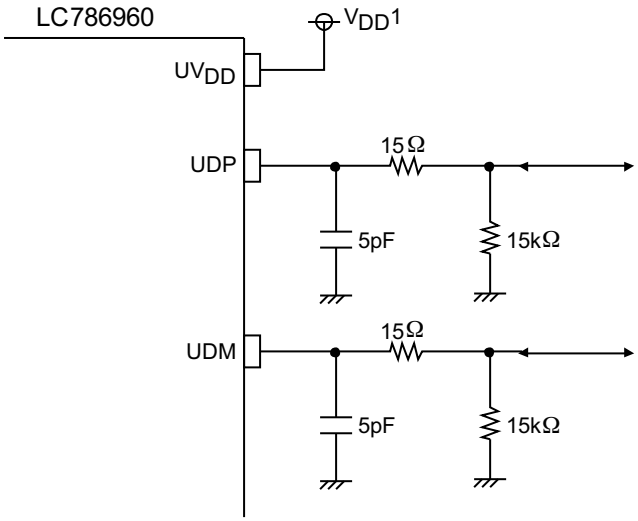
Internal CPU operating speed mode Upper step : Normal speed
Lower step : Low speed

*1: The tCDON and tCDOF specifications are for when the SIFDO pin is set to the 3-State mode.

USB Specification at Ta = -40°C to +85°C, $V_{DD}1$ = 3.0V to 3.6V,
$DV_{SS} = AV_{SS} = LRV_{SS} = XV_{SS}1 = XV_{SS}2 = VV_{SS}1 = VV_{SS}2 = 0V$

Parameter	Symbol	Pin names	Conditions	min	typ	max	unit
High-level input voltage	V_{IH} (USB)	UDM, UDP		2.0			V
Low-level input voltage	V_{IL} (USB)					0.8	
Input leakage current	ILI		Output driver: OFF	-10.0		10.0	μA
Differential input sensitivity	VDI		|(UDP) - (UDM)|	0.2			V
Common mode voltage range	VCM		Includes VDI range	0.8		2.5	V
High-level output voltage	V_{OH} (USB)		Connect 15kΩ ±5% pull-down resistor to GND (0V).	2.8		3.6	V
Low-level output voltage	V_{OL} (USB)		Connect 1.5kΩ ±5% pull-up resistor to $V_{DD}1$.	0		0.3	V
Crossover voltage	VCR			1.3		2.0	V
USB data rising time	TUR		CL = 50pF	4.0		20.0	ns
USB data falling time	TUF			4.0		20.0	

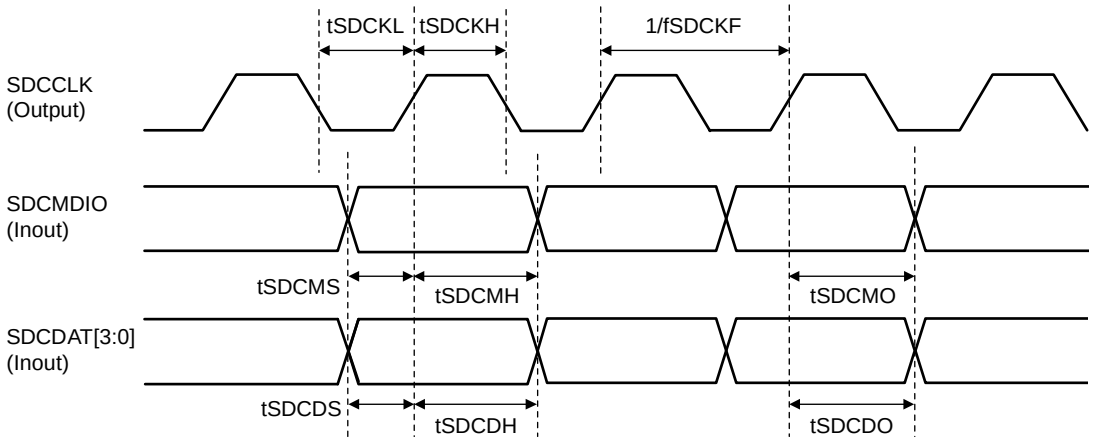
Example circuit for USB application



* The value of resistors and capacitors in this circuit might be needed to be adjusted for each application.

SD Memory Card Interface

SD Memory Card Input/Output Timing specification



* Relationship between signal name and pin name

SDCCLK	: GP34	SDCMDIO	: GP35	SDCDAT [3]	: GP36
SDCDAT [2]	: GP37	SDCDAT [1]	: GP32	SDCDAT [0]	: GP33

Parameter	Symbol	Pin names	min	typ	max	unit
SDCCLK clock frequency	fSDCKF	SDCCLK		6.0		MHz
SDCCLK clock "H" level width	tSDCKH	SDCCLK		83.3		ns
SDCCLK clock "L" level width	tSDCKL	SDCCLK		83.3		ns
Setup time for command input	tSDCMS	SDCMDIO, SDCCLK	30.0			ns
Hold time for command input	tSDCMH	SDCMDIO, SDCCLK	30.0			ns
Command output valid time	tSDCMO	SDCMDIO, SDCCLK			30.0	ns
Setup time for data input	tSDCDS	SDCDAT [3:0], SDCCLK	30.0			ns
Hold time for data input	tSDCDH	SDCDAT [3:0], SDCCLK	30.0			ns
Data output valid time	tSDCDO	SDCDAT [3:0], SDCCLK			30.0	ns

Note: Internal CPU (ARM7) must be set to normal mode. Never use the SD Memory Card interface at the internal CPU's Low speed mode.

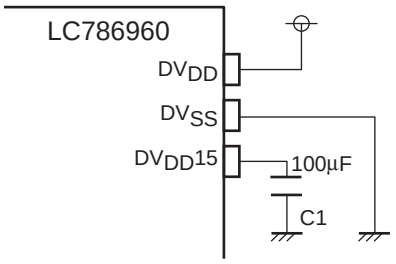
Internal Voltage Regulator at Ta = -40°C to +85°C,

$DV_{SS} = AV_{SS} = LRV_{SS} = XV_{SS}1 = XV_{SS}2 = VV_{SS}1 = VV_{SS}2 = 0V$

Parameter	Symbol	Condition	min	typ	max	unit
Output voltage	$DV_{DD}15$	$V_{DD}1$ = 3.0V to 3.6V	1.35	1.50	1.65	V
Load current	Iope	$V_{DD}1$ = 3.3V			200	mA

Note : The spec. of "load current" above is sum of the load current of two internal voltage regulator.

Example circuit for Regulator



* Same circuit need to be mounted both for two regulator pins. (No.42 and No.90)
* The capacitor C1 must be greater than 50µF and low Secure 50µF or more for low ESR and the capacity value in the range of the operating temperature so that there is a possibility of the oscillation when the capacity value changes by the temperature change etc.
  (The recommended value is 100µF.)

A/D, D/A converter Characteristics for servo

at Ta = -40°C to +85°C, $V_{DD}1$ = 3.3V, $DV_{SS} = AV_{SS} = LRV_{SS} = XV_{SS}1 = XV_{SS}2 = VV_{SS}1 = VV_{SS}2 = 0V$

Parameter	Symbol	Condition	min	typ	max	unit
Resolution	Res			8		bit
Maximum input/output range	Vaio1			$4/5 \times V_{DD}1$		V
Minimum input/output range	Vaio2			$1/5 \times V_{DD}1$		V

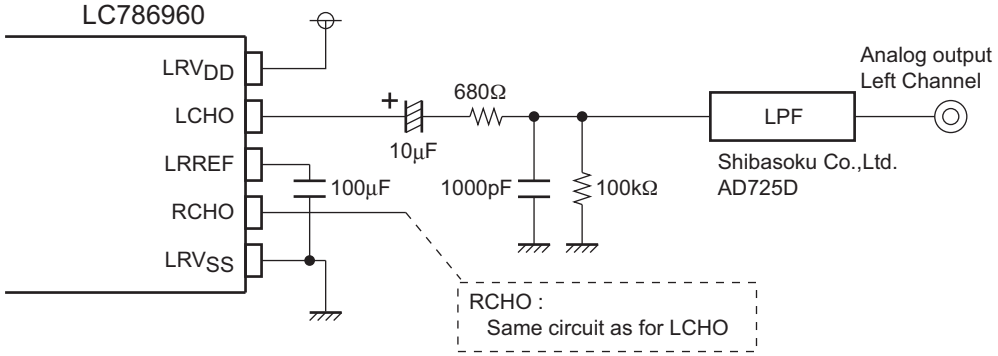
1-Bit D/A converter Characteristics

at Ta = 25°C, $V_{DD}1$ = 3.3V, $DV_{SS} = AV_{SS} = LRV_{SS} = XV_{SS}1 = XV_{SS}2 = VV_{SS}1 = VV_{SS}2 = 0V$

Parameter	Symbol	Pin names	Conditions	min	typ	max	unit
Output level	LEVEL	LCHO, RCHO	With a 1kHz, 0dB data signal		0.63		Vrms
Total harmonics distortion	THD+N	LCHO, RCHO	With a 1kHz, 0dB data signal, Using the 20kHz Low-pass filter (built-in AD725D)		0.008	0.012	%
Dynamic range	DR	LCHO, RCHO	With a 1kHz, -60dB data signal, Using the 20kHz Low-pass filter and A-filter (built-in AD725D)	92	96		dB
Signal to noise ratio	S/N	LCHO, RCHO	With a 1kHz, 0dB data signal, Using the 20kHz Low-pass filter and A-filter (built-in AD725D)	95	98		dB
Cross talk	CT	LCHO, RCHO	With a 1kHz, 0dB data signal, Using the 20kHz Low-pass filter (built-in AD725D)	82	85		dB

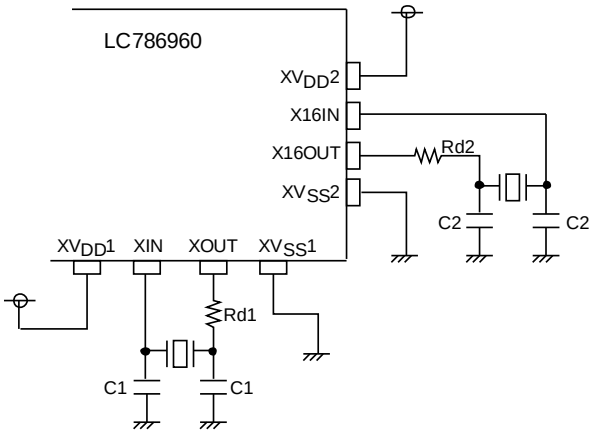
Note : Measured in normal speed playback mode in Ours 1-bit D/A converter block reference circuit.

1-Bit D/A converter output reference circuit



Oscillator

Example circuit for Oscillator



(1) XIN/XOUT: 12.0000MHz

- For System Main clock, USB control
- Recommended Oscillator

Nihon Dempa Kogyo Co., Ltd.

Type	Recommended value
NX5032GA	Rd1 = 0Ω, C1 = 4pF
NX8045GB	Rd1 = 0Ω, C1 = 4pF

(2) X16IN/X16OUT: 16.9344MHz

- For CD control, Audio control
- Recommended Oscillator

Murata Manufacturing Co., Ltd.

Type	Recommended value
CSTCE16M9V53-R0	Rd2 = 0Ω, C2 = open
CSTCW16M9X51008-R0	Rd2 = 0Ω, C2 = open
CSTLS16M9X53-B0	Rd2 = 0Ω, C2 = open

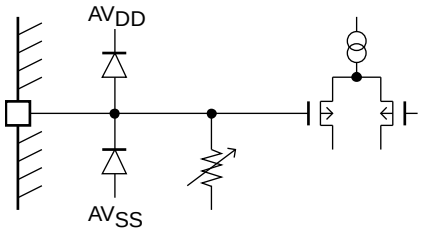
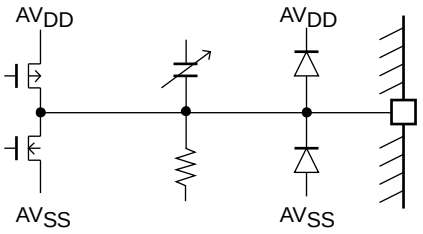
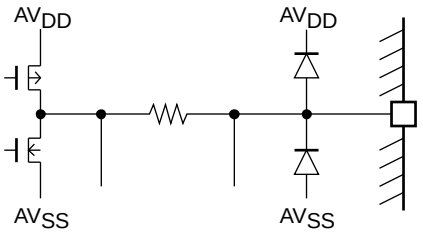
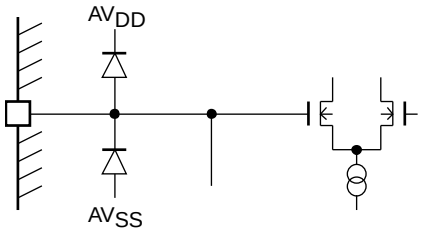
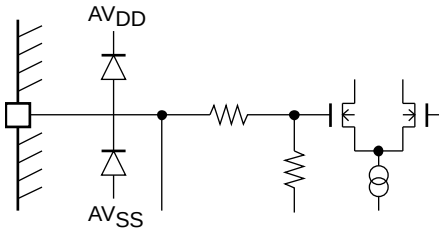
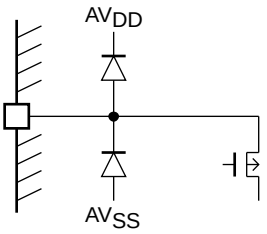
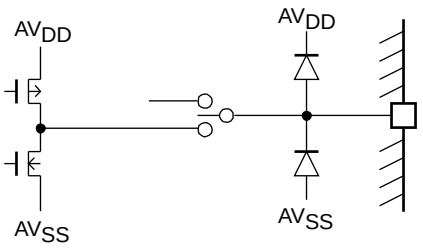
Nihon Dempa Kogyo Co., Ltd.

Type	Recommended value
AT51-CD2	Rd2 = 0Ω, C2 = 8pF

<Notes>

- Because the characteristics of oscillator could be changed according to the circuit board, ask evaluation with the individual original circuit board to the oscillator maker.
- The accuracy of 12MHz oscillator (XIN/XOUT) must be in ±500ppm when this oscillator clock is used for USB Host function.
- Concerning about internal circuit for XIN/XOUT and X16IN/X16OUT, refer to the “Analog Pin Internal Equivalent Circuits” section.

Analog Pin Internal Equivalent Circuits

Pin Name (Pin No.)	Equivalent circuit
EFMIN (1)	
RFOUT (2)	
LPF (3)	
PHLPF (4)	
AIN (5) CIN (6) BIN (7) DIN (8)	
SLCISET (9)	
RFMON (10)	

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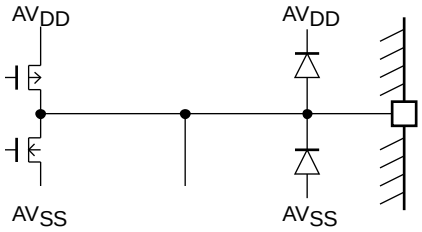
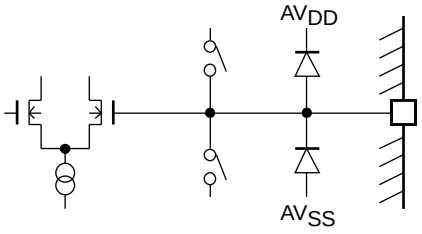
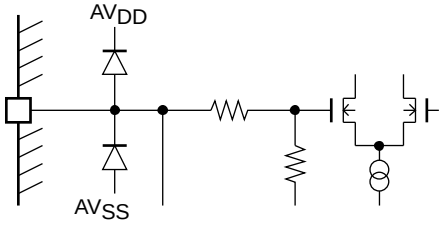
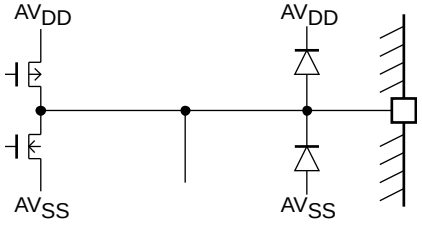
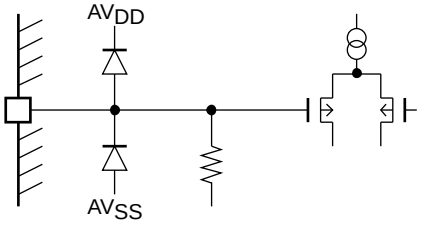
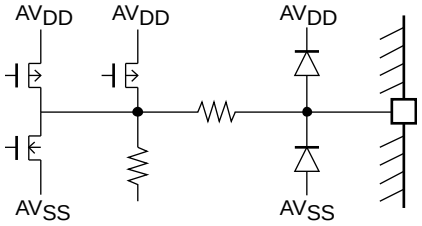
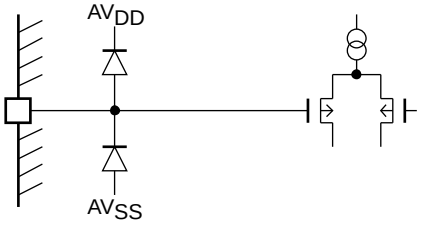
Pin Name (Pin No.)	Equivalent circuit
VREF (11)	
JITTC (12)	
EIN (13) FIN (14)	
TE (15)	
TEIN (16)	
LDD (17)	
LDS (18)	

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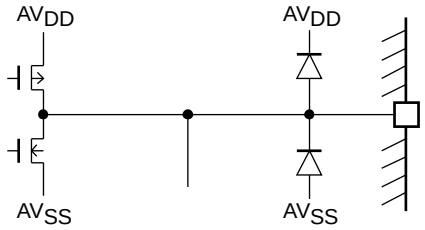
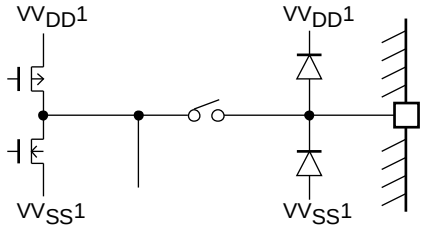
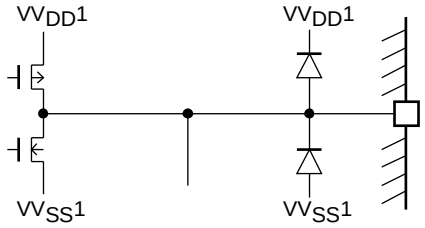
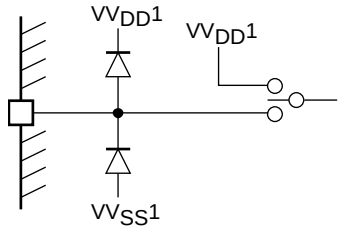
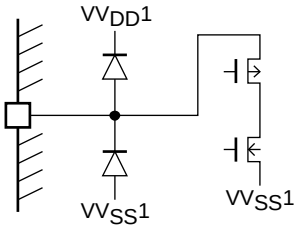
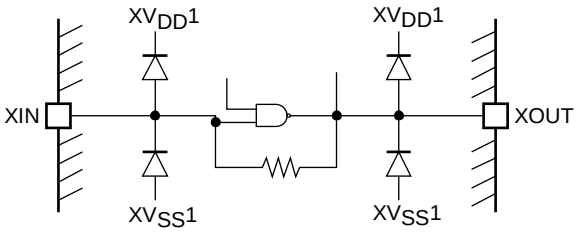
Pin Name (Pin No.)	Equivalent circuit
FDO (21) TDO (22) SLDO (23) SPDO (24)	
PDOUT1 (26)	
PDOUT0 (27)	
PCNCNT (28)	
PCKIST (29)	
XIN (71) XOUT (72)	

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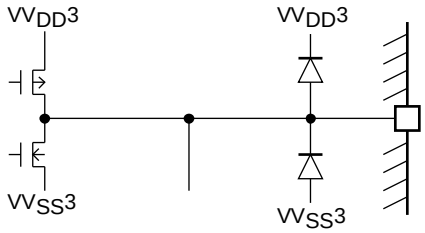
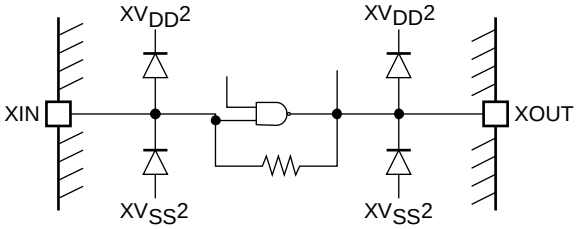
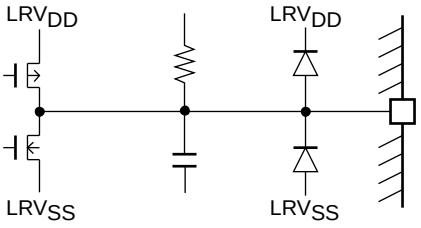
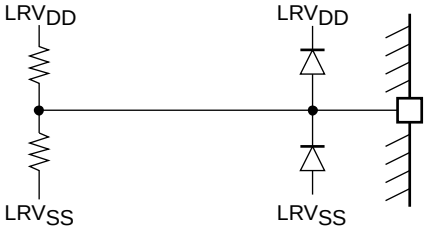
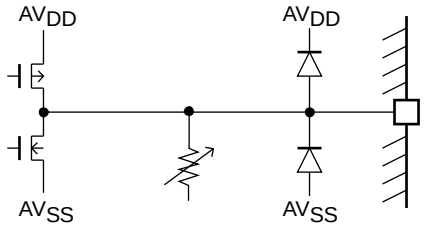
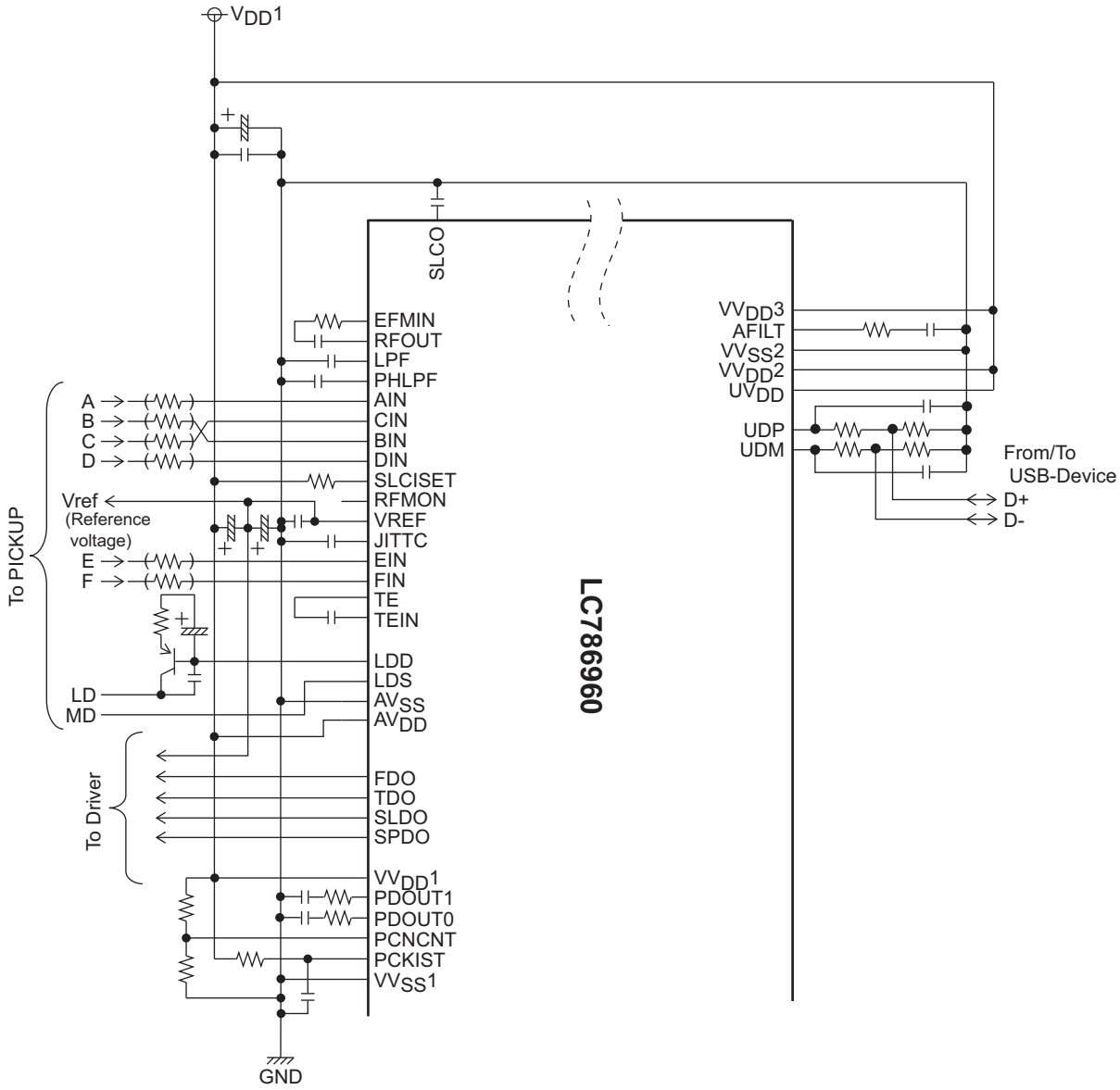
Pin Name (Pin No.)	Equivalent circuit
AFILT (79)	
X16OUT (92) X16IN (93)	
LHCO (96) RCHO (98)	
LRREF (97)	
SLCO (100)	

Sample Application Circuit



* This sample circuit is only for CD servo block, each PLL block and USB block.
The value of each component needs to be adjusted under the target conditions.
The circuit for CD servo shown above could be changed depending on the CD mechanism used.

Concerning to the application circuit for Regulator, Audio DAC and Oscillator, refer to the page 17 and 18 respectively.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC786960E-H	QIP100E(14X20) (Pb-Free / Halogen Free)	250 / Tray Foam