Ordering number : ENN7457A

LC89052TA-E

CMOS IC

Digital Audio Interface Receiver

ON Semiconductor®

http://onsemi.com

1. Overview

The LC89052TA-E is an audio LSI that demodulates according to the data format for the data transferred between digital audio devices via the IEC 60958/61937 and EIAJ CP-1201. It supports sampling frequencies of up to 192kHz and output data lengths up to 28 bits.

Despite it is compact and made in a low cost, the LC89052TA-E includes a built-in oscillator and serial data input circuits and allows the system microcontroller to read the sub-code Q data and channel status. It supports low-power modes that allow low-voltage operation. It also supports a lower power mode, which is suitable for application that requires long battery life, such as cell phones, PDAs, and portable audio devices.

2. Features

- Incorporates a built-in PLL circuit to synchronize with transferred bi-phase mark signal.
- Can receive input with sampling frequencies of 32kHz to 192kHz.
- Can set the upper limit of sampling frequency of received data.
- Can receive input data of specific sampling frequencies.
- Outputs the following clocks: fs, 64fs, 128fs, 256fs, 384fs, and 512fs.
- Contains a built-in oscillation amplifier that can construct a oscillation circuit. An external clock can be also provided.
- Outputs an externally input clock signal that can be used as the A/D converter clock when the PLL is unlocked.
- Maintains the continuity of the output clock when the clock is switched.
- Equipped with a serial digital audio data input pin that can be configured for a demodulated signal output.
- Can output up to 28 bits of data, and also supports output of I^2S and input NRZ data.
- Can output bi-phase mark signal synchronized with the 128fs bit clock.
- Provides an output pin for the channel status bit 1 non-PCM data detection bit.
- Provides an output pin for the channel status emphasis detection bit.
- Supports a lower-power mode.
- Calculates the input signal sampling frequency and outputs it from the microcontroller interface.
- Can output the first 48 bits of the channel status with the microcontroller interface.
- Can output the 80-bit sub-code Q data with CRC flags via microcontroller interface.
- Outputs various state changes as interrupt signals to the microcontroller interface.

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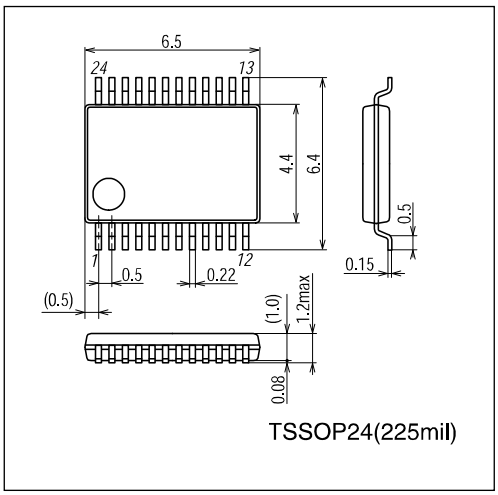
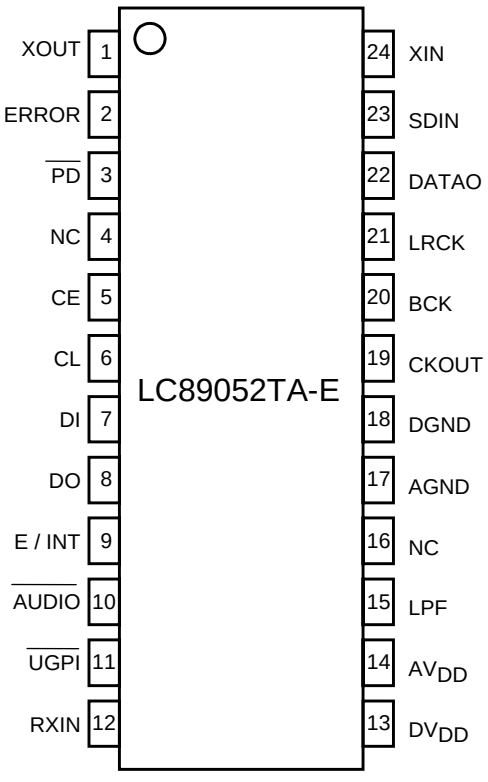
- Equipped with a user definable output port that can be selected from the following functions.
  —Microcontroller interface register output (for power saving mode optical module control signals, etc.)
  —Signal output of transitional period where VCO clock and external input clock are switched.
- Can dispense with un-used microcontroller control.
- 3.3V single source power supply (Can operate at a minimum voltage of 2.7V.)
- The TTL input ports can support 5V interface operation.
- Package: TSSOP-24

3. Package Dimensions

unit : mm
3260A



4. Pin Assignments



Top view

5. Pin Description

Table 5.1 Pin Functions

Pin No.	Name	I/O	Function
1	XOUT	O	Oscillation amplifier circuit output pin
2	ERROR	O	PLL lock error and data error output pin
3	$\overline{PD}$	I_5	System reset and low-power mode control input pin
4	NC		Non connection
5	CE	I_5	Microcontroller interface: chip enable input pin
6	CL	I_5	Microcontroller interface: serial clock input pin
7	DI	I_5	Microcontroller interface: write data input pin
8	DO	O	Microcontroller interface: read data output pin
9	E / INT	O	Pre-emphasis detection or microcontroller interface interrupt output pin
10	$\overline{AUDIO}$	O	Channel status bit 1 non-PCM data detection output pin
11	$\overline{UGPI}$	O	User settable output pin *
12	RXIN	I_5	Digital data input pin
13	DV_{DD}		Digital power supply pin
14	AV_{DD}		Analog power supply pin
15	LPF	O	PLL loop filter pin
16	NC		Non connection
17	AGND		Analog GND pin
18	DGND		Digital GND pin
19	CKOUT	O	System clock output pin **
20	BCK	O	64fs clock output pin
21	LRCK	O	Fs clock output pin ***
22	DATAO	O	Demodulated data output pin
23	SDIN	I_5	Serial digital data input pin
24	XIN	I	Oscillator or external clock input pin

* : Microcontroller register output or clock switching transition period signal.

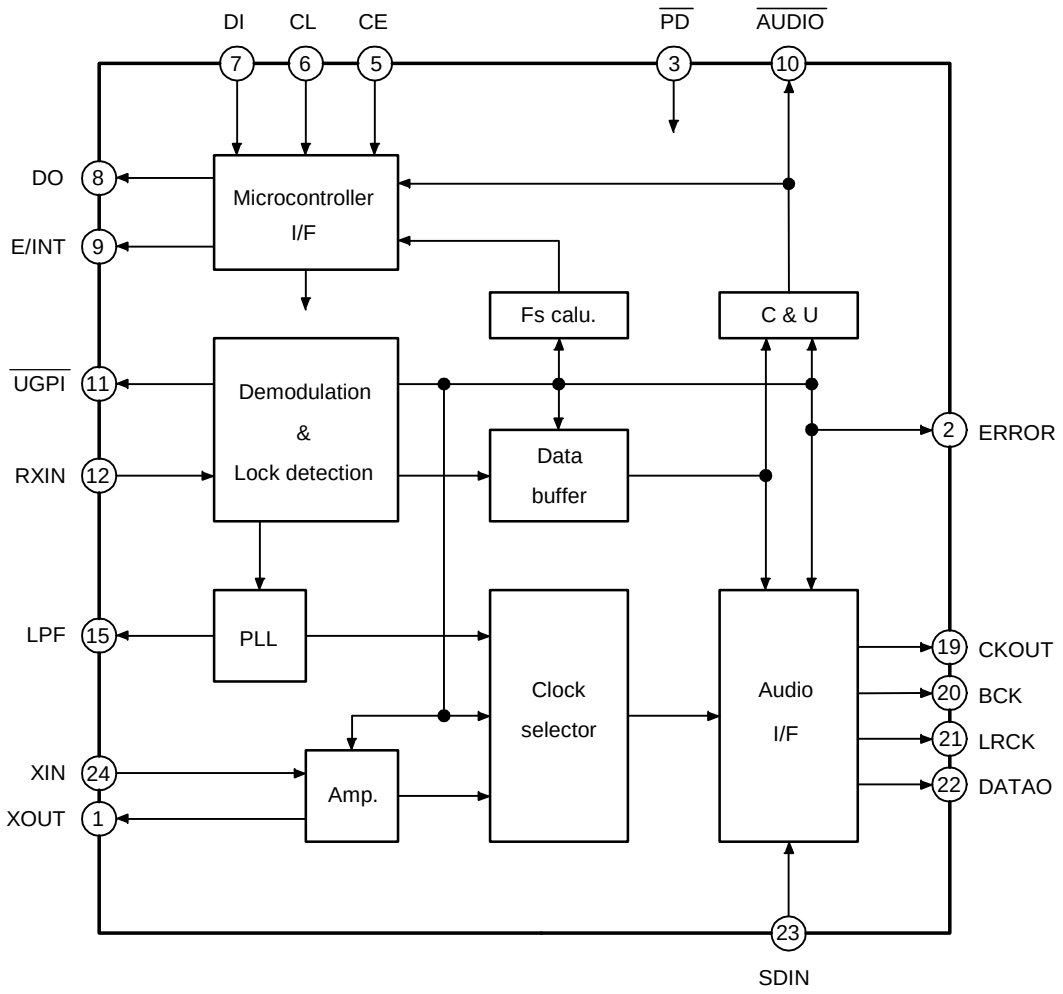
** : 128fs, 256fs, 384fs, 512fs, or oscillator amplifier outputs.

*** : Other than I^2S mode ; Low: right channel, High: left channel.
I^2S mode ; Low: left channel, High: right channel.

1) I/O voltage handling :
I or O pins : –0.3 to +3.6V,
I_5 pins : –0.3 to +5.5V

2) To prevent logic circuit latch-up, all power supply must be applied or removed simultaneously.

6. Block Diagram



7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 7.1 Absolute Maximum Ratings at AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage	AV_{DD} max	7-1-1	–0.3 to 4.6	V
Maximum supply voltage	DV_{DD} max	7-1-2	–0.3 to 4.6	V
Input voltage 1	$V_{IN}1$	7-1-3	–0.3 to 3.9	V
Input voltage 2	$V_{IN}2$	7-1-4	–0.3 to 5.8	V
Output voltage	V_{OUT}	7-1-5	–0.3 to 3.9	V
Storage temperature	Tstg		–55 to 125	°C
Operating temperature	Topg		–30 to 70	°C
Maximum output current	Ii, I_{OUT}	7-1-6	±20	mA

7-1-1 : AV_{DD} pin.
7-1-2 : DV_{DD} pin.
7-1-3 : XIN pin.
7-1-4 : RXIN, SDIN, $\overline{PD}$, CE, CL, and DI pins.
7-1-5 : XOUT, ERROR, DO, E/INT, $\overline{AUDIO}$, $\overline{UGPI}$, CKOUT, BCK, LRCK, and DATAO pins.
7-1-6 : Per single input or output pin.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

7.2 Recommended Operating Conditions

Table 7.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	min	typ	max	unit
Supply voltage 1	AV_{DD}, DV_{DD}	7-2-1	2.7	3.3	3.6	V
Supply voltage 2	AV_{DD}, DV_{DD}	7-2-2	3.0	3.3	3.6	V
Input voltage range 1	$V_{IN}1$	7-2-3	0	3.3	3.6	V
Input voltage range 2	$V_{IN}2$	7-2-4	0	3.3	5.5	V
Operating temperature	Vopg		–30		70	°C

7-2-1 : PLLCK [1:0] = "00" or PLLCK [1:0] = "01"
7-2-2 : PLLCK [1:0] = "10" or PLLCK [1:0] = "11"
7-2-3 : XIN pin
7-2-4 : RXIN, SDIN, $\overline{PD}$, CE, CL, and DI pins

7.3 Input and Output Pin Capacitances

Table 7.3 Input and Output Pin Capacitances

Parameter	Symbol	Conditions	min	typ	max	unit
Input pins	C_{IN}	7-3-1			10	pF
Output pins	C_{OUT}	7-3-1			10	pF

7-3-1 : $AV_{DD} = DV_{DD} = V_{IN}1 = V_{IN}2 = 0$ V, Ta = 25°C, f = 1MHz

7.4 DC Characteristics

Table 7.4 DC Characteristics at Ta = -30 to 70°C, AV_{DD} = DV_{DD} = 3.0 to 3.6V, AGND = DGND = 0V

Parameter	Symbol	Conditions	min	typ	max	unit
High-level input voltage	V_{IH}	7-4-1	$0.7DV_{DD}$			V
Low-level input voltage	V_{IL}				$0.2DV_{DD}$	V
High-level input voltage	V_{IH}	7-4-2	2.0		5.8	V
Low-level input voltage	V_{IL}		–0.3		0.8	V
High-level output voltage	V_{OH}	7-4-3	DV_{DD} – 0.8			V
Low-level output voltage	V_{OL}				0.4	V
High-level output voltage	V_{OH}	7-4-4	DV_{DD} – 0.8			V
Low-level output voltage	V_{OL}				0.4	V
High-level output voltage	V_{OH}	7-4-5	DV_{DD} – 0.8			V
Low-level output voltage	V_{OL}				0.4	V
Power consumption	$I_{DD}1$	7-4-6		6.5	13	mA
Power consumption	$I_{DD}2$	7-4-7			0.1	μA
Power consumption	$I_{DD}3$	7-4-8		4.5	9	mA
Power consumption	$I_{DD}4$	7-4-9		5	10	mA

7-4-1 : CMOS level pins: XIN pin.
7-4-2 : TTL level pins: Input pins other than those listed above.
7-4-3 : I_{OH} = –8mA, I_{OL} = 6mA: CKOUT pin.
7-4-4 : I_{OH} = –2mA, I_{OL} = 2mA: BCK, LRCK, DATAO, and DO pins.
7-4-5 : I_{OH} = –1mA, I_{OL} = 1mA: Output pins other than those listed above.
7-4-6 : Operating mode: PLLSEL = "0", AMPOPR = "0", fs = 44.1kHz, C_L = 30pF
7-4-7 : Low power mode condition 1) : $\overline{PD}$ = low
7-4-8 : Low power mode condition 2) : PDOWN [1:0] = "01", XIN = 11.2896MHz, C_L = 30pF
7-4-9 : Low power mode condition 3) : PDOWN [1:0] = "10", XIN = 11.2896MHz, C_L = 30pF

7.5 AC Characteristics

Table 7.5 AC Characteristics at Ta = -30 to 70°C, AV_{DD} = DV_{DD} = 3.0 to 3.6V, AGND = DGND = 0V

Parameter	Symbol	Conditions	min	typ	max	unit
RXIN sampling frequency	$f_{FS}1$	7-5-1	30		195	kHz
RXIN sampling frequency	$f_{FS}2$	7-5-2	30		108	kHz
XIN clock frequency	$f_{XF}1$	7-5-3		11.2896		MHz
XIN clock frequency	$f_{XF}2$	7-5-4		12.2880		MHz
XIN clock frequency	$f_{XF}3$	7-5-5		16.9344		MHz
XIN clock frequency	$f_{XF}4$	7-5-6		22.5792		MHz
XIN clock frequency	$f_{XF}5$	7-5-7		24.5760		MHz
XIN clock frequency	$f_{XF}6$	7-5-8		33.8688		MHz
CKOUT clock frequency	f_{MCK}		2		100	MHz
CKOUT clock jitter	t_j			200		ps
CKOUT to BCK delay	t_{MBO}				10	ns
BCK to DATAO delay	t_{BDO}				5	ns
$\overline{\text{UGPI}}$ low-level pulse width	t_{CKT}	7-5-9			100	ms

7-5-1 : PLLCK [1:0] = "00"
7-5-2 : Settings other than PLLCK [1:0] = "00".
7-5-3 : XISEL [3:0] = "0000"
7-5-4 : XISEL [3:0] = "0001"
7-5-5 : XISEL [3:0] = "0010"
7-5-6 : XISEL [3:0] = "0100"
7-5-7 : XISEL [3:0] = "0101"
7-5-8 : XISEL [3:0] = "0110"
7-5-9 : When signal output is set during a transitional period of clock switching.

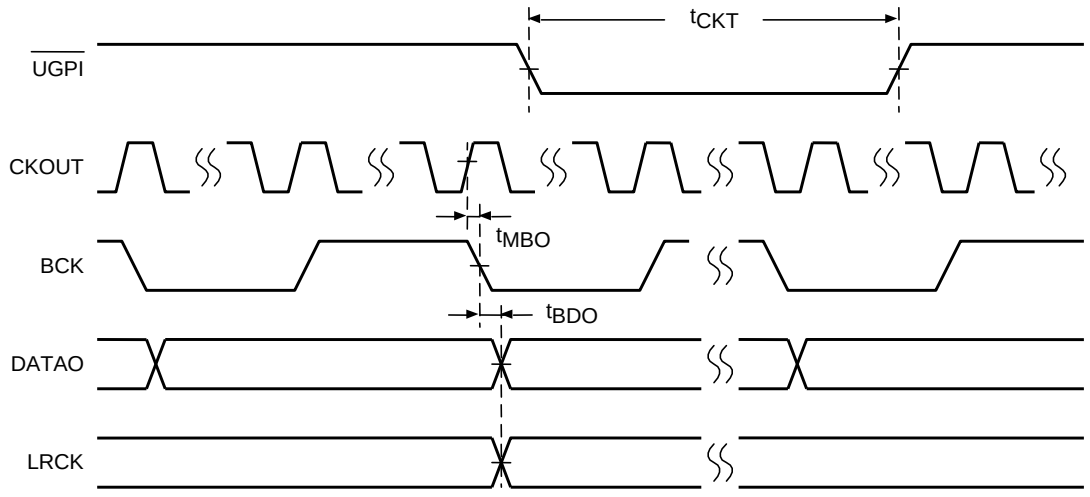


Figure 7.1 AC Characteristics

7.6 Microcontroller Interface AC Characteristics

Table 7.6 Microcontroller Interface AC Characteristics
at Ta = -30 to 70°C, AV_{DD} = DV_{DD} = 3.0 to 3.6V, AGND = DGND = 0V

Parameter	Symbol	Conditions	min	typ	max	unit
$\overline{PD}$ low-level pulse width	t_{PDdw}		200			µs
E/INT high-level pulse width	t_{INTuw}	7-6-1	5	1/fs	63	µs
CL low-level pulse width	t_{CLdw}		100			ns
CL high-level pulse width	t_{CLuw}		100			ns
CL to CE setup time	$t_{CEsetup}$		50			ns
CL to CE hold time	t_{CEhold}		50			ns
CL to DI setup time	$t_{DIsetup}$		50			ns
CL to DI hold time	t_{DIhold}		50			ns
CL to CE hold time	t_{CLhold}		50			ns
CL to DO delay time	t_{CLtoDO}				20	ns
CE to DO delay time	t_{CEtoDO}				20	ns

7-6-1 : INTOPF = "1", INTSEL = "1", and fs is the input sampling frequency.

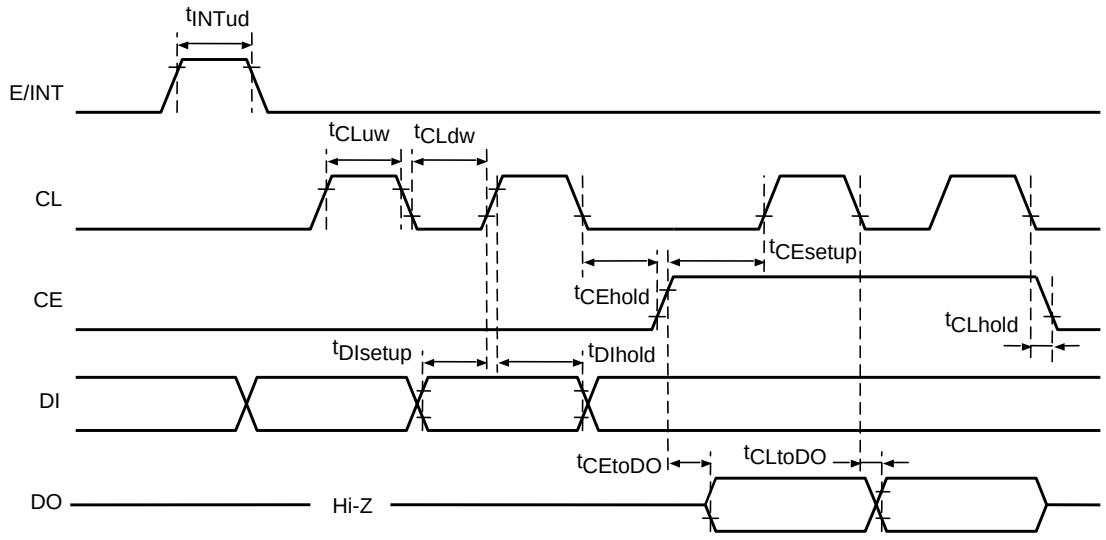


Figure 7.2 Microcontroller AC Characteristics

8. Function Description

8.1 System Reset ($\overline{PD}$)

- The system operates normally when $\overline{PD}$ pin is set to high level after a supply voltage is rises to 2.7V or higher. When you set the $\overline{PD}$ pin to low again after power is applied, the system is reset.
- When power is on, resetting must be done with the $\overline{PD}$ pin set to low.
- If a crystal oscillator is used, you must wait to start normal operation for at least 10ms until the oscillation gets stable after the $\overline{PD}$ pin goes from low to high.

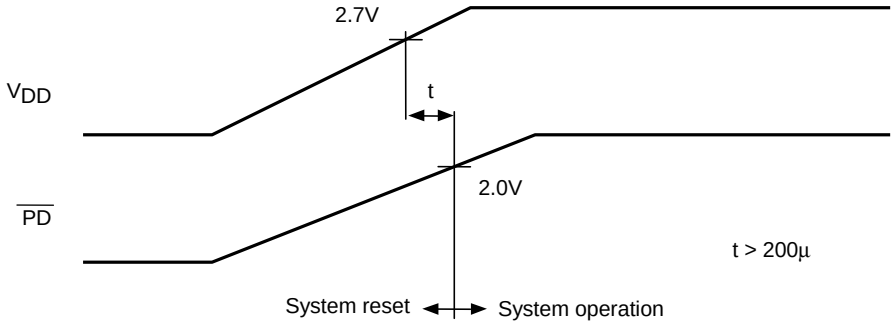


Figure 8.1 $\overline{PD}$ Pin Levels at Power On

8.2 Low-Power Modes

- The LC89052TA-E supports two low-power modes: the mode in which whole circuit is controlled with the $\overline{PD}$ pin and the mode in which only special functions are controlled by the PDOWN[1:0].
- The low-power mode controlled by the $\overline{PD}$ applies to the entire circuit of the LC89052TA-E. All clocks are stopped and the registers are initialized.
- The pins that are available with the low-power settings except for the oscillation amplifier are only the XIN pin and XOUT pin. These can be used to provide the master clock for the DSP and other circuits.
- The pins that are available with the PDOWN[1:0] low-power mode settings except those for the oscillator amplifier and its divider circuit are only the CKOUT, BCK, LRCK, DATAO, SDIN, XIN and XOUT pins. This mode can be used to minimize power consumption during analog data processing.
- When the oscillator amplifier is stopped by the AMPOPR in a low-power mode setup with PDOWN[1:0] or when this circuit is already stopped, it is impossible for the LC89052TA-E to provide a clock output. Thus the AMPOPR takes precedence. Note that the PLLOPR setting is invalid and the PLL circuit is stopped.
- When the low-power mode is set with PDOWN[1:0], it is possible to write to the microcontroller registers. However, all the sub-code Q and channel status that are read are fixed at a low level.

• The table below summaries the low-power modes.

Table8.1 Low-power Modes

Mode	$\overline{PD}$	AMPOPR	PLLOPR	PDOWN1	PDOWN0	Function
(1)	Low	×	×	×	×	Reset (stand-by)
(2)	High	0	0	0	0	Normal operation
(3)		0	1	0	0	VCO stopped.
(4)		0	×	0	1	All circuits except the oscillator amplifier stopped.
(5)		0	×	1	0	All circuits except the oscillator amplifier and divider circuit stopped.
(6)		1	0	0	0	Oscillator amplifier stopped.
(7)		1	1	×	×	All circuits stopped.

• The table below lists the output pin states in the above modes.

Table 8.2 Output Pin States in Modes (1) to (7)

Output pin	Mode (1)	Mode (2)	Mode (3)	Mode (4)	Mode (5)	Mode (6)	Mode (7)
$\overline{AUDIO}$	Low	Output	Low	Low	Low	Output	Low
$\overline{UGPI}$	High	Output	Output	Output	Output	Output	Output
CKOUT	Low	Output	Output	Output	Output	Output	Low
BCK	Low	Output	Output	Low	Output	Output	L or H
LRCK	Low	Output	Output	Low	Output	Output	L or H
DATAO	Low	Output	Output	Low	Output	Output	Low
XOUT	High	Output	Output	Output	Output	High	High
ERROR	High	Output	High	High	High	Output	High
E/INT	Low	Output	Low	Low	Low	Output	Low

1) In modes (3), (4), and (5), the clock supplied from the XIN pin is used as the source.
2) Mode (3) applies to the state where an external clock other than CKOUT is supplied to XIN. If XIN pin and CKOUT pin are connected, no clock signals are output in this mode.
3) Mode (6) applies when the PLL circuit is locked.
   When the PLL circuit is unlocked, all circuits are stopped since no clock signal is supplied from XIN pin.
4) In mode (7), the states immediatly before the setup is retained.

8.3 Clocks

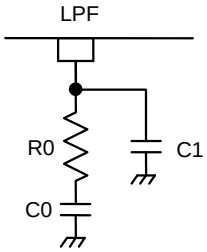
8.3.1 PLL (LPF)

- The LC89052TA-E incorporates a VCO (Voltage Controlled Oscillator) that can synchronize with sampling frequencies of 30kHz to 195kHz.
- The locking frequency is selected with PLLCK[1:0]. The VCO circuit can be stopped with PLLOPR.
- The range of input data that can be received differs depending on the settings of PLLCK[1:0].
- The (512/2)fs for the PLLCK[1:0] = "11" in the table below is the state where the PLL itself is synchronized with the 512fs clock, but the clock signal output from the CKOUT pin is 1/2 of the PLL locked frequency, which is 256fs. See the chapter on the of output clock for further information.
- We recommend the 256fs setting with PLLCK[1:0] = "00" for the systems such as portable equipment that need to restrain the consumption electric power. We also recommend the 512fs setting with PLLCK[1:0] = "10" or the (512/2)fs with PLLCK[1:0] = "11" for the systems such as AV amplifiers that require improved performance.

Table 8.3 Input Data Reception Ranges and PLL Lock Frequency Settings

PLLCK1	PLLCK0	PLL lock frequency	Input data reception range
0	0	256fs	30k to 195kHz
0	1	384fs	30k to 108kHz
1	0	512fs	30k to 108kHz
1	1	(512/2)fs	30k to 108kHz

- LPF is the PLL loop filter connection pin. Use the correct recommended resistance and capacitance as values listed in the table below according to the PLLCK[1:0] settings.



PLLCK1	PLLCK0	R0	C0	C1
0	0	150Ω	0.047µF	0.0068µF
0	1			
1	0	150Ω	0.068µF	0.0047µF
1	1			

Figure 8.2 PLL Loop Filter Configuration

8.3.2 Oscillator amplifier (XIN and XOUT)

- The following methods can be used to supply the clock signal to the internal oscillator amplifier.

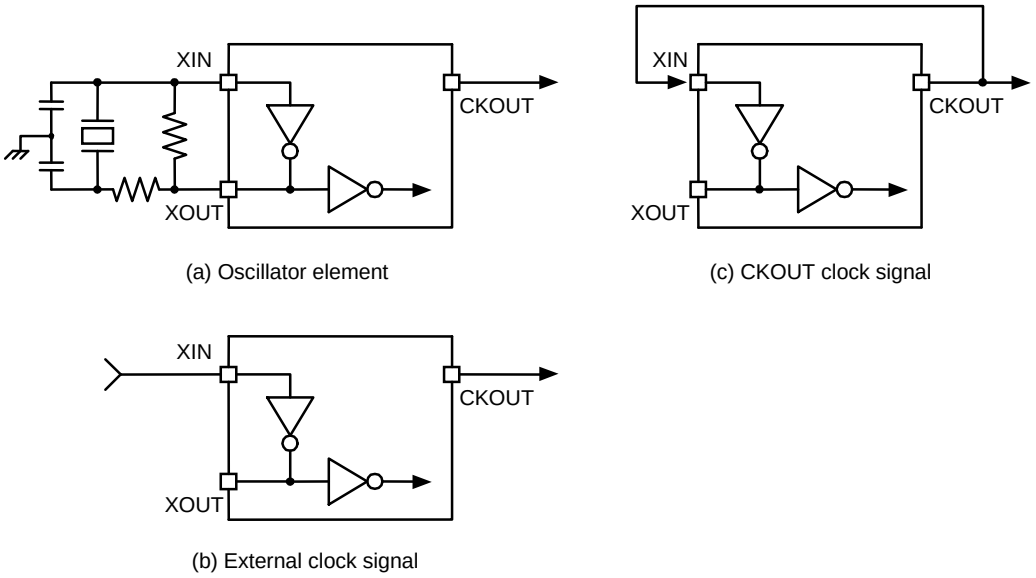


Figure 8.3 XIN and XOUT Pin Circuit Configurations

- When you connect an oscillator, use the one with the fundamental frequency. Since the load capacitance depends on the oscillator characteristics, give careful consideration.
- Since the clock supplied to the XIN pin is normally used for the following purposes, the clock signal should be present all the time.
  —Externally supplied clock used when the PLL circuit is unlocked and when XIN is the clock source
  —For calculation of sampling frequencies of the input data
- Input a clock with a frequency of 11.2896M, 12.288M, 16.9344M, 22.5792M, 24.576M, or 33.8688MHz according to the setting of the XISEL[2:0]. Input digital data only after the XISEL[2:0] has been set to match the set frequency and the oscillator or external clock input frequency. The LC89052TA-E may malfunction if data is input when the input frequency and the set frequency are not consistent.
- The LC89052TA-E operates even when the frequency set with the XISEL[2:0] and the frequency supplied to the XIN pin are different. However, continuity at clock switching time and correct input fs calculation are not guaranteed.
- The LC89052TA-E supports a structure in which CKOUT pin is connected to the XIN pin to set XISEL3, requiring no oscillator. However, since only VCO can be used as the source clock, the VCO free-running frequency (10M to 16MHz) is output from the CKOUT pin when the PLL is not locked. Furthermore, input fs calculation and limitation are impossible with this approach. Also, since no clock is supplied to the oscillator amplifier circuit when the VCO is set to stop, the whole system stops. This function is available only for the PLLCK[1:0] = "00" setting, which is 256fs. Other system clock settings might cause malfunction.
- Normally the oscillator amplifier stops automatically when the PLL is locked. It is possible to change to a continuous operation mode with AMPCNT. Setting the LC89052TA-E to the continuous operation mode makes it possible to calculate the input sampling frequency even when the PLL is locked. However, since both the oscillator amplifier clock and the PLL clock signals coexist in that case the user must pay attention and make sure audio quality is not adversely affected.
- The oscillator amplifier can be stopped when not required by setting the AMPOPR. However, the application must maintain its state for at least 10ms until the oscillator stabilizes, when returning from stop to operation mode. After that the LC89052TA-E must be returned to the normal operation mode.

8.3.3 Output clocks (CKOUT, BCK, LRCK)

- The clock source for the clocks output from CKOUT, BCK, and LRCK can be selected from two master clocks, the PLL circuit and the XIN pin.
- Normally, when the PLL circuit is locked, the master clock is switched to the PLL source, and when the PLL circuit is unlocked, the master clock automatically switches to the XIN source. To switch the clock source forcibly, set with OCKSEL. Clock continuity is maintained when the clock source is selected by the locked/unlocked state of the PLL circuit or OCKSEL.
- Clock switching depends on the PLL circuit locked/unlocked state at the time of the register setup. If the PLL source is selected with OCKSEL when the PLL circuit is unlocked, the clock is automatically switched after the PLL circuit is locked.
- When VCO operation is stopped with PLLOPR, XIN becomes the clock source. However, clock continuity cannot be maintained if the operation is stopped with PLLOPR while the PLL circuit is locked. When a low-power mode is set, continuity cannot be maintained if the mode is switched from the locked PLL.

Table 8.4 Register Settings, PLL States, and the Clock Source

OCKSEL	0		1	
PLL state	Locked	Unlocked	Locked	Unlocked
Clock source	PLL	XIN	XIN	XIN

- Either the PLL clock or the XIN clock is output from the CKOUT pin. The divided clock of CKOUT is output from the BCK pin and LRCK pin.
- The PLL lock time frequency is set with PLLCK[1:0]. However, it is possible to maintain clock continuity without losing the PLL locked state when switching, in the PLL locked state, from the 512fs setting mode with PLLCK[1:0] = "10" to the (512/2)fs setting with the PLLCK[1:0] = "11", as well as when switching in the reverse direction.
- If you use the following procedure to switch between 512fs and (512/2)fs, the BCK and LRCK output clock continuity can be maintained, and the CKOUT output clock frequency can be held within a narrow band. Other PLLCK[1:0] switching would result in a lock error.

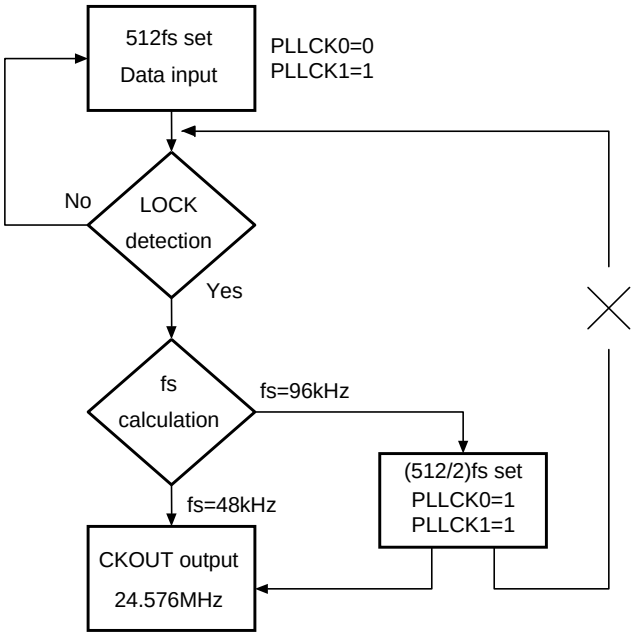


Figure 8.4 Flowchart for CKOUT Output Clock Narrow Band Operation

- The tables below show the output clocks generated in the XIN and PLL clock source modes.

Table 8.5 XIN Output Clocks in Clock Source Mode (XISEL2 = "0", PLL unlocked state or forced setting)

PLLCK1	PLLCK0	XISEL1	XISEL0	CKOUT pin	BCK pin	LRCK pin
0	0	0	0	11.2896MHz	2.8224MHz	44.1kHz
0	0	0	1	12.2880MHz	3.0720MHz	48kHz
0	0	1	0	16.9344MHz	4.2336MHz	66.15kHz
0	1	0	0	11.2896MHz	1.8816MHz	29.4kHz
0	1	0	1	12.2880MHz	2.0480MHz	32kHz
0	1	1	0	16.9344MHz	2.8224MHz	44.1kHz
1	0	0	0	11.2896MHz	2.8224MHz	44.1kHz
1	0	0	1	12.2880MHz	3.0720MHz	48kHz
1	0	1	0	16.9344MHz	4.2336MHz	66.15kHz
1	1	0	0	11.2896MHz	2.8224MHz	44.1kHz
1	1	0	1	12.2880MHz	3.0720MHz	48kHz
1	1	1	0	16.9344MHz	4.2336MHz	66.15kHz

Table 8.6 XIN Output Clocks in Clock Source Mode (XISEL2 = "1", PLL unlocked state or forced setting)

PLLCK1	PLLCK0	XISEL1	XISEL0	CKOUT pin	BCK pin	LRCK pin
0	0	0	0	22.5792MHz	5.6448MHz	88.2kHz
0	0	0	1	24.5760MHz	6.1440MHz	96kHz
0	0	1	0	33.8688MHz	8.4672MHz	132.3kHz
0	1	0	0	22.5792MHz	3.7632MHz	58.8kHz
0	1	0	1	24.5760MHz	4.0960MHz	64kHz
0	1	1	0	33.8688MHz	5.6448MHz	88.2kHz
1	0	0	0	22.5792MHz	5.6448MHz	88.2kHz
1	0	0	1	24.5760MHz	6.1440MHz	96kHz
1	0	1	0	33.8688MHz	8.4672MHz	132.3kHz
1	1	0	0	22.5792MHz	5.6448MHz	88.2kHz
1	1	0	1	24.5760MHz	6.1440MHz	96kHz
1	1	1	0	33.8688MHz	8.4672MHz	132.3kHz

Table 8.7 PLL Output Clocks in Clock Source Mode (PLL locked state)

PLLCK1	PLLCK0	CKOUT pin	BCK pin	LRCK pin
0	0	256fs	64fs	fs
0	1	384fs	64fs	fs
1	0	512fs	64fs	fs
1	1	256fs	64fs	fs

- The CKOUT output clock frequency can be set to 1/2 of its normal value with MCKHFO, regardless of the PLL locked/unlocked state. Clock switching with this setting can be done without unlocking the PLL but clock continuity is not maintained.
- If the audio output format is set to bi-phase data output, the BCK output clock frequency is doubled to 128fs when the PLL circuit is locked. However, when unlocked, a BCK signal shown in the above tables is output. Note that the clock continuity is not maintained when this output format is set.

8.3.4 Clock system diagram

- This section shows the relationship between the two types of master clock and clock switching and dividing functions.
- The items in square brackets near the switch and function blocks are the names of write commands.
- Lock/Unlock is switched automatically according to the PLL lock/unlock state.

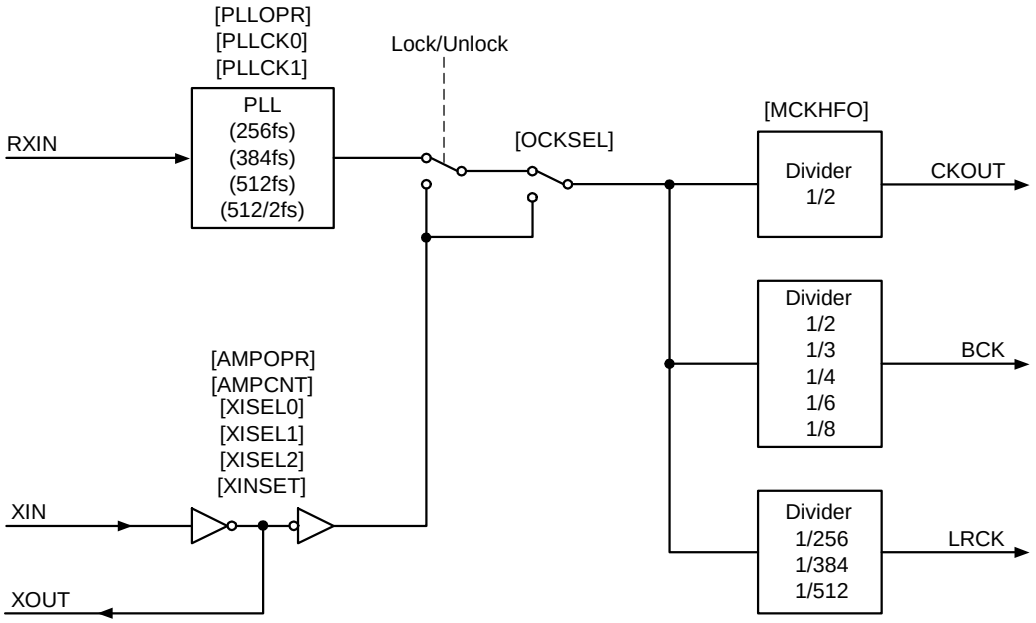


Figure 8.5 Master Clock System Diagram

8.3.5 Point to notice when switching the clock source

- If an attempt is made to switch the clock source from PLL lock state (oscillator amplifier stopped) to XIN using OCKSEL when a mode in which the results of input fs calculation are reflected in the error flags is specified through FLIMIT, an error signal (H) is temporarily placed at the ERROR pin though the continuity of the clock is preserved. The reason for this follows. When the clock switching is carried out, the oscillator amplifier is activated and the input fs calculation is restarted. At the same time, the old results of fs calculation are reset and consequently, a change in the fs value is recognized when the old fs value is compared with the newly calculated fs value.
- To switch the clock source using OCKSEL while maintaining the state of the ERROR pin when the PLL is locked in this mode setting, it is necessary to put the oscillator amplifier into the continuous mode using AMPCNT.
- Note that when the clock source is switched to XIN from the state where the oscillator amplifier is stopped with the PLL circuit locked, output clocks whose source is XIN start outputting after the oscillator amplifier has started operation. While the PLL is locked, clock source switching from XIN to PLL is carried out immediately. In both cases, clock continuity is maintained.
- When the CKOUT clock is supplied to XIN without using an oscillator or an external clock, the VCO free-running frequency output from the CKOUT pin with the PLL unlocked is somewhere between 10M and 16MHz. Clock signals created by dividing CKOUT are output from BCK and LRCK pins. However, these clock frequencies vary depending on the LC89052TA-E sample and fluctuate depending on supply voltage and operating environments. Therefore, the frequency is not fixed. You need to take care when using the CKOUT, BCK, and LRCK clocks while the PLL circuit is unlocked.

8.4 Data Input and Output

8.4.1 Bi-phase mark modulated digital data input (RXIN)

- RXIN is an input pin for bi-phase mark modulated digital data.
- The RXIN pin supports TTL levels. This allows a 5V-optical reception module to be connected directly.

8.4.2 Setting the bi-phase mark modulated input data reception range

- The LC89052TA-E allows the user to set the upper limit sampling frequency of the receivable input data and can receive input data of specific sampling frequencies.
- These are set with FLIMIT and FSSEL[3:0].
- However, this function does not work in modes where the reception range is not limited with the FLIMIT.

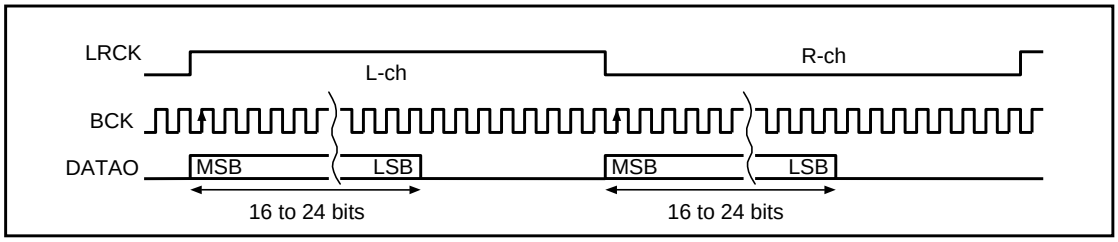
Table 8.8 Input Data Reception Range (FS4XIN = "0")

FSSEL3	FSSEL2	FSSEL1	FSSEL0	Input data reception range
0	0	0	0	32kHz to 96kHz
0	0	0	1	32kHz only
0	0	1	0	44.1kHz only
0	0	1	1	48kHz only
0	1	0	0	88.2kHz only
0	1	0	1	96kHz only
0	1	1	0	44.1kHz or 88.2kHz only
0	1	1	1	48kHz or 96kHz only
1	0	0	0	32kHz or 44.1kHz or 48kHz
1 …. 1	0 ….. 1	0 ….. 1	1 ….. 1	Reserved

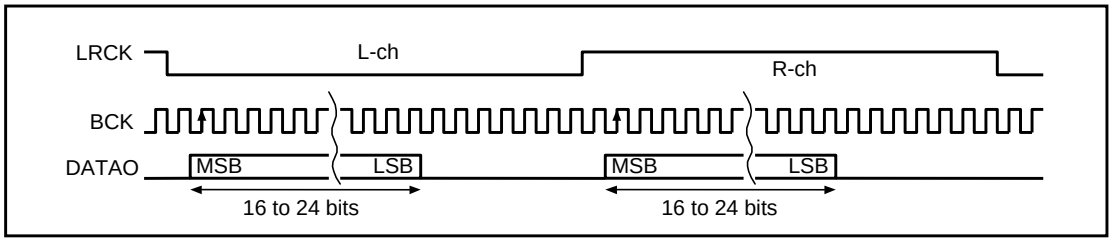
- The notation 32kHz to 96kHz means 32k, 44.1k, 48k, 64k, 88.2k, or 96kHz.
- The table above only applies when the input fs calculation mode (FS4XIN) is set to "0". When FS4XIN is set to "1", input data reception range is doubled.
- Input data out of the set range is treated as an error, in which case the XIN source clock is output. At this time, the DATAO output data is subject to the RDTSEL setting.
- When the PLL follows a source with a variable fs, such as a CD player with variable pitch control, from the state where the oscillator amplifier is stopped while PLL is locked, the fs is not calculated. As a result, an input frequency not within the set range is not regarded as an error. The oscillator amplifier must be set to a continuous operation mode to support such sources.
- The reception range of input data can not be limited when setting up a system where no oscillator is required as XIN and CKOUT are connected, because fs calculation is impossible in that case.

8.4.3 Output data formats: normal mode (DATAO)

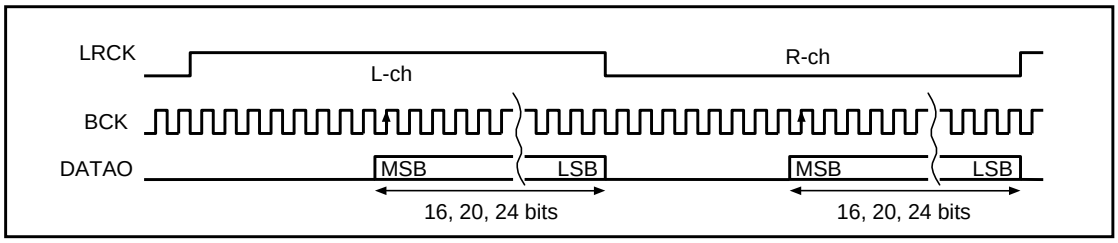
- The output format of after-demodulation audio data must be set with OFSEL[2:0].
- In the format shown below, the input data only within the audio data range is output.
- BCK, LRCK, and DATAO are output in synchronization with the rising edge of CKOUT. DATAO is output in synchronization with the falling edge of BCK.
- Generation of output data starts at the LRCK edge immediately after the ERROR output turns low.
- The low level is output all the time except for the effective bit length of output data.



(0) : MSB first left-justified data output (OFSEL[2 : 0]=000)



(1) : I^2S data output (OFSEL[2 : 0]=001)

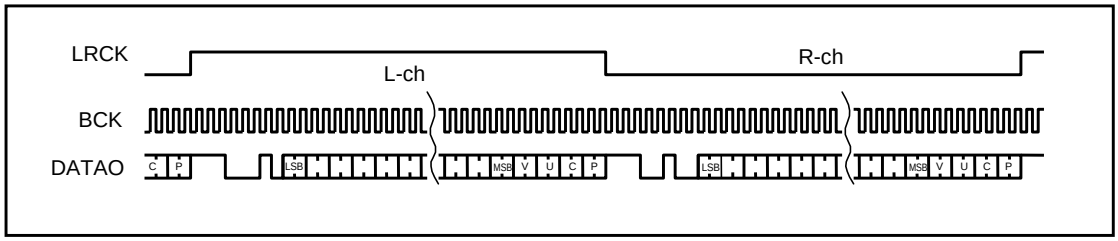


(2) : MSB first right-justified data output (OFSEL[2 : 0]=010, 011 or 100)

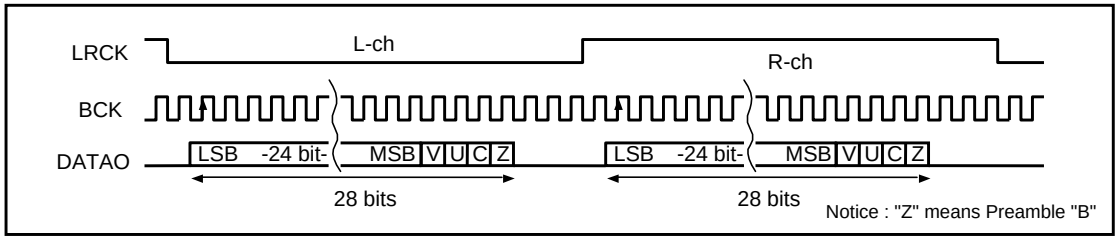
Figure 8.6 Data Output Timing (Normal Mode)

8.4.4 Output data formats: special mode (DATAO)

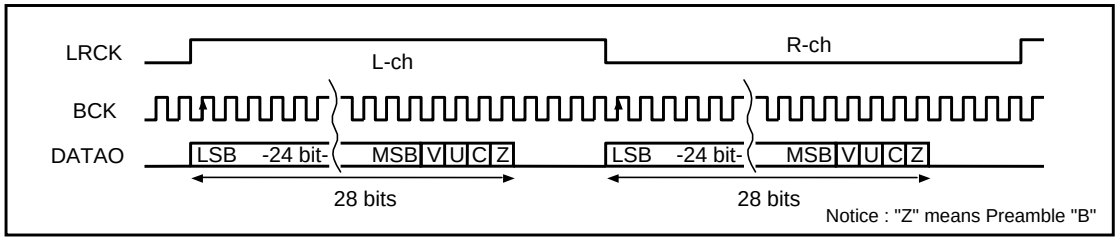
- The output format of after-demodulation audio data must be set with OFSEL[2:0].
- In the format shown below, input data information except the audio data is output as well.
- BCK, LRCK, and DATAO are output in synchronization with the rising edge of CKOUT. DATAO is output in synchronization with the falling edge of BCK.
- Generation of output data starts at the LRCK edge immediately after the ERROR output turns low.
- (3) as bi-phase data output, the input bi-phase data is output in synchronization with 128fs clock BCK and fs clock LRCK. However, BCK in PLL unlocked state is set to the 64fs clock.
- As for NRZ data output in (4), (5), 28bits are output. 4 bits of validity (V), user data (U), channel status (C) and also preamble B (Z) plus 24 bits of LSB first audio data. H is output as Z bit in the frames (L-ch and R-ch) whose preamble B is confirmed.
- The low level is output all the time except for the effective bit length of the NRZ data output.



(3) : Biphase data output (OFSEL[2 : 0]=101)



(4) : NRZ data I^{2}S output (OFSEL[2 : 0]=110)

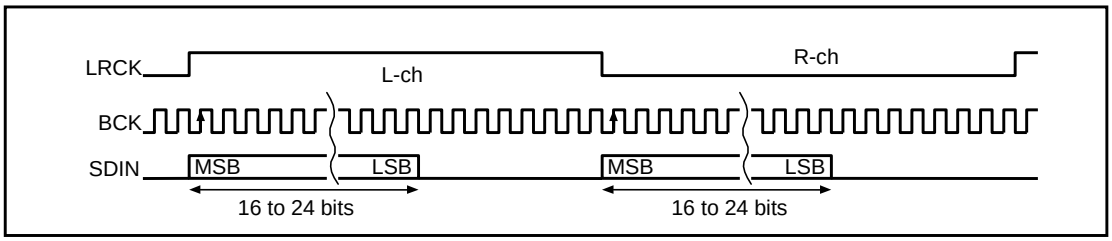


(5) : NRZ data LSB first left-justified output (OFSEL[2 : 0]=111)

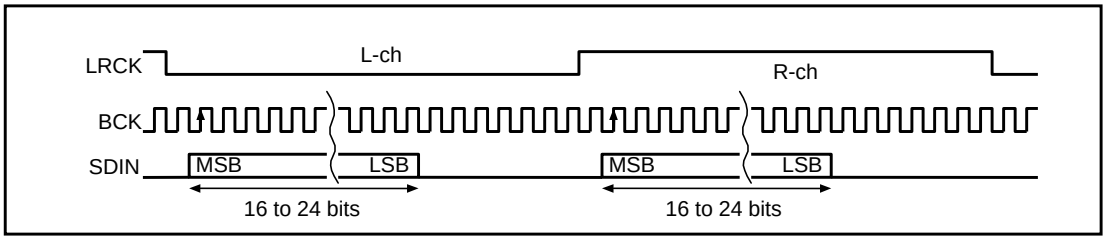
Figure 8.7 Data Output Timing (Special Mode)

8.4.5 Serial audio data input format (SDIN)

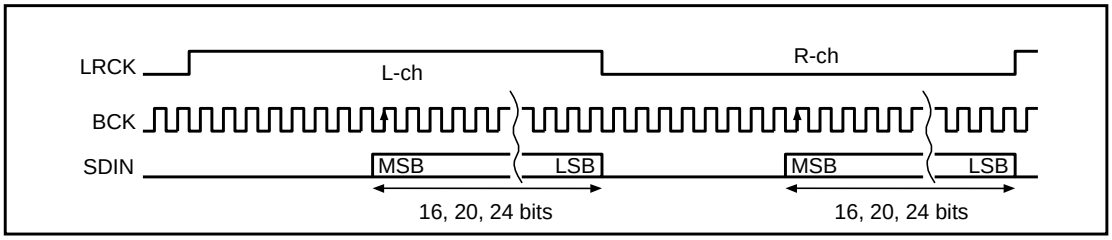
- SDIN is the pin that inputs serial digital audio data such as A/D converter output.
- Data input to the SDIN can be output from the DATAO pin. The data to be input to SDIN must synchronize with BCK and LRCK.
- Given below shows an example of a serial audio data input timing.
- Except for a special setting, we suggest the SDIN input format be consistent with the format of output data after demodulation.



(0) : MSB first left-justified data input



(1) : I^2S data input



(2) : MSB first right-justified data input

Figure 8.8 Example of Serial Audio Data Input Timing

8.4.6 Output data switching (SDIN, DATAO)

- The DATAO pin outputs the demodulated data when the PLL circuit is locked and the SDIN input data when the PLL circuit is unlocked. This switching is performed automatically according to the locked/unlocked state of the PLL circuit.
- The data input to SDIN must be synchronized with CKOUT, BCK, and LRCK clocks when XIN is the clock source.
- The SDIN input data is output to DATAO by setting RDTSTA, regardless of the PLL circuit locked/unlocked state. In this case, the CKOUT, BCK, and LRCK clocks are also switched to the XIN clock source. The switch occurs in synchronization with the LRCK edge after RDTSTA setup.
- The DATAO output data can also be forcibly muted by setting RDTMUT. The muting processing is output in synchronization with the LRCK edge after RDTMUT setup.
- The DATAO output can also be muted in the PLL unlocked state by RDTSEL setup.
- These setups take priority in the following order: RDTSEL < RDTSTA < RDTMUT.
- When XIN is set to be the clock source with OCKSEL, the PLL circuit operates as long as PLL operation is not stopped with PDOWN[1:0] or PLLOPR. In this mode the state of the PLL circuit is always output from the ERROR pin. Information processed regardless of the PLL state can be read out over the microcontroller interface.

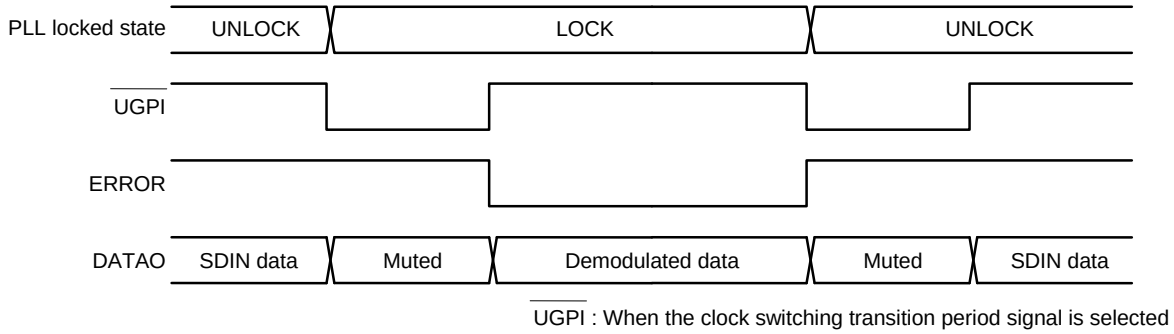


Figure 8.9 Timing Chart for DATAO Output Data Switching (When RDTSEL is set to "0")

8.4.7 Calculation of input data sampling frequency

- The input data sampling frequency is calculated using the XIN clock.
- Normally, in modes where the oscillator amplifier is automatically stopped when the PLL circuit is locked, the calculation is done during the error period associated with ERROR and completed, and the value is retained when the oscillator amplifier is stopped. Therefore, after the calculation is confirmed, the value does not change until the PLL circuit is unlocked.
- In continuous operation mode, the oscillator amplifier continuously repeats calculations.
- The calculation result can be read out from CCB address 0xEC or output registers DO4 to DO6. However, note that while the PLL can synchronize with data of 32k to 192kHz, fs calculation mode can be selected from two modes: 32k to 96kHz calculation mode and 64k to 192kHz calculation mode. These modes are switched by FS4XIN. It is not possible to monitor the fs calculation result of 32k to 192kHz in the same mode.
- If a system where the XIN and CKOUT pins are connected and no oscillator is required is being setup, the fs calculation result will always be "out of range".

8.5 Error Output Processing (ERROR)

8.5.1 Lock error and data error output

- The ERROR pin outputs high level when a PLL lock error happens or an error occurs in the transmitted data.

8.5.2 PLL lock error

- The PLL circuit will unlock the input data which does not conform to the bi-phase modulation rules or can not detect the preamble B, M, or W.
- ERROR turns to H when a PLL lock error occurs. When data modulation returns to the normal state, it remains high for 15m to 50ms, before going to the to low level.
- The output of ERROR is synchronized with LRCK.

8.5.3 Input data transmission error

- An odd number of input parity errors are detected from the parity bits in the input data.
- When input parity errors occur 9 times or more in a row, ERROR turns to high level. After the high level is held for 15m to 50ms following the detection of the PLL lock state, the ERROR returns to low level.
- When 8 or fewer input parity errors occur consecutively, an error is output only for intervals between sub-frames where the errors occurred when non-PCM data is recognized by data delimiter bit 1 in the channel status. In this case, the parity error flag is not output when PCM data is recognized.

8.5.4 Other errors

- Even when ERROR has turned to low, the LC89052TA-E always acquires bits 24 to 27 (sampling frequency) of the channel status and compares the current data with the data of the previous block. If any differences are found, ERROR is immediately set to high and processes similar to those for the PLL lock error are carried out.
- Similarly, even when the mode that reflects fs calculation results in an error flag is set with FLIMIT, the fs calculation results are always compared. Here as well, if a disparity occurs in the data, ERROR is immediately turned to high, and the processing similar to that for the PLL lock error is carried out.

8.5.5 Data processing upon occurrence of errors

- This section describes the data processing performed when an error occurs. When up to 8 consecutive input parity errors occur, if the transmitted data is PCM audio data, the data is replaced with the corresponding left and right channel data from the immediately preceding frame. However, if the transmitted data is non-PCM data, the error data is output as it is. Non-PCM data is based on the data that is detected before the input parity error has occurred, and is the data for which the channel status bit 1 non-PCM data detection bit is "1". Non-PCM data refers to the data established when bit 1 non-PCM data detection bit of the channel status turns to high based on the data detected prior to the occurrence of the input parity error.
- The output data when a PLL lock error or 9 or more parity errors occur consecutively are muted.
- For the channel status data, the data for the previous block held in 1 bit units is output when an 8 or less parity error occurs successively.

Table 8.9 Data Processing when Errors Occur

Data and detection flags	PLL lock error	Input parity error (a)	Input parity error (b)	Input parity error (c)
DATAO output pin	Low	Low	Previous data	Output
Input fs calculation	Low	Low	Output	Output
Channel status data	Low	Low	Previous data	Previous data
Sub-code Q data	Low	Low	Output	—

1) Input parity error (a): When 9 or more consecutive parity errors occur
2) Input parity error (b): When up to 8 consecutive parity errors occur in audio data
3) Input parity error (c): When up to 8 consecutive parity errors occur in non-PCM burst data

- The figure below presents an example of the data processing performed when a parity error occurs.

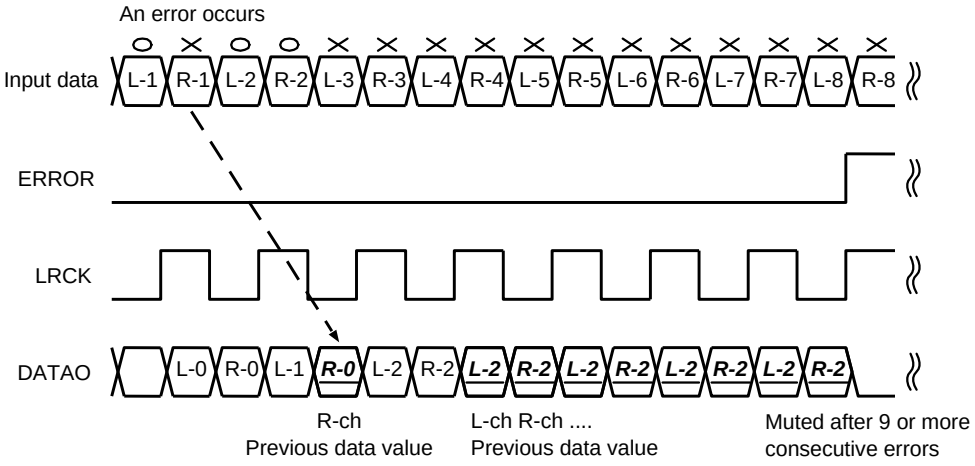


Figure 8.10 Data Processing Example for a Parity Error (When PCM data is received)

8.5.6 Processing during error recovery

- When the preambles B, M, and W are detected, the PLL circuit goes to the locked state and data demodulation starts.
- The DATAO output data is output on the first LRCK edge after ERROR goes low.

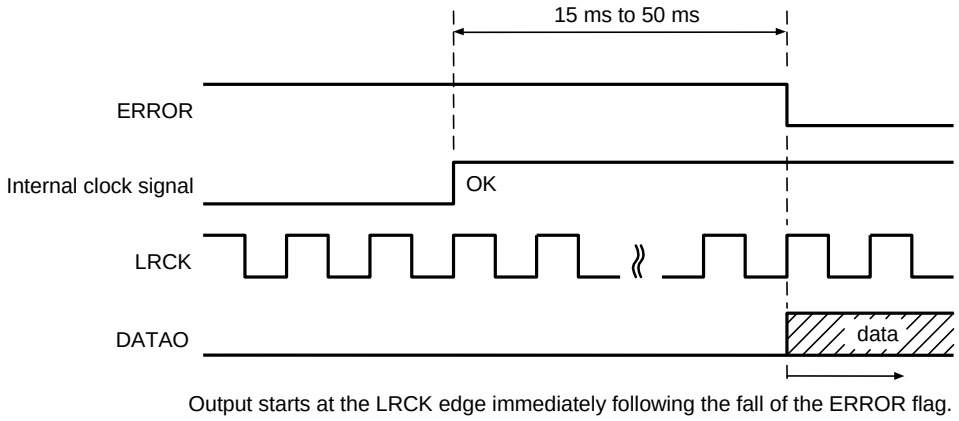


Figure 8.11 Data Processing when Data Demodulation Starts

8.6 Channel Status Data Output

8.6.1 Data delimiter bit 1 output ($\overline{\text{AUDIO}}$)

- $\overline{\text{AUDIO}}$ outputs channel status bit 1, which indicates whether or not the input bi-phase data is PCM audio data.

Table 8.10 $\overline{\text{AUDIO}}$ Output

$\overline{\text{AUDIO}}$ pin	Output conditions
Low	PCM audio data (CS bit 1 = low)
High	Non-PCM data (CS bit 1 = high)

8.6.2 Emphasis information output (E/INT)

- E/INT is shared by the microcontroller interface interrupt function. However, in the initial state, it outputs the presence or absence of emphasis with a time constant of 50/15μs for use in consumer products or broadcast studios.

Table 8.11 E/INT Output

E/INT pin	Output conditions
Low	No pre-emphasis
High	50/15μs pre-emphasis

8.7 User General Definable Output Port ($\overline{\text{UGPI}}$)

- $\overline{\text{UGPI}}$ pin is a user-definable output port that can be selected for the following functions.
  —Microcontroller interface register output
  —Signal output during clock switching transitional period
- Selection is done by GPISEL. The initial setting is set to the microcontroller interface register GPIDAT. However, the initial setting of this GPIDAT register is "1", so high level is output from the $\overline{\text{UGPI}}$ pin.

8.7.1 Microcontroller interface register output (Example of signals that control low power of optical module)

- This section describes an example in which $\overline{\text{UGPI}}$ is used as a power supply control signal for an optical module as a microcontroller interface register output.
  (a) Connect the $\overline{\text{UGPI}}$ output to the power supply control switch of the optical module.
  (b) After a reset due to $\overline{\text{PD}}$, microcontroller interface register output is selected as the initial state of $\overline{\text{UGPI}}$. As a result, the default GPIDAT value is output.
  (c) After a reset, the initial value of GPIDAT is set to "1", so H is output from $\overline{\text{UGPI}}$. Therefore, after a reset, the control switch is turned off, and data is not supplied from the optical module.
  (d) The application must set GPIDAT to "0" to have the optical module supply data. That is, the $\overline{\text{UGPI}}$ output can be controlled with GPIDAT, and the current drain can be minimized when the optical module is not used.

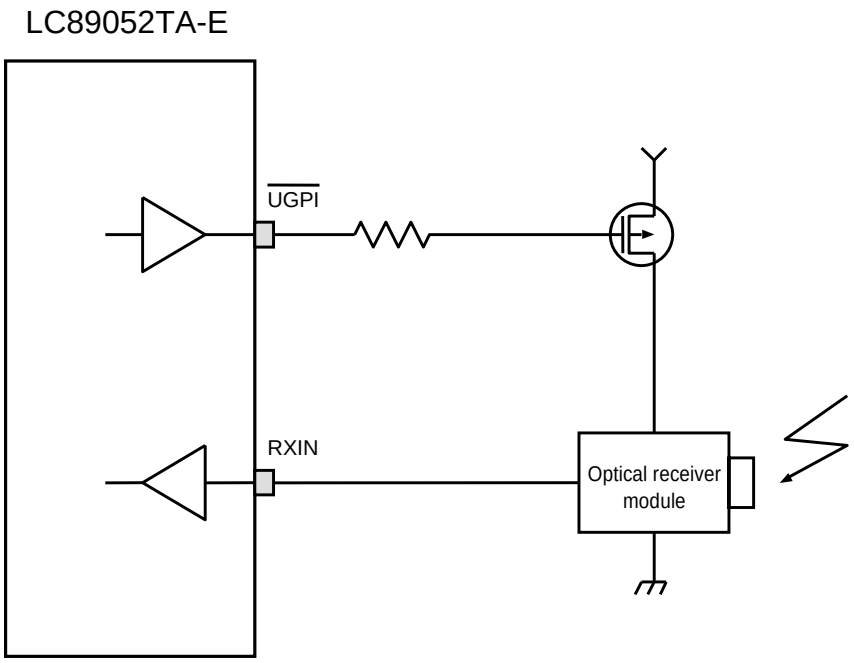


Figure 8.12 $\overline{\text{UGPI}}$ Output Example (Power supply control signal for an optical module)

8.7.2 Microcontroller interface register output (Example of signals that control switching of Digital data input)

- $\overline{\text{UGPI}}$, when used as a microcontroller interface register output, can be used as a control signal that switches the digital data input.
- When increasing the number of digital data input systems, an peripheral circuit such as an input selector and a control signal for that selector is required. The number of digital data input ports can be increased to two systems without having to provide a control signal from the microcontroller by using the $\overline{\text{UGPI}}$ output.
- Note that after a reset, the initial value of GPIDAT is set to "1", so high level is output from $\overline{\text{UGPI}}$. Be aware that the initial value of the switching signal is high level.

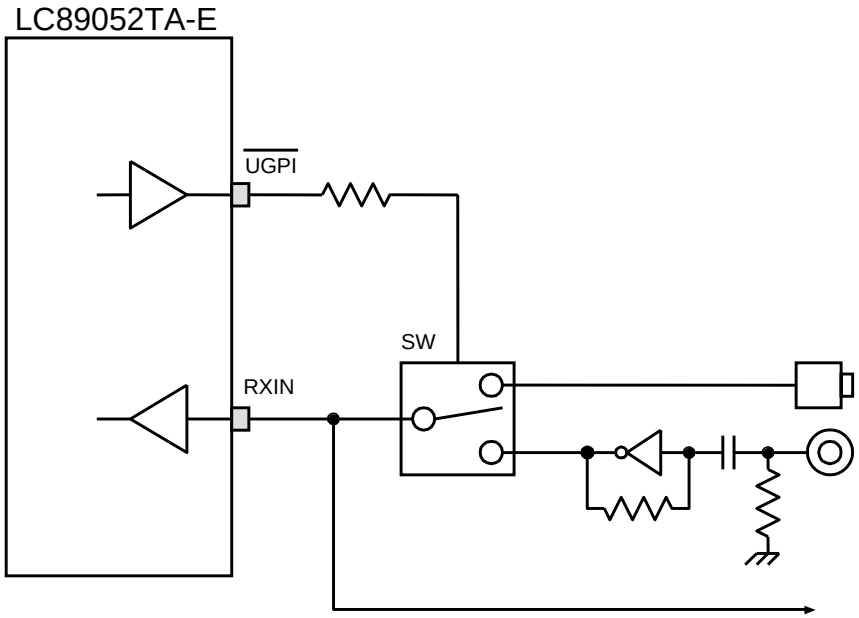
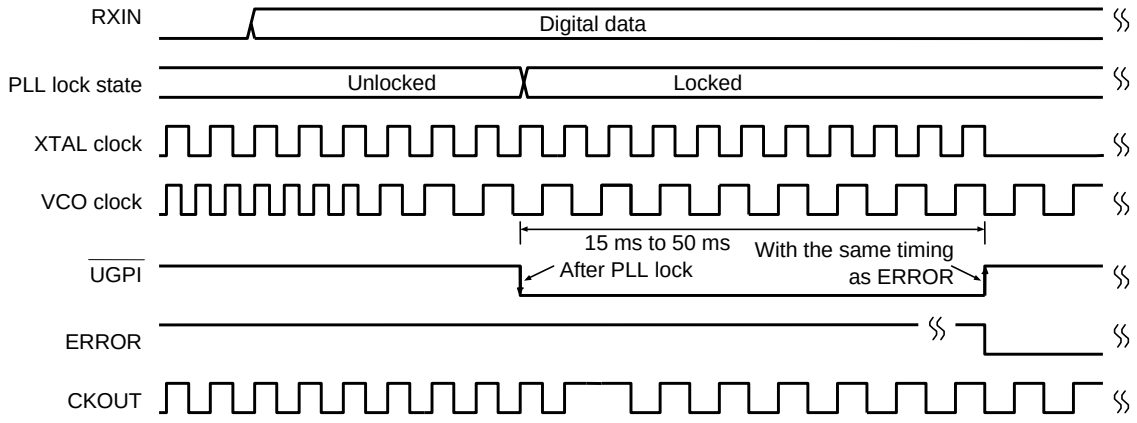


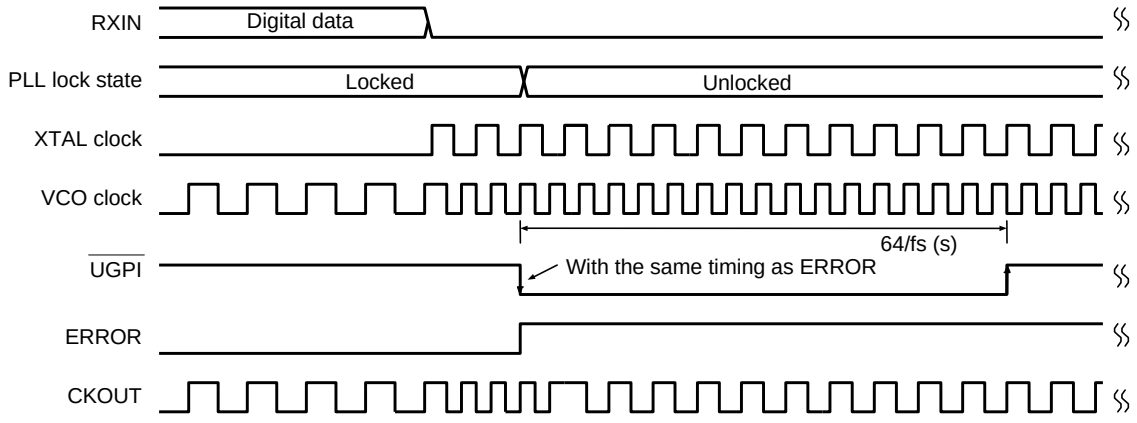
Figure 8.13 $\overline{\text{UGPI}}$ Output Example (Signal that controls the switching of data input)

8.7.3 Output of clock switch transition signal

- This section describes the operation when $\overline{\text{UGPI}}$ is selected as an output pin during the clock switching transitional period.
- A clock switching transitional period signal is a signal that reports a clock switching condition to external circuits due to a change in the PLL locked/unlocked state. This signal allows the application to grasp the PLL lock state transitions and the timing of change in the clock signals. This setup is selected with GPISEL.
- After setting GPISEL, high level is output from $\overline{\text{UGPI}}$. Low pulse is output when the output clock changes due to the change in the PLL circuit locked/unlocked state.
- In the lock in process, the $\overline{\text{UGPI}}$ low pulse rises with the word clock generated by the XIN clock after input data is detected and PLL is locked. After a certain period, it rises with the same timing as ERROR.
- In the unlock process, the $\overline{\text{UGPI}}$ low pulse falls at the same timing as ERROR, which is the PLL lock detecting signal and it rises after the word clocks generated from the XIN clock are counted for a certain period.



(a) : During the lock-in process



(b) : During the unlock process

Figure 8.14 Clock Switching Timing

9 Microcontroller Interface (E/INT, CE, CL, DI, DO)

9.1 Interrupt Output (E/INT)

- The E/INT pin can be set to function as the microcontroller interface interrupt output by setting INTSEL.
- An interrupt output is issued when a change occurs in the PLL lock state or output data information.
- The interrupt output consists of registers for selecting interrupts, the E/INT pin, which outputs those state transitions, and registers that store interrupt related data.
- The E/INT pin normally is at the low level, and goes to the high level when an interrupt occurs. After going to high level, it returns to low level according to the INTOPF setting.
- INTOPF determines whether the E/INT pin holds the high pulse for a certain period and is then cleared (returning to low), or the E/INT pin is cleared at the same time as the output register is read.
- The interrupts can be selected from the sources listed below. More than one items can be set as interrupt sources at the same time by setting the contents of CCB address 0xEA. The interrupt signal is issued whenever any one of the interrupt sources arises.

E/INT output = (selected interrupt 1) + (selected interrupt 2) + ... + (selected interrupt n)

Table 9.1 Interrupt Source Settings

No.	Command	Description
1	INTERR	Output when the state of the ERROR pin changes.
2	INTPCM	Output when the state of the $\overline{\text{AUDIO}}$ pin changes.
3	INTEMP	Output when the state of the pre-emphasis information changes.
4	INTVFL	Output when the state of the validity flag changes.
5	INTFSC	Output when the input fs calculation result changes.
6	INTCSF	Output when the first 48 bits of the channel status data are updated.
7	INTSQY	Output when the sub-code Q data can be read out.

- The contents of the set interrupt source are stored in output registers DO1 to DO7 at CCB address 0xEB when an interrupt source arises. However, the registers read for source items 1 through 4 output the current state of those sources regardless of the E/INT output. For source items 5 through 7, the states are stored when an interrupt source arises.
- To monitor interrupt source item 5 in the PLL locked state, the oscillator amplifier must be set to continuous operation mode, since the oscillator amplifier clock is used.
- When the LC89052TA-E is set to the mode in which a H pulse is output from E/INT when an interrupt source occurs, the pulse width of each interrupt source is somewhere between 1/2 fs and 3/2 fs.
- The action to clear the E/INT pin output simultaneously with the reading of the output registers following the occurrence of an interrupt is carried out immediately after the output registers at 0xEB are set up. Since, however, the data associated with interrupt sources 6 and 7 is updated at the intervals listed below, it must be read promptly whenever the corresponding interrupt sources are detected.

Table 9.2 Data Update Intervals (Input fs = 32k to 96kHz)

Data	Update interval
Channel status and preamble B	2ms to 6ms
Sub-code Q data	13.3ms (fs = 44.1kHz), 6.65ms (2x speed)

9.2 CCB Addresses

- Setting various functions, and reading and writing data must be carried out though the microcontroller interface.
- The data through the microcontroller interface conforms to the Our original serial bus format (CCB). However, the three-state is employed instead of open-drain as the data output type.
- Data must be input or output after the CCB address is input. See the I/O timing chart for details of the data input and output timing.

Table 9.3 Register I/O Content and CCB Addresses

Register content	R/W	CCB address	B0	B1	B2	B3	A0	A1	A2	A3
Function settings data 1	Write	0xE8	0	0	0	1	0	1	1	1
Function settings data 2	Write	0xE9	1	0	0	1	0	1	1	1
Function settings data 3	Write	0xEA	0	1	0	1	0	1	1	1
Interrupt data output	Read	0xEB	1	1	0	1	0	1	1	1
Fs value, CS data output	Read	0xEC	0	0	1	1	0	1	1	1
Sub-code Q data output	Read	0xED	1	0	1	1	0	1	1	1

9.3 Data Write Procedure

- The bit length of data input is 16 bits.
- After inputting one of the CCB addresses data 0xE8 to 0xEA, set CE to the high level.
- Input data is taken in on the rising edge of CL.
- The bits marked "0" in the table are reserved bits. 0 (zero) must be input to these bits.

9.4 Data Read Procedure

- Read data is output from DO. DO goes to the high-impedance state when CE is low, and output starts on the CE rising edge that follows the output setup with the CCB address. After that, the DO pin is returned to the high-impedance state when CE is set low.
- The number of data bits read differs with the data to be read. Interrupt data (0xEB) is 8 bits long, the channel status related data (0xEC) is 56 bits long, and the sub-code Q data (0xED) is 88 bits long. However, it is not necessary to read out all data bits. During readout, an application can stop providing CL input and set CE low and still have acquired the data read up to that point. For example, when reading the sub-code Q data, if the CRC flags are read and the data is found no good, there is no need to read the subsequent data.

9.5 Input/Output Timing

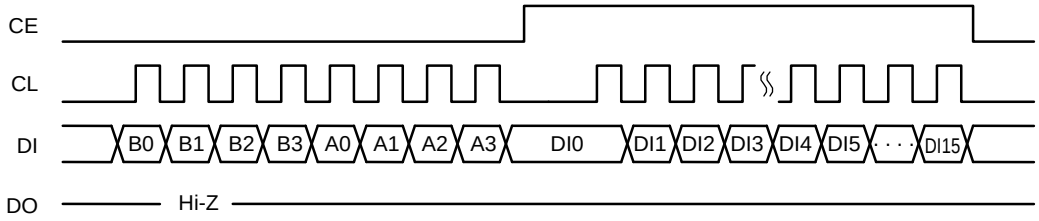


Figure 9.1 Input Timing Chart (Normal low clock)

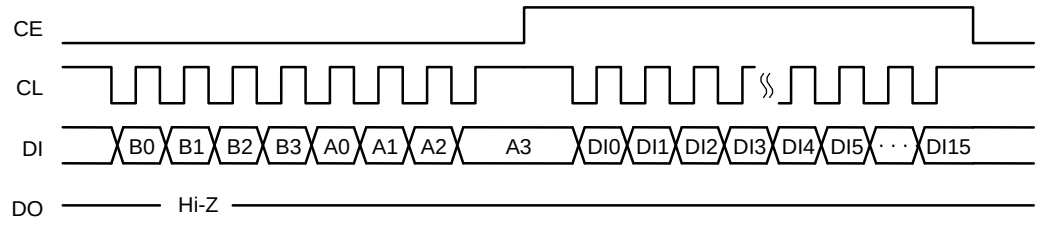


Figure 9.2 Input Timing Chart (Normal high clock)

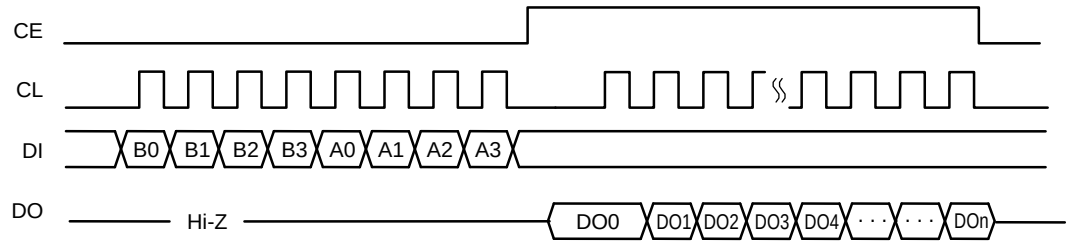


Figure 9.3 Output Timing Chart (Normal low clock)

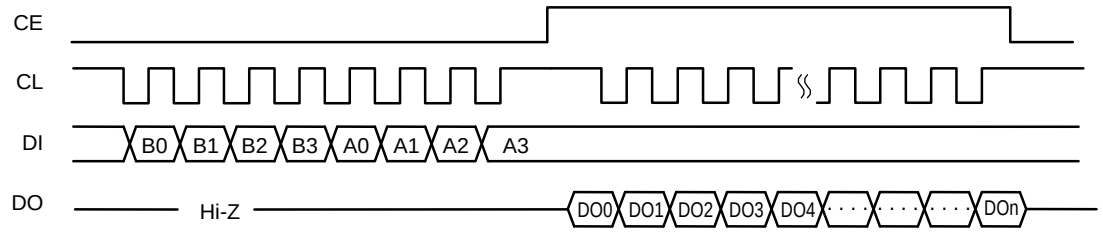


Figure 9.4 Output Timing Chart (Normal high clock. It is necessary to read DO0 with a port.)

- In the output timing shown in figure 9.4, data is allocated so that there are no problems even if the output register DO0 is not read. See the read register table for details.

9.6 Write Registers

9.6.1 List of write registers

• The table shows the write registers.

Table 9.4 Write Register Map

Input register	0xE8	0xE9	0xEA
DI0	SYSRST	GPISEL	INTOPF
DI1	0	GPIDAT	0
DI2	PDOWN0	FLIMIT	0
DI3	PDOWN1	FS4XIN	0
DI4	PLLOPR	FSSEL0	0
DI5	PLLCK0	FSSEL1	0
DI6	PLLCK1	FSSEL2	0
DI7	MCKHFO	FSSEL3	0
DI8	0	OFSEL0	INTSEL
DI9	AMPOPR	OFSEL1	INTERR
DI10	AMPCNT	OFSEL2	INTPCM
DI11	OCKSEL	0	INTEMP
DI12	XISEL0	RDTSEL	INTVFL
DI13	XISEL1	RDTSTA	INTFSC
DI14	XISEL2	RDTMUT	INTCSF
DI15	XISEL3	0	INTSQY

• The shaded columns indicate reserved bits. Input 0 (zero) to these bits.

9.6.2 Details of write data

Table 9.5 Input Register Function Settings 1: System Settings (0xE8)

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
MCKHFO	PLLCK1	PLLCK0	PLLOPR	PDOWN1	PDOWN0	0	SYSRST
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
XISEL3	XISEL2	XISEL1	XISEL0	OCKSEL	AMPCNT	AMPOPR	0

SYSRST: System reset
0: No reset performed (initial value)
1: Reset all circuits other than the command registers.

PDOWN[1:0]: Low power mode settings (Only specific functions are enabled.)
00: Normal operation (initial value)
01: Only the oscillator amplifier is enabled.
10: Only the oscillator amplifier and the output clock divider are enabled.
11: Reserved

PLLOPR: PLL (VCO) operate/stop setting
0: Operate (initial value)
1: Stop

PLLCK[1:0]: Clock frequency setting in the PLL locked state
00: 256fs (initial value)
01: 384fs
10: 512fs
11: (512/2)fs = 256fs

MCKHFO: Frequency setting of CKOUT output clock
0: 1/1 output (initial value)
1: 1/2 output

- It is possible to maintain clock continuity when switching from the 512fs setting with PLLCK[1:0] = "10" to the (512/2) fs setting with PLLCK[1:0] = "11", and switching vice versa without entering the PLL lock error state.
- For systems that must minimize power consumption such as portable equipment, we recommend the PLLCK[1:0] = "00" (256fs) setting. For systems that require improved performance such as AV amplifiers, we recommend the PLLCK[1:0] = "10" (512fs) or PLLCK[1:0] = "11" (512/2fs) setting.

AMPOPR: Oscillator amplifier operate / stop setting
0: Operate (initial value)
1: Stop

AMPCNT: Oscillator amplifier state setting
0: Automatically stop in the PLL locked state (initial value)
1: Always operate continuously

OCKSEL: Clock source setting
0: Use the XIN clock as the source when the PLL is unlocked. (initial value)
1: Use the XIN clock as the source regardless of the PLL state.

XISEL[3:0]: XIN input frequency setting
0000: 11.2896MHz (initial value)
0001: 12.288MHz
0010: 16.9344MHz
0011: Reserved
0001: 22.5792MHz
0010: 24.576MHz
0010: 33.8688MHz
0011: Reserved
1xxx: Must be set when the CKOUT pin and the XIN pin are connected.

Table 9.6 Input Register Function Settings 1: I/O Data Settings (0xE9)

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
FSSEL3	FSSEL2	FSSEL1	FSSEL0	FS4XIN	FLIMIT	GPIDAT	GPISEL
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	RDTMUT	RDTSTA	RDTSEL	0	OFSEL2	OFSEL1	OFSEL1

GPISEL: $\overline{\text{UGPI}}$ pin setting
0: Outputs the microcontroller interface register state. (initial value)
1: Outputs clock switching transitional period signal.

GPIDAT: $\overline{\text{UGPI}}$ output setting (valid only when register output mode is set.)
0: Outputs the low level.
1: Outputs the high level. (initial value)

FLIMIT: Input data reception limit setting
0: Reception is not limited. All data within the PLL locked range can be received. (initial value)
1: Reception is limited. The input fs calculation result is reflected in the error flag according to the FSSEL[3:0] setting.

FS4XIN: Input fs calculation range setting
0: Perform fs calculation for input data in the range of 32k to 96 kHz. (initial value)
1: Perform fs calculation for input data in the range of 64k to 192 kHz.

FSSEL[3:0]: Input data reception range setting (When FLIMIT = "1" and FS4XIN = "0")
0000: 32k, 44.1k, 48k, 64k, 88.2k, or 96kHz (initial value)
0001: 32kHz only
0010: 44.1kHz only
0011: 48kHz
0100: 88.2kHz only
0101: 96kHz only
0110: 44.1k or 88.2kHz only
0111: 48k or 96kHz only
1000: 32k or 44.1k or 48kHz
1001-1111:Reserved

FSSEL[3:0]: Input data reception range setting (When FLIMIT = "1" and FS4XIN = "1")
0000: 64k, 88.2k, 96k 128k, 176.4k, or 192kHz (initial value)
0001: 64kHz only
0010: 88.2kHz only
0011: 96kHz only
0100: 176.4kHz only
0101: 192kHz only
0110: 88.2k or 176.4kHz only
0111: 96k or 192kHz only
1000: 64k or 88.2k or 96kHz only
1001-1111: Reserved

OFSEL[2:0]: Serial audio data output format setting
000: 24-bit MSB first left-justified data output (initial value)
001: 24-bit I^2S data output
010: 24-bit MSB first right-justified data output
011: 20-bit MSB first right-justified data output
100: 16-bit MSB first right-justified data output
101-100: Reserved
101: Bi-phase data output
110: 28-bit I^2S data output (NRZ data output)
111: 28-bit LSB first left-justified data output (NRZ data output)

RDTSEL: PLL unlocked state DATAO output setting
0: Output the SDIN data in the PLL unlocked state. (initial value)
1: Mute the output in the PLL unlocked state.

RDTSTA: DATAO output setting
0: Follow the RDTSEL setting. (initial value)
1: Output the SDIN data regardless of the PLL state.

RDTMUT: DATAO mute setting
0: Output the data selected by RDTSEL. (initial value)
1: Mute the output.

Table 9.7 Input Register Function Settings 1: Interrupt Settings (0xEA)

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	0	0	0	0	0	INTOPF
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
INTQSY	INTCSF	INTFSC	INTVFL	INTEMP	INTPCM	INTERR	INTSEL

INTOPF: E/INT output setting (Valid only when the interrupt output function is selected.)
0: Output a high level when an interrupt occurs. (initial value)
1: Output a high-level pulse when an interrupt occurs.

- When E/INT is set up with INTOPF for going to the high level when an interrupt is generated, the high level state is maintained until the interrupt source output (address 0xEB) is read out. When that data is read, the E/INT output returns to the normal low level.

INTSEL: E/INT pin setting
0: Output emphasis information of the channel status. (initial value)
1: Output the interrupt signal for the microcontroller interface.

INTERR: ERROR signal output setting
0: Do not output this signal. (initial value)
1: Output the change in the ERROR pin state.

INTPCM: $\overline{\text{AUDIO}}$ signal output setting
0: Do not output this signal. (initial value)
1: Output the change in the $\overline{\text{AUDIO}}$ pin state.

INTEMP: Setting of emphasis detection flag output of channel status
0: Do not output this flag. (initial value)
1: Output the emphasis detection flag.

INTVFL: Setting of validity flag detection flag output
0: Do not output this flag. (initial value)
1: Output the validity flag.

INTFSC: Setting of updated flag output of PLL lock frequency calculation result
0: Do not output this flag. (initial value)
1: Output updated flag for the PLL lock frequency calculation result.

INTCSF: Setting of updated flag output of the first 48 bits channel status data
0: Do not output this flag. (initial value)
1: Output the updated flag for the first 48 bits of channel status data.

INTQSY: Setting of signal detection flag output of Sub-code Q data readout load
0: Do not output this flag. (initial value)
1: Output the updated flag for the 80 bits of sub-code Q data including the CRC.

- Use INTFSC, the updated flag, of PLL lock frequency calculation result together with INTERR that output the change in the ERROR state. INTFSC is compared with the target fs of the input fs calculation result. When an fs change other than the target fs is found and the fs change doesn't contain a PLL lock error, INTFSC is valid and the updated flag is output. However, if the fs change contains a PLL lock error, then INTFSC is not valid as a lock error process occurs first and the updated flag is not output.
- The channel status updated flag is computed by comparing the current data with the first 48 bits of the previous block. If those data are identical, the channel status is updated and the flag is output.

9.7 Read Registers

9.7.1 List of read registers

- The table shows the read registers.

Table 9.8 Read Register Map

Output register	0xEB	0xEC	0xED
DO0	0	0	CRC
DO1	OUTERR	OUTERR	CRC
DO2	OUTPCM	OUTPCM	0
DO3	OUTEMP	0	0
DO4	OUTVFL	FSCAL0	0
DO5	OUTFSC	FSCAL1	0
DO6	OUTCSF	FSCAL2	0
DO7	OUTSQY	0	0
DO8	0	Bit 0	Control
DO9	0	Bit 1	Control
DO10	0	Bit 2	Control
DO11	0	Bit 3	Control
DO12	0	Bit 4	Address
DO13	0	Bit 5	Address
DO14	0	Bit 6	Address
DO15	0	Bit 7	Address
DO16	0	Bit 8	Track
DO17	0	Bit 9	Track
DO18	0	Bit 10	Track
DO19	0	Bit 11	Track
DO20	0	Bit 12	Track
DO21	0	Bit 13	Track
DO22	0	Bit 14	Track
DO23	0	Bit 15	Track
DO24	0	Bit 16	Index
…..	0	…..	…..
DO54	0	Bit 46	Frame
DO55	0	Bit 47	Frame
DO56	0	0	Zero
…..	0	0	…..
DO86	0	0	Abs frame
DO87	0	0	Abs frame

- D00 and D01 (CRC) at chip address 0xED are loaded with the same value.

9.7.2 Details of read data

Table 9.9 Output Register: Interrupt Data Output (0xEB)

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
OUTSQY	OUTCSF	OUTFSC	OUTVFL	OUTEMP	OUTPCM	OUTERR	0

OUTERR: ERROR output (Outputs the read-time state.)
0: No transmission error in the PLL locked state
1: Either a transmission error occurred or the PLL circuit is in the unlocked state.

OUTPCM: $\overline{\text{AUDIO}}$ output (Outputs the read-time state.)
0: Non-PCM signal not detected.
1: Non-PCM signal detected.

OUTEMP: Channel status emphasis detection (Outputs the read-time state.)
0: No pre-emphasis.
1: 50/15μs pre-emphasis.

OUTVFL: Validity flag detection (Outputs the read-time state.)
0: No error.
1: Error detected.

OUTFSC: Updated result of Input fs calculation (Cleared after read.)
0: Input fs calculation result not updated.
1: Input fs calculation result updated.

OUTCSF: Updated result of first 48 bits of channel status (Cleared after read.)
0: Not updated.
1: Updated.

OUTQSY: Detection of sub-code Q data readout load signal (Cleared after read.)
0: Not detected.
1: Detected.

Table 9.10 Output Register: Input fs Calculation Result and Channel Status Data (0xEC)

	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
0	0	FSCAL2	FSCAL1	FSCAL0	0	OUTPCM	OUTERR	0
8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
24	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
32	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
40	Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
48	Bit 47	Bit 46	Bit 45	Bit 44	Bit 43	Bit 42	Bit 41	Bit 40

- The error information, non-PCM information, input fs calculation result, and channel status data can be read from this register. Note that the error information and the non-PCM data information are identical to those at 0xEB.

OUTERR: ERROR output (Outputs the read-time state.)
0: No transmission error in the PLL locked state
1: Either a transmission error occurred or the PLL circuit is in the unlocked state.

OUTPCM: $\overline{\text{AUDIO}}$ output (Outputs the read-time state.)
0: Non-PCM signal not detected.
1: Non-PCM signal detected.

- The input data fs calculation results are allocated as follows. The target calculation frequency differs depending on the FS4XIN setting. The calculation range also differs slightly depending on the XIN clock frequency.

Table 9.11 Input fs Calculation Result (Ta = 25°C, V_{DD} = 3.3V, XIN = 11.2896MHz)

FSCAL2	FSCAL1	FSCAL0	FS4XIN = 0		FS4XIN = 1	
			Target fs	Calculated range	Target fs	Calculated range
0	0	0	Out of range	—	Out of range	—
0	0	1	32kHz	30.9k to 33.2kHz	64kHz	62.0k to 66.4kHz
0	1	0	44.1kHz	42.5k to 45.8kHz	88.2kHz	85.5k to 91.0kHz
0	1	1	48kHz	46.3k to 49.9kHz	96kHz	92.6k to 99.0kHz
1	0	0	64kHz	62.1k to 66.4kHz	128kHz	124.0k to 132.8kHz
1	0	1	88.2kHz	85.6k to 91.0kHz	176.4kHz	171.0k to 182.2kHz
1	1	0	96kHz	92.6k to 99.0kHz	192kHz	185.1k to 198.0kHz
1	1	1	—	—	—	—

- The first 48 bits of channel status can be read.
- Since the channel status consists of 192 frames, updated data can always be read by reading at the interval 192 times the period of the input sampling frequency.
- It is also possible to read by using the updated flag of the interrupt source and setting E/INT to interrupt output to reduce the load of the microcontroller. This flag is output when the first 48 bits of the current data is compared with the data of the previous block and found that those data are identical.

Table 9.12 Output Register: Sub-code Q Data with CRC Flag (0xED)

	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
0	0	0	0	0	0	0	CRC	CRC
8	Address	Address	Address	Address	Control	Control	Control	Control
16	Track	Track	Track	Track	Track	Track	Track	Track
24	Index	Index	Index	Index	Index	Index	Index	Index
32	Minute	Minute	Minute	Minute	Minute	Minute	Minute	Minute
40	Second	Second	Second	Second	Second	Second	Second	Second
48	Frame	Frame	Frame	Frame	Frame	Frame	Frame	Frame
56	Zero	Zero	Zero	Zero	Zero	Zero	Zero	Zero
64	abs minute	abs minute	abs minute	abs minute	abs minute	abs minute	abs minute	abs minute
72	abs second	abs second	abs second	abs second	abs second	abs second	abs second	abs second
80	abs frame	abs frame	abs frame	abs frame	abs frame	abs frame	abs frame	abs frame

- When sub-code Q data is included in the input data, this data can be read together with the CRC calculation result.
- To read the sub-code Q data, E/INT must be set to be selected as an interrupt output so that the sub-code Q data readout load signal can be output.
- When sub-code Q data is detected, the E/INT signal outputs a high level or a high-level pulse. The sub-code Q data is updated on each rising edge of the E/INT signal. The readout must be completed within 13.3ms (standard speed) or 6.6ms (2× speed), starting at the E/INT rising edge.
- The cyclic redundancy code (CRC) is a set of flags that decide whether the 80 bits of sub-code Q data is correct. Note that the same data is loaded into both the DO0 and DO1 CRC flags.

Table 9.13 CRC Flag Output

CRC	Output conditions
Low	Errors are found in the sub-code Q data.
High	The sub-code Q data is correct.

10 Application Example

- Decoupling capacitors (0.1μF) for the power supply pin, should be located as close to the LC89052TA-E as possible. Use ceramic capacitors with good high frequency characteristics as the decoupling capacitors. Use a capacitor with a minimal thermal coefficient for the PLL loop filter capacitor.
- There are no constraints on the NC pin configuration. IC operation is not affected by leaving them open or by holding them fixed at particular levels.

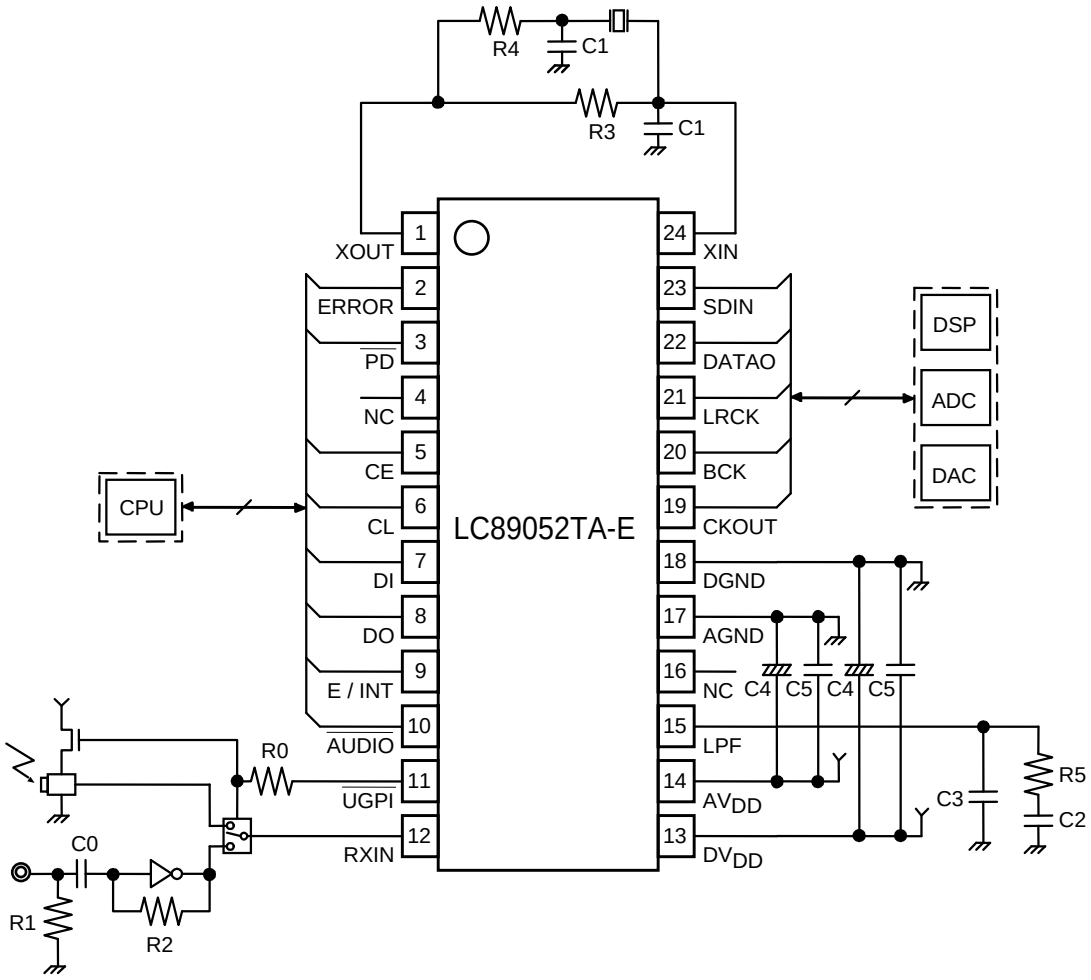


Table 10.1 Recommended Circuit Constant Values

Symbol	Recommended value	Use	Remarks
R0	50 to 1kΩ	—	
R1	75Ω	Coaxial terminator	
R2	50k to 100kΩ	Input amplifier feedback	
R3	1MΩ	Oscillator amplifier feedback	
R4	150 to 330Ω	Oscillator amplifier current constraint	
R5	*	PLL loop filter	Tolerance: ±5%
C0	0.01μ to 0.1μF	AC coupling	
C1	1p to 33pF	Oscillator element load	NP0 special ceramic capacitor
C2	*	PLL loop filter	Film capacitor
C3	*	PLL loop filter	Ceramic capacitor
C4	Over 1μF	Power supply decoupling	Electrolytic capacitor
C5	0.1μF	Power supply decoupling	Ceramic capacitor

* : See section 8.3.1.