

# FAM65CR51DZ1, FAM65CR51DZ2, FAM65CR51DZ3

## Boost Converter Stage in APM16 Series for Multiphase and Semi-Bridgeless PFC

### Features

- Integrated SIP or DIP Boost Converter Stage Power Module for On-board Charger (OBC) in EV-PHEV
- 5 kV/1 sec Electrically Isolated Substrate for Easy Assembly
- Compact Design for Low Total Module Resistance
- Module Serialization for Full Traceability
- Lead Free, RoHS and UL9V4-0 Compliant
- Automotive Qualified per AEC Q101 and LV324 Guidelines

### Applications

- PFC Stage of an On-board Charger in PHEV-HEV

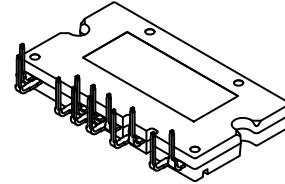
### Benefits

- Enable Design of Small, Efficient and Reliable System for Reduced Vehicle Fuel Consumption and CO<sub>2</sub> Emission
- Simplified Assembly, Optimized Layout, High Level of Integration, and Improved Thermal Performance



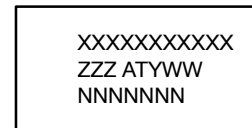
ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)



APMCD-B16  
12 LEAD  
CASE MODGK

### MARKING DIAGRAM



XXXX = Specific Device Code  
ZZZ = Lot ID  
AT = Assembly & Test Location  
Y = Year  
W = Work Week  
NNN = Serial Number

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

# FAM65CR51DZ1, FAM65CR51DZ2, FAM65CR51DZ3

## ORDERING INFORMATION

Part Number	Package	Lead Forming	Pb-Free and RoHS Compliant	Operating Temperature	Packing Method
FAM65CR51DZ1	APM16-CDA	Y-Shape	Yes	-40°C ~ 125°C	Tube
FAM65CR51DZ2	APM16-CDB	L-Shape	Yes	-40°C ~ 125°C	Tube
FAM65CR51DZ3	APM16-CDD	L-Shape*	Yes	-40°C ~ 125°C	Tube

\*Lead length 11.55 mm

## Pin Configuration and Block Diagram

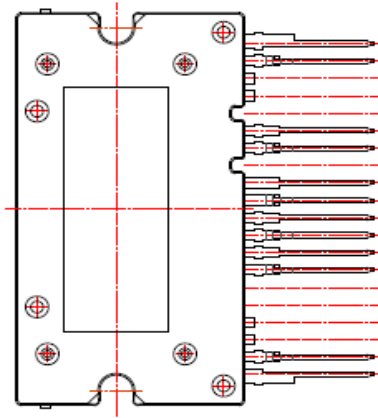


Figure 1. Pin Configuration

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Pin Description
1, 2	AC1	Phase 1 Leg of the PFC Bridge
3	NC	Not Connected
4	NC	Not Connected
5, 6	B+	Positive Battery Terminal
7, 8	Q1 Source	Source Terminal of Q1
9	Q1 Gate	Gate Terminal of Q1
10	Q2 Gate	Gate Terminal of Q2
11, 12	Q2 Source	Source Terminal of Q2
13	NC	Not Connected
14	NC	Not Connected
15, 16	AC2	Phase 2 Leg of the PFC Bridge

# FAM65CR51DZ1, FAM65CR51DZ2, FAM65CR51DZ3

## Block Diagram

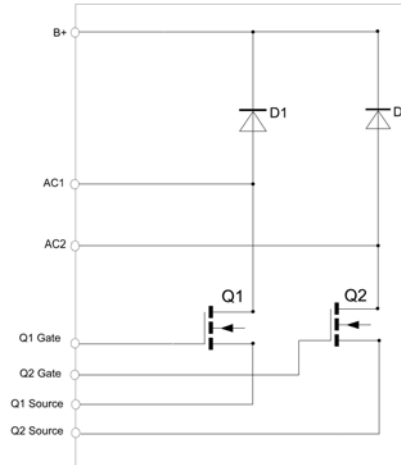


Figure 2. Schematic

Table 2. ABSOLUTE MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)

Symbol	Parameter	Max	Unit
$V_{DS}$ (Q1~Q2)	Drain-to-Source Voltage	650	V
$V_{GS}$ (Q1~Q2)	Gate-to-Source Voltage	$\pm 20$	V
$I_D$ (Q1~Q2)	Drain Current Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 10\text{ V}$ ) (Note 1)	33	A
	Drain Current Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 10\text{ V}$ ) (Note 1)	23	A
$E_{AS}$ (Q1~Q2)	Single Pulse Avalanche Energy (Note 2)	21	mJ
$P_D$	Power Dissipation (Note 1)	160	W
$T_J$	Maximum Junction Temperature	-55 to +150	$^\circ\text{C}$
$T_C$	Maximum Case Temperature	-40 to +125	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-40 to +125	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Maximum continuous current and power, without switching losses, to reach  $T_J = 150^\circ\text{C}$  respectively at  $T_C = 25^\circ\text{C}$  and  $T_C = 100^\circ\text{C}$ ; defined by design based on MOSFET  $R_{DS(ON)}$  and  $R_{\theta JC}$  and not subject to production test
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 6.5\text{ A}$ ,  $V_{DD} = 125\text{ V}$  during inductor charging and  $V_{DD} = 0\text{ V}$  during time in avalanche

### DBC Substrate

0.63 mm  $\text{Al}_2\text{O}_3$  alumina with 0.3 mm copper on both sides.  
DBC substrate is NOT nickel plated.

### Lead Frame

OFC copper alloy, 0.50 mm thick. Plated with 8  $\mu\text{m}$  to 25.4  $\mu\text{m}$  thick Matte Tin

### Flammability Information

All materials present in the power module meet UL flammability rating class 94V-0.

### Compliance to RoHS Directives

The power module is 100% lead free and RoHS compliant 2000/53/C directive.

### Solder

Solder used is a lead free SnAgCu alloy.

Solder presents high risk to melt at temperature beyond  $210^\circ\text{C}$ . Base of the leads, at the interface with the package body, should not be exposed to more than  $200^\circ\text{C}$  during mounting on the PCB or during welding to prevent the re-melting of the solder joints.

# FAM65CR51DZ1, FAM65CR51DZ2, FAM65CR51DZ3

**Table 3. ELECTRICAL SPECIFICATIONS** ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	650	-	-	V
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 3.3 \text{ mA}$	3.0	-	5.0	V
$R_{DS(ON)} Q1$	Q1 Low Side MOSFET	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	44	51	$\text{m}\Omega$
$R_{DS(ON)} Q2$	Q2 Low Side MOSFET		-	44	51	$\text{m}\Omega$
$R_{DS(ON)} Q1$	Q1 Low Side MOSFET	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A},$ $@ T_C = 125^\circ\text{C}$ or $T_J = 150^\circ\text{C}$	-	79	-	$\text{m}\Omega$
$R_{DS(ON)} Q2$	Q2 Low Side MOSFET		-	79	-	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_D = 20 \text{ A}$	-	30	-	S
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-100	-	+100	nA
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	10	$\mu\text{A}$

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 400 \text{ V}$ $V_{GS} = 0 \text{ V}$ $f = 1 \text{ MHz}$	-	4864	-	pF
$C_{oss}$	Output Capacitance		-	109	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	16	-	pF
$C_{oss(eff)}$	Effective Output Capacitance	$V_{DS} = 0 \text{ to } 520 \text{ V}$ $V_{GS} = 0 \text{ V}$	-	652	-	pF
$R_g$	Gate Resistance	$f = 1 \text{ MHz}$	-	2	-	$\Omega$
$Q_{g(tot)}$	Total Gate Charge	$V_{DS} = 380 \text{ V}$ $I_D = 20 \text{ A}$ $V_{GS} = 0 \text{ to } 10 \text{ V}$	-	123	-	nC
$Q_{gs}$	Gate-to-Source Gate Charge		-	37.5	-	nC
$Q_{gd}$	Gate-to-Drain "Miller" Charge		-	49	-	nC

### SWITCHING CHARACTERISTICS

$t_{on}$	Turn-on Time	$V_{DS} = 400 \text{ V}$ $I_D = 20 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_G = 4.7 \text{ Ohm}$	-	56.7	-	ns
$t_{d(on)}$	Turn-on Delay Time		-	40.7	-	ns
$t_r$	Turn-on Rise Time		-	16	-	ns
$t_{off}$	Turn-off Time		-	146	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	117	-	ns
$t_f$	Turn-off Fall Time		-	29	-	ns

### BODY DIODE CHARACTERISTICS

$V_{SD}$	Source-to-Drain Diode Voltage	$I_{SD} = 20 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.95	-	V
$T_{rr}$	Reverse Recovery Time	$V_{DS} = 520 \text{ V}, I_D = 20 \text{ A},$ $dI/dt = 100 \text{ A}/\mu\text{s}$	-	133	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	669	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Defined by design, not subject to production test

# FAM65CR51DZ1, FAM65CR51DZ2, FAM65CR51DZ3

**Table 4. ABSOLUTE MAXIMUM RATINGS OF THE BOOST DIODE** ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)

Symbol	Parameter	Rating	Unit
$V_{RRM}$	Peak Repetitive Reverse Voltage (Note 4)	600	V
$V_{RWM}$	Working Peak Reverse Voltage (Note 4)	600	V
$V_R$	DC Blocking Voltage	600	V
$I_{F(AV)}$	Average Rectified Forward Current $T_C = 25^\circ\text{C}$	15	A
$I_{FSM}$	Non-Repetitive Peak Surge Current (Half Wave 1 Phase 60 Hz)	45	A
$T_J$	Maximum Junction Temperature	-55 to +175	$^\circ\text{C}$
$T_C$	Maximum Case Temperature	-40 to +125	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-40 to +125	$^\circ\text{C}$
$E_{AVL}$	Avalanche Energy (2.85 A, 1 mH)	4	mJ

4.  $V_{RRM}$  and  $I_{F(AV)}$  value referenced to TO220-2L Auto Qualified Package Device ISL9R1560P\_F085

**Table 5. ELECTRICAL SPECIFICATIONS** ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	
$I_R$	Instantaneous Reverse Current	$V_R = 600\text{ V}$	$T_C = 25^\circ\text{C}$	-	-	100	$\mu\text{A}$
			$T_C = 125^\circ\text{C}$	-	-	1	mA
$V_{FM}$	Instantaneous Forward Voltage (Note 5)	$I_F = 15\text{ A}$	$T_C = 25^\circ\text{C}$	-	1.65	2.2	V
			$T_C = 125^\circ\text{C}$	-	1.24	1.7	V
$t_{rr}$	Reverse Recovery Time (Note 6)	$I_F = 15\text{ A}$ $dI_F/dt = 200\text{ A}/\mu\text{s}$ $V_R = 390\text{ V}$	$T_C = 25^\circ\text{C}$	-	29	-	ns
$t_a$	Time to reach peak reverse current		$T_C = 25^\circ\text{C}$	-	16	-	ns
$t_b$	Time from peak $I_{RRM}$ to projected zero crossing of $I_{RRM}$ based on a straight line from peak $I_{RRM}$ through 25% of $I_{RRM}$		$T_C = 25^\circ\text{C}$	-	13	-	n
$Q_{rr}$	Reverse Recovered Charge	$T_C = 25^\circ\text{C}$	-	43	-	nC	

5. Test pulse width = 300  $\mu\text{s}$ , Duty Cycle = 2%

6. Guaranteed by design

**Table 6. THERMAL RESISTANCE**

Parameters		Min	Typ	Max	Unit
$R_{\theta JC}$ (per MOSFET chip)	Q1~Q4 Thermal Resistance Junction-to-Case (Note 7)	-	0.66	0.92	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$ (per MOSFET chip)	Q1~Q4 Thermal Resistance Junction-to-Sink (Note 8)	-	1.20	-	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$ (per DIODE chip)	Q1~Q4 Thermal Resistance Junction-to-Case (Note 7)	-	1.98	2.72	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$ (per DIODE chip)	Q1~Q4 Thermal Resistance Junction-to-Sink (Note 8)	-	2.97	-	$^\circ\text{C}/\text{W}$

7. Test method compliant with MIL STD 883-1012.1, from case temperature under the chip to case temperature measured below the package at the chip center, Cosmetic oxidation and discoloration on the DBC surface allowed

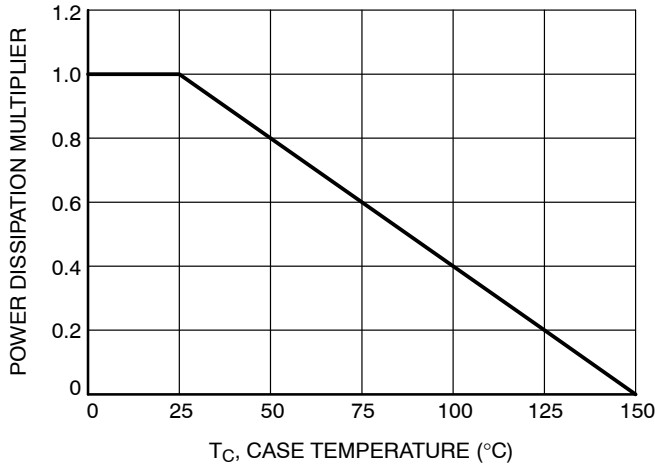
8. Defined by thermal simulation assuming the module is mounted on a 5 mm Al-360 die casting material with 30  $\mu\text{m}$  of 1.8 W/mK thermal interface material

**Table 7. ISOLATION VOLTAGE** (Isolation voltage between the base plate and to control pins or power terminals.)

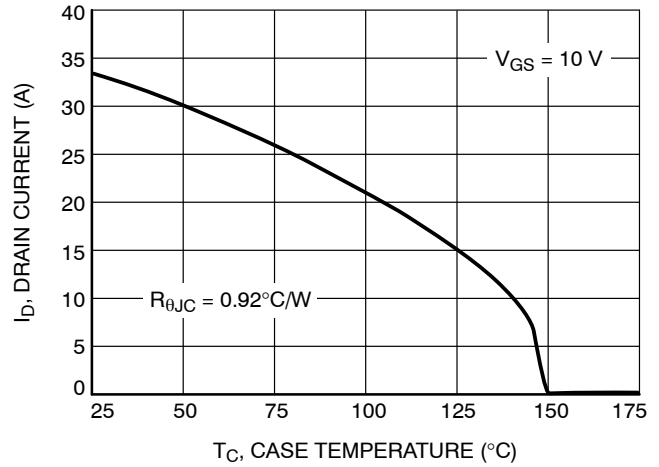
Test	Test Conditions	Isolation Resistance	Unit
Leakage @ Isolation Voltage (Hi-Pot)	$V_{AC} = 5\text{ kV}$ , 60 Hz	100M <	$\Omega$

# FAM65CR51DZ1, FAM65CR51DZ2, FAM65CR51DZ3

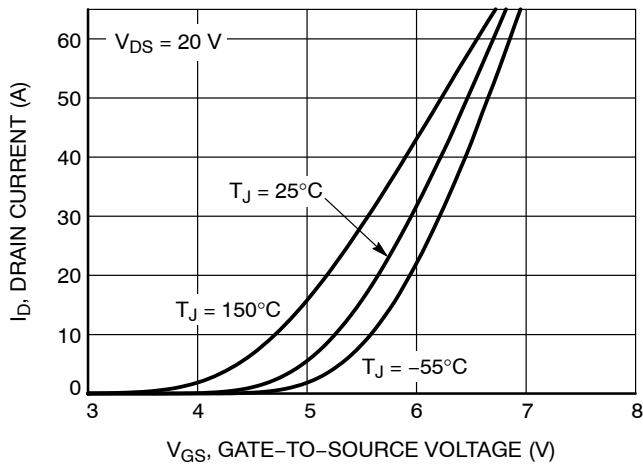
## TYPICAL CHARACTERISTICS – MOSFETs



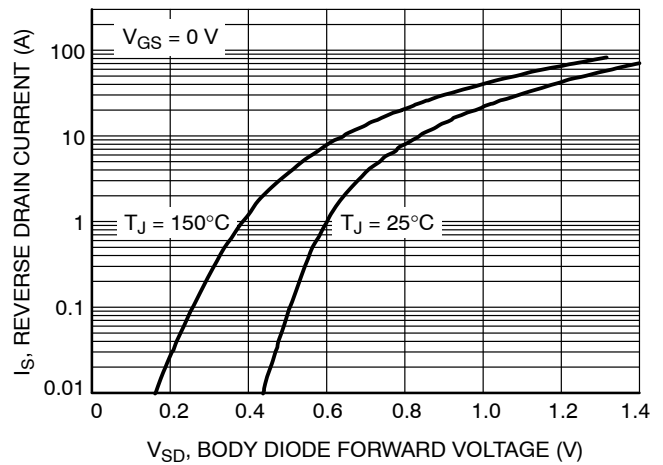
**Figure 3. Normalized Power Dissipation vs. Case**



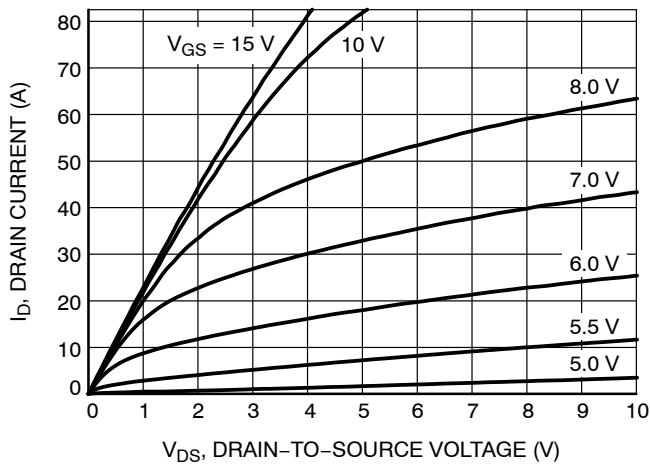
**Figure 4. Maximum Continuous I<sub>D</sub> vs. Case Temperature**



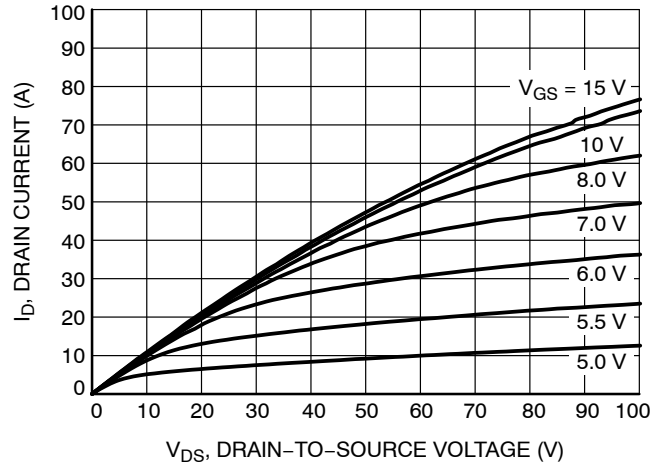
**Figure 5. Transfer Characteristics**



**Figure 6. Forward Diode**



**Figure 7. Saturation (25°C)**



**Figure 8. Saturation (150°C)**

TYPICAL CHARACTERISTICS – MOSFETS

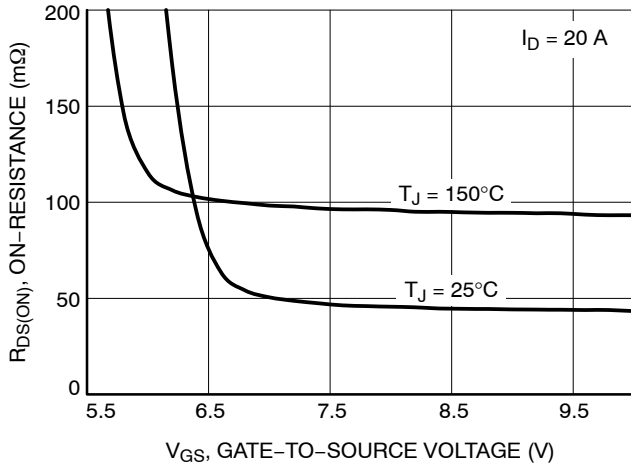


Figure 9. On-Resistance vs. Gate-to-Source Voltage

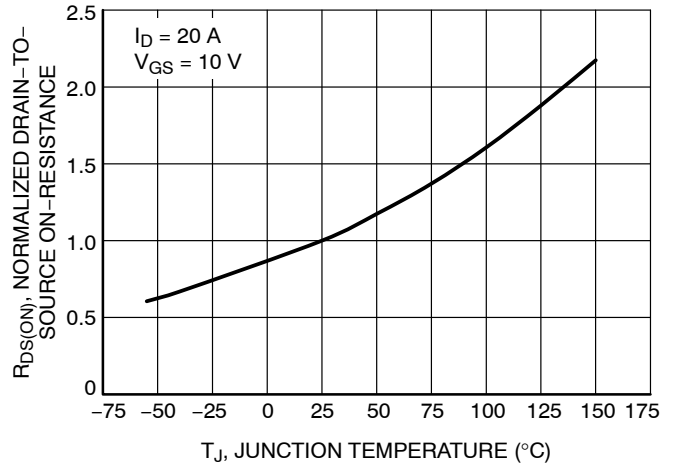


Figure 10.  $R_{DS(norm)}$  vs. Junction Temperature

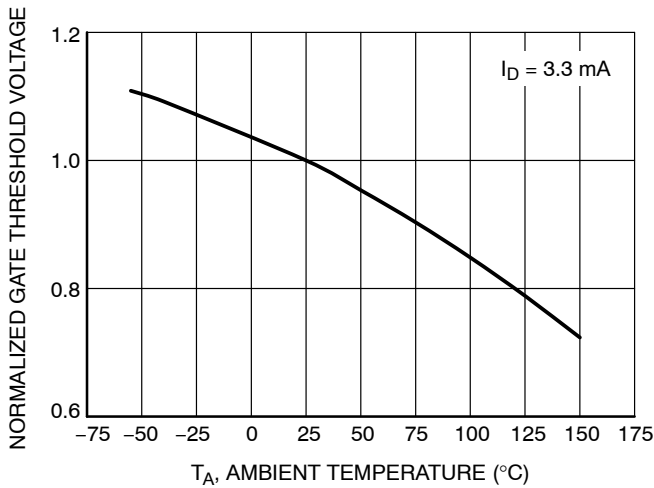


Figure 11. Normalized  $R_{D(on)}$  vs. Temperature

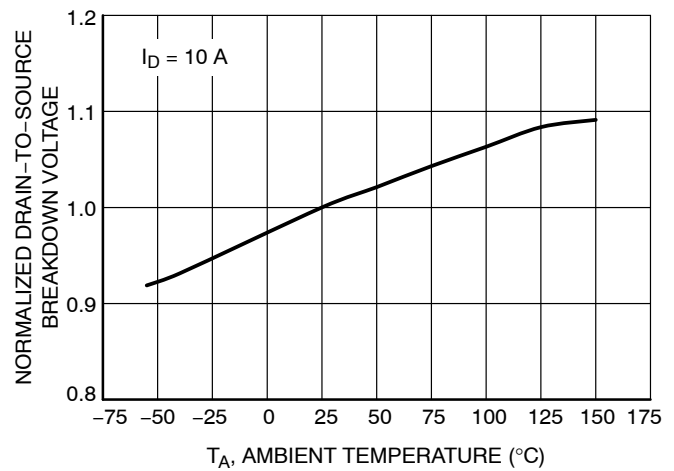


Figure 12. Breakdown Voltage vs. Temperature

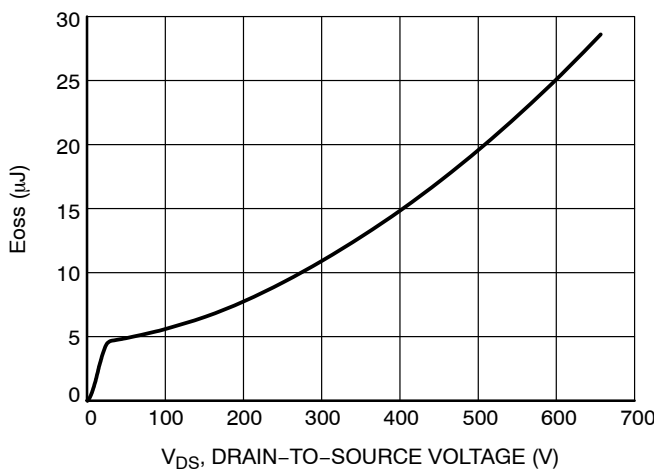


Figure 13.  $E_{oss}$  vs. Drain-to-Source Voltage

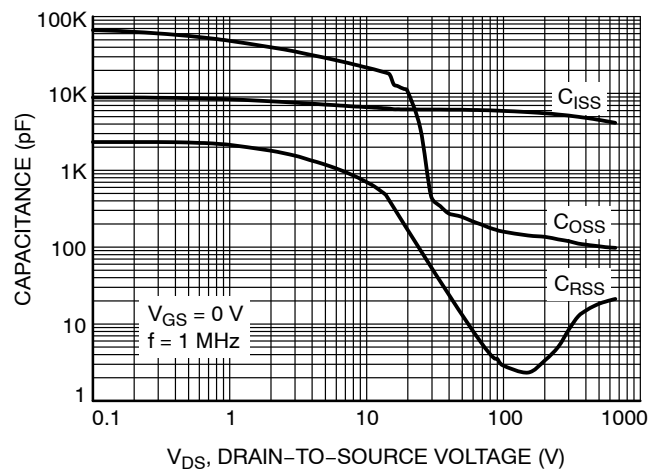


Figure 14. Capacitance Variation

TYPICAL CHARACTERISTICS – MOSFETs

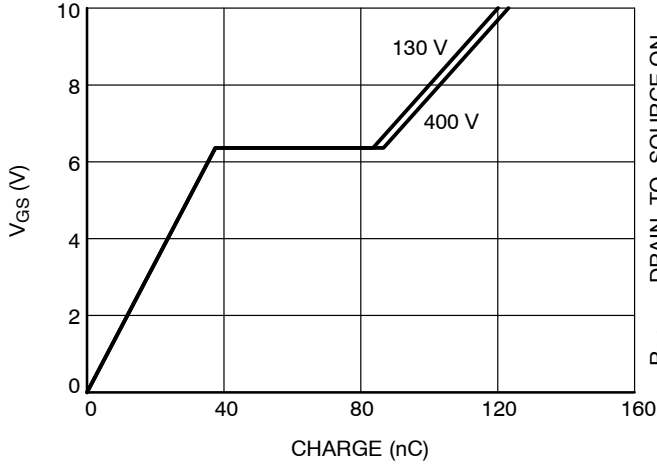


Figure 15. Gate Charge

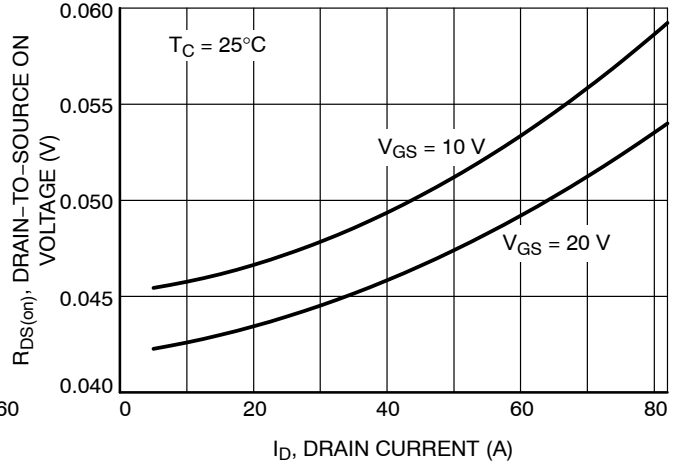


Figure 16.  $R_{DS(on)}$  vs.  $I_D$

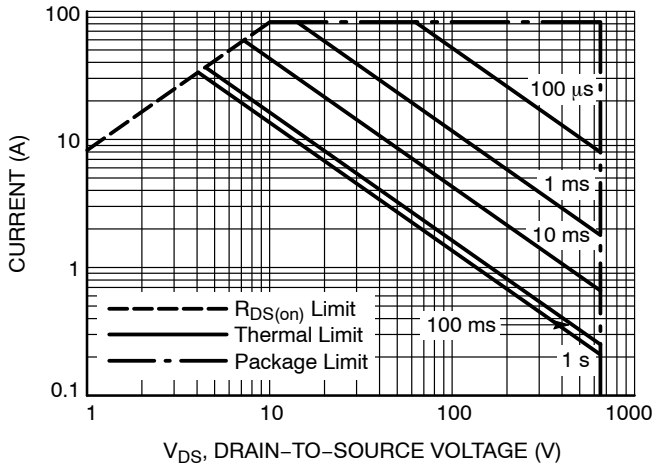


Figure 17. Safe Operating Area

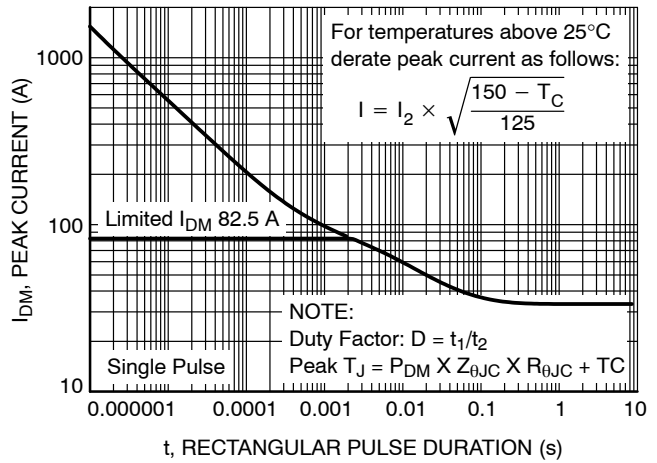


Figure 18. Peak Current Capability

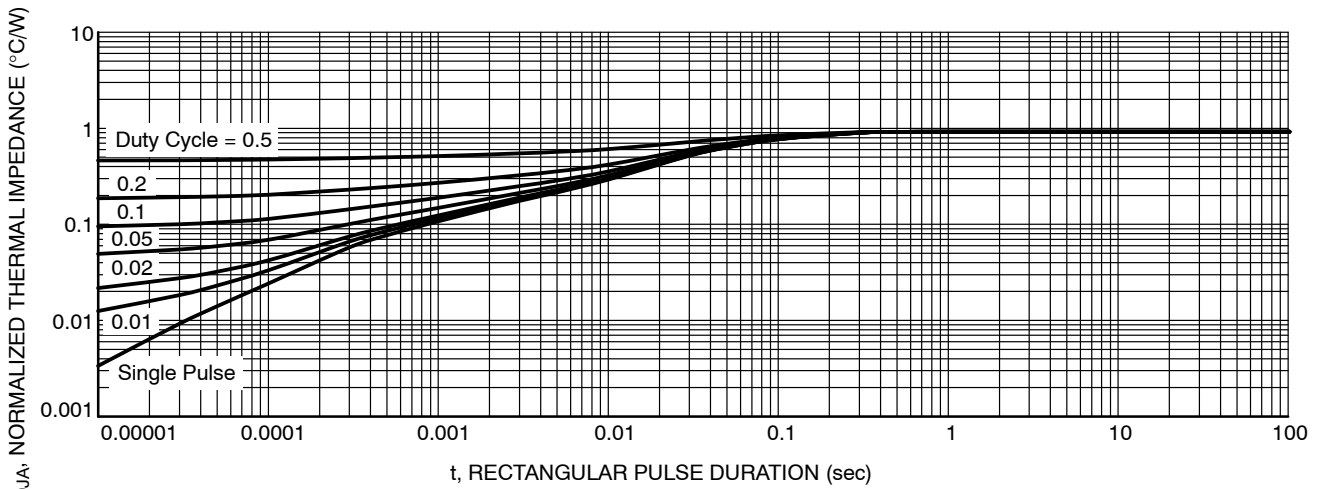


Figure 19. Transient Thermal Impedance



TYPICAL CHARACTERISTICS – DIODES

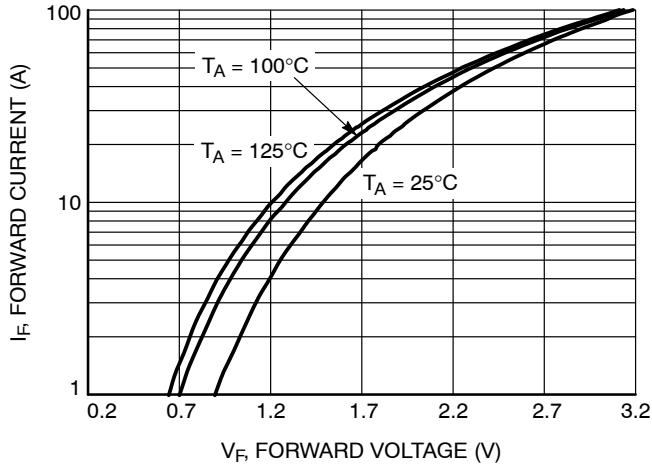


Figure 20. Typical Forward Voltage Drop vs. Forward Current

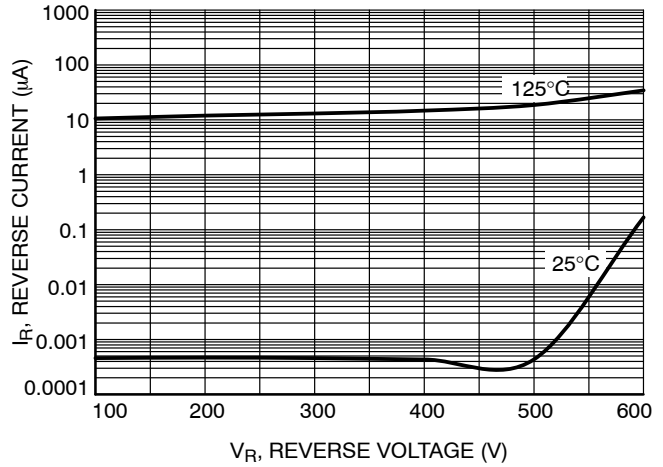


Figure 21. Typical Reverse Current vs. Reverse Voltage

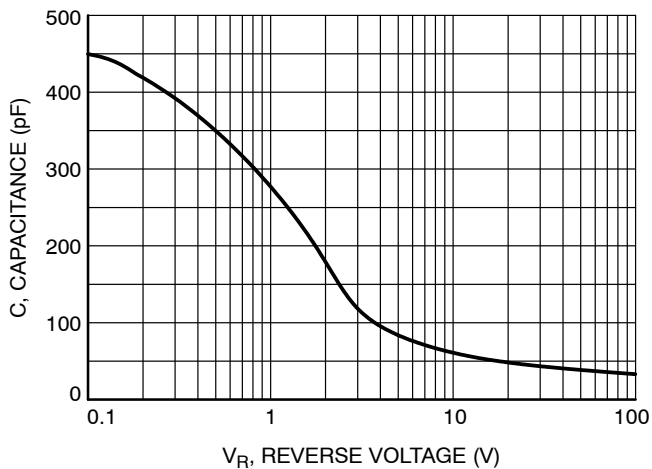


Figure 22. Capacitance

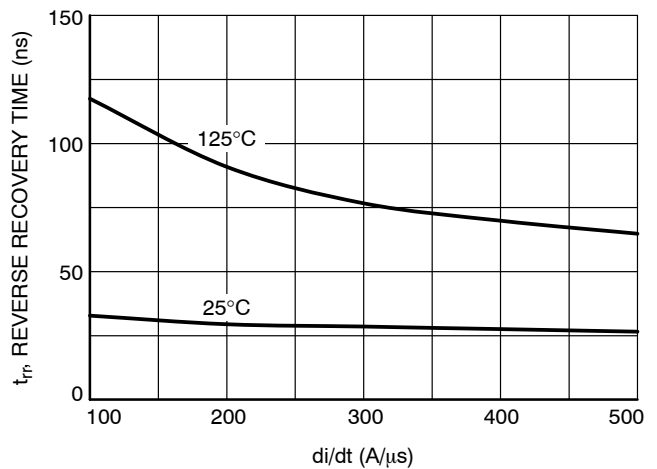


Figure 23. Reverse Recovery Time vs. di/dt

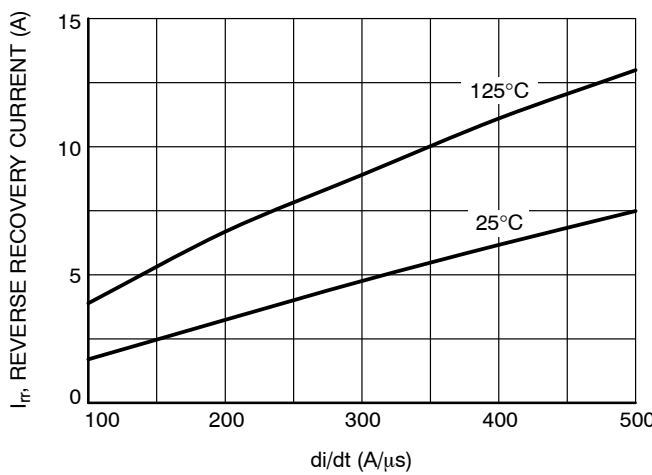


Figure 24. Reverse Recovery Current vs. di/dt

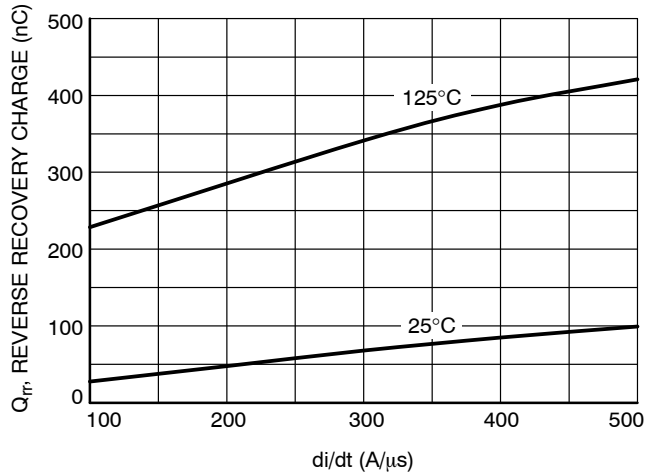


Figure 25. Reverse Recovery Charge vs. di/dt

# FAM65CR51DZ1, FAM65CR51DZ2, FAM65CR51DZ3

## TYPICAL CHARACTERISTICS – DIODES

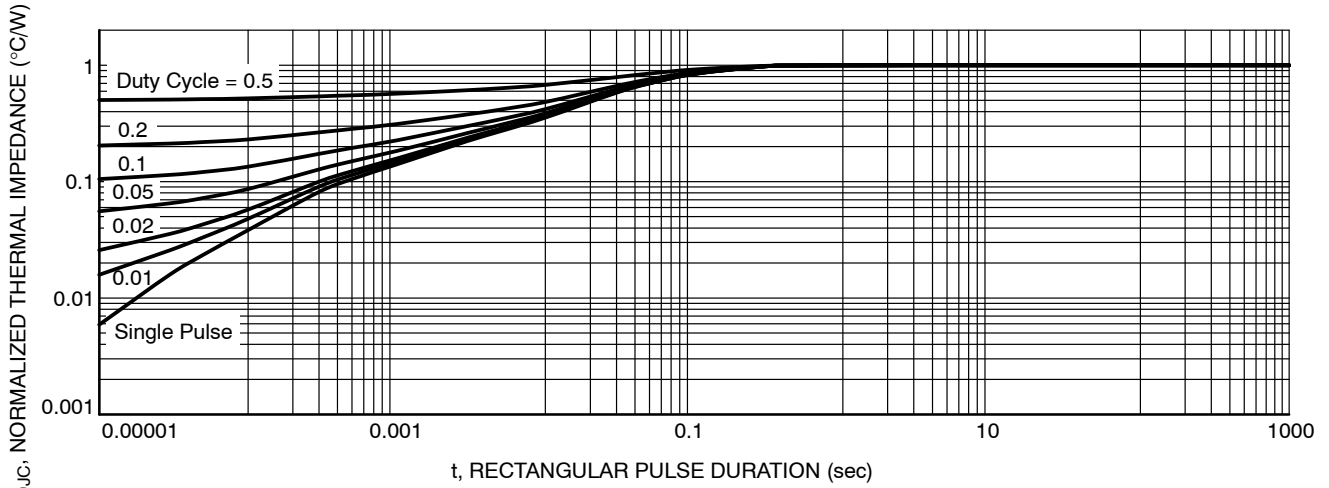
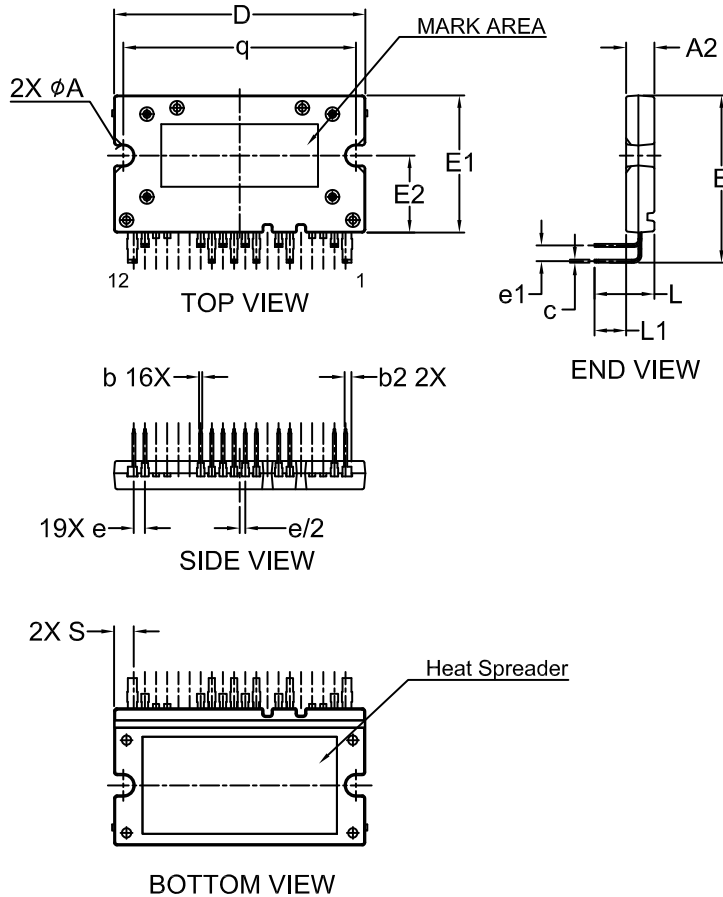


Figure 26. Transient Thermal Impedance

# FAM65CR51DZ1, FAM65CR51DZ2, FAM65CR51DZ3

## PACKAGE DIMENSIONS

### APMCD-B16 / 12LD, AUTOMOTIVE MODULE CASE MODGK ISSUE O



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A2	4.30	4.50	4.70
b	0.45	0.50	0.60
b2	1.15	1.20	1.30
c	0.45	0.50	0.60
D	39.90	40.10	40.30
E	33.80	34.30	34.80
E1	21.70	21.90	22.10
E2	12.10	12.30	12.50
e	1.478	1.778	2.078
e1	2.20	2.50	2.80
L	9.20	9.55	9.90
L1	5.05 REF		
q	36.85	37.10	37.35
S	3.519 REF		
φA	2.95	3.20	3.45

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### PUBLICATION ORDERING INFORMATION

##### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative