

FAM65HR51DS1, FAM65HR51DS2, FAM65HR51DS3

H-Bridge in APM16 Series for LLC and Phase-shifted DC-DC Converter

Features

- SIP or DIP H-Bridge Power Module for On-board Charger (OBC) in EV-PHEV
- High Voltage Snubber Capacitor for Low Noise at High Voltage Battery
- 5 kV/1 sec Electrically Isolated Substrate for Easy Assembly
- Compact Design for Low Total Module Resistance
- Module Serialization for Full Traceability
- Lead Free, RoHS and UL9V4-0 Compliant
- Automotive Qualified per AEC Q101 and LV324 Guidelines

Applications

- DC-DC Converter for On-board Charger in EV-PHEV

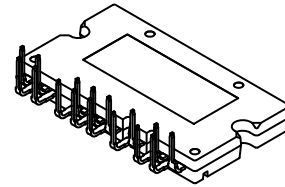
Benefits

- Enable Design of Small, Efficient and Reliable System for Reduced Vehicle Fuel Consumption and CO₂ Emission
- Simplified Assembly, Optimized Layout, High Level of Integration, and Improved Thermal Performance



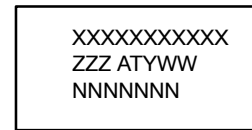
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APMCA-B16
16 LEAD
CASE MODGJ

MARKING DIAGRAM



XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
W = Work Week
NNN = Serial Number

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

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ORDERING INFORMATION

Part Number	Package	Lead Forming	Pb-Free and RoHS Compliant	Operating Temperature	Packing Method
FAM65HR51DS1	APM16-CAA	Y-Shape	Yes	-40°C ~ 125°C	Tube
FAM65HR51DS2	APM16-CAB	L-Shape	Yes	-40°C ~ 125°C	Tube
FAM65HR51DS3	APM16-CAD	L-Shape*	Yes	-40°C ~ 125°C	Tube

*Lead length 11.55 mm

Pin Configuration and Block Diagram

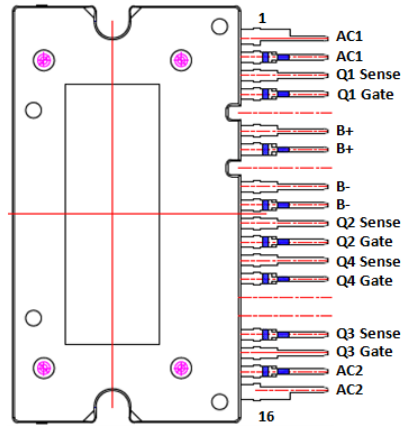


Figure 1. Pin Configuration

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Pin Description
1, 2	AC1	Phase 1 Leg of the H-Bridge
3	Q1 Sense	Source Sense of Q1
4	Q1 Gate	Gate Terminal of Q1
5, 6	B+	Positive Battery Terminal
7, 8	B-	Negative Battery Terminal
9	Q2 Sense	Source Sense of Q2
10	Q2 Gate	Gate Terminal of Q2
11	Q4 Sense	Source Sense of Q4
12	Q4 Gate	Gate Terminal of Q4
13	Q3 Sense	Source Sense of Q3
14	Q3 Gate	Gate Terminal of Q3
15, 16	AC2	Phase 2 Leg of the H-Bridge

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Block Diagram

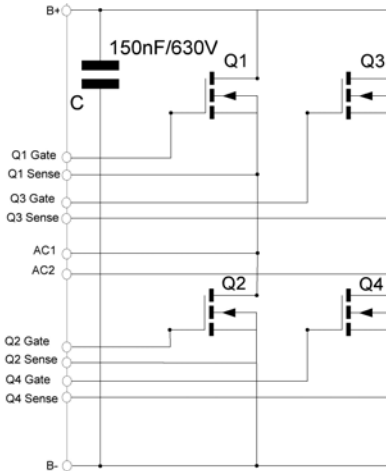


Figure 2. Schematic

Table 2. ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)

Symbol	Parameter	Max	Unit
V_{DS} (Q1~Q4)	Drain-to-Source Voltage	650	V
V_{GS} (Q1~Q4)	Gate-to-Source Voltage	± 20	V
I_D (Q1~Q4)	Drain Current Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10\text{ V}$) (Note 1)	33	A
	Drain Current Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 10\text{ V}$) (Note 1)	21	A
E_{AS} (Q1~Q4)	Single Pulse Avalanche Energy (Note 2)	21	mJ
P_D	Power Dissipation (Note 1)	135	W
T_J	Maximum Junction Temperature	-55 to +150	$^\circ\text{C}$
T_C	Maximum Case Temperature	-40 to +125	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to +125	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Maximum continuous current and power, without switching losses, to reach $T_J = 150^\circ\text{C}$ respectively at $T_C = 25^\circ\text{C}$ and $T_C = 100^\circ\text{C}$; defined by design based on MOSFET $R_{DS(ON)}$ and $R_{\theta JC}$ and not subject to production test
- Starting $T_J = 25^\circ\text{C}$, $L = 1\text{ mH}$, $I_{AS} = 6.5\text{ A}$, $V_{DD} = 145\text{ V}$ during inductor charging and $V_{DD} = 0\text{ V}$ during time in avalanche

Table 3. COMPONENTS

Supplier	Part Number	Parameter	Min	Typ	Max	Unit
Murata (Note 3)	GCJ43QR7LV154KXJ1	Capacitance	135	150	165	nF
		VDC Rating	-	630	-	V

- Please refer to datasheet of the Murata capacitor

DBC Substrate

0.63 mm Al_2O_3 alumina with 0.3 mm copper on both sides. DBC substrate is NOT nickel plated.

Lead Frame

OFC copper alloy, 0.50 mm thick. Plated with 8 μm to 25.4 μm thick Matte Tin

Flammability Information

All materials present in the power module meet UL flammability rating class 94V-0.

Compliance to RoHS Directives

The power module is 100% lead free and RoHS compliant 2000/53/C directive.

Solder

Solder used is a lead free SnAgCu alloy.

Solder presents high risk to melt at temperature beyond 210°C . Base of the leads, at the interface with the package body, should not be exposed to more than 200°C during mounting on the PCB or during welding to prevent the re-melting of the solder joints.

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Table 4. ELECTRICAL SPECIFICATIONS ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain-to-Source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	650	-	-	V
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 3.3 \text{ mA}$	3.0	-	5.0	V
$R_{DS(ON)}$	Q1 – Q4 MOSFET On Resistance	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	44	51	m Ω
$R_{DS(ON)}$	Q1 – Q4 MOSFET On Resistance	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}, T_C = 125^\circ\text{C}$ (Note 4)	-	79	-	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_D = 20 \text{ A}$	-	30	-	S
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-100	-	+100	nA
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	10	μA

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 400 \text{ V}$ $V_{GS} = 0 \text{ V}$ $f = 1 \text{ MHz}$	-	4864	-	pF
C_{oss}	Output Capacitance		-	109	-	pF
C_{rss}	Reverse Transfer Capacitance		-	16	-	pF
$C_{oss(eff)}$	Effective Output Capacitance	$V_{DS} = 0 \text{ to } 520 \text{ V}$ $V_{GS} = 0 \text{ V}$	-	652	-	pF
R_g	Gate Resistance	$f = 1 \text{ MHz}$	-	2	-	Ω
$Q_{g(tot)}$	Total Gate Charge	$V_{DS} = 380 \text{ V}$ $I_D = 20 \text{ A}$ $V_{GS} = 0 \text{ to } 10 \text{ V}$	-	123	-	nC
Q_{gs}	Gate-to-Source Gate Charge		-	37.5	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge		-	49	-	nC

SWITCHING CHARACTERISTICS

t_{on}	Turn-on Time	$V_{DS} = 400 \text{ V}$ $I_D = 20 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_G = 4.7 \text{ Ohm}$	-	60.5	-	ns
$t_{d(on)}$	Turn-on Delay Time		-	50.5	-	ns
t_r	Turn-on Rise Time		-	10	-	ns
t_{off}	Turn-off Time		-	241	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	117	-	ns
t_f	Turn-off Fall Time		-	125	-	ns

BODY DIODE CHARACTERISTICS

V_{SD}	Source-to-Drain Diode Voltage	$I_{SD} = 20 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.95	-	V
T_{rr}	Reverse Recovery Time	$V_{DS} = 520 \text{ V}, I_D = 20 \text{ A},$ $d_i/d_t = 100 \text{ A}/\mu\text{s}$	-	133	-	ns
Q_{rr}	Reverse Recovery Charge		-	669	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Defined by design, not subject to production test

Table 5. THERMAL RESISTANCE

Parameters		Min	Typ	Max	Unit
$R_{\theta JC}$ (per chip)	Q1~Q4 Thermal Resistance Junction-to-Case (Note 5)	-	0.66	0.92	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$ (per chip)	Q1~Q4 Thermal Resistance Junction-to-Sink (Note 6)	-	1.2	-	$^\circ\text{C}/\text{W}$

5. Test method compliant with MIL STD 883-1012.1, from case temperature under the chip to case temperature measured below the package at the chip center, Cosmetic oxidation and discoloration on the DBC surface allowed

6. Defined by thermal simulation assuming the module is mounted on a 5 mm Al-360 die casting material with 30 μm of 1.8 W/mK thermal interface material

Table 6. ISOLATION VOLTAGE (Isolation voltage between the base plate and to control pins or power terminals.)

Test	Test Conditions	Isolation Resistance	Unit
Leakage @ Isolation Voltage (Hi-Pot)	$V_{AC} = 5 \text{ kV}, 60 \text{ Hz}$	100M <	Ω

TYPICAL CHARACTERISTICS

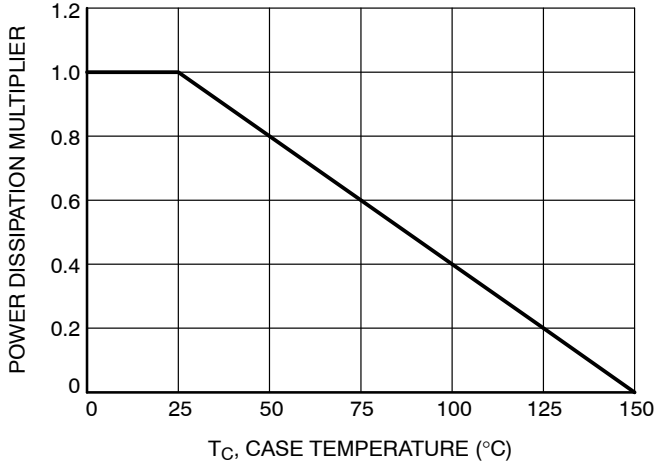


Figure 3. Normalized Power Dissipation vs. Case

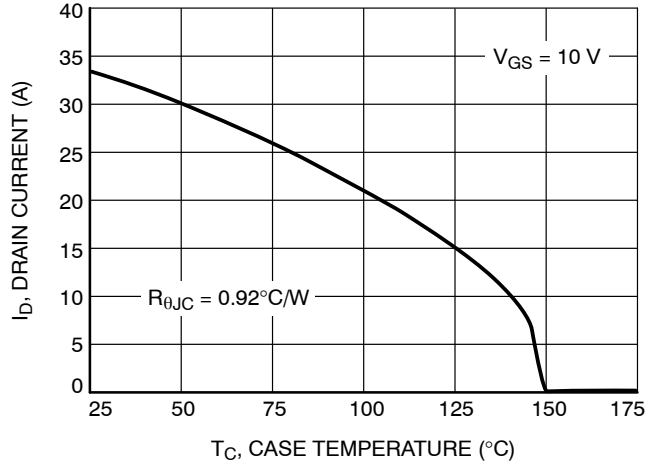


Figure 4. Maximum Continuous I_D vs. Case Temperature

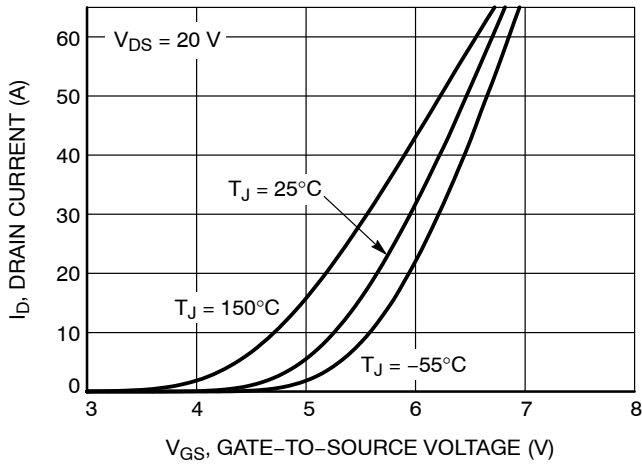


Figure 5. Transfer Characteristics

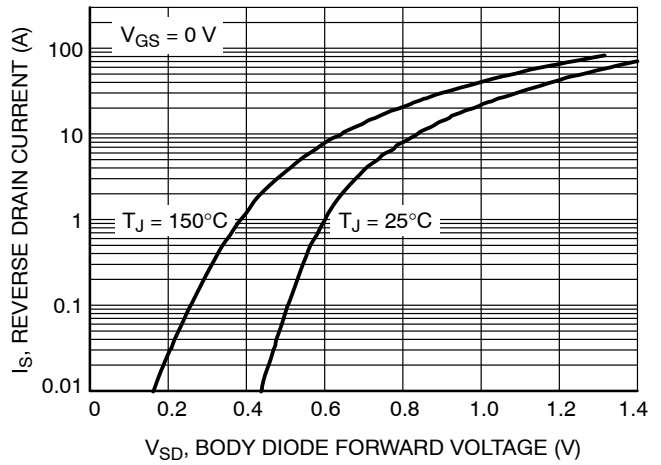


Figure 6. Forward Diode

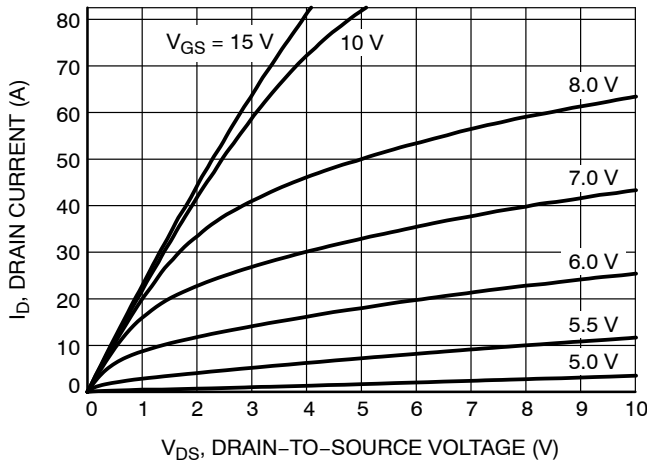


Figure 7. Saturation (25°C)

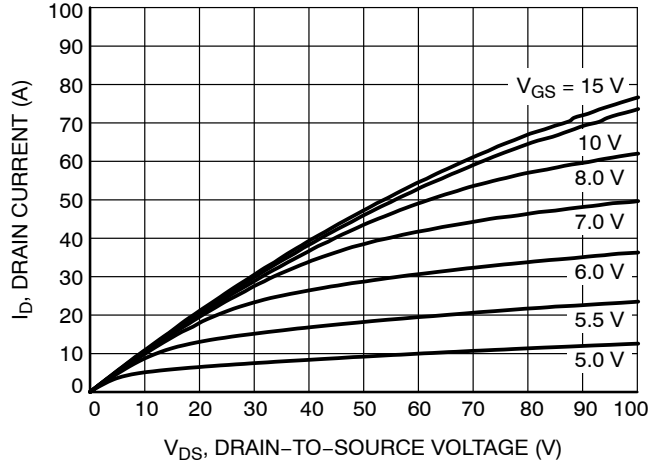


Figure 8. Saturation (150°C)

TYPICAL CHARACTERISTICS

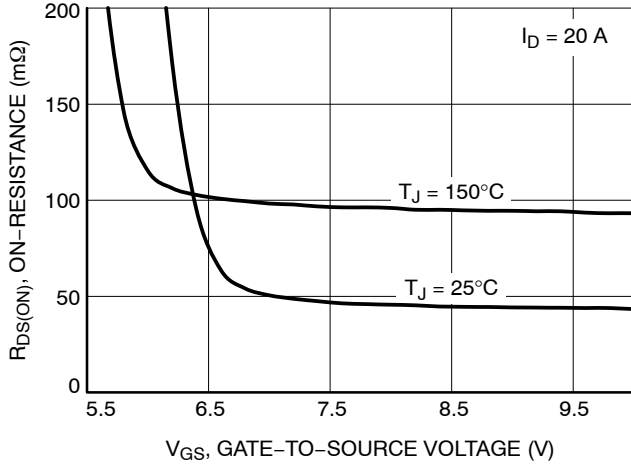


Figure 9. On-Resistance vs. Gate-to-Source Voltage

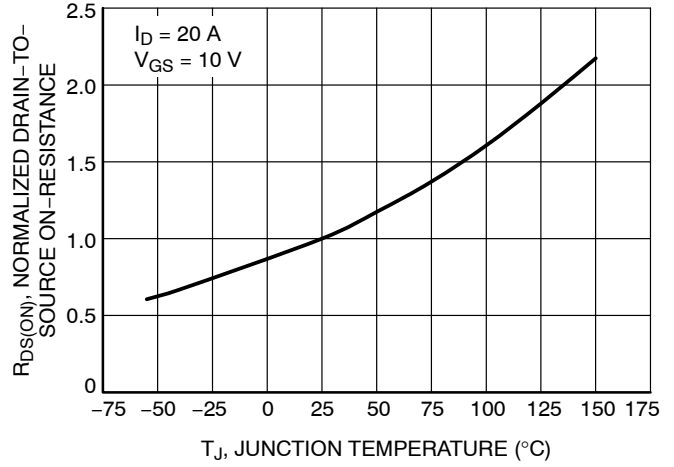


Figure 10. $R_{DS(norm)}$ vs. Junction Temperature

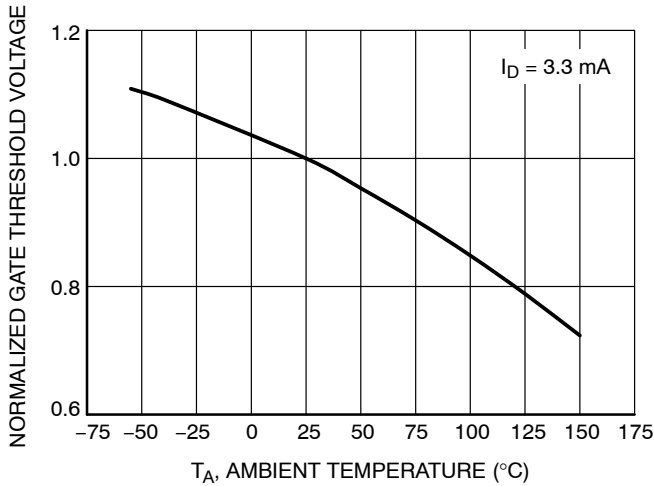


Figure 11. Normalized $R_{D(on)}$ vs. Temperature

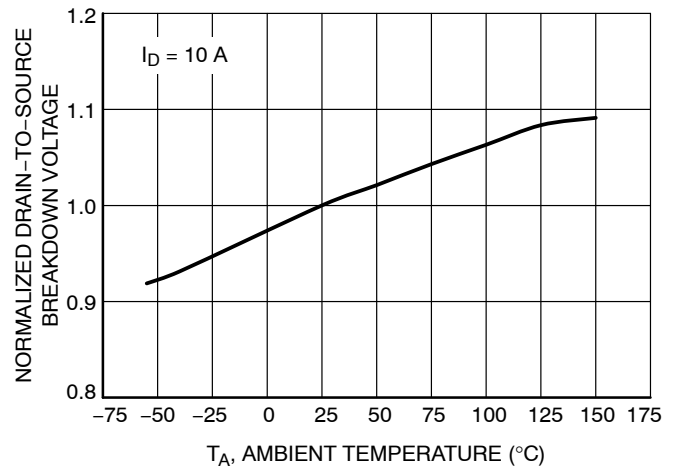


Figure 12. Breakdown Voltage vs. Temperature

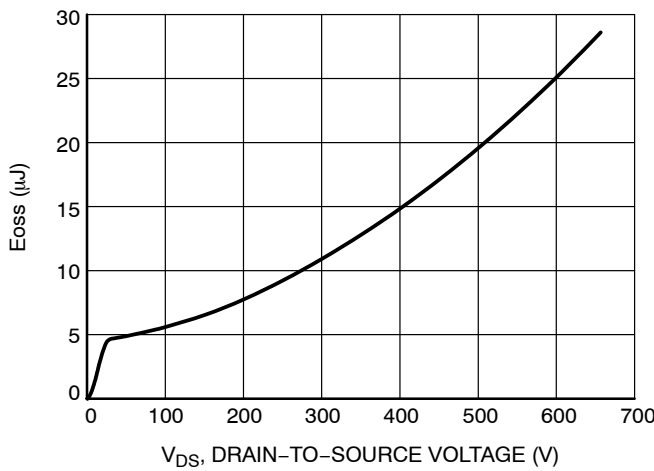


Figure 13. E_{oss} vs. Drain-to-Source Voltage

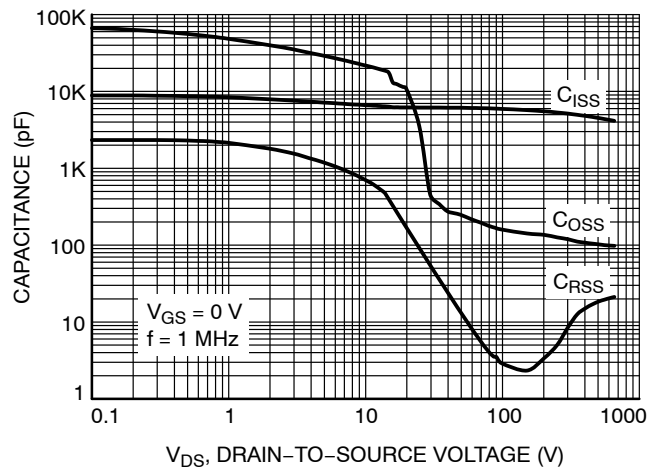


Figure 14. Capacitance Variation

TYPICAL CHARACTERISTICS

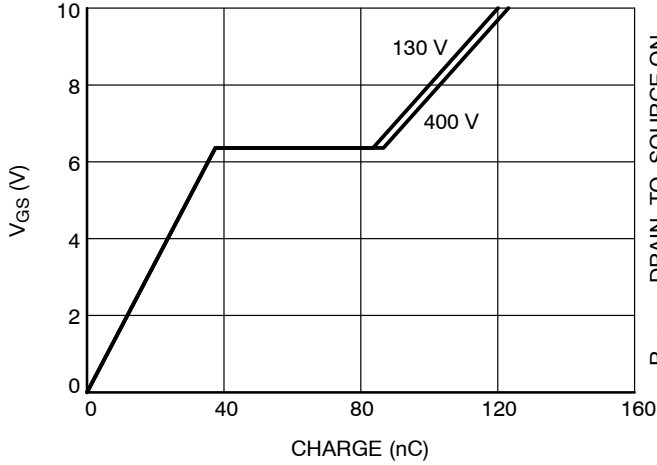


Figure 15. Gate Charge

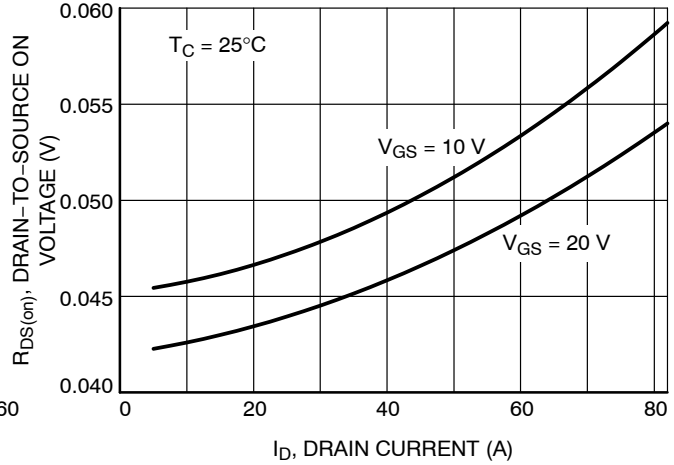


Figure 16. $R_{DS(on)}$ vs. I_D

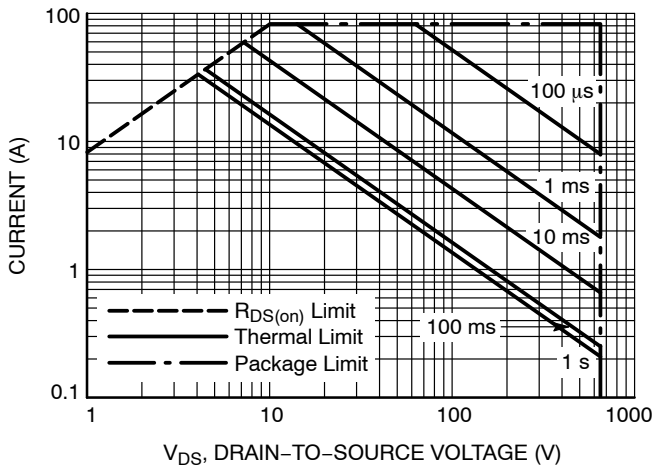


Figure 17. Safe Operating Area

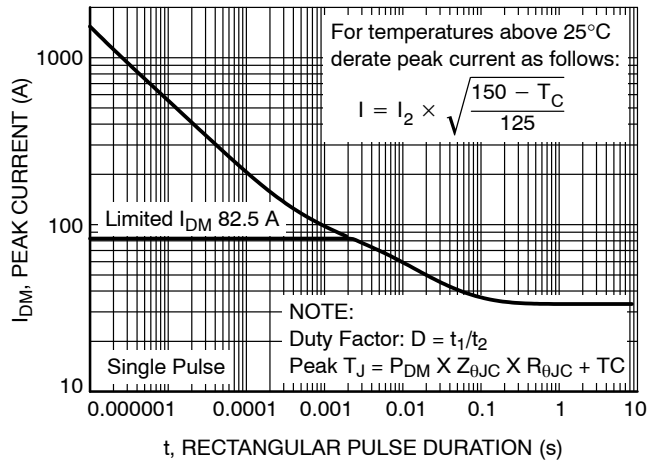


Figure 18. Peak Current Capability

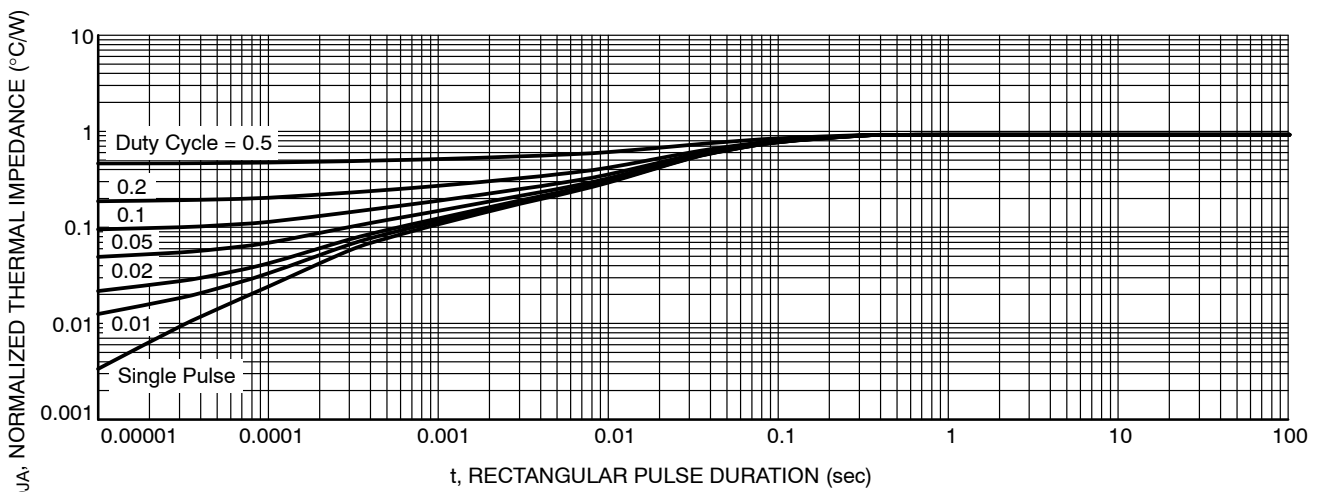
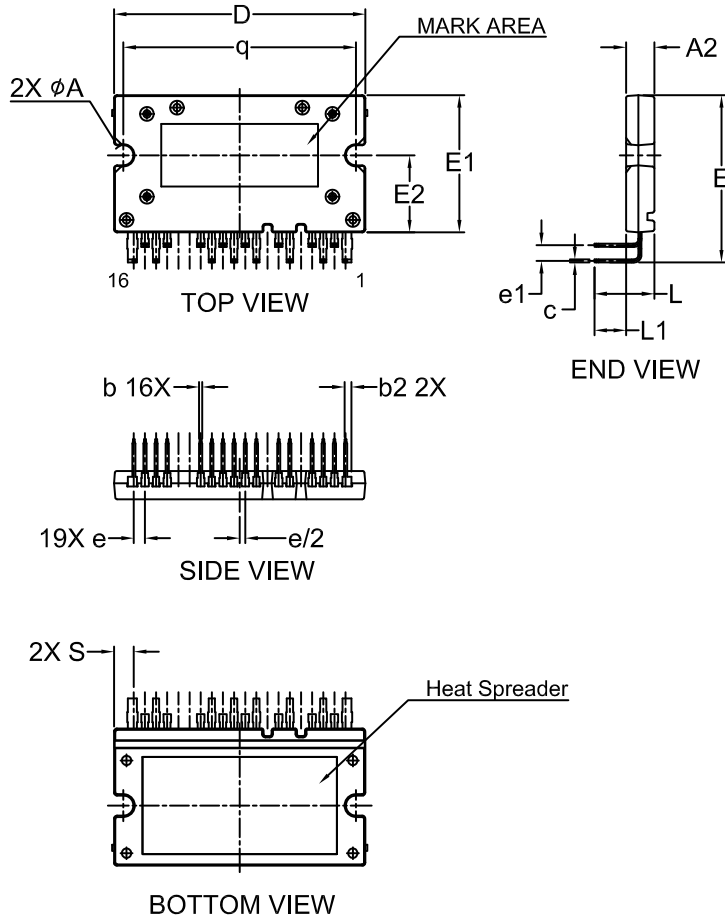


Figure 19. Transient Thermal Impedance

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PACKAGE DIMENSIONS

APMCA-B16 / 16LD, AUTOMOTIVE MODULE CASE MODGJ ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A2	4.30	4.50	4.70
b	0.45	0.50	0.60
b2	1.15	1.20	1.30
c	0.45	0.50	0.60
D	39.90	40.10	40.30
E	33.80	34.30	34.80
E1	21.70	21.90	22.10
E2	12.10	12.30	12.50
e	1.478	1.778	2.078
e1	2.20	2.50	2.80
L	9.20	9.55	9.90
L1	5.05 REF		
q	36.85	37.10	37.35
S	3.519 REF		
φA	2.95	3.20	3.45

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