FAN250225S

Advance Information

25 A Synchronous Buck Regulator

The FAN250225S is a highly efficient synchronous buck regulator. The regulator is capable of operating with an input range from 4.5 V to 18 V and supporting up to 25 A load currents.

The FAN250225S utilizes a constant on−time control architecture to provide excellent transient response and to maintain a relatively constant switching frequency. The device utilizes Pulse Frequency Modulation (PFM) mode to maximize light−load efficiency by reducing switching frequency when the inductor is operating in discontinuous conduction mode at light loads.

Switching frequency and over−current protection can be programmed to provide a flexible solution for various applications. Output over−voltage, under−voltage, over−current, and thermal shutdown protections help prevent damage to the device during fault conditions. After thermal shutdown is activated, a hysteresis feature restarts the device when normal operating temperature is reached.

Features

- VIN Range: 4.5 V to 18 V
- High Efficiency: Over 96% Peak
- Continuous Output Current: 25 A
- Internal Linear Bias Regulator
- Accurate Enable facilitates VIN UVLO Functionality
- PFM Mode for Light−Load Efficiency
- Excellent Line and Load Transient Response
- Adjustable internal ripple injection
- No DC offset due to ripple injection
- Precision Reference: ±0.5%
- Output Voltage Range: 0.8 V to 5 V
- Programmable Frequency: 200 kHz to 2 MHz
- Programmable Soft−Start
- Low Shutdown Current
- Internal Boot Diode
- Thermal Shutdown
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Servers
- Desktop Computers, Notebooks, Gaming
- Telecommunications
- Storage

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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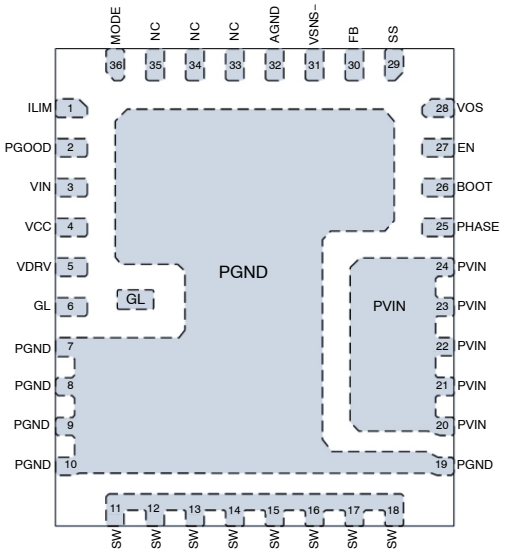
MARKING DIAGRAM

PackageName
SUFFIX
CASE TBD

xx	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

PINOUT



ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

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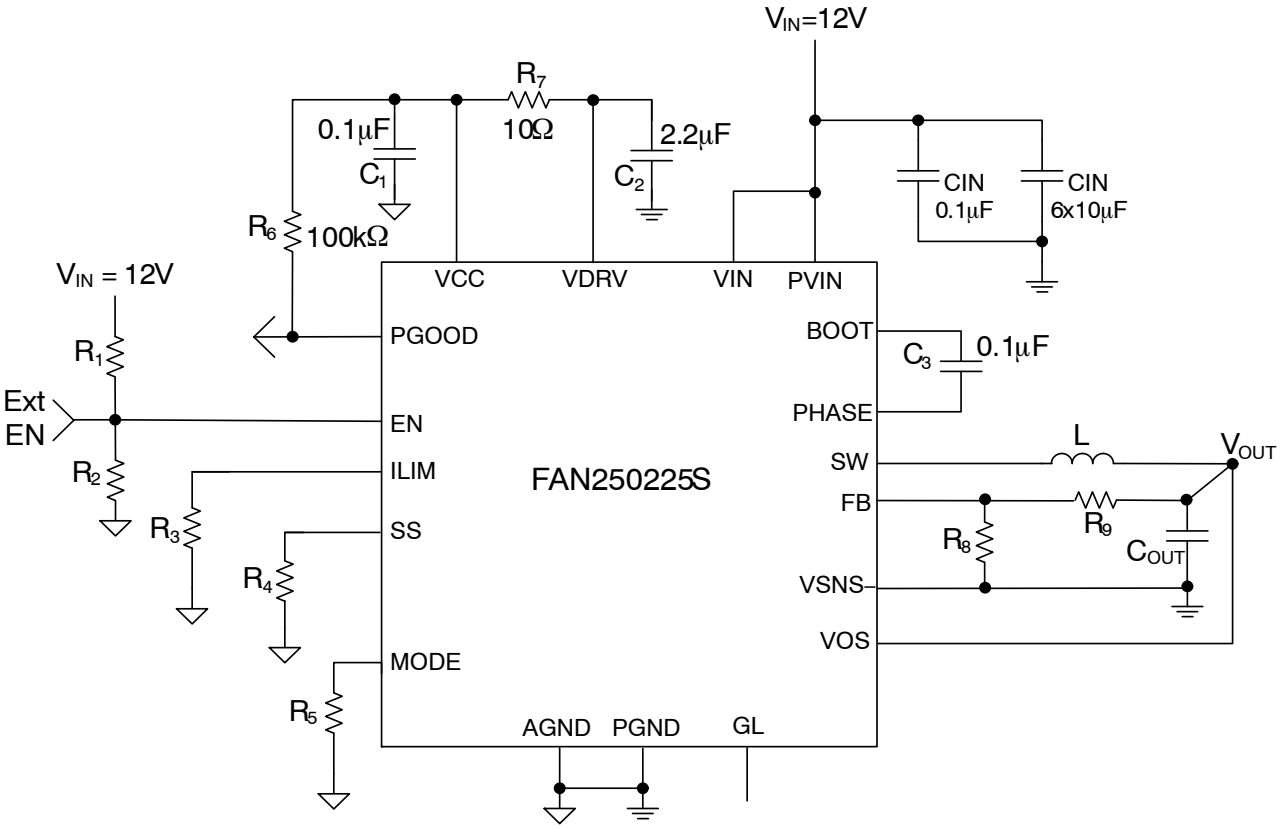

Figure 1. Simplified Application Circuit

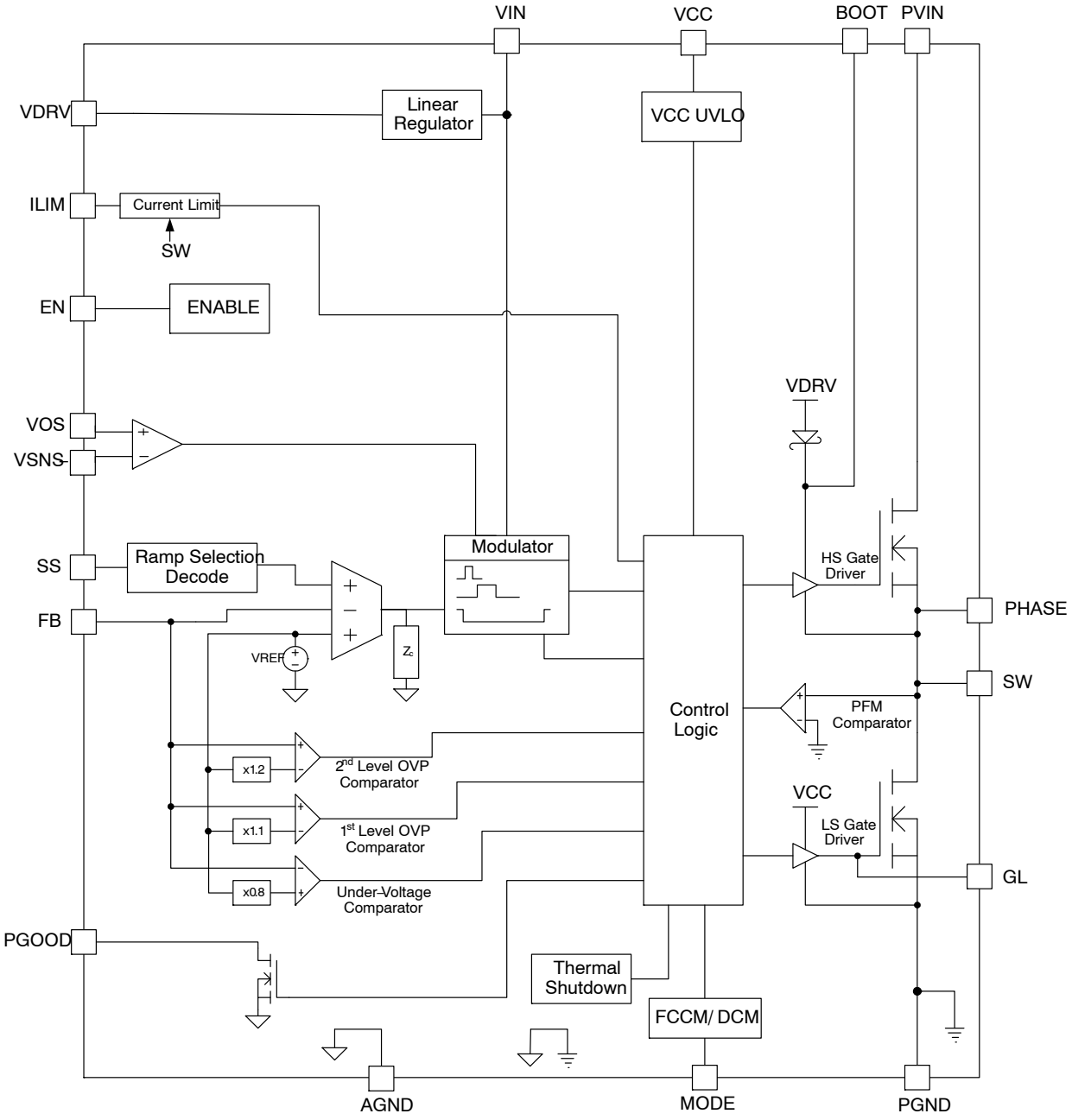

Figure 2. Functional Block Diagram

PIN CONFIGURATION

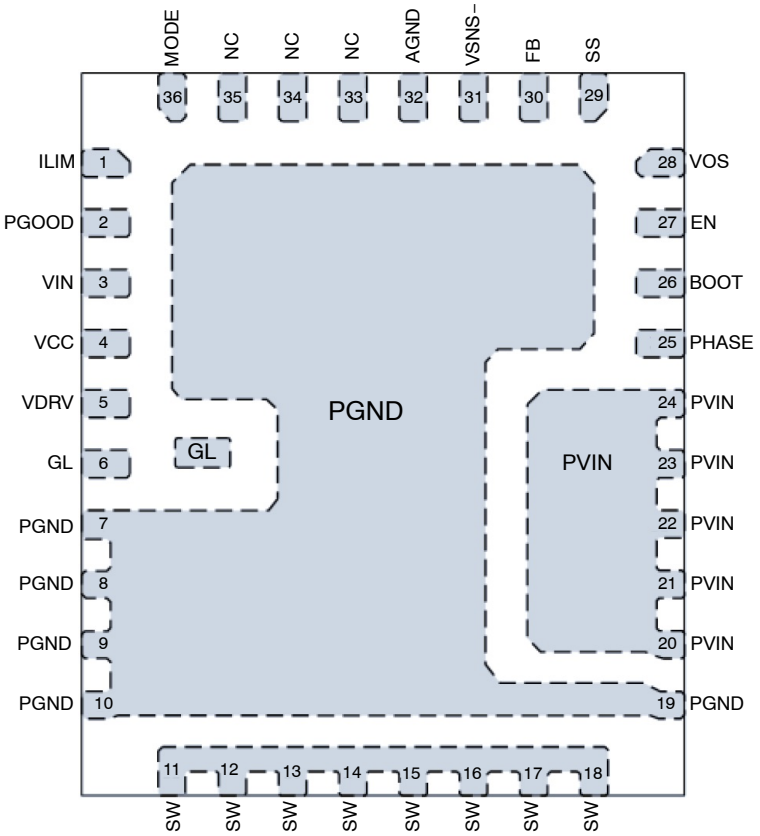

Figure 3. Pin Assignment, Top Transparent View (5x6 mm, 0.5 mm pin pitch)

Table 1. PIN DESCRIPTION

Pad / Pin	Name	Type	Description
1	ILIM	I/O	Current limit programming pin. A resistor between this pin and AGND to set the current limits, based on 4 different setting, described in Table 10, page 12.
2	PGOOD	I/O	Power Good; Open−drain output provides a logic high valid power good output signal, indicating VOUT is within set limits.
3	VIN	Power	Power supply input pin of internal 5V LDO. A ceramic capacitors must bypass this input to power ground. The capacitors should be placed as close as possible to this pin.
4	VCC	Power	Supply Voltage Input of Controller. A ceramic capacitor bypasses this Input to GND. This capacitor should be placed as close as possible to this pin.
5	VDRV	Power	Output of LDO and Supply Voltage Input of Gate Drivers. Output of integrated 5.0V LDO and power supply input pin of gate drivers. A 2.2μF or larger ceramic capacitor bypasses this input to PGND. This capacitor should be placed as close as possible to this pin.
6	GL	I/O	Low side MOSFET gate connection.
7−10, 19	PGND	Ground	These pins are the power supply ground pins of the device, which are connected to source of internal low−side power MOSFET. Must be connected to the system ground.
11−18	SW	Power	Switching node; junction between high−and low−side MOSFETs. Pins to be connected to an external inductor.
20−24	PVIN	Power	Power Supply Input. These pins are the power supply input pins of the device, which are connected to drain of internal high−side power MOSFET. A 22 μF or more ceramic capacitors must bypass this input to PGND. The capacitors should be placed as close as possible to these pins.
25	PHASE	Power	Phase Node. Provides a return path for integrated high−side gate driver and the boot capacitor. It is internally connected to source of high−side MOSFET.
26	BOOT	Power	Bootstrap. Supply for high−side MOSFET gate driver. A capacitor from BOOT to PHASE supplies the charge to turn on the N−channel high−side MOSFET. During the freewheeling interval (low−side MOSFET on), the high−side capacitor is recharged by an internal diode connected to VCC.
27	EN	I/O	Accurate enable. Connect to digital signal to enable the device, or use a resistor divider from VIN to set the UVLO.
28	VOS	I/O	Voltage Sense. Direct voltage sense for output voltage feed−forward.
29	SS	I/O	Soft start programming pin. A resistor between this pin and GND to program the soft−start slew rate and ramp options described in Table 9, page 11.
30	FB	I/O	Feedback. Output voltage feedback to the error amplifier and modulator.
31	VSNS−	I/O	Voltage Sense Negative Input. Connect this pin to remote voltage negative sense point.
32	AGND	Ground	Analog Ground. Ground of controller. Must be connected to the system ground.
33−35	NC	_	No Connection
36	MODE	I/O	Mode and Frequency Set. A resistor between this pin and AGND to program operation mode and nominal switching frequency options described in Table 8, page 10.

Table 2. ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Conditions	Min	Max	Unit
V_{PVIN}	Power Input	Referenced to GND	−0.3	25.0	V
V_{IN}	Modulator Input	Referenced to GND	−0.3	25.0	V
V_{SW}	SW Voltage to GND	Referenced to GND	−1	25	V
		Referenced to GND < 20 ns	−5	25	V
V_{BOOT}	Boot to SW Voltage	Referenced to SW	−0.3	6.0	V
	Boot to PGND	Referenced to GND	−0.3	30	V
V_{VCC}	Controller Supply Input	Referenced to GND	−0.3	6.0	V
V_{FB}	Output Voltage Feedback	Referenced to GND	−0.3	6.0	V
V_{PGOOD}	Power Good Output	Referenced to GND	−0.3	6.0	V
V_{OS}	Positive Output Sense	Referenced to GND	−0.3	6.0	V
V_{SNS-}	Negative Output Sense	Referenced to GND	−0.3	0.3	V
V_{EN}	Enable Pin	Referenced to GND	−0.3	6.0	V
V_{MODE}	Mode Pin	Referenced to GND	−0.3	6.0	V
V_{ILIM}	Current Limit Set Pin	Referenced to GND	−0.3	6.0	V
V_{SS}	Soft Start Pin	Referenced to GND	−0.3	6.0	V
ESD	Electrostatic Discharge	Human Body Model, JESD22−A114		2000	V
		Charged Device Model, JESD22−C101		500	V
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature		−55	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the data sheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	Power Input	Referenced to GND	4.5	18	V
T_J	Junction Temperature		−40	+125	°C
I_{LOAD}	Continuous Load Current	T_A = 85°C, No Airflow, on demonstration board		25	A
V_{OUT}	Output Voltage		0.8	5	V

Table 4. THERMAL CHARACTERISTICS

The thermal characteristics were evaluated on a 6−layer pcb structure (TBD oz) measuring 7 cm x 7 cm).

Symbol	Parameter	Typ	Unit
Θ_{JA}	Thermal Resistance, Junction−to−Ambient	TBD	°C/W
ψ_{JC}	Thermal Characterization Parameter, Junction−to−Top of Case	TBD	°C/W
ψ_{JPCB}	Thermal Characterization Parameter, Junction−to−PCB	TBD	°C/W

Table 5. ELECTRICAL CHARACTERISTICS

Unless otherwise noted; V_{IN}=12 V, V_{OUT}=1.2 V, and $T_A = T_J$ = −40 to +125°C.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SUPPLY CURRENT						
$I_{VIN,Q,SLEEP}$	Shutdown Current	EN=0 V		1.6	4	μA
$I_{VIN,Q,OFF}$	Quiescent Current, No Switching	EN=5 V, FB = 0.84V		300	450	μA
$I_{VIN,Q,ON}$	Quiescent Current, Switching	EN=5 V, f_{SW}=600 kHz		22		mA
LINEAR REGULATOR						
V_{REG}	Regulator Output Voltage		4.75	5.00	5.25	V
I_{REG}	Regulator Current Limit		60			mA
$V_{DROPOUT}$	Regulator Drop Out Voltage	$I_{LDO} \leq$ 60mA			0.4	V
$V_{SWTOLDO}$	Threshold voltage above which LDO is in LDO mode	VIN is rising		5.5		V
$V_{LDOTOSW}$	Threshold voltage below which LDO is in Switch mode	VIN is falling		5.3		V
REFERENCE						
V_{FB}	FB Voltage Trip Point	−10°C ≤ T_J ≤ 105°C	796	800	804	mV
			792	800	808	
I_{FB}	FB Pin Bias Current		−100	0	100	nA
MODULATOR						
t_{ON}	On−Time Accuracy		−20		20	%
$t_{ON,MIN}$	Minimum On−Time				50	ns
$t_{OFF,MIN}$	Minimum SW Off−Time		250	310	375	ns
MODE PIN FREQUENCY SETTING						
$f_{sw,1}$	Switching frequency setting for FCCM	MODE pin Resistor to GND=0 (GND)		600		kHz
$f_{sw,2}$		MODE pin Resistor to GND=Floating		800		kHz
$f_{sw,3}$		MODE pin Resistor to GND=2.49 kΩ		1000		kHz
$f_{sw,1}$	Switching frequency setting for DCM	MODE pin Resistor to GND=10.2 kΩ		600		kHz
$f_{sw,2}$		MODE pin Resistor to GND= 12.1 kΩ		800		kHz
$f_{sw,3}$		MODE pin Resistor to GND=14 kΩ		1000		kHz
SOFT−START SETTING AND RAMP SELECTION						
t_{SS1}	Ramp1	SS pin Resistor to GND=0 (GND)		1		ms
t_{SS2}		SS pin Resistor to GND=1.5 kΩ		2		ms
t_{SS3}		SS pin Resistor to GND=Floating		4		ms
t_{SS4}		SS pin Resistor to GND=3.48 kΩ		8		ms

Table 5. ELECTRICAL CHARACTERISTICS

Unless otherwise noted; V_{IN}=12 V, V_{OUT}=1.2 V, and $T_A = T_J$ = −40 to +125°C.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SOFT−START SETTING AND RAMP SELECTION						
t_{SS1}	Ramp2	SS pin Resistor to GND=4.53 kΩ		1		ms
t_{SS2}		SS pin Resistor to GND=5.76 kΩ		2		ms
t_{SS3}		SS pin Resistor to GND=8.66 kΩ		8		ms
CURRENT LIMIT						
$K_{ILIM,PEAK}$	Current Limit Set Factor			0.518		A/kΩ
$I_{LIM,PEAK,ACC}$	Peak (High Side) Current Limit Accuracy	I_{PEAK}=33 A	−20		20	%
$I_{LIM,VALLEY,ACC}$	Valley (Low Side) Current Limit Accuracy	I_{PEAK}=33 A	−20		20	%
$I_{LIM,NEG,ACC}$	Negative (Low Side) Current Limit Accuracy	I_{PEAK} = 33 A	−20		20	%
$K_{PEAK, VALLEY}$	Peak to Valley Current Limit Ratio			125		%
$K_{NEG, VALLEY}$	Negative to Valley Current Limit Ratio			100		%
$K_{PEAK2, VALLEY}$	Peak 2 to Valley Current Limit Ratio			160		%
ZERO−CROSSING DETECTION COMPARATOR						
I_{ZCD}	DC ZCD Current limit trip	$T_A = T_J$ = 25°C		800		mA
ENABLE						
$V_{EN,TH}$	EN/UVLO High Level	EN/UVLO Rising	1.172	1.22	1.268	V
$V_{EN,HYS}$	EN/UVLO Hysteresis	EN/UVLO Falling		115		mV
R_{PD}	EN/UVLO Internal Pull Down Resistance			500		kΩ
V_{EN_CLP}	Enable Clamp Voltage			2.5		V
R_{EN_CLP}	EN/UVLO Clamp Resistance			200		kΩ
I_{EN_CLP}	EN/UVLO Clamp Current	V_{EN} = 2.5 V		22		μA
UVLO						
$V_{IN,UVLO}$	V_{IN} UVLO Threshold Rising			4.0	4.3	V
$V_{IN,UVLO, HYS}$	V_{IN} UVLO Hysteresis Voltage			200		mV
$V_{CC,UVLO}$	V_{CC} UVLO Threshold Rising			4.0	4.3	V
$V_{CC,UVLO, HYS}$	V_{CC} UVLO Hysteresis Voltage			200		mV
THERMAL SHUTDOWN						
T_{OFF}	Thermal Shutdown Trip Point (Note 1)			155		°C
T_{HYS}	Hysteresis[2]			20		°C
INTERNAL BOOTSTRAP DIODE						
$V_{F,BOOT}$	Forward Voltage	I_F = 50 mA		0.1	0.3	V
$V_{R,BOOT}$	Breakdown Voltage	I_R = 1 mA			30	V
$V_{BT,UVLO}$	Bootstrap voltage UVLO Falling		2.9	3.2		V
$V_{BT,UVLO,HYS}$	Bootstrap voltage UVLO Hysteresis			350		mV
OUTPUT VOLTAGE PROTECTION						
$V_{FB,UV}$	FB UV Fault Threshold			80		%
$V_{FB,OV1}$	FB OV1 Fault Threshold			110		%

Table 5. ELECTRICAL CHARACTERISTICS

Unless otherwise noted; V_{IN}=12 V, V_{OUT}=1.2 V, and $T_A = T_J$ = −40 to +125°C.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
OUTPUT VOLTAGE PROTECTION						
$V_{FB,OV1,HYS}$	FB OV1 Fault Hysteresis			5		%
$V_{FB,OV2}$	FB OV2 Fault Threshold			120		%
POWER GOOD						
V_{PGOOD}	PGOOD Pull−Down Voltage	I_{PGOOD} = 1 mA		6	10	mV
$t_{PG,DELAY}$	PGOOD Assert Delay			500		μs
$t_{PG,FLT}$	PGOOD De−Glitch Filter			5		μs
$I_{PG,LEAK}$	PGOOD Leakage Current				1	μA
$V_{FBUVPG,FALL}$	PGOOD De−asserted Point	FB Falling		92		%
$V_{FBUVPG,RISE}$	PGOOD Asserted Point	FB Rising		94		%
t_{HIC}	Hiccup Time			1		s

1. Guaranteed by design; not production tested.
2. Device is 100% production tested at T_A=25°C. Limits over that temperature are guaranteed by design.

Table 6. TYPICAL PERFORMANCE CHARACTERISTICS

Tested using evaluation board circuit shown in TBD, with V_{IN}=12 V, T_A = 25°C, and no airflow; unless otherwise specified.

Table 7. FAULT CONDITION

Fault Condition	Fault Response	Relevant Limits
Peak Over Current	Terminate high side on time, turn on low side for at least min−off time and valley over current needs to clear	KPEAK,PEAK
Gross Peak Over Current	Hiccup, pull down on power good flag	KPEAK,PEAK2
Valley Over Current	Prohibit high side on time until valley over current clears	KPEAK,VALLEY
Negative Over Current	Turn off low side until 2nd rising edge of internal 250 kHz clock.	KPEAK,NEG
VOUT Over Voltage 1	Turn off both FETs until fault clears, pull down power good flag	VFB,OV1; VFB OV1,HYS
VOUT Over Voltage 2	Turn on the low side FET until VFB < VREF (Negative Over Current still engaged), Hiccup, Turn on Low side during Hiccup if VOUT OV2 limit is reached, pull down power good flag	VFB,OV2
Power Not Good	Pull down on power good flag	VFBUVPG,FALL; VFBUVPG,RISE
VOUT Under Voltage	Hiccup, pull down on power good flag	VFB,UV
OTP	Turn off until OTP is cleared, restart immediately	TOFF; THYS
VIN Under Voltage	Turn off until UVLO is cleared, restart immediately	VIN,UVLO; VIN,UVLO, HYS
VCC Under Voltage	Turn off until UVLO is cleared, restart immediately	VCC,UVLO; VCC,UVLO,HYS
VBOOT Under Voltage	Terminate high side on time, turn on low side to refresh	VBT,UVLO; VBT,UVLO, HYS
LG Pin Fault	Hiccup	
Soft Start High at Startup	Hiccup	
Soft Start Not Good	Hiccup	VFBUVPG,RISE
Switch Node Short	Hiccup	

Circuit Operation

The FAN250225S uses a constant on−time modulation architecture with a V_{IN} feed−forward input to accommodate a wide V_{IN} range. This method provides fixed switching frequency (f_{SW}) operation when the inductor operates in Continuous Conduction Mode (CCM) and variable frequency when operating in Pulse Frequency Mode (PFM) at light loads (depending on the state of the mode pin). Additional benefits include excellent line and load transient response, cycle−by−cycle current limiting, and no external loop compensation is required.

At the beginning of each cycle, FAN250225S turns on the high−side MOSFET (HS) for a fixed duration (t_{ON}). At the end of t_{ON}, HS turns off for a duration (t_{OFF}) determined by the operating conditions. Once the FB voltage (V_{FB}) falls below the reference voltage (V_{REF}), a new switching cycle begins.

The modulator provides a minimum off−time ($t_{OFF−MIN}$) of 320 ns to provide a guaranteed interval for low−side MOSFET (LS) current sensing and PFM operation. $t_{OFF−MIN}$ is also used to provide stability against multiple pulsing and limits maximum switching frequency during transient events.

Enable (EN)

The enable pin can be driven with an external logic signal, connected to a resistive divider from PVIN/Vin to ground to create an Under−Voltage Lockout (UVLO) based on the PVIN/VIN supply, or connected to PVIN/VIN through a single resistor to auto−enable while operating within the EN pin internal clamp current sink capability.

To implement the UVLO function based on PVIN/VIN voltage level, select values for R1 and R2 in Figure 1 such that the tap point reaches 1.26 V when V_{IN} reaches the desired startup level using the following equation:

$$R1 = R2\left(\frac{V_{IN,on}}{V_{EN,on}} - 1\right) \qquad \text{(eq. 1)}$$

where $V_{IN,on}$ is the input voltage for startup and $V_{EN,on}$ is the EN pin rising threshold of 1.26 V.

Also, the EN pin can be directly driven by logic voltages of 5 V, 3.3 V, 2.5 V, etc. If the EN pin is driven by 5 V logic, a small current flows into the pin when the EN pin voltage exceeds the internal clamp voltage of 4.3 V. To eliminate clamp current flowing into the EN pin use a voltage divider to limit the EN pin voltage to < 4 V.

The EN pin can be pulled high with a single resistor connected from VIN to the EN pin. With VIN > 5.5 V a series resistor is required to limit the current flow into the EN pin clamp to less than 22 μA to keep the internal clamp within normal operating range. The resistor value can be calculated from the following equation:

$$R_{EN} > \frac{V_{IN,max} - V_{EN\_,Clamp,min}}{22\ \mu A} \qquad \text{(eq. 2)}$$

Constant On−Time Modulation

The FAN250225S uses a constant on−time modulation technique, in which the HS MOSFET is turned on for a fixed time, set by the modulator, in response to the input voltage and the frequency setting. This on−time is proportional to the desired output voltage, divided by the input voltage. With this proportionality, the frequency is essentially constant over the load range where inductor current is continuous.

For buck converter in Continuous−Conduction Mode (CCM), the switching frequency f_{SW} is expressed as:

$$f_{SW} = \frac{V_{OUT}}{V_{IN} \cdot t_{ON}} \qquad \text{(eq. 3)}$$

The on−time generator sets the on−time (t_{ON}) for the high−side MOSFET, which results in the switching frequency of the regulator during steady−state operation. To maintain a relatively constant switching frequency over a wide range of input conditions, the input voltage information is fed into the on−time generator.

Soft−Start (SS)

A conventional soft−start ramp is implemented to provide a controlled startup sequence of the output voltage. A resistor between this pin and GND is used to program the soft−start slew rate and ramp options described in Table 8.

Table 8. SS PIN DEFINITION

	SS Pin to GND Resistor (kΩ)	SS time (ms)	Ramp Selection
0	GND	1	Ramp1
1	1.5	2	
2	3.48	8	
3	4.53	1	Ramp2
4	5.76	2	
5	8.77	8	
6	Floating	4	Ramp1

Startup on Pre−Bias

FAN250225S allows the regulator to start on a pre−bias output, V_{OUT}, and ensures V_{OUT} is not discharged during the soft−start operation.

To guarantee no glitches on V_{OUT} at the beginning of the soft−start ramp, the LS is disabled until the first positive−going edge of the PWM signal. The regulator is also forced into PFM Mode during soft−start to ensure the inductor current remains positive, reducing the possibility of discharging the output voltage.

Internal Linear Regulator

The FAN250225S includes a linear regulator to facilitate single−supply operation for self−biased applications.

VDRV is the linear regulator output and supplies power to the internal gate drivers. The VDRV pin should be bypassed with a 2.2 μF ceramic capacitor. The device can operate from a 5 V rail if the V_{IN}, P_{VIN}, and VDRV pins are connected together to bypass the internal linear regulator.

V_{CC} Bias Supply and UVLO

The V_{CC} rail supplies power to the controller. It is generally connected to the VDRV rail through a low−pass filter of a 10 Ω resistor and 0.1 μF capacitor to minimize any noise sources from the driver supply.

An Under−Voltage Lockout (UVLO) circuit monitors the V_{CC} voltage to ensure proper operation. Once the V_{CC} voltage is above the UVLO threshold, the part begins operation after an initialization routine of 50 μs. There is no UVLO circuitry on either the VDRV or V_{IN} rails.

Protection Features

The converter output is monitored and protected against over−current, over−voltage, under−voltage, and high−temperature conditions.

Over−Current Protection (OCP)

The FAN250225S uses current information through the LS to implement valley−current limiting. While an OC event is detected, the HS is prevented from turning on and the LS is kept on until the current falls below the user−defined set point. Once the current is below the set point, the HS is allowed to turn on.

During an OC event, the output voltage may droop if the load current is greater than the current the converter is providing. If the output voltage drops below the UV threshold, the device will shut down.

The ILIM pin has an open and short detection circuit to provide protection against operation without a current limit.

Under−Voltage Protection (UVP)

If V_{FB} is below the under−voltage threshold and < 80% of V_{REF} (640 mV), the part enters UVP and PGOOD pulls LOW.

Over−Voltage Protection (OVP)

There are two levels of OV protection: +10% and +20%. During an OV event, PGOOD pulls LOW.

When V_{FB} is > 110% of V_{REF} (880 mV), both HS and LS turn off. By turning off the LS during an OV event, V_{OUT} overshoot can be reduced when there is positive inductor current by increasing the rate of discharge. Once the V_{FB} voltage falls below V_{REF}, the latched OV signal is cleared and operation returns to normal.

A second over−voltage detection is implemented to protect the load from more serious failure. When V_{FB} is > 120% of V_{REF} (960 mV), the HS turns off and the LS is forced on until 100% of V_{REF} and device enters into latch−off mode until a power cycle on VCC.

Over−Temperature Protection (OTP)

FAN250225S incorporates an over−temperature protection circuit that disables the converter when the controller die temperature reaches 155°C. The IC restarts when the die temperature falls below 140°C.

Power Good (PGOOD)

The PGOOD pin serves as an indication to the system that the output voltage of the regulator is stable and within regulation. Whenever V_{OUT} is outside the regulation window or the regulator is at over−temperature (UV, OV, and OT), the PGOOD pin is pulled LOW.

PGOOD is an open−drain output that asserts LOW when V_{OUT} is out of regulation or when OT is detected.

Application Information

5 V VDRV

The VDRV is the output of the internal regulator that supplies power to the drivers and V_{CC}. It is crucial to keep this pin decoupled to PGND with a ≥1 μF X5R or X7R ceramic capacitor. Because V_{CC} powers internal analog circuit, it is filtered from VDRV with a 10 Ω resistor and 0.1 μF X7R decoupling ceramic capacitor to AGND.

Setting the Output Voltage (V_{OUT})

The output voltage V_{OUT} is regulated by initiating a high−side MOSFET on−time interval when the valley of the divided output voltage appearing at the FB pin reaches V_{REF}. Since this method regulates at the valley of the output ripple voltage, the actual DC output voltage on V_{OUT} is offset from the programmed output voltage by the average value of the output ripple voltage. The initial V_{OUT} setting of the regulator can be programmed from 0.6 V to 5.5 V by an external resistor divider (R8 and R9):

$$R8 = \frac{R9}{\left(\frac{V_{OUT}}{V_{REF}}\right) - 1} \qquad \text{(eq. 4)}$$

where V_{REF} is 800 mV.

For example; for V_{OUT}= 1.6 V and 10 kΩ R9, then R8 is 10 kΩ. For V_{OUT}= 800 mV, R8 is left open.

Setting (f_{SW}) with Mode Pin

A resistor between Mode pin and AGND sets operation mode and nominal switching frequency (fsw) options as described in Table 9.

Table 9. MODE PIN DEFINITION AND FSW SETTING

	Mode Pin (Resistor to GND)	Frequency (kHz)	FCCM/DCM
0	GND	600	FCCM
1	Floating	800	
2	2.49K	1000	
3	10.5K	600	DCM
4	12.1K	800	
5	14K	1000	

Inductor Selection

The inductor is typically selected based on the ripple current (ΔI_L), which is usually selected as 25% to 45% of the maximum DC load. The inductor current rating should be selected such that the saturation and heating current ratings exceed the intended currents encountered in the application over the expected temperature range of operation. Regulators that require fast transient response use smaller inductance and higher current ripple; while regulators that require higher efficiency keep ripple current on the low side. The inductor value is given by:

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I_L \cdot f_{SW}} \cdot \frac{V_{OUT}}{V_{IN}} \quad \text{(eq. 5)}$$

Input Capacitor Selection

Input capacitor C_{IN} is selected based on voltage rating, RMS current $I_{CIN(RMS)}$ rating, and capacitance. For capacitors having DC voltage bias de−rating, such as ceramic capacitors, higher rating is strongly recommended. RMS current rating is given by:

$$I_{CIN(RMS)} = I_{LOAD-MAX} \cdot \sqrt{D \cdot (1 - D)} \quad \text{(eq. 6)}$$

where $I_{LOAD-MAX}$ is the maximum load current and D is the duty cycle V_{OUT}/V_{IN}. The maximum $I_{CIN(RMS)}$ occurs at 50% duty cycle.

The capacitance is given by:

$$C_{IN} = \frac{I_{LOAD-MAX} \cdot D \cdot (1 - D)}{f_{SW} \cdot \Delta V_{IN}} \quad \text{(eq. 7)}$$

where ΔV_{IN} is the input voltage ripple, normally 1% of V_{IN}.

Select six 10 μF 25 V−rated ceramic capacitors with X7R or similar dielectric, recognizing that the capacitor DC bias characteristic indicates that the capacitance value falls approximately 40% at V_{IN}=12 V, with a resultant small increase in ΔV_{IN} ripple voltage above 120 mV used in the calculation. Also, each 10 μF can carry over 3 A_{RMS} in the frequency range from 100 kHz to 1 MHz, exceeding the input capacitor current rating requirements. An additional 0.1 μF capacitor may be needed to suppress noise generated by high frequency switching transitions.

Output Capacitor Selection

Output capacitor C_{OUT} is selected based on voltage rating, RMS current $I_{COUT(RMS)}$ rating, and capacitance. For capacitors having DC voltage bias de−rating, such as ceramic capacitors, higher rating is highly recommended. When calculating C_{OUT}, usually the dominant requirement is the current load step transient. If the unloading transient requirement (I_{OUT} transitioning from HIGH to LOW), is satisfied, then the load transient (I_{OUT} transitioning LOW to HIGH), is also usually satisfied. The unloading C_{OUT} calculation, assuming C_{OUT} has negligible parasitic resistance and inductance in the circuit path, is given by:

$$C_{OUT} = L \cdot \frac{I^2_{MAX} - I^2_{MAX}}{(V_{OUT} + \Delta V_{OUT})^2 - V^2_{OUT}} \quad \text{(eq. 8)}$$

where I_{MAX} and I_{MIN} are maximum and minimum load steps, respectively and ΔV_{OUT} is the voltage overshoot, usually specified at 3 to 5%.

Setting the Current Limit

Current limit is implemented by sensing the inductor valley current across the LS MOSFET V_{DS} during the LS on−time. The current limit comparator prevents a new on−time from being started until the valley current is less than the current limit.

The set point is configured by connecting a resistor from the ILIM pin to AGND as described in Table 10.

Table 10. ILIM PIN WITH 4 SETTING

(T_J = 25°C, V_{CC} = 5 V)

	RLIM Resistor to AGND (kΩ)	OCP (A)
0	36.5	19
1	51.1	26
2	63.4	33
3	75	39

Current ripple ΔI_L is given by:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \cdot t_{ON}}{L} \quad \text{(eq. 9)}$$

From the equation above, the worst−case ripple occurs during an output short circuit (where V_{OUT} is 0 V). This should be taken into account when selecting the current limit set point.

The FAN250225S uses valley−current sensing; the current limit (I_{ILIM}) set point is the valley (I_{VALLEY}).

The valley current level for calculating R_{ILIM} is given by:

$$I_{VALLEY} = I_{LOAD(CL)} - \frac{\Delta I_L}{2} \quad \text{(eq. 10)}$$

where $I_{LOAD\ (CL)}$ is the DC load current when the current limit threshold is reached.

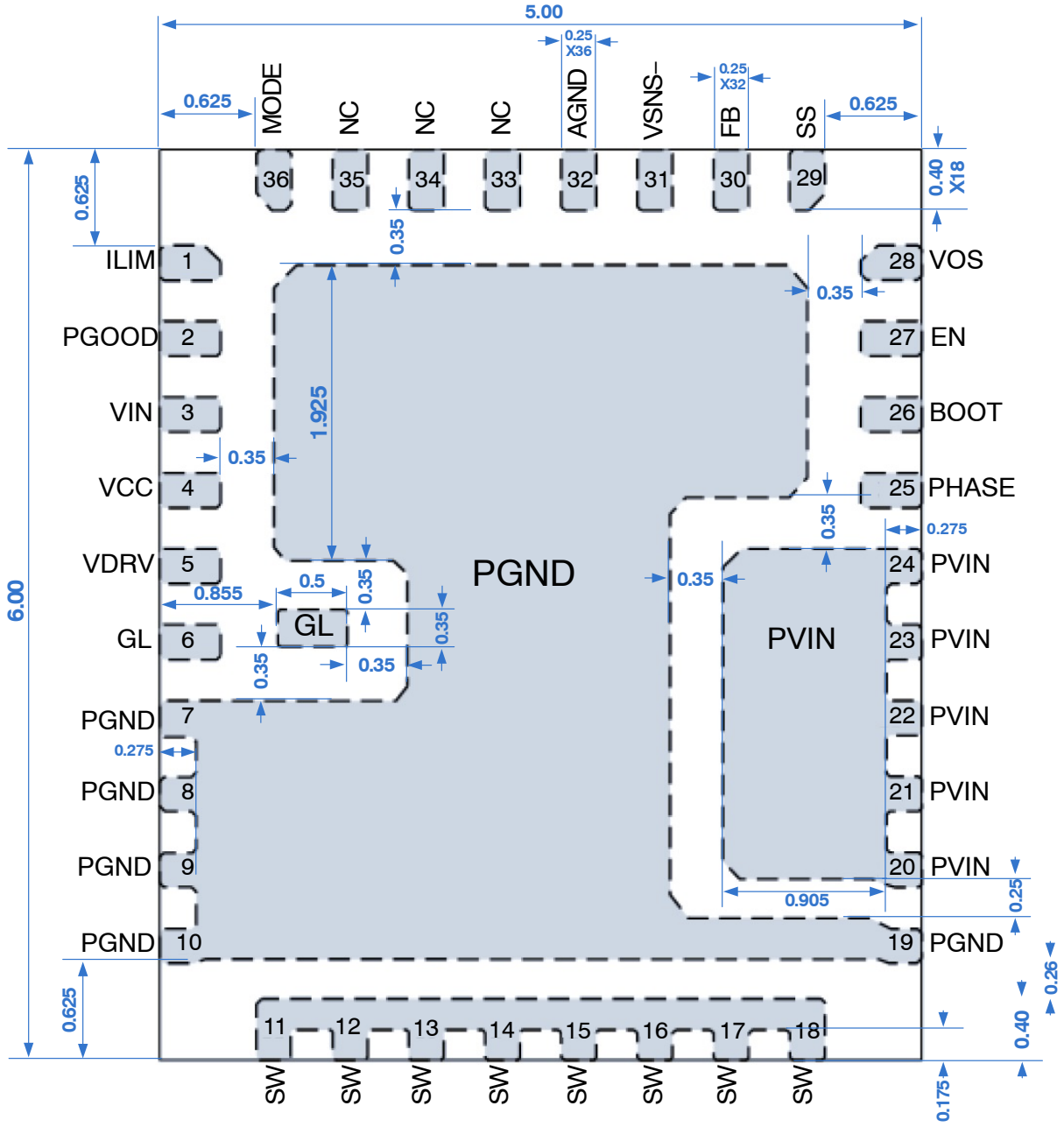

Figure 4. Package

ORDERING INFORMATION

Device	Current	Marking	Package	Shipping†
FAN250225S	25 A	TBD	PQFN34 5 x 6 mm (Pb−Free)	TBD / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FAN250225S

PACKAGE DIMENSIONS

PQFN34
CASE TBD
ISSUE TBD

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