FAN6292CMX

Secondary Side Synchronous Rectifier Controller for Flyback Converters

ON Semiconductor®

www.onsemi.com

SOIC8
CASE 751EB

Descriptions

The FAN6292CMX is a secondary−side synchronous rectifier (SR) controller for an isolated flyback converter operating in Discontinuous Conduction Mode (DCM). The adaptive dead time control algorithm minimizes the body diode conduction of SR MOSFET while guaranteeing stable and robust SR operation against noise and disturbance caused by the circuit parasitic.

When pair with FAN1080, PSR controller, FAN6292CMX can execute functions that are more valuable. Dynamic Response Enhancement (DRE) awakes primary controller quickly during load transient thus improves voltage dip.

FAN6292C are also source only USB Type−C controllers which are optimized for mobile chargers and power adapters. It supports standard 3 A VBUS current level is compatible as a load switch, and helps to reduce BOM cost.

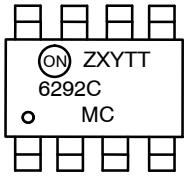
Features

- Support Discontinuous Conduction Modes (DCM) and Boundary Conduction Mode (BCM)
- Adaptive Turn−Off Dead Time Tuning for General SR MOSFET Application
- Turn−On Trigger Blanking Time (Minimum Gate OFF Time) for Improved Noise Immunity
- Dynamic Response Enhancement (DRE) Function to Improve System Dynamic Response
- Type−C Control for Standard 3 A VBUS Current Level
- N−Channel MOSFET Control as a Load Switch for USB Type−C
- Minimum Turn−On Delay (20 ns)
- Supporting General Output Voltage (VIN) Range : 3.25 V ~ 20 V for LDO Input
- Fewest External Component Allowed

Applications

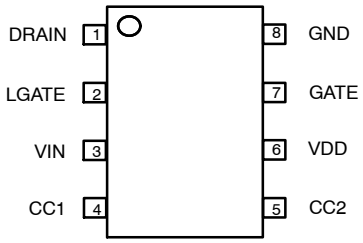
- Travel Adapter for Smart Phones, Feature Phones and Tablet PCs
- AC−DC Adapters for Portable Devices that Require CV/CC Control
- IoT Power Applications

MARKING DIAGRAM



Z	= Assembly Plant Code
X	= Year Code
Y	= Week Code
TT	= Die Run Code
6292C	= FAN6292C
M	= SOP
C	= Manufacture Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Operating Temperature	Package	Packing Method
FAN6292CMX	−40 to 85°C	8−Lead, SOIC (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

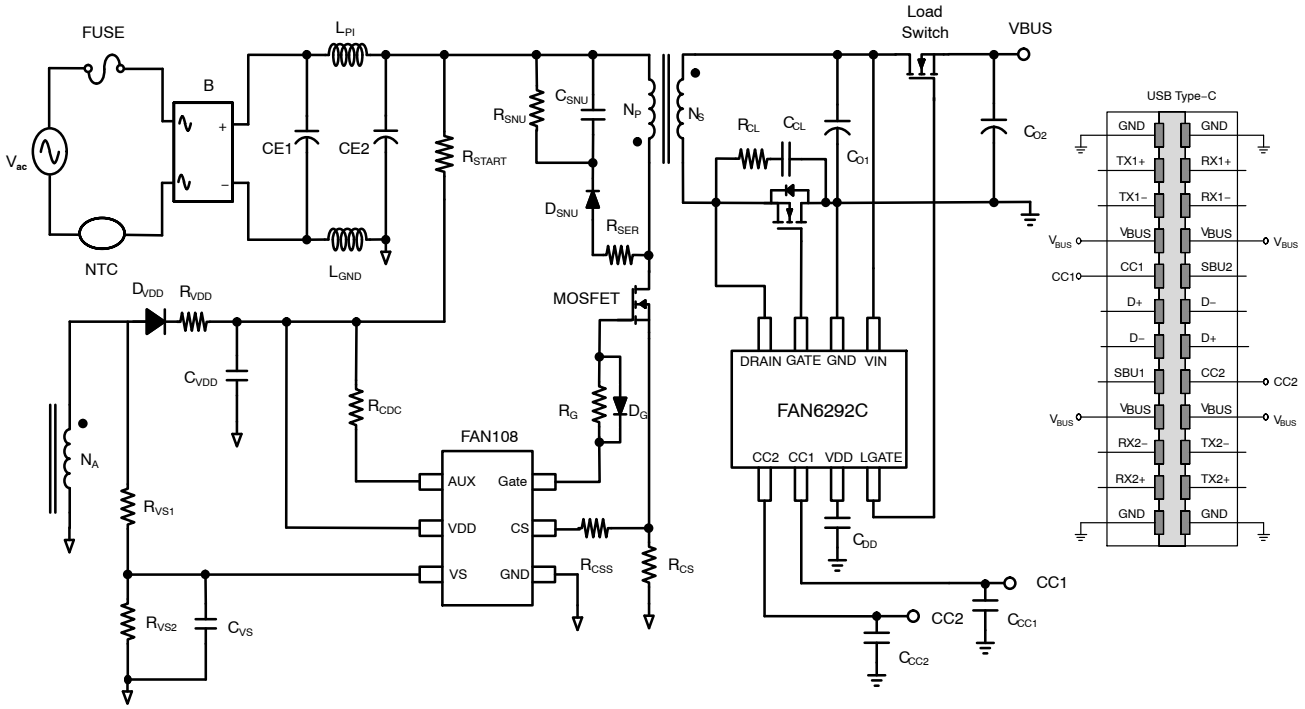


Figure 1. FAN6292C Typical Application Schematic

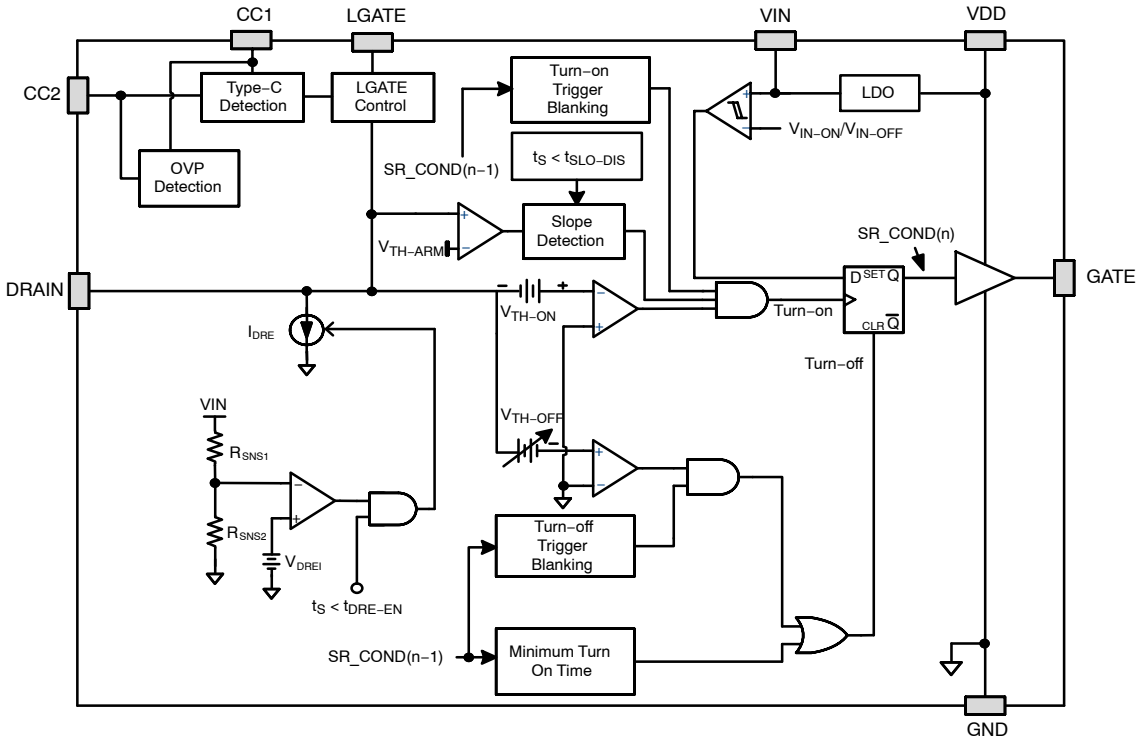


Figure 2. FAN6292C Function Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin #	Name	Description
1	DRAIN	**Synchronous rectifier drain sense input.**
2	LGATE	**Load switch controlling.**
3	VIN	**Input voltage pin.** This pin is connected to the output of the adaptor to monitor its output voltage and supply internal bias. IC operating current, and MOSFET gate drive current are supplied through this pin.
4	CC1	**Configuration Channel 1.** This pin is used to detect connections of Type−C cables and connectors. It is tied to the USB−C CC1.
5	CC2	**Configuration Channel 2.** This pin is used to detect connections of Type−C cables and connectors. It is tied to the USB−C CC2.
6	VDD	**Internal regulator 5 V output** and gate drive power supply rail. Bypass with 1uF capacitor to GND.
7	GATE	**Gate driver output.**
8	GND	**Ground.**

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	Power Supply Pin Voltage	−0.3 to 20	V
V_{DRAIN}	Drain Sense Pin Voltage	−1 to 65	V
V_{LGATE}	LGATE PIN Voltage	−0.3 to 20	V
V_{DD}	Internal Regulator Pin Voltage	−0.3 to 6.5	V
V_{GATE}	Gate Pin Voltage	−0.3 to 6.5	V
V_{CC1}	CC1 Pin Input Voltage	−0.3 to 6.0	V
V_{CC2}	CC2 Pin Input Voltage	−0.3 to 6.0	V
P_D	Power Dissipation (T_A = 25°C)	0.651	W
T_J	Operation Junction Temperature	−40 to 125	°C
T_{STG}	Storage Temperature Range	−60 to 150	°C
T_L	Lead Temperature (Soldering) 10 Seconds	260	°C
ESD	Electrostatic Discharge Capability − Charged Device Model (CDM)	0.5	kV
	Electrostatic Discharge Capability − Human Body Model (HBM)	2	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. All voltage values, except differential voltages, are given with respect to the GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. Meets JEDEC standards JS−001−2012 and JESD 22−C101.

Table 3. THERMAL CHARACTERISTICS

Symbol	Parameter	Min	Unit
θ_{JA}	Junction−to−Ambient Thermal Impedance	150.9	°C/W
θ_{JT}	Junction−to−Top Thermal Impedance	13.4	°C/W

4. T_A = 25°C unless otherwise specified.

Table 4. RECOMMENDED OPERATING RANGES

Symbol	Parameter	Min	Max	Unit
V_{DRAIN}	Drain Pin Voltage	−1	60	V
V_{IN}	VIN Pin Voltage	3.5	20	V
V_{LGATE}	LGATE Pin Voltage	0	19.5	V
V_{GATE}	GATE Pin Voltage	0	5.5	V

Table 4. RECOMMENDED OPERATING RANGES (continued)

Symbol	Parameter	Min	Max	Unit
V_{DD}	VDD Pin Voltage	3.1	5.5	V
V_{CC1}/V_{CC2}	CC1/CC2 Pin Voltage	0	5.8	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS

V_{IN} = 5.5 V and T_A = −40°C to 125°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VDD SECTION						
V_{IN-ON}	Turn−On Threshold	V_{IN} rising	3.06	3.15	3.25	V
V_{IN-OFF}	Turn−Off Threshold	V_{IN} falling	2.78	2.9	3.05	V
I_{IN-OP}	Operating Current	f_{SW} = 100 kHz, C_{GATE} = 3.3 nF, V_{IN} = 5 V		2.5	3.2	mA
POWER SUPPLY SECTION						
V_{DD}	Internal LDO Output Voltage	V_{IN} = 20 V	5.0	5.25	5.5	V
V_{DO}	Dropout Voltage of LDO	I_{OUT} = 10 mA, V_{IN} = 3.3 V			0.3	V
DRAIN VOLTAGE SENSING SECTION						
V_{OSI}	Comparator Input Offset Voltage (Note 5)	Internal Design Suggestion	−1	0	1	mV
V_{TH-ON}	Turn−On Threshold Voltage	R_{DRAIN} = 0 Ω (includes comparator input offset voltage)	−250	−200	−150	mV
$t_{SLO-DIS}$	Slope Detection Disable Criteria (Note 7)		53	58	63	μs
$t_{SLO-HYS}$	Slope Detection Disable Criteria Hysteresis (Note 5)			8		μs
t_{ON-DLY}	Turn On Delay (Note 5)	With 50 mV overdrive From V_{TH-ON} to Gate voltage over 1 V		20		ns
V_{TH-OFF}	Turn−Off Threshold Tuning Range		−5		5	mV
$t_{OFF-DLY}$	Comparator Delay for V_{TH-OFF} (Note 5)	With 0 mV overdrive From V_{TH-OFF} to Gate voltage equal 1 V		20		ns
V_{TH-ARM}	Gate Re−arming Threshold	VIN = 5 V (typically 0.7 V_{DD})	3.3	3.5	3.7	V
t_{ARM}	Gate Re−arming Time for Slope Detection (Note 5)		70	85	100	ns
V_{TH-HGH}	Slope Detection High Threshold (Note 5)		0.4	0.5	0.6	V
MINIMUM ON−TIME AND MINIMUM OFF−TIME SECTION						
t_{ON-MIN}	Minimum On−Time	$t_S < (t_{SLO-DIS} - t_{SLO-HYS})$	2.16	2.4	2.64	μs
$t_{ON-MIN-L}$	Minimum On−Time at Light Load	$t_S \geq t_{SLO-DIS}$	1.50	1.65	1.80	μs
$N_{ON-MIN-ST}$	Minimum t_{ON} Cycles during Start−up			3		Cycles
$t_{OFF-MIN-L}$	Minimum Off−Time (Note 6)	$t_S < (t_{SLO-DIS} - t_{SLO-HYS})$	1.53	1.70	1.87	μs
$t_{OFF-MIN-H}$	Minimum On−Time at Light Load (Note 6)	$t_S \geq t_{SLO-DIS}$	3.6	4	4.4	μs
DEAD TIME CONTROL SECTION						
t_{DEAD}	Dead Time Self−Tuning Target (Note 5)	From GATE OFF to V_{DRAIN} rising above 0.5 V	170	200	230	ns

Table 5. ELECTRICAL CHARACTERISTICS (continued)
V_{IN} = 5.5 V and T_A = −40°C to 125°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
TYPE−C SECTION						
$V_{LGATE-ON}$	Drain Pin Threshold Voltage for LGATE Turn On		6.8	7.5	8.2	V
I_{P-CC1}	Source Current on CC1 Pin	V_{IN} = 5 V, V_{CC1} = 0 V	304	330	356	μA
I_{P-CC2}	Source Current on CC2 Pin	V_{IN} = 5 V, V_{CC2} = 0 V	304	330	356	μA
$Z_{OPEN-CC1}$	Input Impedance on CC1 Pin		126			kΩ
$Z_{OPEN-CC2}$	Input Impedance on CC2 Pin		126			kΩ
V_{RA-CC1}	Ra Impedance Detection Threshold on CC1 Pin	V_{IN} = 5 V, V_{CC2} = 0 V, decreasing V_{CC1}	0.75	0.80	0.85	V
V_{RA-CC2}	Ra Impedance Detection Threshold on CC2 Pin	V_{IN} = 5 V, V_{CC1} = 0 V, decreasing V_{CC2}	0.75	0.80	0.85	V
V_{RD-CC1}	Rd Impedance Detection Threshold on CC1 Pin	V_{IN} = 5 V, V_{CC2} = 0 V, increasing V_{CC1}	2.45	2.60	2.75	V
V_{RD-CC2}	Rd Impedance Detection Threshold on CC2 Pin	V_{IN} = 5 V, V_{CC1} = 0 V, increasing V_{CC2}	2.45	2.60	2.75	V
$t_{CC-Detach-Debounce}$	UFP Detachment Debounce Time	V_{IN} = 5 V, V_{CC2} = 0 V, decreasing V_{CC1}	10	15	20	ms
$t_{CC-Attach-Debounce}$	UFP Attachment Debounce Time	V_{IN} = 5 V, V_{CC2} = 0 V, increasing V_{CC1}	100	150	200	ms
V_{INGATE}	LGATE High Voltage for Load Switch Control	V_{IN} = 5 V	8		11	V
DRE SECTION						
V_{DRE}	VIN Pin DRE Function Trigger Level (Note 6)	VIN = 5.5 V → 4.5 V	4.68	4.78	4.85	V
t_{DREI}	DRE Current Sinking Period (Note 5)	VIN = 5.5 V → 4.5 V	1.2	1.5	1.8	μs
t_{DRE-EN}	DRE Enable Period	VIN = 5.5 V → 4.5 V	64	72	80	μs
t_{RE-ARM}	DRE Re−arm Period	VIN = 5.5 V → 4.5 V		4		μs
I_{DRE}	DRE Sinking Current	Maximum I_{DRE} cycle are 14 every gate switching cycles	50			mA
OUTPUT DRIVER SECTION						
V_{OL}	Gate Low Voltage	V_{IN} = 6 V			0.25	V
V_{OH}	Gate High Voltage	V_{IN} = 6 V	4.9			V
t_R	Gate Rise Time	V_{IN} = 6 V, C_L = 3300 pF, GATE = 1 V → 4 V			90	ns
t_F	Gate Fall Time	V_{IN} = 6 V, C_L = 3300 pF, GATE = 4 V → 1 V			30	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
5. Guaranteed by Design.
6. Specification operation temperature range −5°C to 85°C.
7. Specification operation temperature range −5°C to 50°C.

TYPICAL PERFORMANCE CHARACTERISTICS

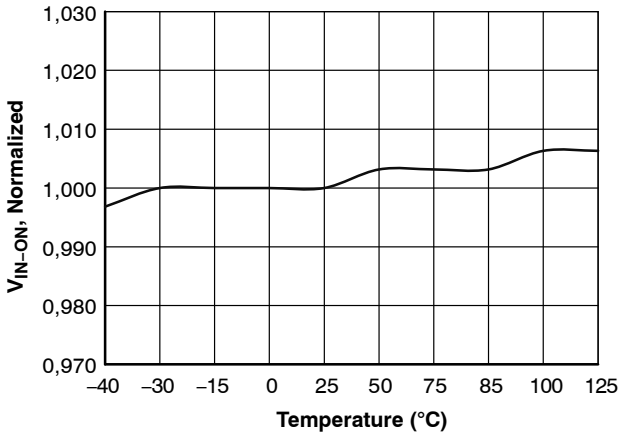


Figure 3. Turn−On Threshold Voltage (V_{IN-ON}) vs. Temperature

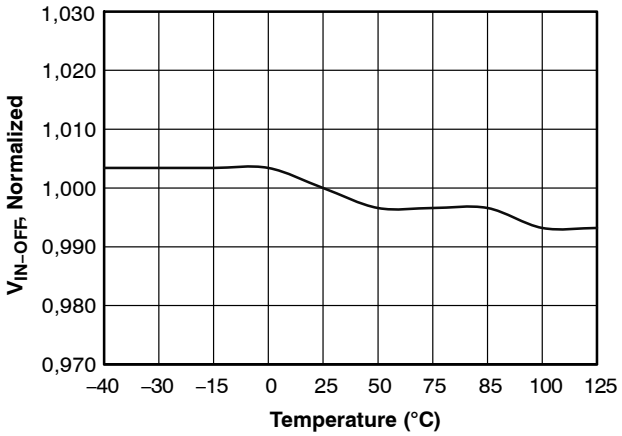


Figure 4. Turn−Off Threshold Voltage (V_{IN-OFF}) vs. Temperature

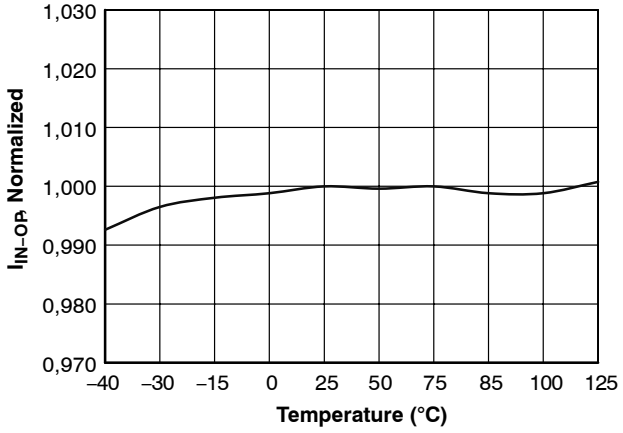


Figure 5. Operating Supply Current (I_{IN-OP}) vs. Temperature

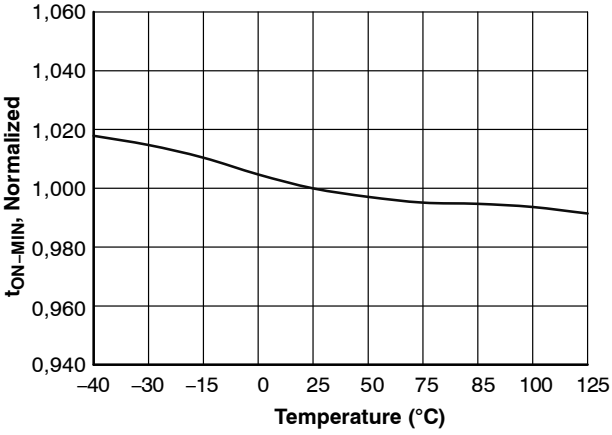


Figure 6. Minimum On Time (t_{ON-MIN}) vs. Temperature

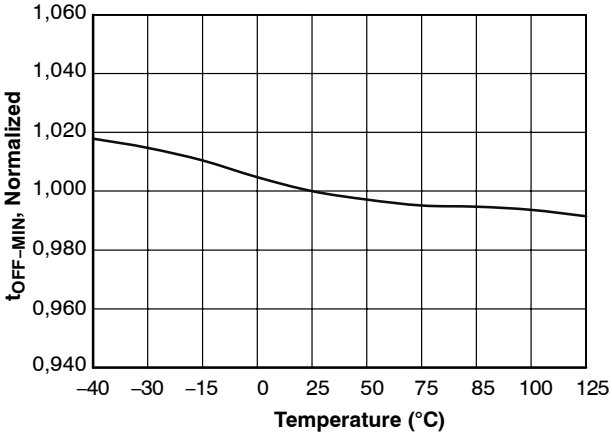


Figure 7. Minimum Gate Turn Off Time ($t_{OFF-MIN}$) vs. Temperature

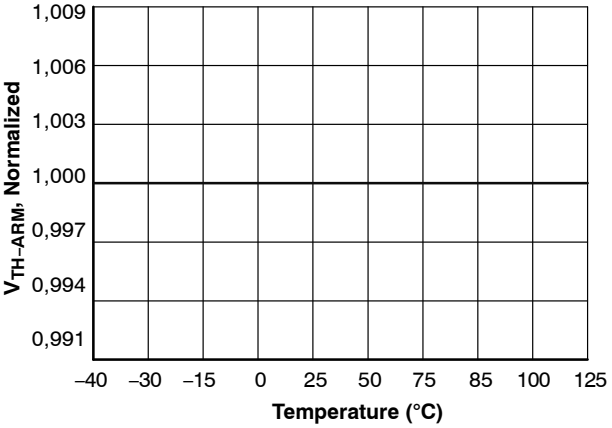


Figure 8. Gate Turn On Threshold Voltage(V_{TH-ARM}) vs. Temperature

TYPICAL PARFORMANCE CHARACTERISTICS (continued)

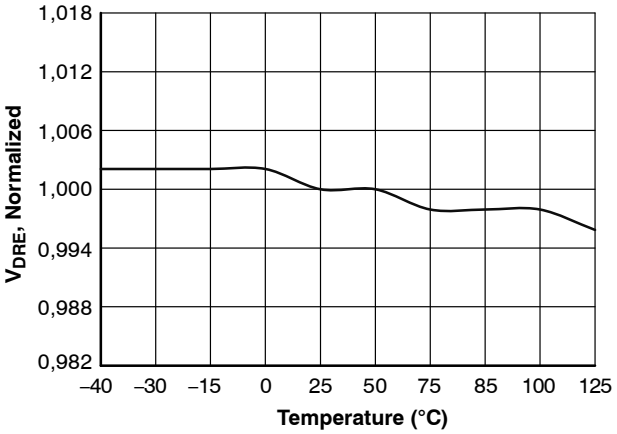


Figure 9. VIN Pin DRE Function Trigger Level (V_{DRE}) vs. Temperature

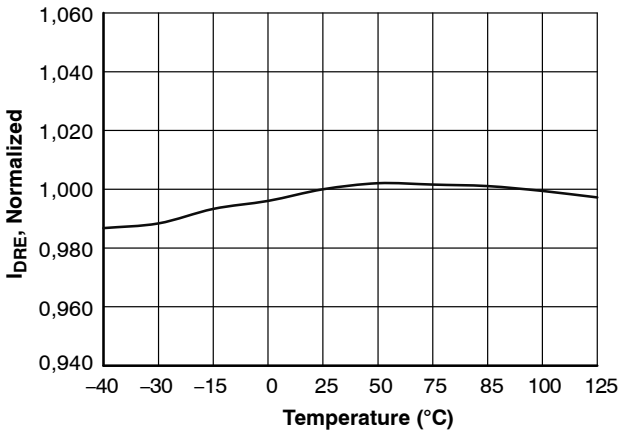


Figure 10. Drain Pin Sinking Current for DRE Triggered (I_{DRE}) vs. Temperature

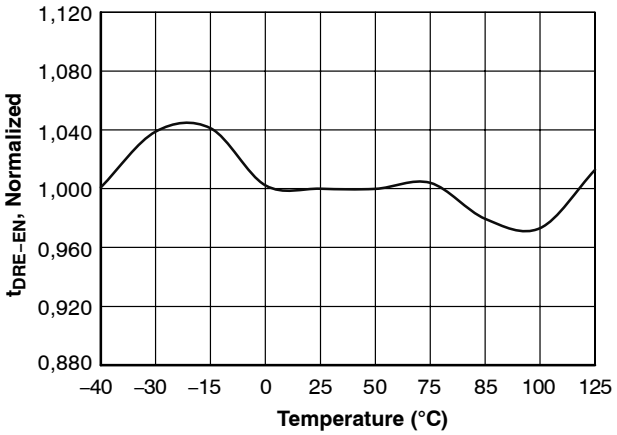


Figure 11. DRE Function Enable Period (t_{DRE-EN}) vs. Temperature

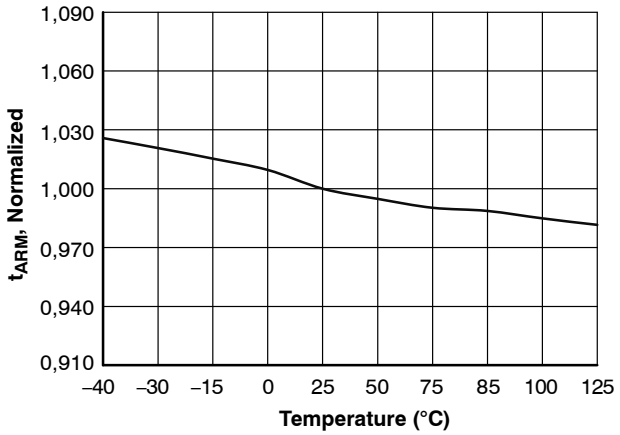


Figure 12. Gate Re–Arming Time for Slope Detection (t_{ARM}) vs. Temperature

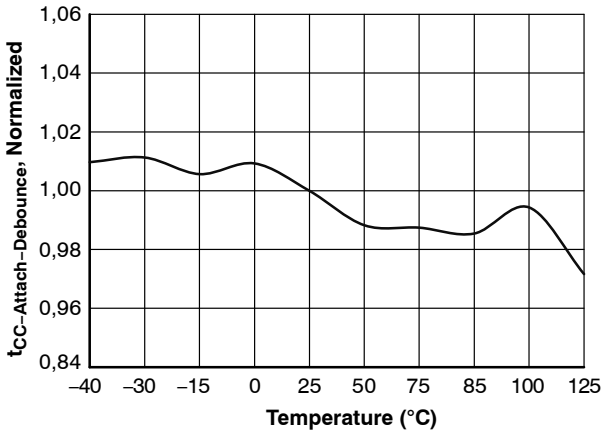


Figure 13. UFP Attachment Debounce Time ($t_{CC-Attach-Debounce}$) vs. Temperature

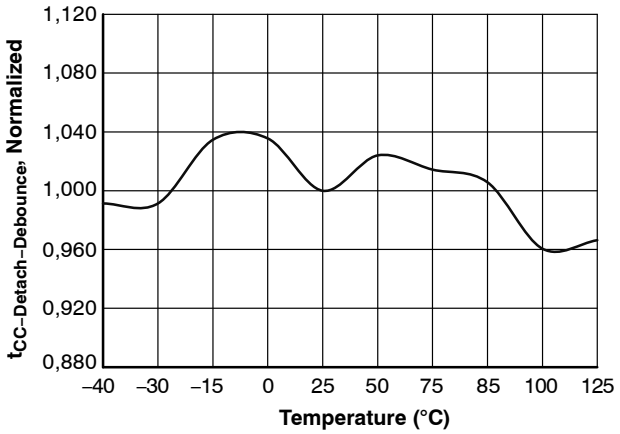


Figure 14. UFP Detachment Debounce Time ($t_{CC-Detach-Debounce}$) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

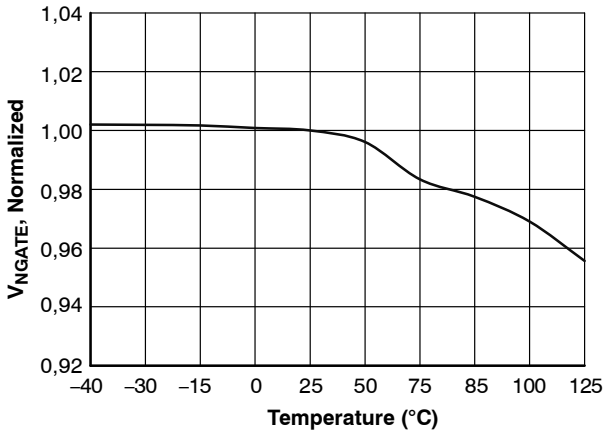


Figure 15. LGATE High Level Voltage (V_{NGATE}) vs. Temperature

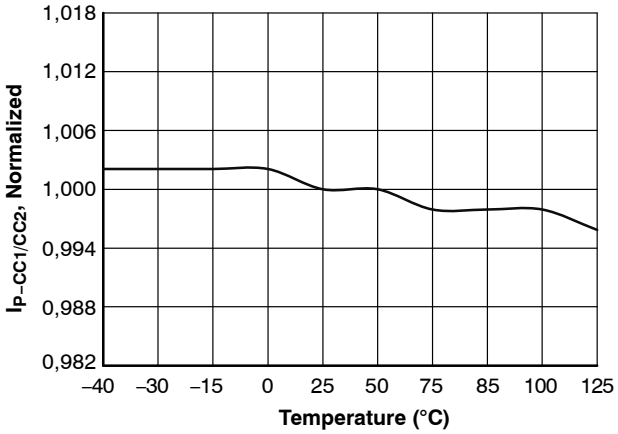


Figure 16. Source Current on CC1/CC2 Pin ($I_{P-CC1/CC2}$) vs. Temperature

FUNCTIONAL DESCRIPTION

Overview

For an ideal circuit operation, the SR control algorithm of FAN6292C is very straightforward. FAN6292C controls the SR MOSFET based on the instantaneous Drain−to−Source voltage as illustrated in Figure 17. When the body diode starts conducting, the drain−to−source voltage drops below the turn−on threshold (V_{TH-ON}) which triggers the turn−on of the gate. Then the product of R_{DS_ON} and instantaneous SR current determines the Drain−to−Source voltage. When the drain−to−source voltage reaches the turn−off threshold (V_{TH-OFF}) as SR MOSFET current decreases to near zero, FAN6292C turns off the gate. If the turn off threshold (V_{TH-OFF}) is very close to zero, the turn off dead time can be minimized.

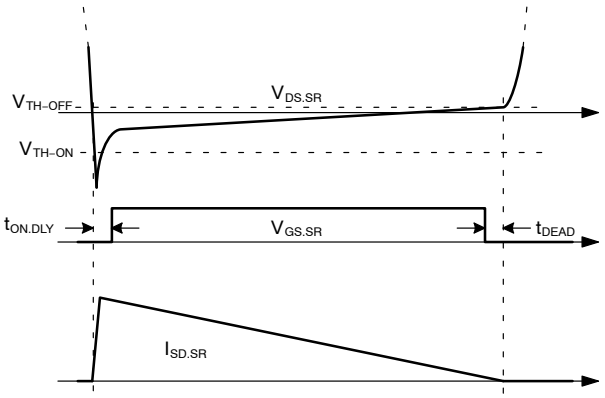


Figure 17. SR MOSFET Operation Waveforms (Ideal Case)

SR Turn−On Algorithm

As the diagram shown in Figure 18, the turn−on of SR GATE is triggered by the three input signals of AND gate. The first input signal is TURN_ON_ALLOW signal, which is given after $t_{OFF-MIN}$ from the falling edge of $V_{GS.SR}$ signal. The second input is the TURN_ON_TRG signal, which is enabled after DRAIN pin voltage drops below V_{TH_ON}. The third signal is t_{ARM} which allows turn−on trigger only when SR drain voltage drops fast with a large slope, preventing SR from triggering by the drain resonance voltage in DCM operation.

SR Turn−Off Algorithm

As diagram shown in Figure 19, the turn−off of SR GATE is triggered by turn off signal, which is enabled when $V_{DS.SR} > V_{TH\_OFF}$.

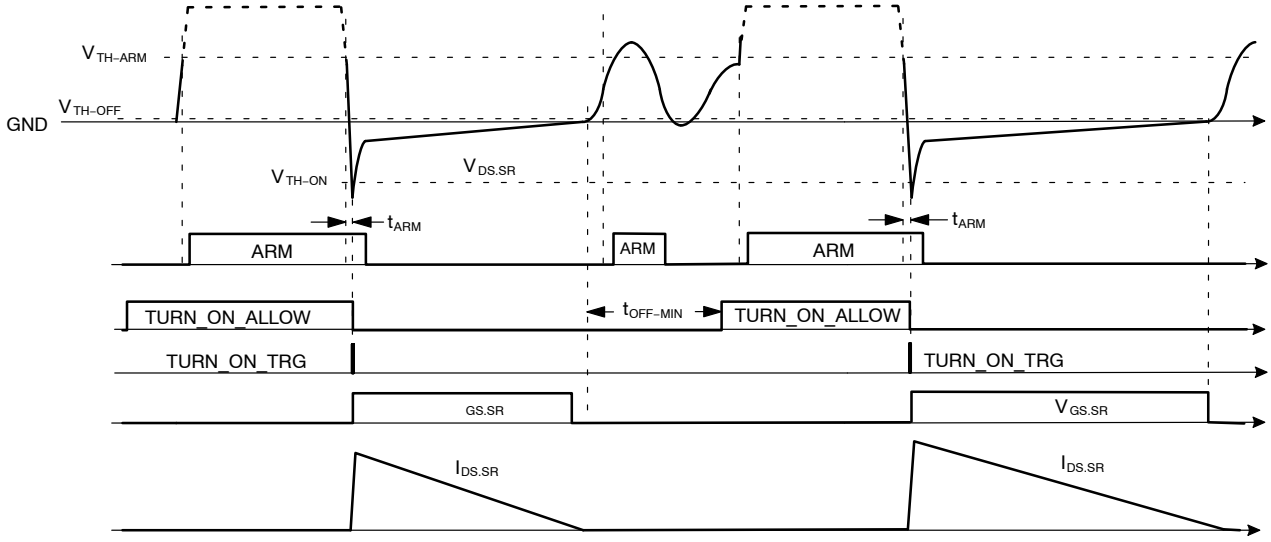


Figure 18. SR Turn−On Algorithm

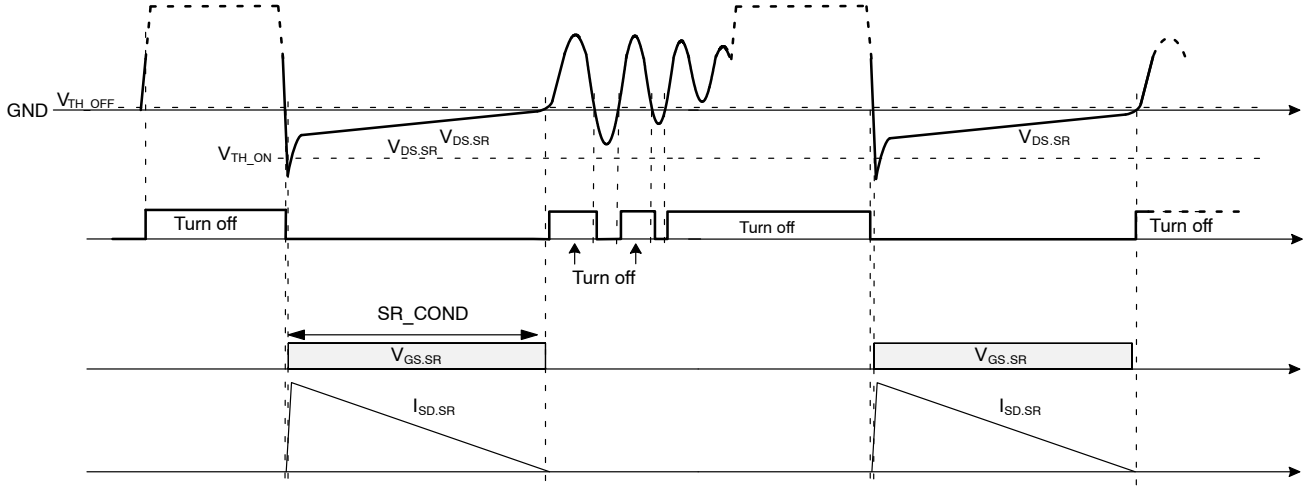


Figure 19. SR Turn−Off Algorithm

Slope Detection

FAN6292C checks SR drain voltage falling slope to distiguish primary FET off instant from the resonant curve. Continuously sees the time gap between SR drain voltage touches V_{TH-ARM} and V_{TH-ON}, this is compared with the internal fixed time of t_{ARM}, gate is only turn on when the time gap is less than t_{ARM} described at Figure 20.

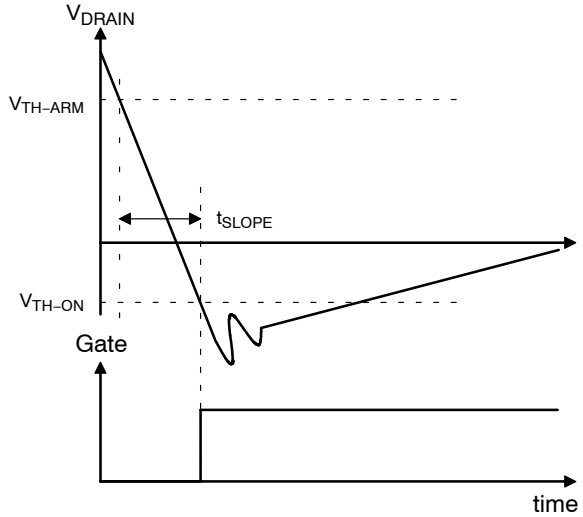


Figure 20. Slope Detection Timing Chart

Slope detection is good for identification SR on instance from the resonance, however, system configuration may give huge impact on the SR drain voltage so slope detection is not always good way for gate ON identification especially at light load. Due to this at light load, slope detection is enabled or disabled depend on period of Gate switching cycles (t_S) as below:

- $t_S < (t_{SLO-DIS} - t_{SLO-HYS})$: continually enable slope detection when t_S is decreasing
- $t_S \geq t_{SLO-DIS}$: basically slope detection is disabled and only enabled after gate rising edge until end of t_{DRE-EN} when t_S increasing

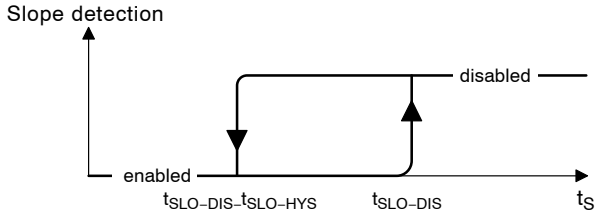


Figure 21. Slope Detect Enable/Disable Depend on t_S

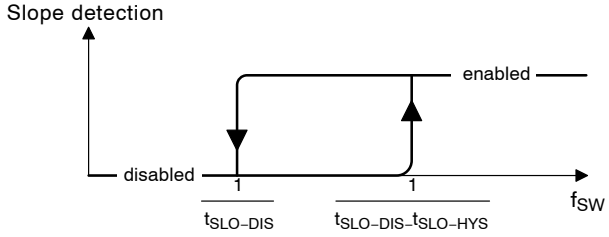


Figure 22. Slope Detect Enable/Disable Depend on f_{SW}

Gate Turn−On

FAN6292C turns on SR FET according to the voltage across SR drain and primary switching period of t_S. Depending on the t_S, gate turn on criteria is different and it is as below:

- $t_S < t_{SLO-DIS}$: SR FET ON when both (a) and (b) meet:
  (a) V_{DRAIN} falling time from V_{TH-ARM} to V_{TH-ON} is less than t_{ARM}
  (b) $V_{DRAIN} \leq V_{TH-ON}$
- $t_S < (t_{SLO-DIS} - t_{SLO-HYS})$:SR FET ON when meet: $V_{DRAIN} \leq V_{TH-ON}$

Gate Turn−On Blanking Time

FAN6292C supports Primary Side Regulation (PSR) operation with Discontinuous Conduction Mode (DCM) and Boundary Conduction Mode (BCM) and the typical operating of Quasi−Resonant valley switching to make the best balance between efficiency and Electro Magnetic Interference (EMI).

Together with slope detection, FAN6292C has a GATE turn on blanking time to avoid SR FET mis−triggered turn on at the first Quasi−Resonant cycle. Blanking time lengths depend on last Gate−to−Gate pulse period. The resonance period is decided by the parasitic capacitance summed at primary side and magnetizing inductance and normally is fixed once system configured but this changes as load changes, typically getting longer as load decreases. This is caused by the parasitic capacitances varies depending on voltage and stored energy at the transformer.

To corresponds this change, FAN6292C adjust minimum OFF time ($t_{OFF-MIN}$) depend on loading condition. Similar as slope detection, when t_S is shorter than $t_{SLO-DIS}$, $t_{OFF-MIN}$ becomes $t_{OFF-MIN-H}$ and when t_S is longer than $t_{SLO-DIS}$ with a hysteresis then $t_{OFF-MIN}$ becomes $t_{OFF-MIN-L}$.

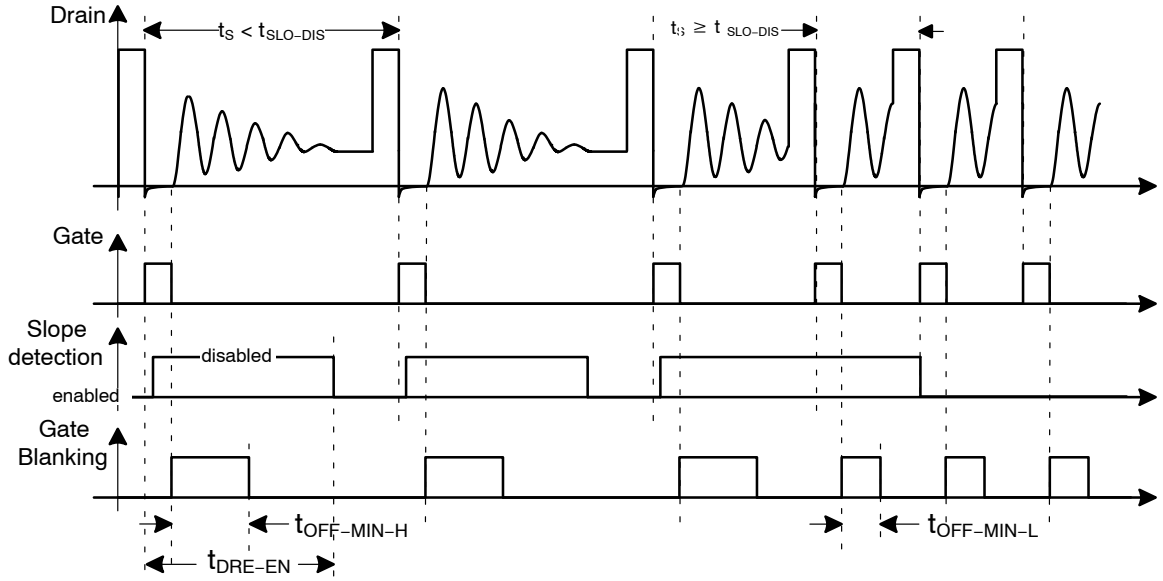


Figure 23. SR Conduction Timing Chart

Gate Turn−Off (Dead Time Self Tuning)

SR controller should turn on SR FET until the secondary discharging current become zero to avoid body diode conduction. Because the conduction loss of body diode is much higher than FET conduction loss. Therefore, the OFF dead time between SR off and magnetizing current become zero is recommended to minimized. But too small OFF dead time may raise the risk of SR FET and primary FET turn on simultaneously and too longer OFF dead time deteriorates the primary auxiliary winding voltage and gives impact on the PSR detection function. So proper value of OFF dead time is needed.

It is possible that offset voltages are induced by the stray inductance by the bonding wires inside MOSFET package and PCB layout. Therefore, it is very difficult to maintain the same OFF dead time against all the circuit tolerances and variation of operating condition. In order to control MOSFET turn off when the secondary magnetizing current is near zero, FAN6292C build−in OFF dead time self−tuning, which has adaptively changing internal turn off thresholds. The off threshold, V_{TH-OFF}, is modulated between 32 steps through internal up/down counter. FAN6292C measures OFF dead time from gate falling edge to drain voltage reaches V_{TH-HGH} and compares with internal timing threshold t_{DEAD}. When $t_{DEAD\_OFF} > t_{DEAD}$ then internal counter increases one−step and gate turned off a little delayed at next switching cycle.

Start−Up Operation

FAN6292C supplies internal circuit power through VIN pin, there is integrate Low Drop Out (LDO) regulator to regulate internal voltage not exceed 5.5 V. In typical application, FAN6292C VIN pin is connect to VBUS of USB port so VIN gradually increases, FAN6292C start operation when VIN touches V_{IN-ON} and stop operation when VIN drop to V_{IN-OFF}.

Accordingly, even before FAN6292C start to working, primary side is normally working and it gives impact on the secondary side. When primary FET turns on, the voltage cross over the primary winding becomes AC input voltage and it gives secondary winding voltage based on primary and secondary turn ratio.

Once SR FET drain voltage is generated by the primary switching, the voltage will be divided by the capacitance of SR FET and some amount of voltage can be shown at the SR FET gate as in the Figure 24 and below equation.

$$V_{GS\_SR} = \frac{C_{GD}}{C_{GD} + C_{GS}} \times V_{Drain} \qquad \text{(eq. 1)}$$

If the divided gate voltage is higher than SR FET urn−on threshold (VGS_TH) then SR FET can be turned on and this may make primary FET turn on and SR FET turn on simultaneously. In order to avoid mis−turn on SR FET, even before VIN voltage reaches VIN−ON, FAN6292C pulls down the gate voltage to GND by using drain voltage.

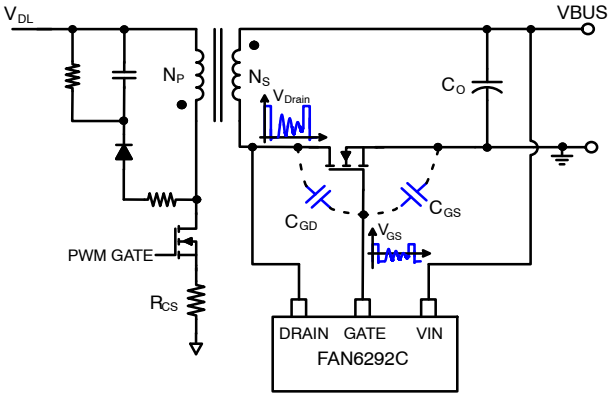


Figure 24. Gate Coupling Signal Via Practice Capacitance

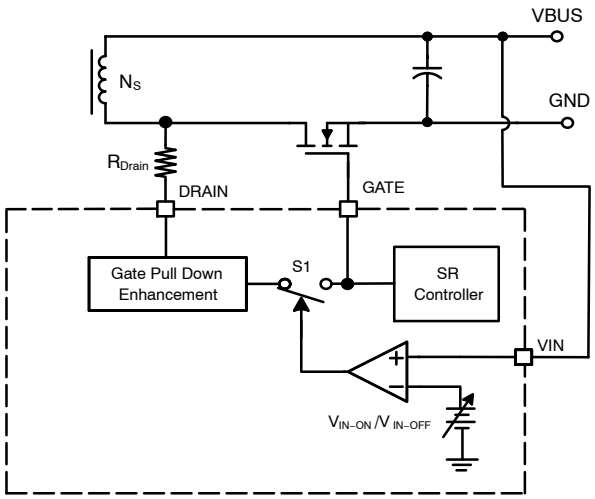


Figure 25. Gate Clamping Function Block Before FAN6292C Start−Up Operation

Dynamic Response Enhancement (DRE)

In PSR system control, the output voltage is regulated through detecting proportional voltage of auxiliary winding (VS) which is reflected from secondary winding. However VS signal can only generate and detects when primary side PWM switched. To get better standby power performance, the switching frequency is decreased to quite low frequency, the output voltage cannot be maintain as load suddenly increases from extremely light load to heavy load.

In order to enhance load transient response time when primary switching frequency is much slower, FAN6292C build−in Dynamic Response Enhancement (DRE) function that continues monitor VIN pin voltage. FAN6292C generate a sinking current pulse from Drain of MOSFET to GND when VIN pin voltage is lower than threshold V_{DRE}. The DRE sinking current which period is t_{DERI} and current level is I_{DRE} at Drain pin. The I_{DRE} current flowing loop is depicted in the Figure 26 as a blue line and this informs the primary controller that output voltage drops lower than V_{DRE} at any loading condition.

In order to give enough detection time window of primary controller FAN6292C enables DRE when primary switching frequency is low enough, FAN6292C starts counting from SR gate rising edge and DRE is enabled when the counted time is longer than t_{DRE-EN}. DRE function generates sinking current (I_{DRE}) for t_{DREI} every 4us (t_{RE-ARM}) until get drain rising edge signal when the primary PWM MOSFET gate turns on. Figure 27 shows DRE function timing chart.

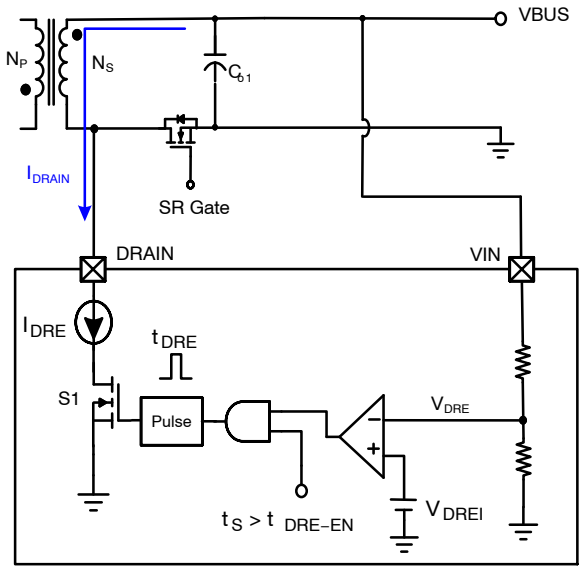


Figure 26. DRE Internal Function Block

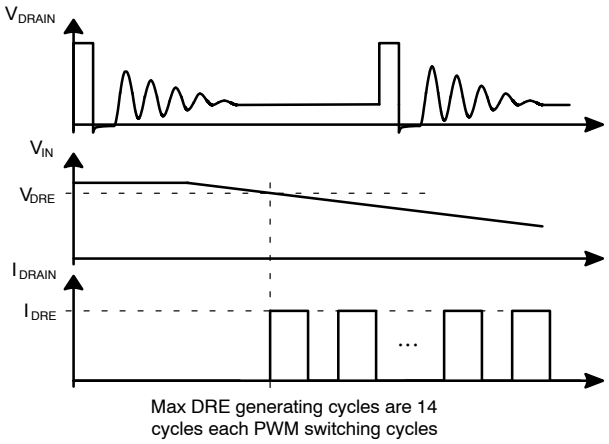


Figure 27. DRE Function Active Sequence

Type−C Control Function Description

FAN6292C implements Type−C block to enable and disable an external load switch. Internally adapted charge pump lets FAN6292C control N−channel MOSFET as a load switch. It helps whole system be more cost competitive compared to P−channel MOSFET as a load switch.

FAN6292C supports output current up to 3 A. In order to meet Type−C specification, 330 μA is applied on CC1 pin and CC2 pin. When Rd (5.1 kΩ) is attached on either CC1 or CC2, Load switch is turned−on after 150 ms denounce time. As soon as load switch is enabled, BC1.2 counter is enabled. To acknowledge detachment, it needs 15 ms denounce time. When load switch is turned−off.

PCB Layout Guidance

Figure 28 shows the connection path of each loop at secondary side. The PCB layout was recommended as below:

- Path1 is connected between Drain of MOSFET and FAN6292C DRAIN pin, trace length is needed as short as possible. R_{DRAIN} could helpful on the drain pin ESD capability but should be less than 30 W to make sure DRE function.
- GND path needs separate as three paths: Path2, Path3 and Path 4. FAN6292C detects Drain to source voltage of SR MOSFET via DRAIN pin and GND pin. Therefore FAN6292C GND pin needs connect to GND of C_{O1} directly then goes to Source of SR MOSFET. The path2 connection should be IC GND → C_{O1} → Source pin of SR MOSFET. Path 3 is connected to GND of C_{O1}, C_{O2}, and USB port after Path 2. Path 4 is connected IC GND and all component are needed connect to GND.
- Path 6 is connected secondary winding and SR MOSFET, It's trace length needs as short as possible to avoids switching noise coupling.

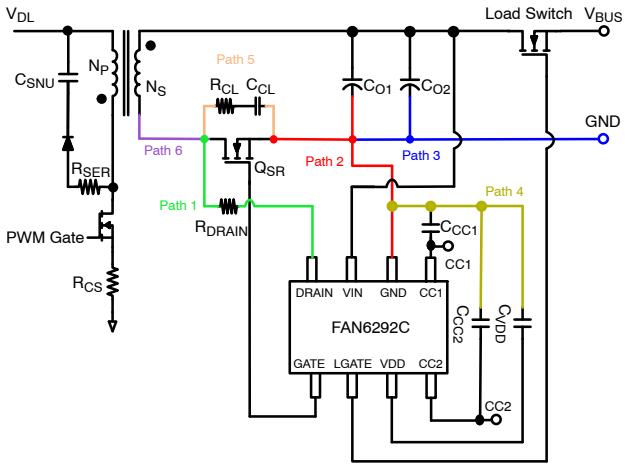
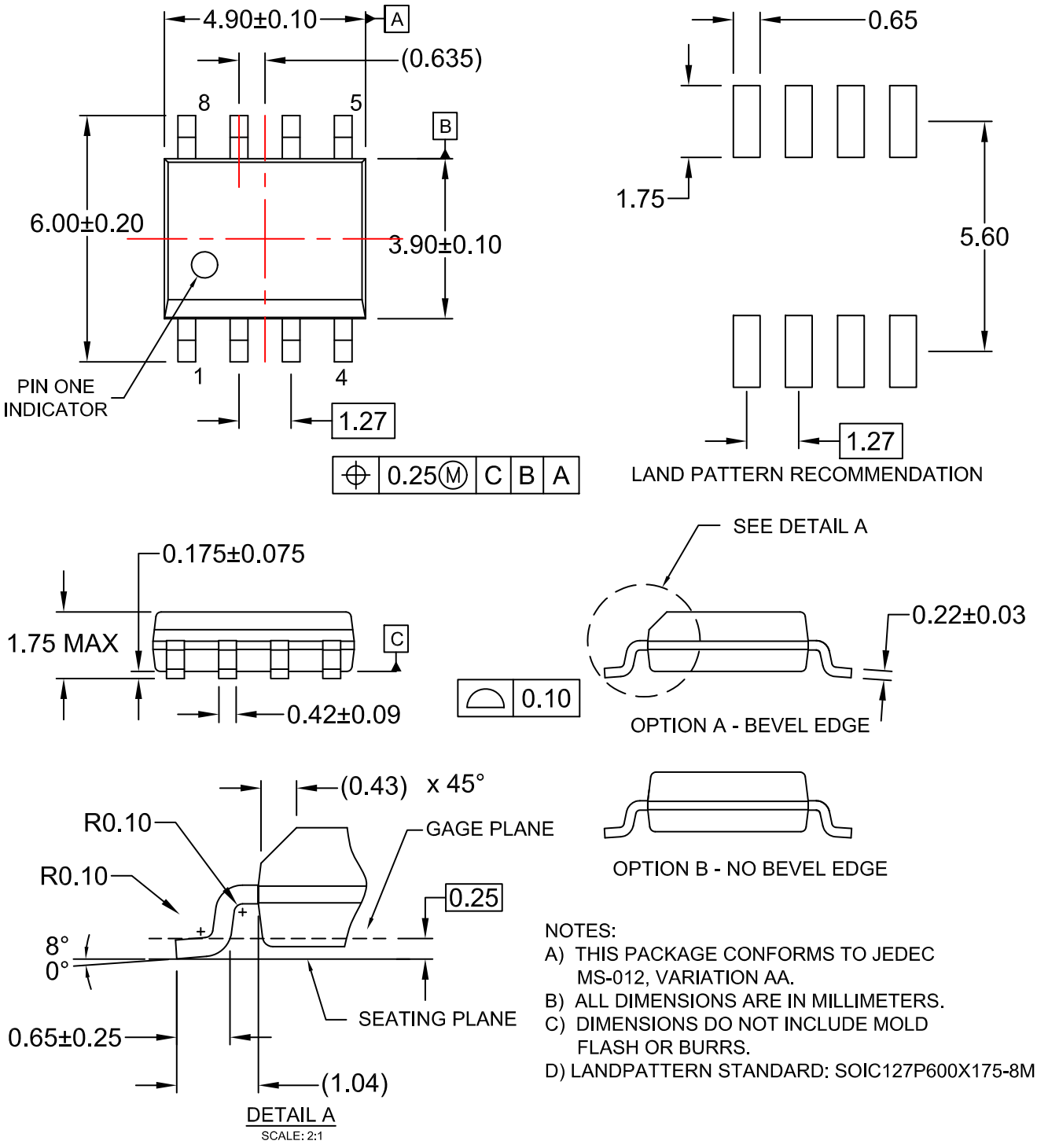


Figure 28. PCB Layout Guideline

PACKAGE DIMENSIONS

SOIC8
CASE 751EB
ISSUE A



NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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