



Is Now Part of



**ON Semiconductor®**

To learn more about ON Semiconductor, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (\_), the underscore (\_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (\_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at [www.onsemi.com](http://www.onsemi.com). Please email any questions regarding the system integration to [Fairchild\\_questions@onsemi.com](mailto:Fairchild_questions@onsemi.com).

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

# FAN8811

## High-Frequency, High Side and Low Side Gate Driver IC

The FAN8811 is high side and low side gate-drive IC designed for high-voltage, high-speed, driving MOSFETs operating up to 100 V.

The FAN8811 integrates a driver IC and a bootstrap diode. The driver IC features low delay time and matched PWM input propagation delays, which further enhance the performance of the part.

The high speed dual gate driver are designed to drive both the high-side and low-side of N-Channel MOSFETs in a half bridge or synchronous buck configuration. The floating high-side driver is capable of operating with supply voltages of up to 100 V. In the dual gate driver, the high side and low side each have independent inputs which allow maximum flexibility of input control signals in the application. The PWM input signal (high level) can be 3.3 V, 5 V or up to  $V_{DD}$  logic input to cover all possible applications. The bootstrap diode for the high-side driver bias supply is integrated in the chip. The high-side driver is referenced to the switch node (HS) which is typically the source pin of the high-side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to  $V_{SS}$  which is typically ground. The functions contained are the input stages, UVLO protection, level shift, bootstrap diode, and output driver stages.

### Features

- Drives two N-Channel MOSFETs in High & Low Side
- Integrated Bootstrap Diode for High Side Gate Drive
- Bootstrap Supply Voltage Range up to 118 V
- 3 A Source, 6 A Sink Output Current Capability
- Drives 1nF Load with Typical Rise/Fall Times of 6 ns/4 ns
- TTL Compatible Input Thresholds
- Wide Supply Voltage Range 8 V to 16 V (Absolute Maximum 18 V)
- Fast Propagation Delay Times (Typ. 30 ns)
- 2 ns Delay Matching (Typical)
- Under-Voltage Lockout (UVLO) Protection for Drive Voltage
- Operating Junction Temperature Range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$

### Typical Applications

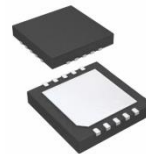
- Power Supplies for Telecom and Datacom
- Half-Bridge and Full-Bridge Converters
- Synchronous-Buck Converters
- Two-Switch Forward Converters
- Class-D Audio Amplifiers



**ON Semiconductor**<sup>®</sup>

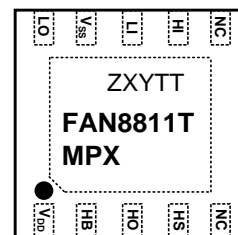
[www.onsemi.com](http://www.onsemi.com)

### PACKAGE PICTURE



**10 Lead MLP**  
(Molded Leadless Package)

### MARKING DIAGRAM



Z : Plant Code  
X : 1-Digit Year Code  
Y : 1-Digit Week Code  
TT : 2-Digit Die Run Code  
MP : Package Type (MLP)  
X : Reel Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this datasheet.

# FAN8811

## Typical Applications

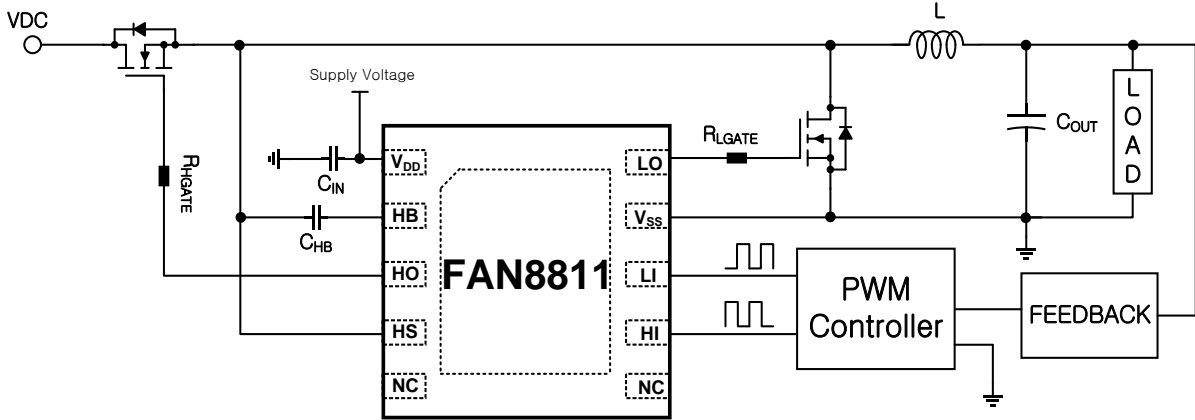


Figure 1. Application Schematic – Synchronous Buck Converter

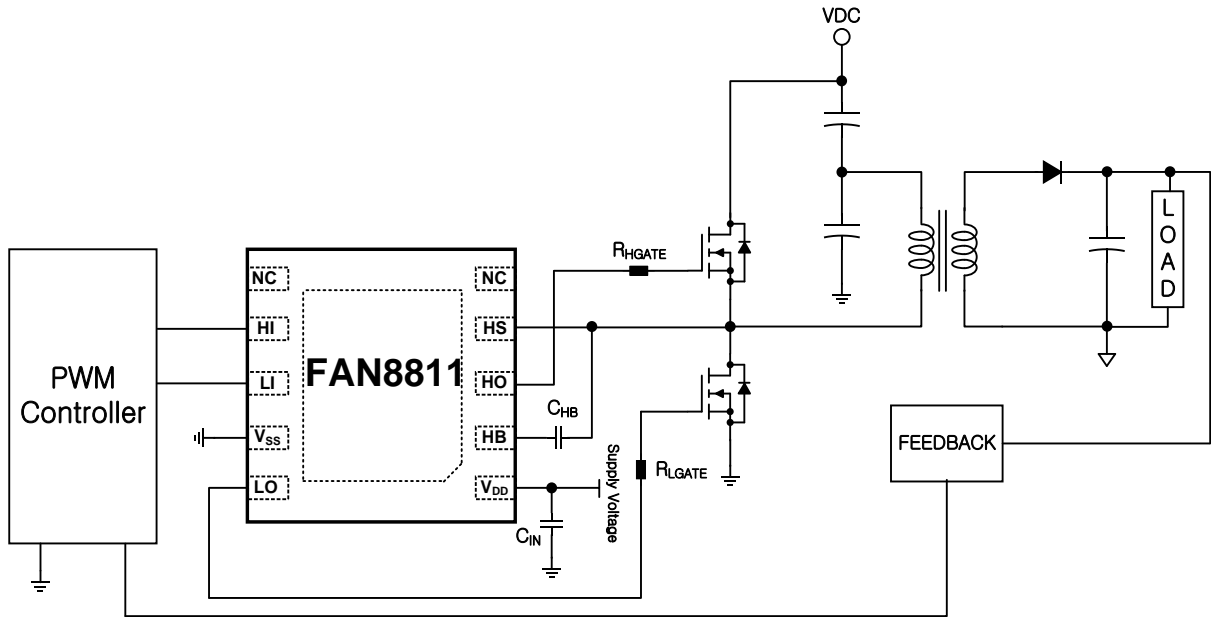


Figure 2. Application Schematic – Half Bridge Converter

# FAN8811

## Block Diagram

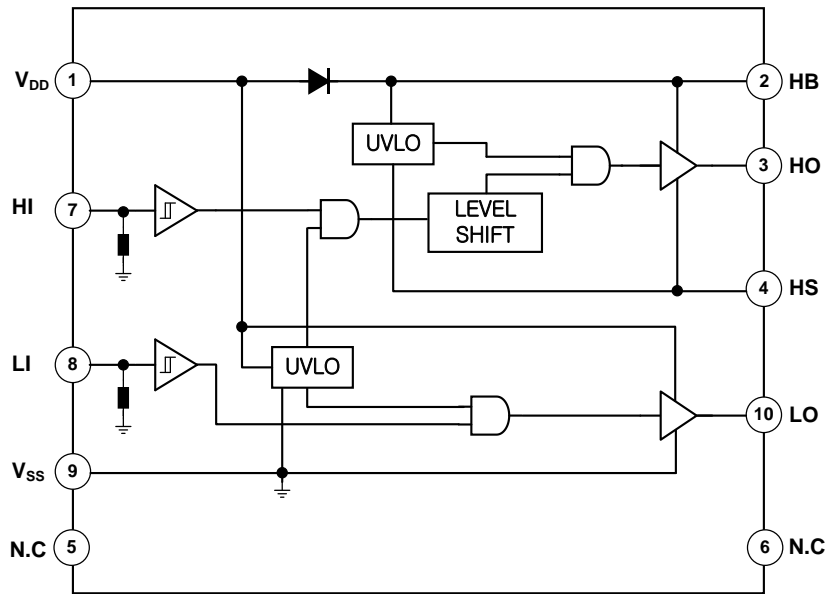


Figure 3. Simplified Block Diagram

# FAN8811

## PIN CONNECTIONS

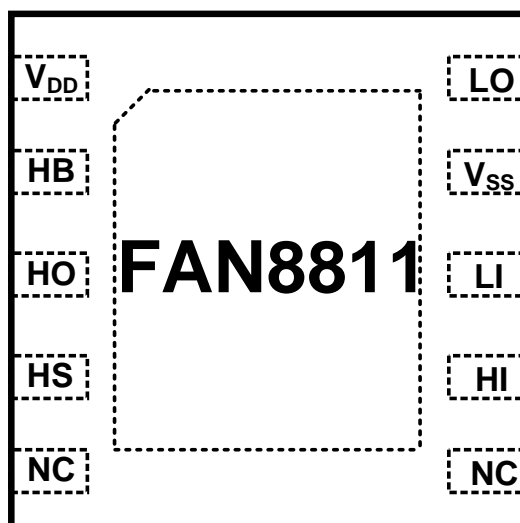


Figure 4. Pin Assignments – 10 Lead MLP (Top View)

### PIN DESCRIPTION

Pin No.	Pin Name	Description
1	$V_{DD}$	Logic and low-side gate driver power supply voltage
2	HB	High-side floating supply
3	HO	High-side driver output
4	HS	High-voltage floating supply return
5	N.C	No Connection
6	N.C	No Connection
7	HI	Logic input for High-side gate driver output
8	LI	Logic input for Low-side gate driver output
9	$V_{SS}$	Logic Ground
10	LO	Low-side driver output

# FAN8811

## MAXIMUM RATINGS (Note 1)

All voltage parameters are referenced to  $V_{SS}$ , unless otherwise noted.

Symbol	Parameter	Min.	Max.	Units
$V_{DD}$	Low-Side and Logic Fixed Supply Voltage	-0.3	18	V
$V_{HS}$	High-Side Floating Supply Offset Voltage(Note 2)	-1	100	V
	Repetitive Pulse (< 100 ns)(Note 3)	$-(24 - V_{DD})$	100	V
$V_{LO}$	Low-Side Output Voltage, LO Pin	-0.3	$V_{DD} + 0.3$	V
	Repetitive Pulse (< 100 ns)(Note 3)	-2	$V_{DD} + 0.3$	V
$V_{HO}$	High-Side Floating Output Voltage, HO Pin	$V_{HS} - 0.3$	$V_{HB} + 0.3$	V
	Repetitive Pulse (< 100 ns)(Note 3)	$V_{HS} - 2$	$V_{HB} + 0.3$	V
$V_{LI}, V_{HI}$	Logic Input Voltage	-0.3	$V_{DD} + 0.3$	V
$V_{HB}$	High-Side Floating Supply Voltage	-0.3	118	V
$V_{HB} - V_{HS}$	$V_{HS}$ to $V_{HB}$ Supply Voltage	-0.3	18	V
$T_J$	Operating Junction Temperature	-55	150	°C

1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. The  $V_{HS}$  negative voltage capability can be calculated using  $(V_{HB} - V_{HS}) - 18$  V base on  $V_{HB}$ , due to its dependence on  $V_{DD}$  voltage level.
3. Verified at bench characterization.

## ESD Ratings

Symbol	Parameters	VALUE	Unit.
$ESD_{HBM}$	Electrostatic Discharge Capability	Human Body Model, JEDEC JS-001-2012	2000
$ESD_{CDM}$		Charged Device Model, JESD22-C101	1000

## Thermal Information

Symbol	Parameter	VALUE	Units
$P_D$	Power Dissipation (Note 4)	1S0P with thermal vias (Note 5)	0.6
		1S2P with thermal vias (Note 6)	2.4
$\theta_{JA}$	Thermal Resistance Junction-Air	1S0P with thermal vias (Note 5)	163
		1S2P with thermal vias (Note 6)	41

4. JEDEC standard: JESD51-2, JESD51-3. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
5. 1S0P with thermal via: one signal layer with zero power plane and thermal via.
6. 1S2P with thermal via: one signal layer with two power plane and thermal via.

## RECOMMENDED OPERATING RANGES (Note 7)

All voltage parameters are referenced to  $V_{SS}$

Sym	Parameters	Test Condition	Min.	Max.	Unit.
$V_{DD}$	Supply Voltage	DC	8	16	V
$V_{HS}$	High Side Floating Return	DC	-1	100	V
		Repetitive Pulse (< 100 ns)	$-(24 - V_{DD})$	100	V
$V_{HB}$	Voltage on HB	DC	$V_{HS} + 8,$ $V_{DD} - 1$	$V_{HS} + 16,$ $V_{DD} + 100$	V
$dV_{SW}/dt$	Voltage Slew Rate on SW			50	V/ns
$T_J$	Operating Temperature		-40	125	°C

7. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# FAN8811

## ELECTRICAL CHARACTERISTICS

$V_{DD}=V_{HB}=12\text{ V}$ ,  $V_{HS}=V_{SS}=0\text{ V}$ ,  $T_A=T_J=-40^\circ\text{C}$  to  $125^\circ\text{C}$ , no load on HO or LO, unless otherwise noted.

Symbol	Parameters	Test Condition	Min.	Typ.	Max.	Unit
<b>Power Supply Section</b>						
$I_{DD}$	$V_{DD}$ Quiescent Current	$V_{HI}=0\text{ V}$ ; $V_{LI}=0\text{ V}$		0.17	0.3	mA
$I_{DDO}$	$V_{DD}$ Operating Current	$f_{SW} = 500\text{ kHz}$		1.5	3.0	mA
$I_{HB}$	HB Quiescent Current	$V_{HI}=0\text{ V}$ ; $V_{LI}=0\text{ V}$		0.1	0.2	mA
$I_{HBO}$	HB Operating Current	$f_{SW} = 500\text{ kHz}$		1.9	3.0	mA
$I_{HBS}$	HB to $V_{SS}$ Quiescent Current	$V_{HS} = V_{HB} = 100\text{ V}$		0	10	$\mu\text{A}$
$I_{HBSO}$	HB to $V_{SS}$ Operating Current	$f_{SW} = 500\text{ kHz}$		0.3	1.0	mA
$V_{DDR}$	$V_{DD}$ UVLO Threshold	$V_{DD}$ Rising	6.2	6.8	7.4	V
$V_{DDH}$	$V_{DD}$ UVLO Hysteresis			0.6		V
$V_{HBR}$	HB UVLO Threshold	HB Rising	5.5	6.3	7.2	V
$V_{HBH}$	HB UVLO Hysteresis			0.4		V
<b>Input Logic Section</b>						
$V_{IH}$	High Level Input Voltage Threshold		1.80	2.2	2.50	V
$V_{IL}$	Low Level Input Voltage Threshold		1.3	1.7	2.0	V
$V_{IHYS}$	Input Logic Voltage Hysteresis			0.5		V
$R_{IN}$	Input Pull-down Resistance			100		k $\Omega$
<b>Bootstrap Diode</b>						
$V_{FL}$	Forward Voltage @ Low Current	$I_{VDD^*HB} = 100\ \mu\text{A}$		0.55	0.8	V
$V_{FH}$	Forward Voltage @ High Current	$I_{VDD^*HB} = 100\ \text{mA}$		0.8	1.0	V
$R_D$	Dynamic Resistance	$I_{VDD^*HB} = 100\ \text{mA}$		0.7	1.5	$\Omega$
$t_{BS}$ (Note 8)	Diode Turn-off Time	$I_F=20\ \text{mA}$ , $I_{REV}=0.5\ \text{A}$		20		ns
<b>Low Side Driver</b>						
$V_{OLL}$	Low Level Output Voltage	$I_{LO} = 100\ \text{mA}$		0.06	0.15	V
$V_{OHL}$	High Level Output Voltage	$I_{LO} = -100\ \text{mA}$ , $V_{OHL} = V_{DD} - V_{LO}$		0.16	0.28	V
$I_{OHL}$ (Note 8)	Peak Pull-up Current	$V_{LO} = 0\ \text{V}$		3		A
$I_{OLL}$ (Note 8)	Peak Pull-down Current	$V_{LO} = 12\ \text{V}$		6		A
$t_{R\_LO}$	LO Rise Time	10% to 90%, $C_{LOAD}=1\ \text{nF}$		6		ns
$t_{F\_LO}$	LO Fall Time	90% to 10%, $C_{LOAD}=1\ \text{nF}$		4		ns
$t_{R\_LO1}$	LO Rise Time	3 V to 9 V, $C_{LOAD}=100\ \text{nF}$		300	500	ns
$t_{F\_LO1}$	LO Fall Time	9 V to 3 V, $C_{LOAD}=100\ \text{nF}$		140	300	ns
$t_{LPHL}$	LI=Low Propagation Delay	$V_{LI}$ Falling to $V_{LO}$ Falling, $C_{LOAD}=0$		28	43	ns
$t_{LPLH}$	LI=High Propagation Delay	$V_{LI}$ Rising to $V_{LO}$ Rising, $C_{LOAD}=0$		30	45	ns
<b>High Side Driver</b>						
$V_{OLH}$	Low Level Output Voltage	$I_{HO} = 100\ \text{mA}$		0.06	0.15	V
$V_{OHH}$	High Level Output Voltage	$I_{HO} = -100\ \text{mA}$ , $V_{OHH} = V_{HB} - V_{HO}$		0.16	0.28	V
$I_{OHH}$ (Note 8)	Peak Pull-up Current	$V_{HO} = 0\ \text{V}$		3		A
$I_{OLH}$ (Note 8)	Peak Pull-down Current	$V_{HO} = 12\ \text{V}$		6		A
$t_{R\_HO}$	HO Rise Time	10% to 90%, $C_{LOAD}=1\ \text{nF}$		6		ns
$t_{F\_HO}$	HO Fall Time	90% to 10%, $C_{LOAD}=1\ \text{nF}$		4		ns
$t_{R\_HO1}$	HO Rise Time	3 V to 9 V, $C_{LOAD}=100\ \text{nF}$		300	500	ns
$t_{F\_HO1}$	HO Fall Time	9 V to 3 V, $C_{LOAD}=100\ \text{nF}$		140	300	ns
$t_{HPHL}$	HI=Low Propagation Delay	$V_{HI}$ Falling to $V_{HO}$ Falling, $C_{LOAD}=0$		28	43	ns
$t_{HPLH}$	HI=High Propagation Delay	$V_{HI}$ Rising to $V_{HO}$ Rising, $C_{LOAD}=0$		30	45	ns
<b>Delay Matching</b>						
$t_{MON}$	HI Turn-OFF to LI Turn-ON			2	10	ns
$t_{MOFF}$	LI Turn-OFF to HI Turn-ON			2	10	ns
<b>Minimum Pulse Width</b>						
$t_{PW}$	Minimum Pulse Width for HI and LI (Note 8)				50	ns

8. These parameters are guaranteed by design.

TYPICAL CHARACTERISTICS

Typical characteristics are provided at 25°C and  $V_{DD}, V_{HB} = 12\text{ V}$  unless otherwise noted.

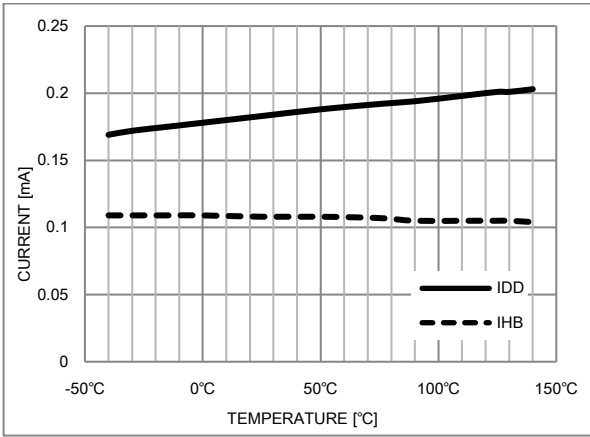


Figure 5. Quiescent Current vs. Temperature

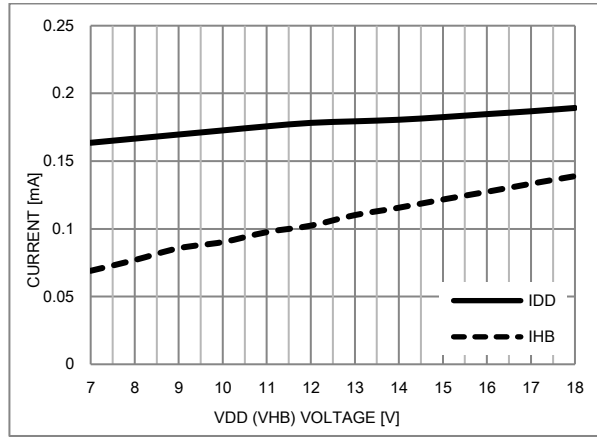


Figure 6. Quiescent Current vs.  $V_{DD}$  ( $V_{HB}$ )

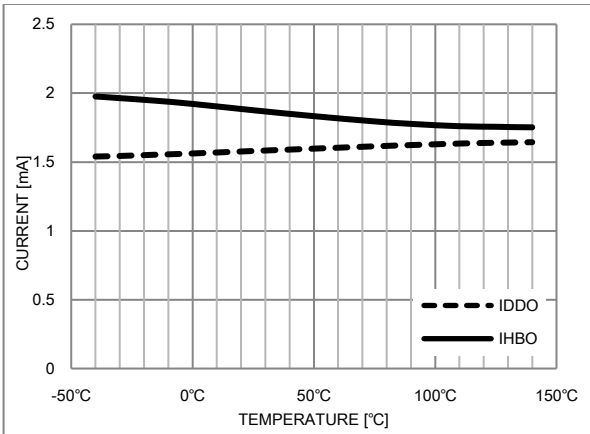


Figure 7. Operating Current vs. Temperature

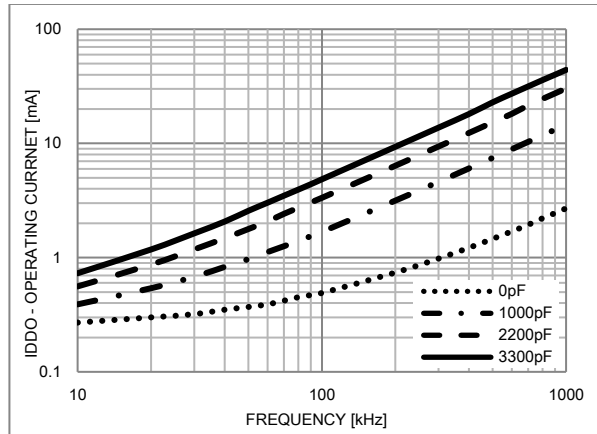


Figure 8.  $I_{DD}$  Operating Current vs. Frequency

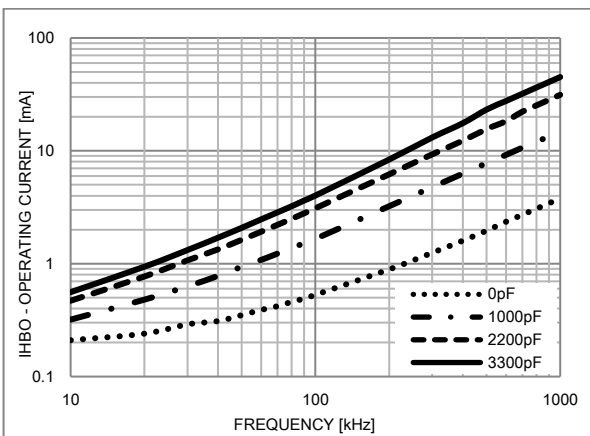


Figure 9.  $I_{HB}$  Operating Current vs. Frequency

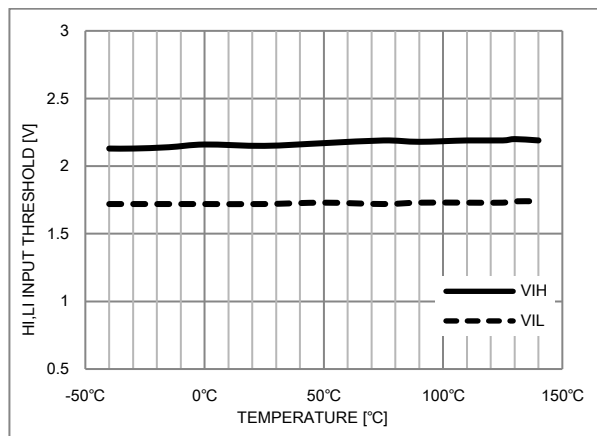


Figure 10. Input Threshold vs. Temperature



TYPICAL CHARACTERISTICS

Typical characteristics are provided at 25°C and  $V_{DD}, V_{HB} = 12\text{ V}$  unless otherwise noted.

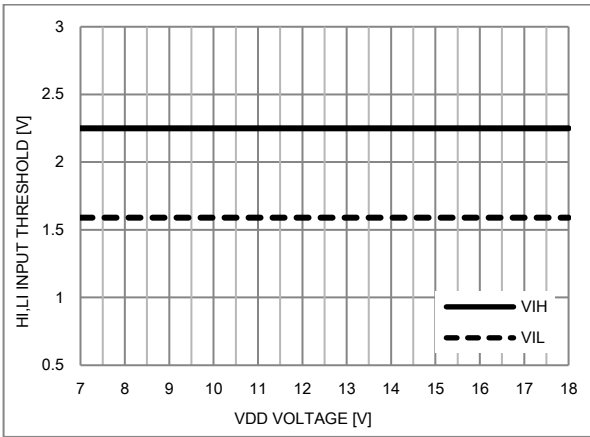


Figure 11. Input Threshold vs.  $V_{DD}$

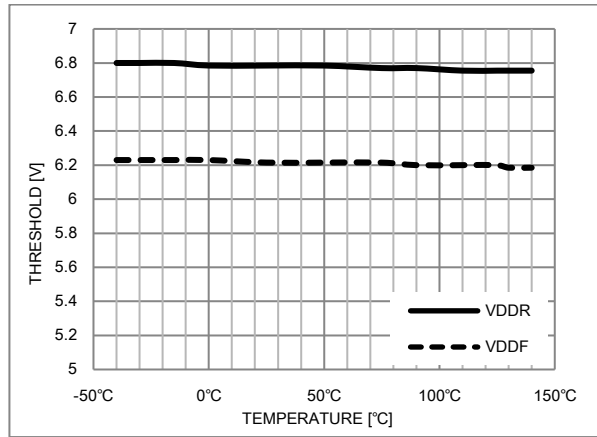


Figure 12.  $V_{DD}$  UVLO Threshold vs. Temperature

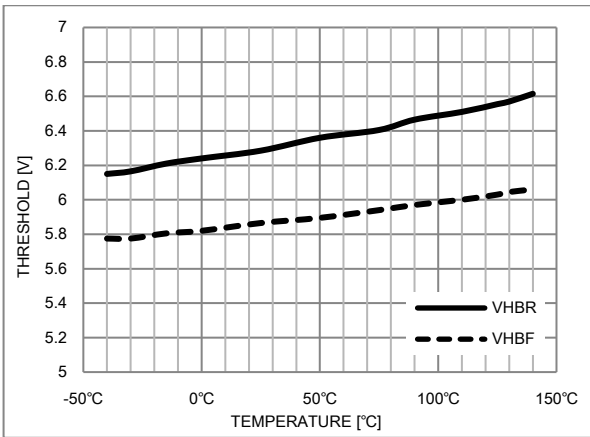


Figure 13.  $V_{HB}$  UVLO Threshold vs. Temperature

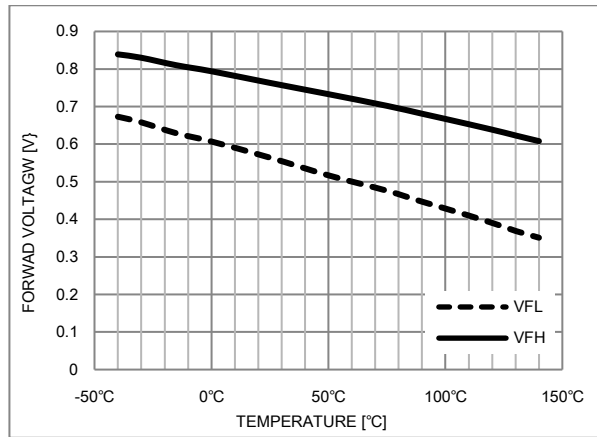


Figure 14. Bootstrap Diode  $V_F$  vs. Temperature

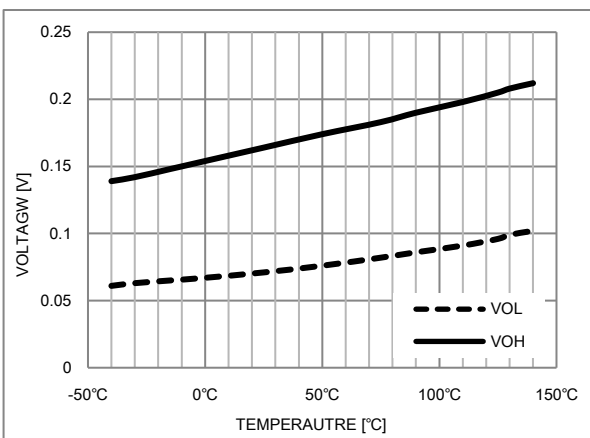


Figure 15.  $V_{OH}, V_{OL}$  Voltage vs. Temperature

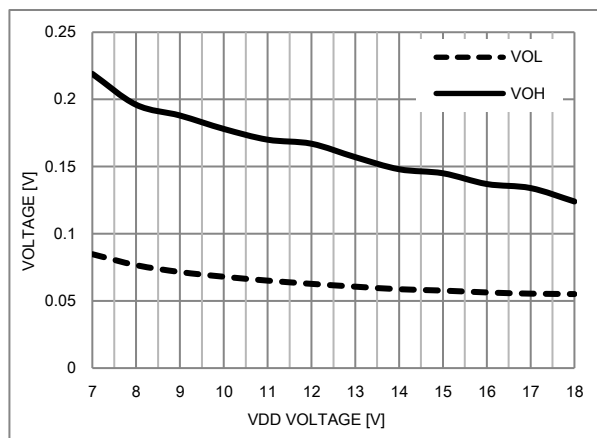


Figure 16.  $V_{OH}, V_{OL}$  Voltage vs.  $V_{DD}(V_{HB})$

TYPICAL CHARACTERISTICS

Typical characteristics are provided at 25°C and  $V_{DD}, V_{HB} = 12\text{ V}$  unless otherwise noted.

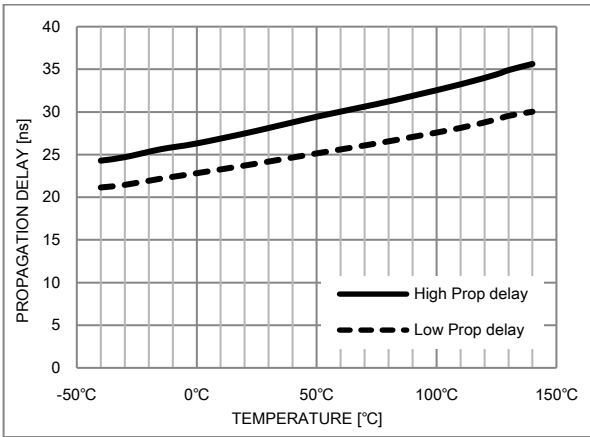


Figure 17. Low Side Propagation Delay vs. Temperature

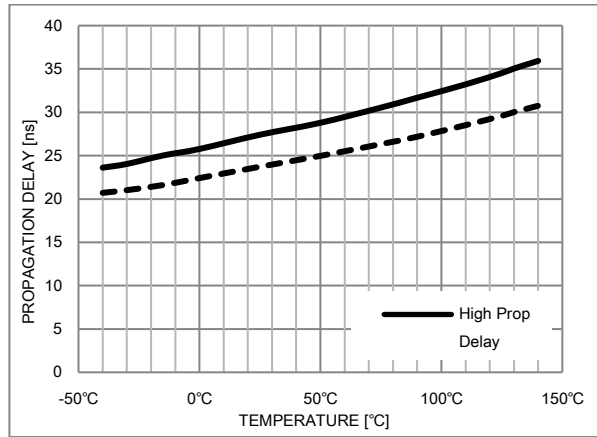


Figure 18. High Side Propagation Delay vs. Temperature

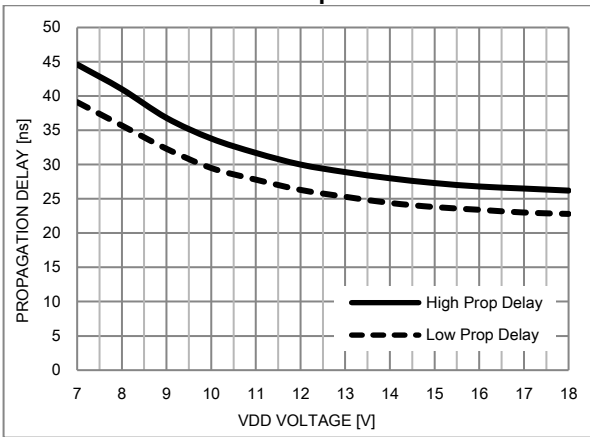


Figure 19. Low Side Propagation Delay vs.  $V_{DD}$

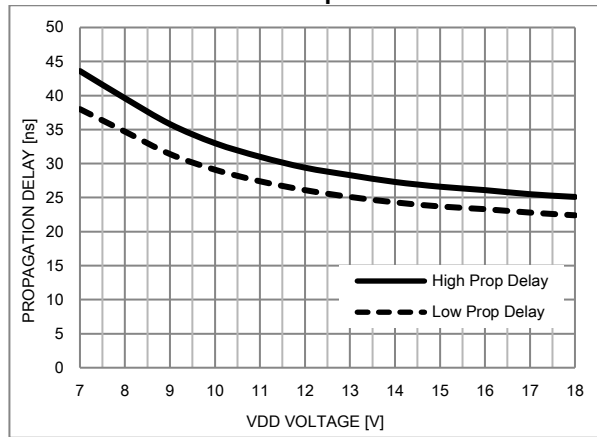


Figure 20. High Side Propagation Delay vs.  $V_{HB}$

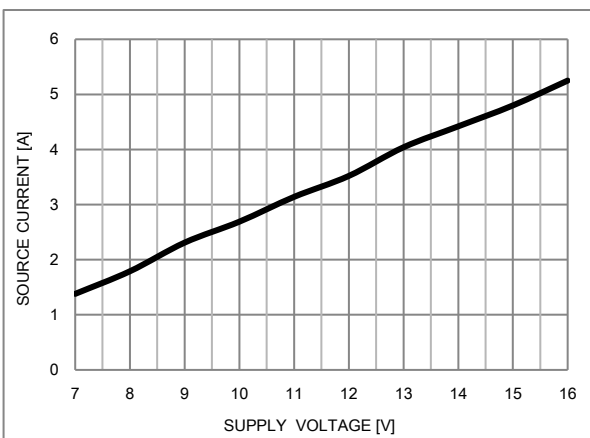


Figure 21. HO, LO Peak Source Current vs. Supply Voltage

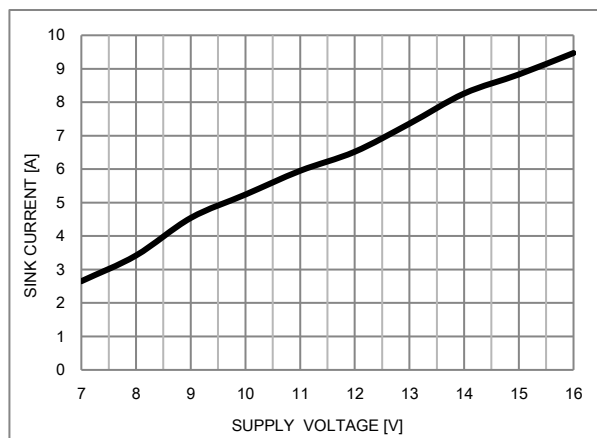
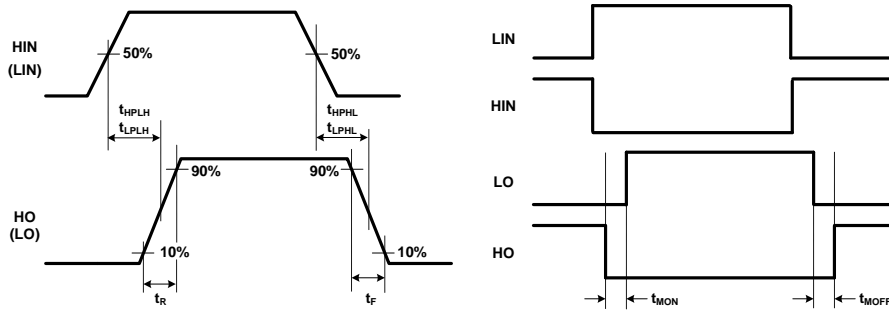


Figure 22. HO, LO Peak Sink Current vs. Supply Voltage

**Switching Time Definitions**

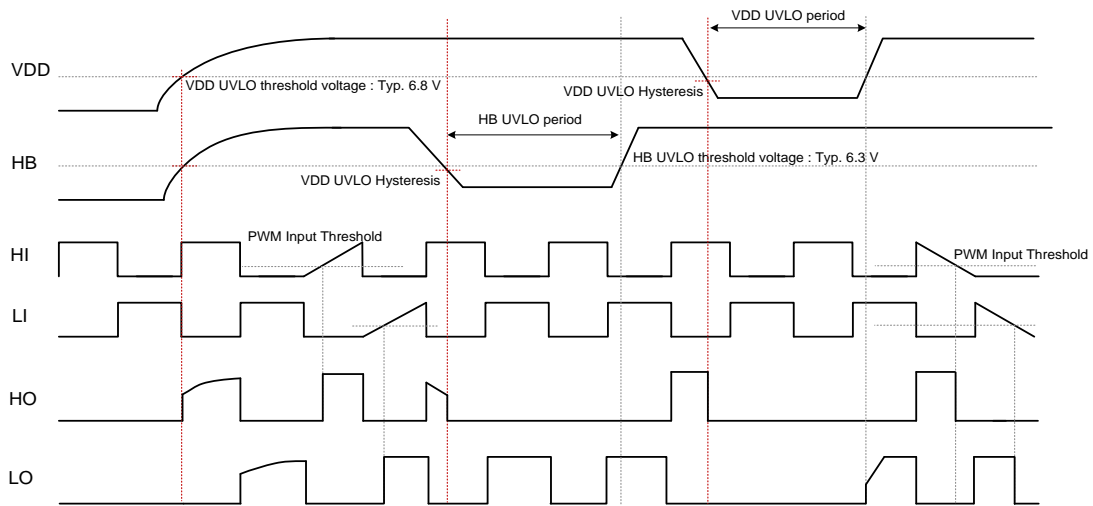
Figure 23 shows the switching time waveform definitions of the turn on and off propagation delay times.



**Figure 23. Timing Diagrams**

**Input to Output Definitions**

Figure 24 shows an input to output timing diagram for overall operation.



**Figure 24. Overall Operation Timing Diagram**

## APPLICATIONS INFORMATION

The FAN8811 are designed for drive the high side and the low side N-channel power MOSFETs in a half bridge or synchronous buck. The bootstrap diode integrates a driver IC for high side driver bias supply. High side and Low side outputs are independently controlled by each of input control signals with TTL or logic compatibly. The floating high side driver can work operate with supply voltage up to 100 V. The FAN8811 functions consist of input stage, level shift, bootstrap diode, The Under-Voltage Lockout (UVLO) protection and output stage. The UVLO function is included in both the high- and low side.

### Input Stage

The input pins (HI,LI) of gate driver devices are based on a TTL compatible input threshold logic that is independent of the  $V_{DD}$  supply voltage. Also, the PWM input signal (high level) can be 3.3 V, 5 V or up to  $V_{DD}$  logic input to cover all possible applications. The input impedance of the FAN8811 is 100 k $\Omega$  nominal. The 100 k $\Omega$  is a pull down resistance to ground (GND). The logic level compatible input provides a rising threshold 2.2 V and a falling threshold of 1.7 V.

### Level Shift

The level shift circuit is the interface from the high side input to the high side driver stage which is referenced to the switch node (HS). The level shift allows to control of the HO output referenced to the HS pin and provides excellent delay matching with the low side driver.

To control the High side output drive utilized a widely used technique for high side level shifter circuit is called pulsed latch level translators. When the HI input signal received from the controller, internal pulse generator make two kinds of pulse signal by the rising edge and falling edge. And then, this signal transmits a Latch through noise canceller. At this time, the pulse generator operating referenced to  $V_{SS}$  (ground), and level shift control of HO referenced to HS.

### Bootstrap Diode

The FAN8811 integrated high voltage bootstrap diode to generate the high side bias. And it is provided to charge high side gate drive bootstrap capacitor. The diode anode is connected to  $V_{DD}$  and cathode connected to HB. The boot capacitor should be connected externally to HB and the HS pins, the HB capacitor charge is refreshed every switching cycle when HS transitions to ground. The bootstrap diode provides fast recovery times, and low resistance value of 0.7  $\Omega$

### Under-Voltage Lockout (UVLO)

Both high side and low side driver have UVLO protection independently which monitors the  $V_{DD}$  supply voltage and HB bootstrap voltage. The  $V_{DD}$  UVLO disables both high side and low side driver when  $V_{DD}$  is below the specified threshold. The rise  $V_{DD}$  threshold is 6.8 V with 0.6 V hysteresis. The HB UVLO disables only the high side driver when the HB to HS differential voltage is below the specified threshold. The HB UVLO rise threshold is 6.3 V with 0.4 V hysteresis.

### Output Stage

The FAN8811 output stage is able to sink/source about 3.0 A /6.0 A typical and interfaces for drive the switching power MOSFETs. High speed switching, low resistance and high current capability of both high side and low side driver allow for efficient switching operation. The low side driver is referenced from  $V_{DD}$  to  $V_{SS}$  and the high side is referenced from HB to HS. The device logic status shows as below.

**Table 1. Device Logic Status**

	HI	LI	HO	LO
Status	L	L	L	L
	L	H	L	H
	H	L	H	L
	H	H	H	H
	X	X	L	L

### Select Bootstrap Capacitor

The maximum allowable voltage drop across the bootstrap capacitor to ensure enough gate-source voltage is highly dependent to the internal under voltage Lockout level of the gate drive IC, and the voltage level at the source connection of switching node HS. So, the maximum allowable drop voltage can obtain as (eq. 1)

$$\Delta V_{HB} = V_{DD} - V_f - V_{HB,UVLO} \quad (\text{eq. 1})$$

Where:

- $V_{DD}$ : Gate drive IC supply voltage
- $V_f$ : Static forward voltage drop of bootstrap diode.
- $V_{HB,UVLO}$ : HB Under-Voltage Lockout level.



# FAN8811

current is consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state. The effect of the static losses within the gate driver can be safely assumed to be negligible due to the FAN8811 has low quiescent current 0.17 mA typically.

The dynamic losses are defined as follows: In the low side driver, the dynamic losses are due to two different sources. One is due to whenever a load capacitor is charged or discharged through a gate resistor, half of energy that goes into the capacitance is dissipated in the resistor. The losses in the gate driver resistance, internal and external to the gate driver, and the switching losses of the internal CMOS circuitry. Also, the dynamic losses of the high side driver have two different sources. One is due to the level shifting circuit and one due to the charging and discharging of the capacitance of the high side. The static losses are neglected here because the total IC power dissipation is mainly dynamic losses of gate drive IC and can be estimated as :

$$P_{DGATE} = 2 \times C_L \times f_S \times V_{DD}^2 [W] \quad (\text{eq.6})$$

The bootstrap circuit power dissipation is the sum of the bootstrap diode losses and the bootstrap resistor losses if any exist. The bootstrap diode loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to switching frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor, resulting in more losses.

## PCB Layout Guideline

First of all, to optimize operation of high side and low side gate driving should be minimize influence of the parasitic inductance and capacitance on the layout. The following should be considered before beginning a PCB layout using the FAN8811.

- The gate driver should be located nearby switching MOSFET as possible.
- The  $V_{DD}$  capacitor and bootstrap capacitor should be locate near by the device.
- In order to reduce ringing voltage of the HS node, the space both high side source and low side drain of the MOSFET should be close as possible.
- The exposed pad should be connect to GND plane and use at least four or more vias for better thermal performance.
- Avoid driver input pulse signal close to the HS node.

One of recommendation layout pattern for the driver is shown in Figure 26.

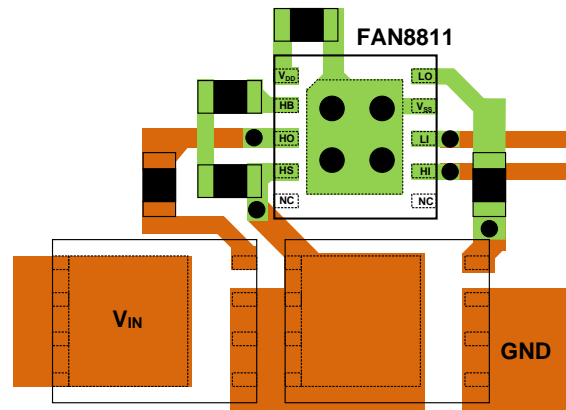


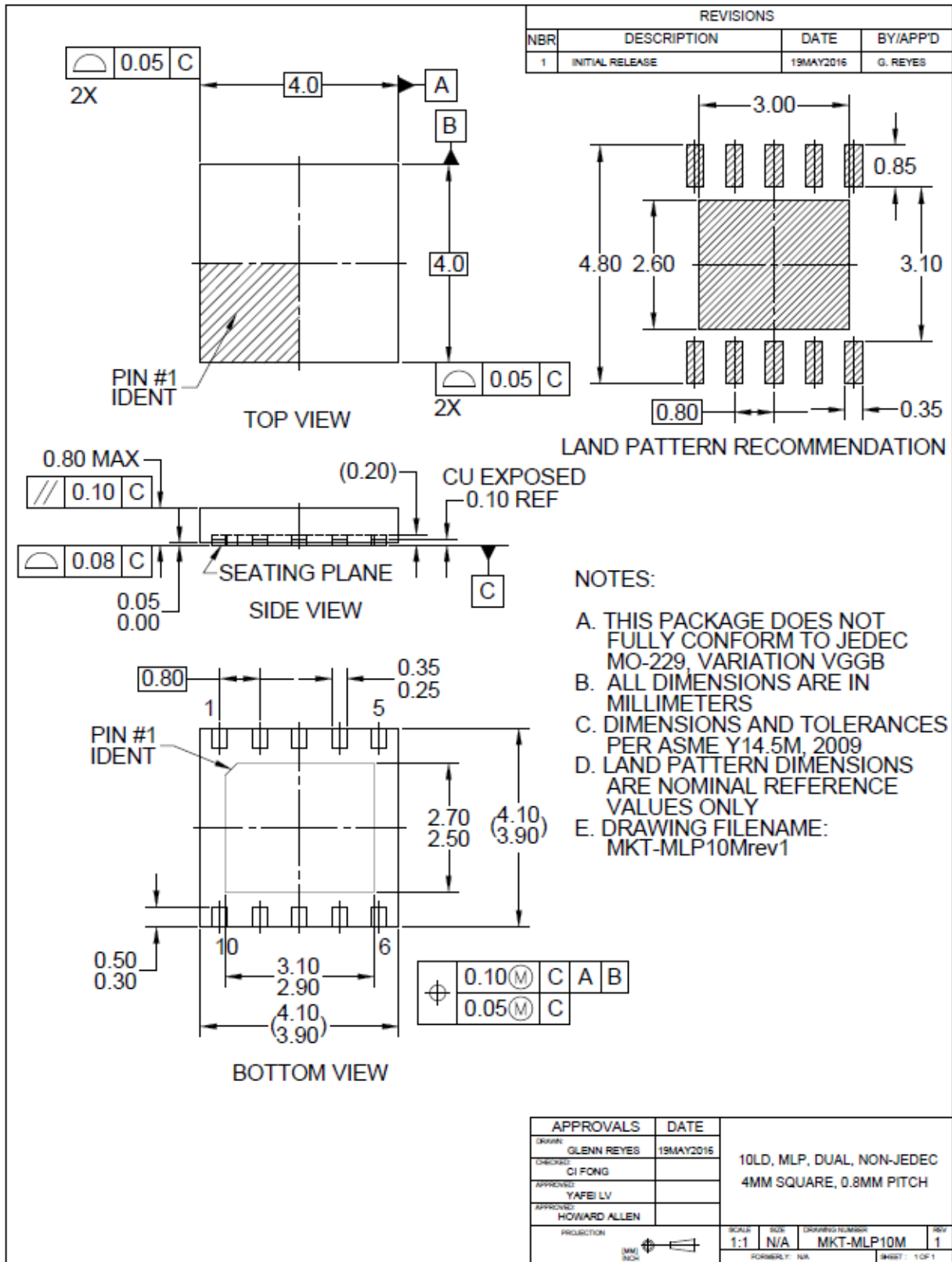
Figure 26. Layout Recommendation


## ORDERING INFORMATION

Device	Output Configuration	Temperature Range (°C)	Package	Shipping
FAN8811TMPX	High-Side and Low-Side	-40 to 125	10-Lead, 4.0 mm x 4.0 mm Molded Leadless Package (MLP)	Tape & Reel

# FAN8811

## PACKAGE DIMENSIONS



ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative