

FCD500N65S3Z

Advance Information

N-Channel SUPERFET[®] III Easy-Drive MOSFET

650 V, 7 A, 500 mΩ

Description

SuperFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SuperFET III MOSFET Easy-drive series helps manage EMI issues and allows for easier design implementation.

Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = \text{TBD m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = \text{TBD nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = \text{TBD pF}$)
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies

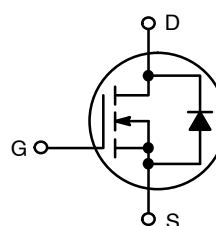
This document contains information on a new product. Specifications and information herein are subject to change without notice.



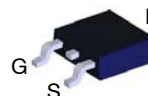
ON Semiconductor[®]

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$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
650 V	500 mΩ	TBD A

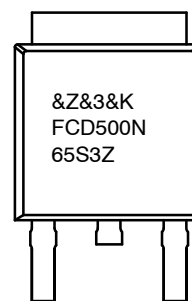


N-Channel MOSFET



D-PAK
(DPAK3 (TO-252 3LD))
CASE 369AS

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
FCD500N65S3Z = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCD500N65S3Z

ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain-to-Source Voltage		650	V
V_{GS}	Gate-to-Source Voltage	DC	± 30	V
		AC ($f > 1\text{ Hz}$)	± 30	V
I_D	Drain Current	Continuous ($T_C = 25^\circ\text{C}$)	7	A
		Continuous ($T_C = 100^\circ\text{C}$)	4.6	
I_{DM}	Drain Current	Pulsed (Note 1)	17.5	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		TBD	mJ
I_{AS}	Avalanche Current (Note 2)		TBD	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		TBD	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	TBD	W/ $^\circ\text{C}$
		Derate Above 25°C	TBD	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
T_L	Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{AS} = 1.6\text{ A}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 3\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 400\text{ V}$, starting $T_J = 25^\circ\text{C}$.

THERMAL RESISTANCE RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case, Steady State	TBD	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient, Steady State (Note 4)	43	

4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2 oz copper.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Reel Size	Tape Width	Shipping (Qty / Packing)
FCD500N65S3Z	FCD500N65S3Z	D-PAK (DPAK3 (TO-252 3LD)) (Pb-Free / Halogen Free)	330 mm	16 mm	2500 / Tape & Reel

FCD500N65S3Z

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650	-	-	V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700	-	-	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	-	TBD	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 520 V, T _C = 125°C	-	TBD	-	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	-	-	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 0.7 mA	2.5	-	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 3.5 A	-	TBD	500	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 3.5 A	-	TBD	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz	-	TBD	-	pF
C _{oss}	Output Capacitance		-	TBD	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	-	TBD	-	pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	-	TBD	-	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 3.5 A, V _{GS} = 10 V (Note 5)	-	TBD	-	nC
Q _{gs}	Gate to Source Gate Charge		-	TBD	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	TBD	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	TBD	-	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 3.5 A, V _{GS} = 10 V, R _g = 4.7 Ω (Note 5)	-	TBD	-	ns
t _r	Turn-On Rise Time		-	TBD	-	ns
t _{d(off)}	Turn-Off Delay Time		-	TBD	-	ns
t _f	Turn-Off Fall Time		-	TBD	-	ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current		-	-	7	A
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current		-	-	17.5	A
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 3.5 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 3.5 A, dI _F /dt = 100 A/μs	-	TBD	-	Ns
Q _{rr}	Reverse Recovery Charge		-	TBD	-	μC

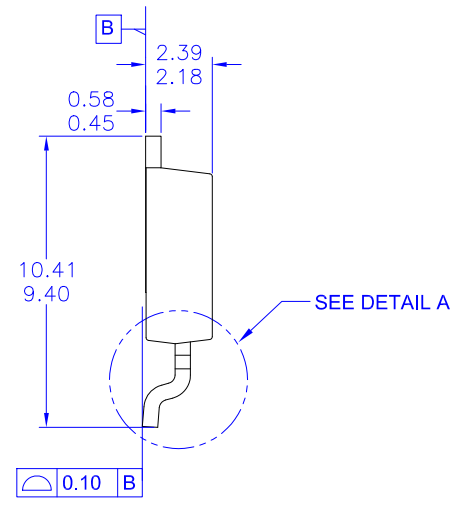
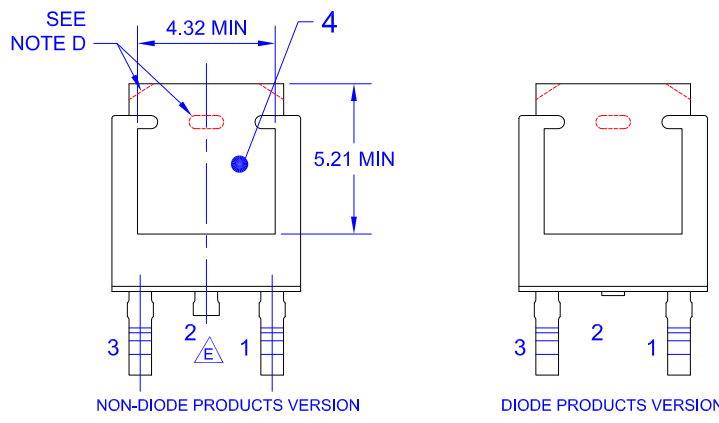
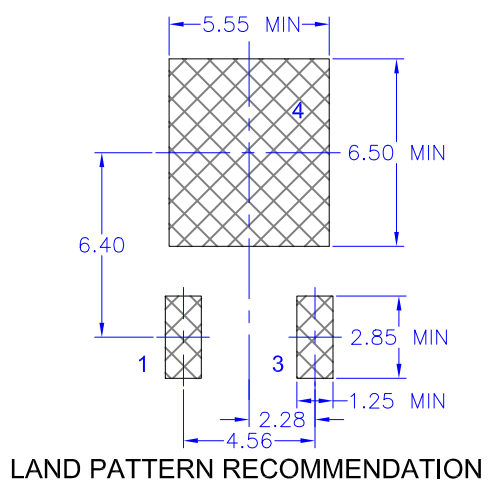
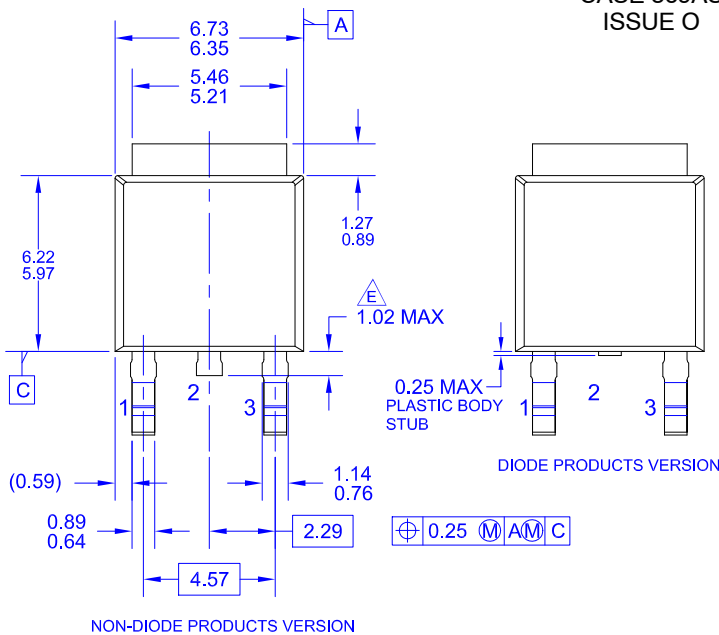
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

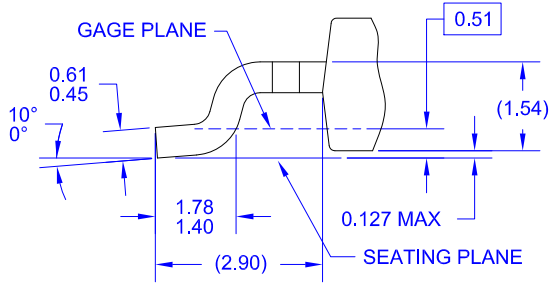
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PACKAGE DIMENSIONS


DPAK3 (TO-252 3 LD) CASE 369AS ISSUE O



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 - D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
 - F) DIMENSIONS ARE EXCLUSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



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