FCD900N65S3Z

Product Preview

Power MOSFET, N-Channel, SUPERFET® III, Easy-Drive

650 V, 4.5 A, 900 mΩ

ON Semiconductor®

www.onsemi.com

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	900 mΩ @ 10 V	4.5 A

Description

SUPERFET III MOSFET is ON Semiconductor's brand−new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

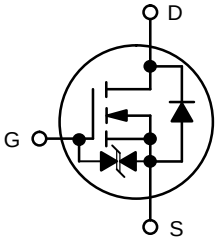
Consequently, SUPERFET III MOSFET Easy−drive series helps manage EMI issues and allows for easier design implementation.

Features

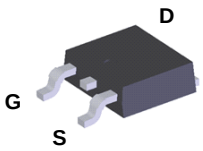
- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 647 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 7 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 105 pF)
- ESD Improved Capability
- 100% Avalanche Tested
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter

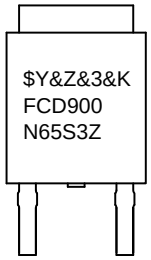


N-Channel MOSFET



D−PAK
CASE 369AS

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FCD900N65S3Z	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		FCD900N65S3Z	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	− DC	±25	V
		− AC (f > 1 Hz)	±25	V
I_D	Drain Current:	− Continuous (T_C = 25°C)	4.5	A
		− Continuous (T_C = 100°C)	2.0	
I_{DM}	Drain Current:	− Pulsed (Note 1)	11.3	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		TBD	mJ
I_{AS}	Avalanche Current (Note 2)		TBD	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		TBD	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	38	W
		Derate Above 25°C	0.30	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = TBD A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 1.75 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FCD900N65S3Z	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, (1 in^2 Pad of 2 oz Copper) Max.	45	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD900N65S3Z	FCD900N65S3Z	TO−252	Tape and Reel	330 mm	16 mm	2500 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650	–	–	V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	–	0.68	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 520 V, T_C = 125°C	–	0.2	–	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 50 μA	2.5	–	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 2.25 A	–	647	900	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 2.25 A	–	2.7	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	–	425	–	pF
C_{oss}	Output Capacitance		–	9.0	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	105	–	pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	13.5	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400 V, I_D = 2.25 A, V_{GS} = 10 V (Note 4)	–	7.0	–	nC
Q_{gs}	Gate to Source Gate Charge		–	2.0	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	4.0	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	TBD	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 2.25 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)	–	5.0	–	ns
t_r	Turn-On Rise Time		–	6.0	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	21	–	ns
t_f	Turn-Off Fall Time		–	2.0	–	ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current		–	–	3.5	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current		–	–	11.3	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 2.25 A	–	–	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 2.25 A, dI_F/dt = 100 A/μs	–	204	–	ns
Q_{rr}	Reverse Recovery Charge		–	1.2	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

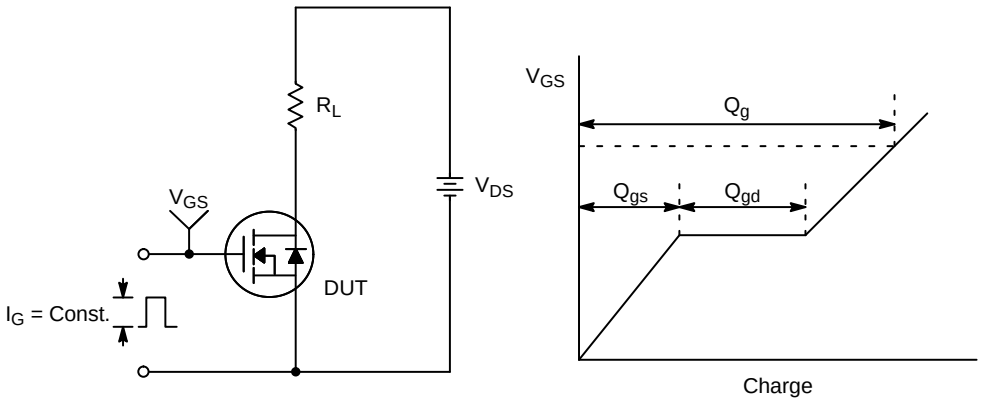


Figure 1. Gate Charge Test Circuit & Waveform

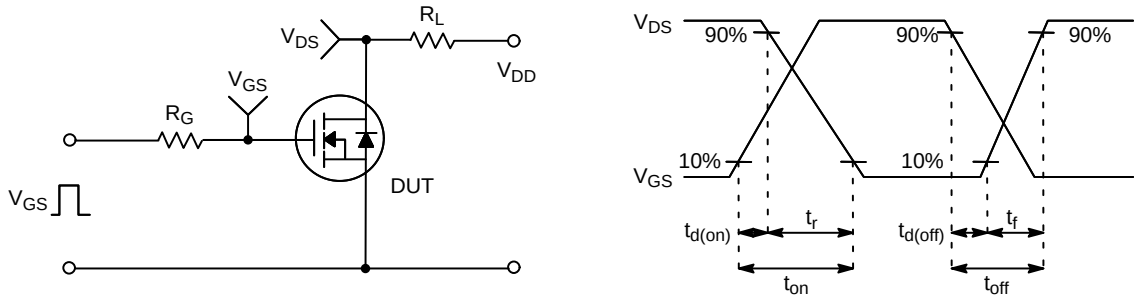


Figure 2. Resistive Switching Test Circuit & Waveforms

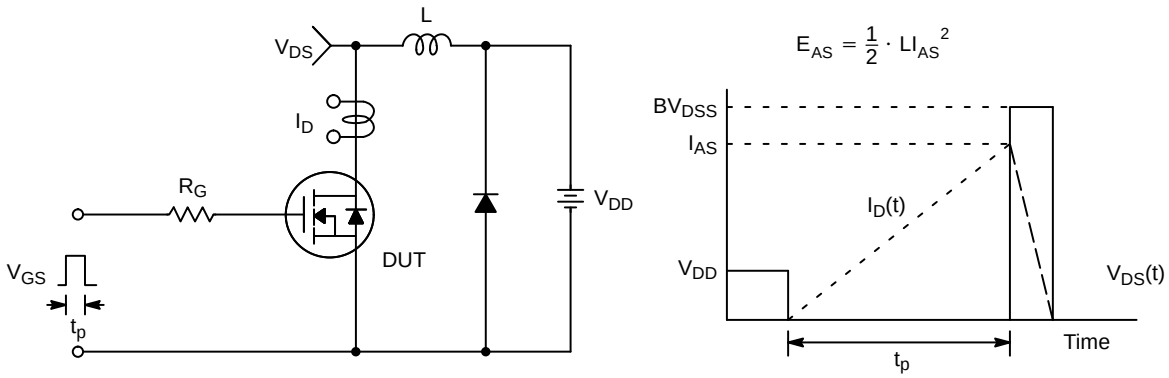


Figure 3. Unclamped Inductive Switching Test Circuit & Waveforms

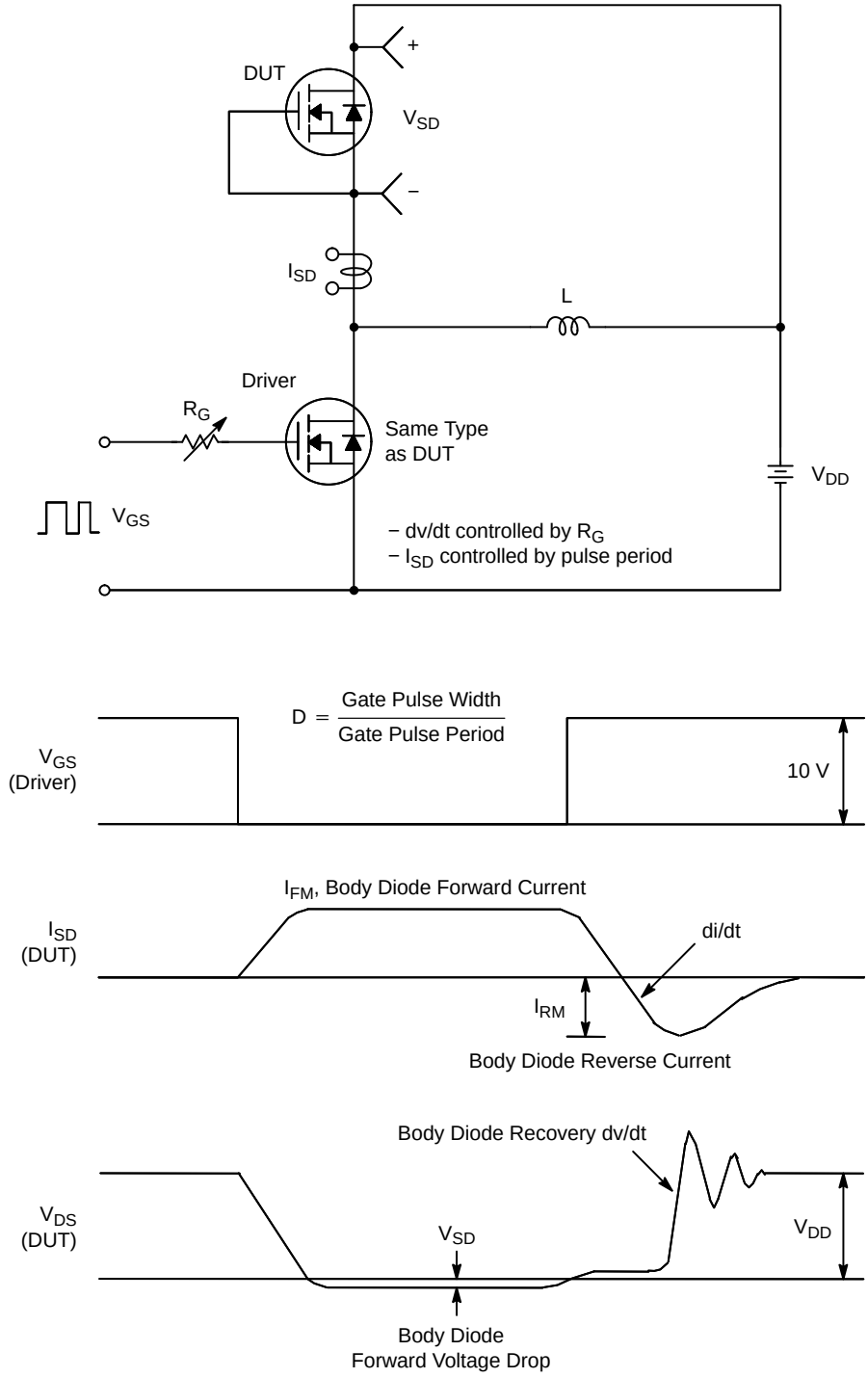
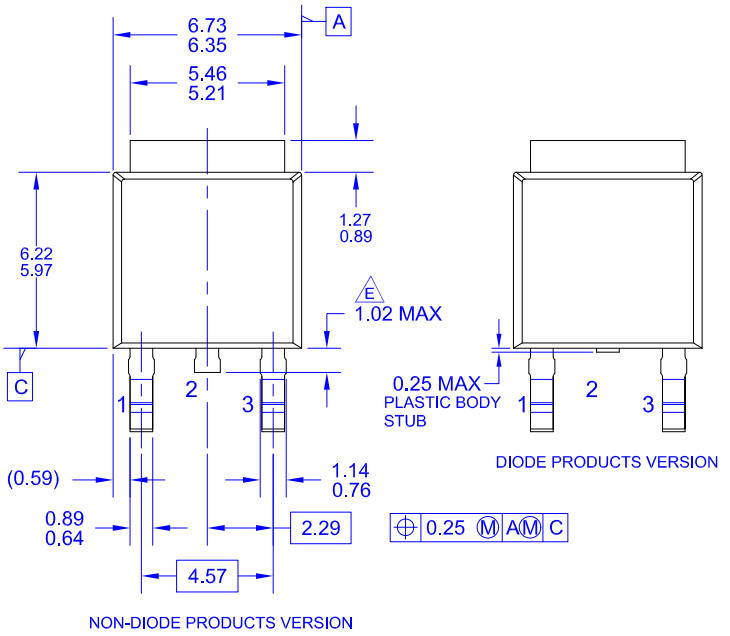
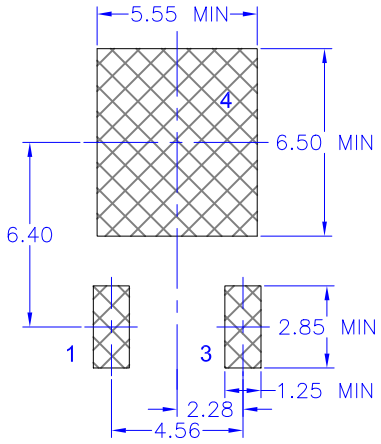


Figure 4. Peak Diode Recovery dv/dt Test Circuit & Waveforms

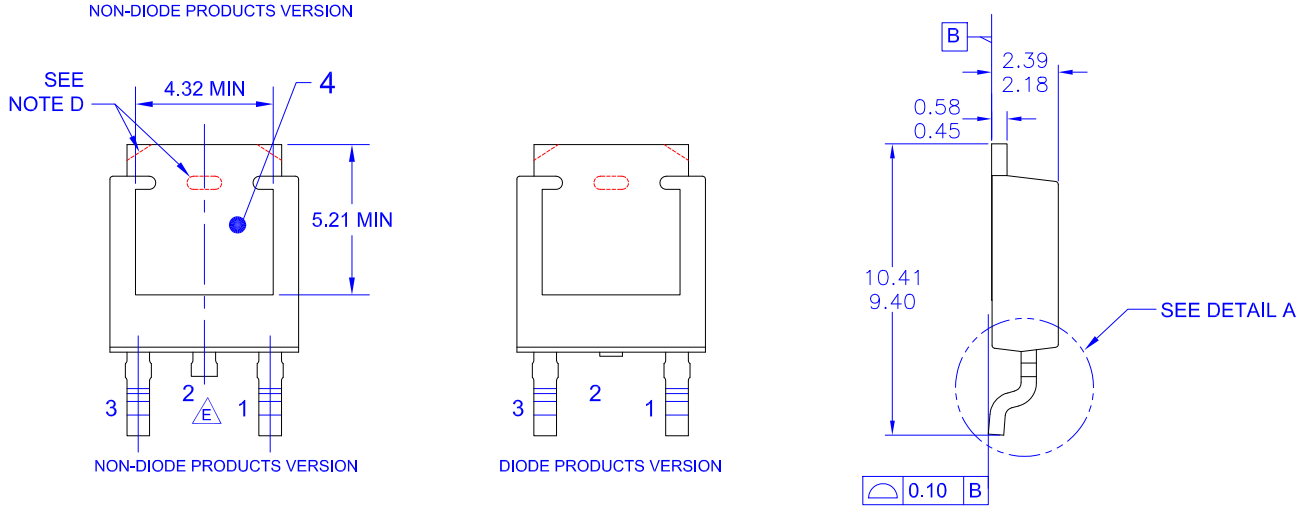
PACKAGE DIMENSIONS

DPAK3 (TO−252 3 LD)
CASE 369AS
ISSUE O

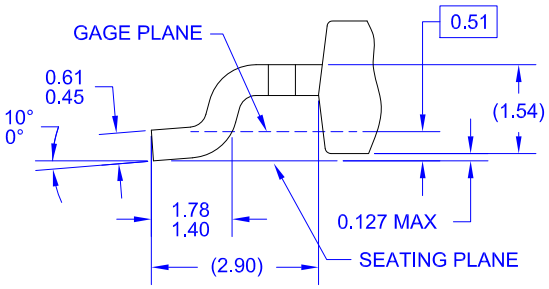




LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)

SUPERFET is a registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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